General Description

The DM9301FP is a physical-layer, single-chip, low-power media converter for 100BASE-TX/FX full duplex repeater applications. On the TX media side, it provides a direct interface to Unshielded Twisted Pair Cable 5 (UTP5) for 100BASE-TX Fast Ethernet. On the FX media side, it provides a direct interface to a Pseudo Emitter Coupled Logic level interface (PECL).

The DM9301FP uses a low power and high performance CMOS process. It contains the entire physical layer functions of 100BASE-TX as defined by IEEE802.3u, including the Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA), Twisted Pair Physical Medium Dependent Sublayer (TP-PMD) and a PECL compliant interface for a fiber optic module, compliant with ANSI X3.166. The DM9301FP provides two independent clock recovery circuits to minimize bit delay through the converter (no FIFO is used to buffer data between the FX and TX interfaces). Furthermore, due to the excellent rise/fall time control by a built-in wave-shaping filter, the DM9301FP needs no external filter to transport signals to the media on the 100Base-TX interface.

Patent-Pending Circuits

- Smart adaptive receiver equalizer
- Digital algorithm for high frequency clock/data recovery circuit
- High speed wave-shaping circuit

Block Diagram

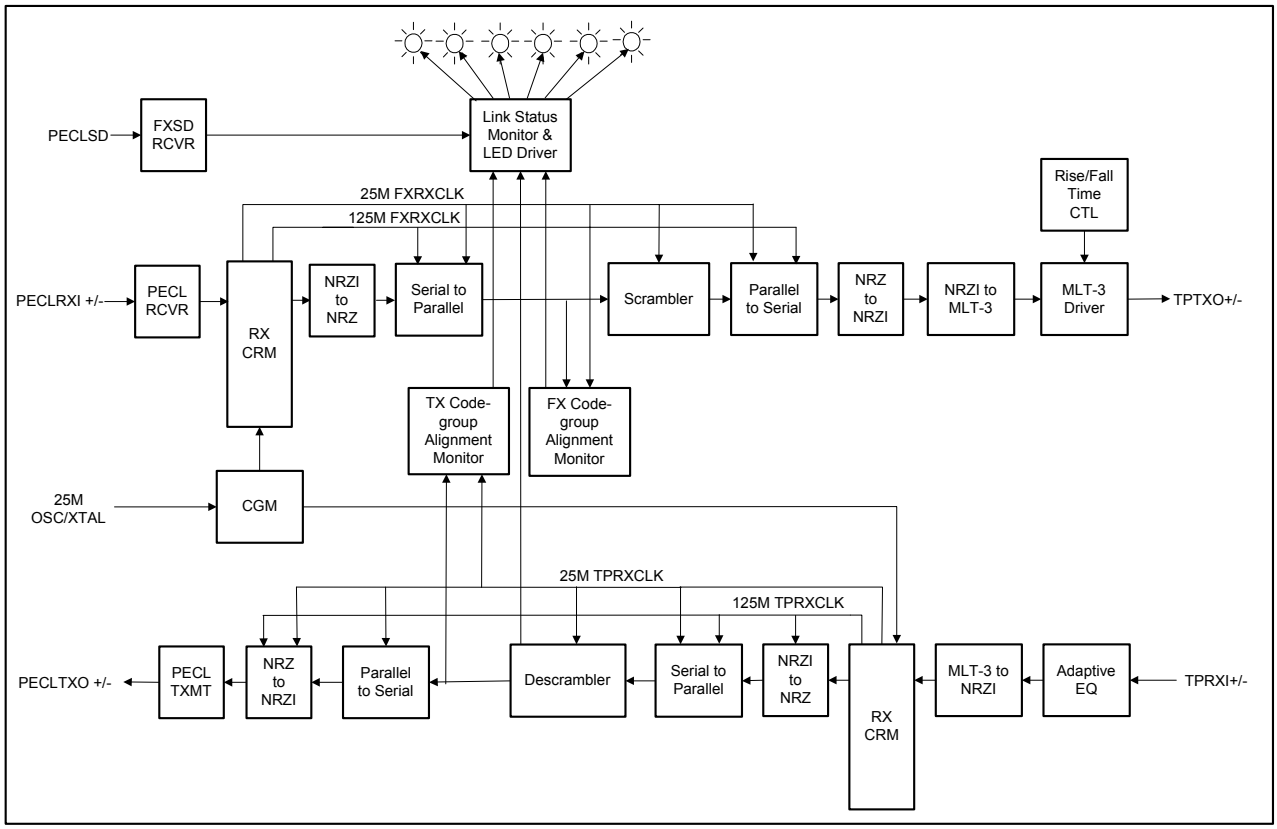


Table of Contents

General Description 1

Block Diagram 1

Table of contents 2

Features 3

Pin Configuration: DM9301FP QFP 4

Pin Description 5

Functional Description 10
100Base-FX to TX Operation 10
- FX PECL Receiver 10
- FX Receiver Clock Recovery Module 10
- FX NRZI to NRZ Converter 10
- FX Serial to Parallel Converter 11
- FX Code Group Alignment Monitor 11
- TX Scrambler 11
- TX Parallel to Serial Converter 11
- TX NRZ to NRZI Converter 11
- TX NRZI to MLT-3 Converter 11
- TX MLT-3 Driver 11

100Base-TX to FX Operation 12
- TX Signal Detect 12
- TX Digital Adaptive Equalization 12
- TX MLT-3 to NRZI Decoder 13
- TX Clock Recovery Module 13
- TX NRZI to NRZ Decoder 13
- TX Serial to Parallel Converter 13
- TX Code Group Monitor 13
- TX Descrambler 13
- FX Parallel to Serial Converter 13
- FX NRZ to NRZI Encoder 13
- Link Monitor and LED Driver 13

Absolute Maximum Ratings 14

DC Electrical Characteristics 15

AC Electrical Characteristics 16

Timing Waveforms 17
- 100BASE-TX to FX Transmit Timing Diagram 17
- 100BASE-FX to TX Transmit Timing Diagram 17
- 5-Bit Symbol 100Base-TX/FX Transmit Timing Diagram 17
- 5-Bit Symbol 100Base-TX/FX Receive Timing Diagram 18

Application Circuit (For Reference Only) 19

Package Information 21

Ordering Information 22

Disclaimer 22

Company Overview 22

Products 22

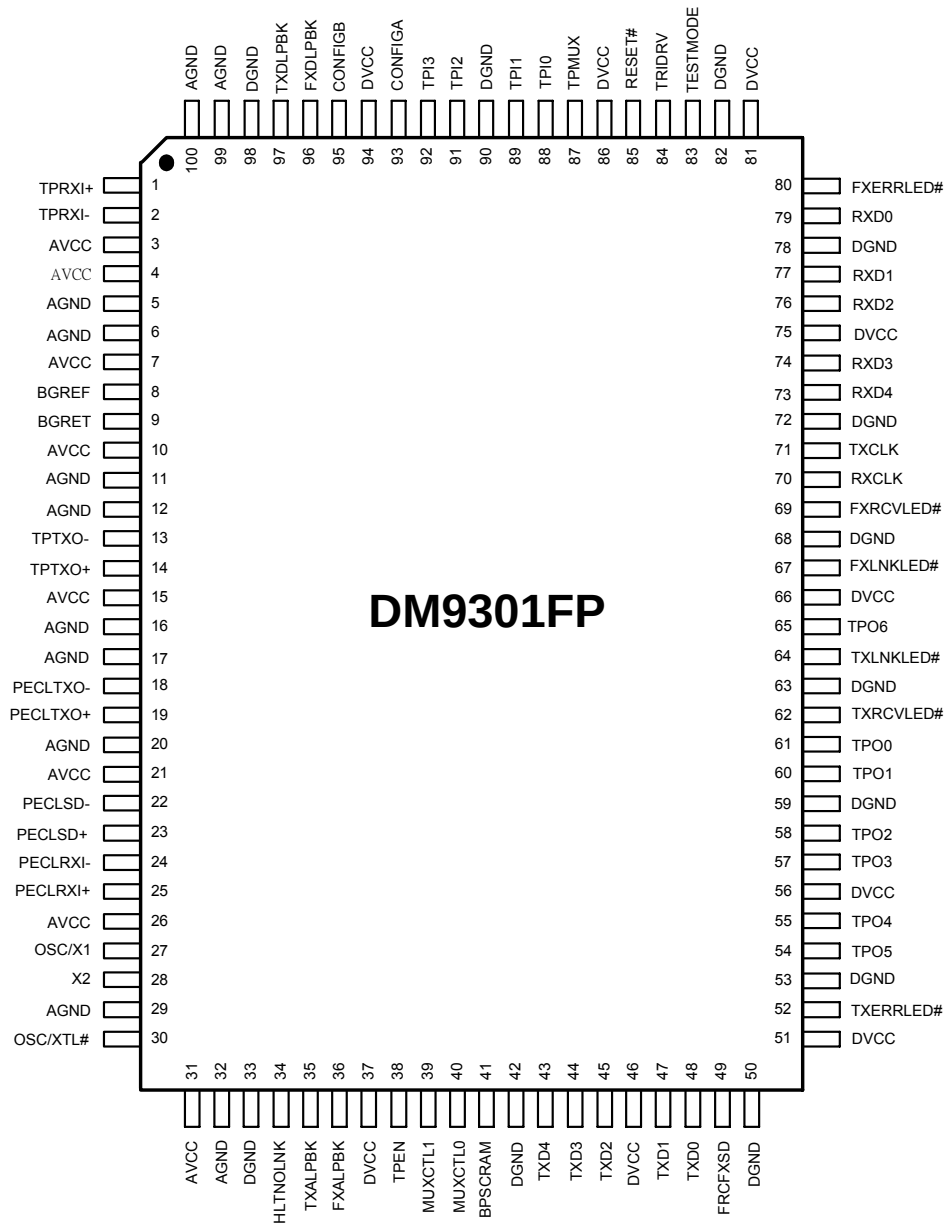
Contact Windows 22

Warning 22

Features

- 100BASE-TX/FX single-chip media converter
- Total bit delay from FX to TX interface is 20 bit times (10 bit times each direction).
- Optional propagate HALT on no Link condition
- Compliant with IEEE802.3u 100BASE-TX standard
- Compliant with ANSI X3T12 TP-PMD 1995 standard
- Compliant with ANSI X3.166 FDDI-PMD
- Supports Half and Full Duplex operation 100Mbps, the DM9301FP operates in Full Duplex mode at all times
- High performance 100Mbps clock generator and data recovery circuit
- Controlled output edge rates in the 100Base-TX transmitter without the need for an external filter
- LED supports for FX Link, TX link, FX receive data; TX receives data, and FX code group error and TX code group error.
- Built in LED test, all LED will light during a reset condition on the DM9301FP
- Digital clock recovery and regeneration circuit using an advanced digital algorithm to minimize jitter
- Supports diagnostic TX to TX analog Loopback and FX to FX analog Loopback (Loopback at the NRZI interface)
- Supports diagnostic TX to TX digital Loopback and FX to FX digital Loopback (Loopback at the 5B symbol interface)
- Low-power, high-performance CMOS process
- Available in a 100 QFP package

Pin Configuration: DM9301FP QFP



Pin Description

Pin No.	Pin Name	I/O	Description
Media Interface			
1, 2	TPRXI+, TPRXI-	I	**100Mbps-TX Differential Input Pair:** These pins are differential receive input for 100BASE-TX. They are capable of receiving 100BASE-TX MLT-3 data.
13, 14	TPTXO-, TPTXO+	O	**100BASE-TX Differential Output Pair:** These outputs drive MLT-3 encoded data over 100Mbps twisted pair cable and provide controlled rise and fall times designed to filter the transmitter output, reducing any associated EMI.
24, 25	PECLRXI-, PECLRXI+	I	**100BASE-FX PECL Receive Data Differential Pair:** These pins are differential receive input for 100BASE-FX PECL. They are capable of receiving PECL 100BASE-FX NRZI data.
18, 19	PECLTXO-, PECLTXO+	O	**100BASE-FX Transmit Differential Output Pair:** These outputs drive NRZI encoded data for PECL FX interface.
22, 23	PECLSD-, PECLSD+	I	**100BASE-FX PECL Signal detect:** These pins are differential signals that indicate to the DM9301FP that the Optical Module interface is detecting valid optical energy.
Clock and Misc. Interface			
27	OSCI/X1	I	**Crystal or Oscillator Input:** This pin should connect to one side of a 25MHz, 50ppm crystal if OSC/XTL#=0. This pin is the 25MHz, 50ppm external TTL oscillator input, if OSC/XTLB=1.
28	X2	O	**Crystal Oscillator Output:** The other side of a 25MHz, 50ppm crystal should connect to this pin if OSC/XTL#=0. Leave this pin open if OSC/XTL#=1.
30	OSC/XTL#	I	**Crystal or Oscillator Selector Pin:** OSC/XTL#=0: An external 25MHz, 50ppm crystal should connect to X1 and X2 pins. OSC/XTL#=1: An external 25MHz, 50ppm oscillator should connect to X1 and left X2 pin open.
8	BGREF	I	**Bandgap Voltage Reference Resistor:** It connects to a 6.49KΩ, 1% error tolerance resistor between this pin and BGRET pin 9 to provide an accurate current reference for the chip.
9	BGRET	I	**Bandgap Return** Return pin for 6.49KΩ resistor connection, **DO NOT CONNECT TO GROUND.**

Clock and Misc. Interface (Continued)			
84	TRIDRV	I	**Tristate Digital Output Pins:** When set high, all digital output pins are set to high impedance.
85	RESET#	I	**Reset:** Active Low input that initializes the DM9301FP, must be asserted low for 30msecs after VCC is stable.
34	HLTNOLNK	I	**Send Halt on no Link Condition:** Causes the DM9301FP to Send out a Halt symbol to the TX interface if no FX link active or send out a Halt symbol to the FX interface if no TX link active. Propagates a no-link condition to the Link Partner if 1, Idle symbol if 0. Active high
93	CONFIGA	I	**Config A:** Must be connected to GND
95	CONFIGB	I	**Config B:** Must be connected to GND
LED Interface			
67	FXLNKLED#	OD	**FX Link LED:** Indicates Good Link status for 100Mbps FX operation. Active low (Open Drain Output)
64	TXLNKLED#	OD	**TX Link LED:** Indicates Good Link status for 100Mbps TX operation. Active low (Open Drain Output)
69	FXRCVLED#	OD	**FX Receive LED:** Indicates the presence of receive activity for 100Mbps FX operation. Active low (Open Drain Output) The DM9301FP incorporates a "monostable" function on the FXRCVLED output. This ensures that even minimum size packets generate adequate LED ON to insure visibility.
62	TXRCVLED#	OD	**TX Receive LED:** Indicates the presence of receive activity for 100Mbps TX operation. Active low (Open Drain Output) The DM9301FP incorporates a "monostable" function on the TXRCVLED output. This ensures that even minimum size packets generate adequate LED ON to insure visibility.
80	FXERRLED#	OD	**FX Error LED:** Indicates an error was detected by the FX Code Group Alignment Monitor function on the FX receiver. Active low (Open Drain Output) The DM9301FP incorporates a "monostable" function on the FXERRLED output. This ensures that even minimum size errors generate adequate LED ON to insure visibility.

LED Interface(Continued)			
52	TXERRLED#	OD	**TX Error LED:** Indicates an error was detected by the TX Code Group Alignment Monitor function on the TX receiver. Active low (Open Drain Output) The DM9301FP incorporates a "monostable" function on the TXERRLED output. This ensures that even minimum size errors generate adequate LED ON to insure visibility.
Diagnostic Port Interface			
36	FXALPBK	I	**FX Interface Analog Loop Back:** Loops the FX NRZI analog transmit data path to the FX NRZI analog receive path. Initiated at an H/W reset. Active high.
35	TXALPBK	I	**TX Interface Analog Loop Back:** Loops the TX NRZI analog transmit data path to the TX NRZI analog receive path. Initiated at an H/W reset. Active high.
96	FXDLPBK	I	**FX Interface Digital Loop Back:** Loops the FX 5-bit symbol digital transmit data path to the FX 5-bit symbol digital receive path. Initiated at an H/W reset. Active high.
97	TXDLPBK	I	**TX Interface Digital Loop Back:** Loops the TX 5-bit symbol digital transmit data path to the TX 5-bit symbol digital receive path. Initiated at an H/W reset. Active high.
79, 77, 76, 74, 73	RXD0, RXD1, RXD2, RXD3, RXD4	0	**Receive Data 4 through 0:** The receive data 5-bit symbol interface. Data is clocked out on the falling edge of RXCLK.
70	RXCLK	O	**Receive Clock:** 25 MHz recovered clock, clock source is selected by the MUXCTL1 and MUXCTL0.
48, 47, 45, 44, 43	TXD0, TXD1, TXD2, TXD3, TXD4	I	**Transmit Data 4 through 0:** The transmit data 5-bit symbol interface. Data is clocked in on the rising edge of TXCLK.
71	TXCLK	O	**Transmit Clock:** 25 MHz recovered clock, clock source is selected by the MUXCTL1 and MUXCTL0.

<table>
<tr><th colspan="4">Diagnostic Port Interface (Continued)</th></tr>
<tr><td>39, 40</td><td>MUXCTL1,
MUXCTL0</td><td>I</td><td>Mux. Control 1 and 0:
Used for testing the DM9301FP Data Paths. Set to zero for normal operation.

Initiated at an H/W reset. Active high.

<u>MUXCTL1</u> <u>MUXCTL0</u> <u>DATA PATH</u>
0 0 Normal, FX to TX and TX to FX

1 0 TX Transmit from TXD[4:0]
TXCLK from TX PLL
TX Receive to RXD[4:0]
RXCLK from TX receive clock

0 1 FX Transmit from TXD[4:0]
TXCLK from FX PLL
FX Receive to RXD[4:0]
RXCLK from FX receive clock

1 1 TX Transmit from TXD[4:0]
TXCLK from TX PLL
FX Receive to RXD[4:0]
RXCLK from FX receive clock</td></tr>
<tr><td>65, 54,
55, 57,
58, 60,
61</td><td>TPO6, TPO5,
TPO4, TPO3,
TPO2, TPO1,
TPO0</td><td>O</td><td>Test Port Output:
Reflects the DM9301FP internal status. Selection of status indicators is made by using TPEN and TPMUX.
Initiated at an H/W reset. Active high.</td></tr>
<tr><td>92, 91, 89,
88</td><td>TPI3, TPI2, TPI1,
TPI0,</td><td>I</td><td>Test Port Input:
Controls the DM9301FP internal test features. Selection of input control is made by using TPEN and TPMUX.
TPEN must be true (one) for this signal to take effect.
Initiated at an H/W reset. Active high.</td></tr>
</table>

Diagnostic Port Interface (Continued)			
49	FRCFXSD	I	**Force FX Signal Detect** Forces the DM9301FP FX interface Signal Detect true Initiated at an H/W reset. Active high.
38	TPEN	I	**Test Port Enable:** Enables the DM9301FP Test Port features. Initiated at an H/W reset. Active high.
87	TPMUX	I	**Test Port Mux:** Controls the DM9301FP Test Port Input and Output bits. A value of zero indicates the TX interface and a value of one indicates the FX interface. TPEN must be true (one) for this signal to take effect. Initiated at an H/W reset. Active high.
41	BPSCRAM	I	**Bypass Scrambler:** Controls the DM9301FP TX interface Scrambler/De-scrambler function. A value of zero indicates to scramble and de-scramble the TX interface 5-bit symbol data to and from the FX interface. A value of one bypasses the scrambler/de-scrambler function. Initiated at an H/W reset. Active high.
Power and Ground Pins : The power (VCC) and ground (GND) pins of the DM9301FP are grouped in pairs of two categories - Digital Circuitry Power/Ground Pairs and Analog Circuitry Power/Ground Pair.			
Group A - Digital Supply Pairs			
33, 42, 50, 53, 63, 68, 72, 78, 82, 90, 98	DGND	P	Digital Logic Ground.
37, 46, 51, 56, 66, 75, 81, 86, 94	DVCC	P	Digital Logic power supply
Group B - Analog Circuit Supply Pairs			
5, 6, 11, 12, 16, 17, 20, 29, 32, 99, 100,	AGND	P	Analog circuit ground
3, 4, 7, 10, 15, 21, 26, 31	AVCC	P	Analog circuit power supply

Functional Description

The DM9301FP Fast Ethernet single-chip TX/FX media converter, provides the functionality as specified in IEEE802.3, integrates the complete 100BASE-TX and a PECL optic module interface for 100Base-FX. The DM9301FP implements the PCS, PMA, and TP-PMD sublayer functions, as defined by specification. The term "X" will be used to describe the sections used in the fiber PHY layer interface. The term "X" will be used to describe the sections used in the twisted-pair PMD layer interface.

100BASE-FX to TX Operation

The block diagram in figure 1 provides an overview of the functional blocks contained in the FX to TX media converter interface.

The FX to TX interface includes the following functional blocks:

- FX PECL Receiver
- FX Receiver Clock Recovery Module
- FX NRZI to NRZ Converter
- FX Serial to Parallel Converter
- FX Code Group Alignment Monitor
- TX Scrambler
- TX Parallel to Serial Converter
- TX NRZ to NRZI Converter
- TX NRZI to MLT-3 Converter
- TX MLT-3 Driver

FX PECL Receiver

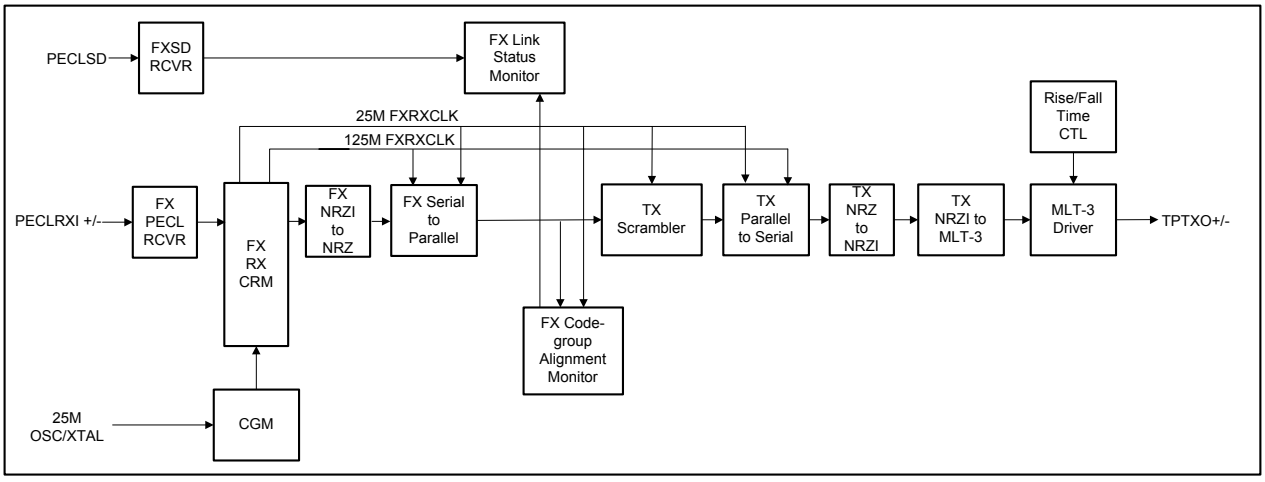
The PECL receiver receives NRZI encoded, differential Pseudo Emitter Coupled Logic level signal. The receiver converts the receive signal into a single-ended NRZI signal and presents this signal to the FX Clock Recovery Module.

FX Receiver Clock Recovery Module

The FX Clock Recovery Module accepts NRZI data from the PECL receiver. The FX Clock Recovery Module locks onto the data stream, using a Phase Lock Loop (PLL) and extracts the 125 MHz reference clock. The extracted and synchronized clock and data are presented to the FX NRZI to NRZ Decoder.

FX NRZI to NRZ Converter

The receive data stream is required to be NRZI encoded for compatibility with the standards for 100Base- FX. This conversion process must be reversed on the transmit end. The FX NRZI to NRZ decoder receives the NRZI data stream from the FX Clock Recovery Module and converts it to a NRZ data stream to be presented to the FX Serial to Parallel conversion block.



FX to TX Block Diagram

Figure 1

FX Serial to Parallel Converter

The Serial to Parallel converter receives a serial data stream from the NRZI to NRZ converter, and converts the data stream to parallel data to be presented to the scrambler. The parallel data format presented to the TX scrambler is 5B coded.

FX Code Group Alignment Monitor

The FX Code Group Alignment block receives non-aligned 5B data from the FX Serial to Parallel converter and monitors it for 5B code group violations. FX Code Group Alignment occurs after the J/K is detected, and subsequent data is monitored on a fixed boundary. If a violation is detected, the FX Code Group Alignment Monitor block signals the error to the Link Status Monitor blocks. In turn, the Link Status Monitor block flashes the FX error LED (FXERRLED#).

TX Scrambler

The scrambler also receives data from the FX Serial to Parallel converter. Data from the serial to parallel conversion block is 5B symbol encoded. The scrambler is required to control the radiated emissions (EMI) by spreading the transmit energy across the frequency spectrum at the media connector and on the twisted pair cable in 100Base-TX transmit operation.

By scrambling the data, the total energy presented to the cable is randomly distributed over a wide frequency range. Without the scrambler, energy levels on the cable could peak beyond FCC limitations at frequencies related to repeated 5B sequences like continuous transmission of IDLE symbols. The scrambler output is combined with the NRZ 5B data from the FX Serial to Parallel converter via an XOR logic function. The result is a scrambled data stream with sufficient randomization to decrease radiated emissions at critical frequencies.

TX Parallel to Serial Converter

The TX Parallel to Serial converter receives parallel 5B scrambled data from the scrambler and serializes it (converts it from a parallel to a serial data stream). The serialized data stream is then presented to the NRZ to NRZI converter block

TX NRZ to NRZI Converter

After the transmit data stream has been scrambled and serialized, the data must be NRZI encoded for compatibility with the TP-PMD standard for 100Base-TX transmission over Category-5 unshielded twisted pair cable.

TX MLT-3 Converter

The MLT-3 conversion is accomplished by converting the data stream output from the NRZI encoder into two binary data streams with alternately phased logic one events.

TX MLT-3 Driver

The two binary data streams created at the MLT-3 converter are fed to the twisted pair output driver which converts these streams to current sources and alternately drives either side of the transmit transformer primary winding resulting in a minimal current MLT-3 signal.

100Base-TX to FX Operation

The block diagram in figure 2 provides an overview of the functional blocks contained in the TX to FX media converter interface.

The TX to FX interface contains the following functional blocks:

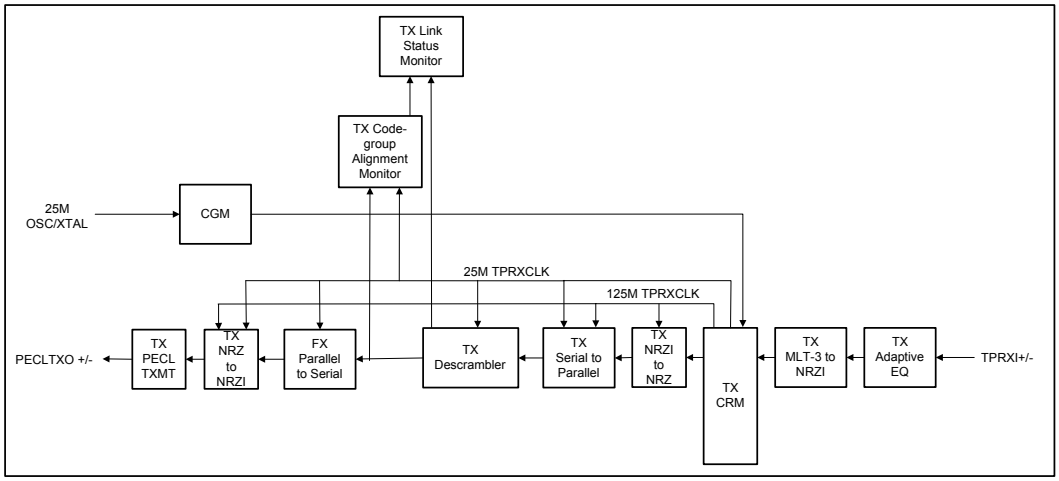
- TX Digital Adaptive Equalization
- TX MLT-3 to NRZI
- TX Clock Recovery Module
- TX NRZI to NRZ Decoder
- TX Serial to Parallel Conversion
- TX Descrambler
- TX Code Group Alignment Monitor
- FX Parallel to Serial Conversion
- FX NRZ to NRZI
- FX PECL Transmitter

TX Signal Detect

The signal detects function meets the specifications mandated by the ANSI XT12 TP-PMD100Base-TX standards for both voltage thresholds and timing parameters.

TX Digital Adaptive Equalization

When transmitting data at high speeds over copper twisted pair cable, attenuation based on frequency becomes a concern. In high speed twisted pair signaling, the frequency content of the transmitted signal can vary greatly during normal operation based on the randomness of the scrambled data stream. This variation in signal attenuation caused by frequency variations must be compensated for to ensure the integrity of the received data. In order to ensure quality transmission when employing MLT-3 encoding, the compensation must be Able to adapt to various cable lengths and cable types depending on the installed environment. The selection of long cable lengths for a given implementation requires significant compensation which will be over-kill in a situation that includes shorter, less attenuating cable lengths. Conversely, the selection of short or intermediate cable lengths requiring less compensation will cause serious under-compensation for longer length cables.



TX to FX Block Diagram

Figure 2

Therefore, the compensation or equalization must be adaptive to ensure proper conditioning of the received signal independent of the cable length.

TX MLT-3 to NRZI Decoder

The DM9301FP decodes the MLT-3 information from the TX Digital Adaptive Equalizer into NRZI data.

TX Clock Recovery Module

The TX Clock Recovery Module accepts NRZI data from the MLT-3 to NRZI decoder. The TX Clock Recovery Module locks onto the data stream and extracts the 125 MHz reference clock. The extracted and synchronized clock and data are presented to the NRZI to NRZ Decoder.

TX NRZI to NRZ Decoder

The TX transmit data stream is required to be NRZI encoded in for compatibility with the TP-PMD standard for 100Base-TX transmission over Category-5 unshielded twisted pair cable. This conversion process must be reversed on the receive end. The NRZI to NRZ decoder receives the NRZI data stream from the TX Clock Recovery Module and converts it to a NRZ data stream to be presented to the TX Serial to Parallel conversion block.

TX Serial to Parallel Converter

The TX Serial to Parallel converter receives a serial data stream from the TX NRZI to NRZ decoder, and converts the data stream to parallel data to be presented to the TX descrambler. The parallel data format presented to the TX descrambler is 5B coded.

TX Code Group Monitor

The TX Code Group Alignment block receives non-aligned 5B data from the TX descrambler and monitors it for 5B code group violations. TX Code Group Alignment occurs after the J/K is detected, and subsequent data is monitored on a fixed boundary. If a violation is detected, the TX Code Group Monitor block signals the error to the Link Status Monitor block. In turn, the Link Status Monitor block flashes the TX error LED (TXERRLED#).

TX Descrambler

Because of the scrambling process required to control the radiated emissions of transmit data streams, the receiver must descramble the receive data streams. The TX Descrambler receives scrambled parallel data streams from the Serial to Parallel converter, descrambles the data streams, and presents the data streams to the Code Group alignment block.

FX Parallel to Serial Converter

The FX Parallel to Serial Converter receives parallel 5B data from the TX de-scrambler and serializes it (converts it from a parallel to a serial data stream). The serialized data stream is then presented to the FX NRZ to NRZI Encoder block

FX NRZ to NRZI Encoder

After the transmit data stream has been serialized, the data must be NRZI encoded for compatibility with the standard for 100Base-FX.

Link Monitor and LED Driver

The Link Monitor block monitors both the TX and FX interfaces for link active, receive data and erring 5-bit stream.

The Link Monitor has the ability to detect each interfaces link status. The TX will transmit either an idle symbol or a Halt symbol if the FX link is not established. Conversely the FX will transmit either an idle symbol or a Halt symbol if the TX link is not established. When an o Link" condition exists, the interface pin called LTNOLNK" will cause Halt symbols to be transmitted instead of idle symbols.

The link active LED is a static indication of the TX and FX links. It will be true to indicate the presence of a link. The receive data and error LED are generated through a ne-Shot" so that even the smallest receive or error condition will be indicated.

Absolute Maximum Ratings*

Absolute Maximum Ratings (25°C)

Symbol	Parameter	Min.	Max.	Unit	Conditions
VCC	Max. Supply Voltage	–	7.0	V	Non-operating
VIN	DC Input Voltage (VIN)	-0.5	5.5	V	
VOUT	DC Output Voltage(VOUT)	-0.5	5.5	V	
Tstg	Storage Temperature Rang (Tstg)	-65	+150	°C	
PD	Power Dissipation (PD)	—	1	W	
LT	Lead Temp. (TL, Soldering, 10 sec.)	—	240	°C	
ESD	ESD rating (Rzap=1.5K,Czap=100pF)	—	4000	V	

Operating Conditions

Symbol	Parameter	Min.	Max.	Unit	Conditions
DVCC,AVCC	Supply Voltage	4.75	—	5.25	
Tc	Case Temperature	0	85	°C	
PD (Power Dissipation)	100BASE-TX	—	200	mA	5V

***Comments**

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{CC} = 5V)

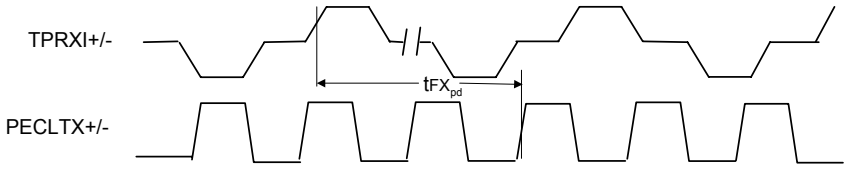
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
TTL Inputs (DPLXSEL, RESET#)						
V_{IL}	Input Low Voltage			0.8	V	I_{IL} = -400uA
V_{IH}	Input High Voltage	2.0			V	I_{IH} = 100uA
I_{IL}	Input Low Current	-200			uA	V_{IN} = 0.4V
I_{IH}	Input High Current			100	uA	V_{IN} = 2.7V
LED Driver Outputs (FXLINKLED#, TXLINKLED#, FXRXD#,RXRXD#)						
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 8mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -0.1mA
TPTX Receiver						
V_{ICM}	RXI+/RXI- Input Common-Mode Voltage	1.5	2.0	2.5	V	100 Ω Termination Across
TPTX Transmitter						
ITD100	100TXO+/- 100BASE-TX Mode Differential Output Current	|19|	|20|	|21|	mA	
PECL FX Transmitter						
IFD100	PECLTX+/- 100BASE-FX Mode Differential Output Current	|19|	|20|	|21|	mA	
V_{OH}	PECL Output Voltage – High	VCC-1.05		VCC-0.88	V	
V_{OL}	PECL Output Voltage – Low	VCC-1.81		VCC-1.62	V	

AC Electrical Characteristics (Over full range of operating condition unless specified otherwise)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Transmitter						
$t_{TR/F}$	100TXO+/- Differential Rise/Fall Time	3.0		5.0	ns	
t_{TM}	100TXO+/- Differential Rise/Fall Time Mismatch	-0.5		0.5	ns	
t_{TDC}	100TXO+/- Differential Output Duty Cycle Distortion	-0.5		0.5	ns	
$t_{T/T}$	100TXO+/- Differential Output Peak-to-Peak Jitter		300		ps	
X_{OST}	100TXO+/- Differential Voltage Overshoot			5	%	
PECL Transmitter (FX Transmit Interface)						
$pt_{TR/F}$	100FXTD+/- Differential Rise/Fall Time	1.0		2.0	ns	
pt_{TM}	100FXTD+/- Differential Rise/Fall Time Mismatch	-0.5		0.5	ns	
pt_{TDC}	100FXTD+/- Differential Output Duty Cycle Distortion	-0.5		0.5	ns	
pt_{PPJ}	100FXTD+/- Differential Output Peak-to-Peak Jitter			300	ps	
pt_{DDJ}	100FXTD+/- Differential Output Data Dependent Jitter			2.0	ns	
Clock Specifications						
X_{NTOL}	TX Input Clock Frequency Tolerance (Oscillator or Crystal input frequency)	-50		+50	ppm	25MHz Frequency
X_{BTOL}	TX Output Clock Frequency Tolerance	-100		+100	ppm	25MHz Frequency
t_{PWH}	OSC Pulse Width High	14			ns	
t_{PWL}	OSC Pulse Width Low	14			ns	
t_{RPWH}	RX_CLK Pulse Width High	14			ns	
t_{RPWL}	RX_CLK Pulse Width Low	14			ns	

Timing Waveforms

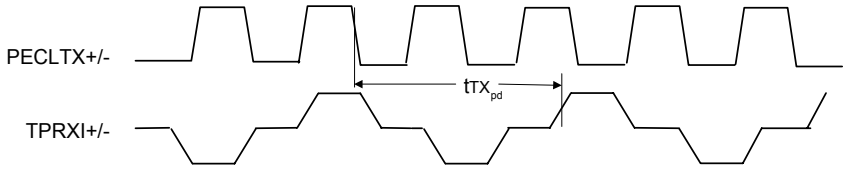
100BASE-TX to FX Transmit Timing Diagram



100BASE-TX to FX Transmit Timing Parameters

Symbol	Parameter	Min.	Typ[1].	Max.	Unit	Conditions
$t_{FX_{pd}}$	TPRXI+/- to PECLTX+/- Out (FX Latency)	-	-	10	BT	

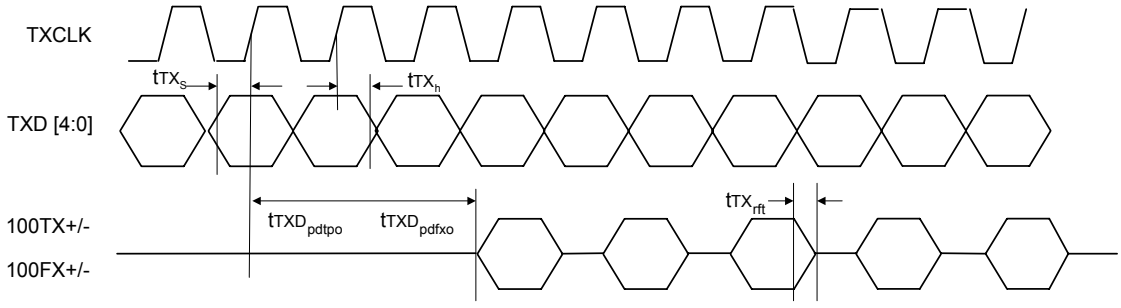
100BASE-FX to TX Transmit Timing Diagram



100BASE-FX to TX Transmit Timing Parameters

Symbol	Parameter	Min.	Typ[1].	Max.	Unit	Conditions
$t_{TX_{pd}}$	PECLRX+/- to TPTXo+/- Out (TX Latency)	-	-	10	BT	

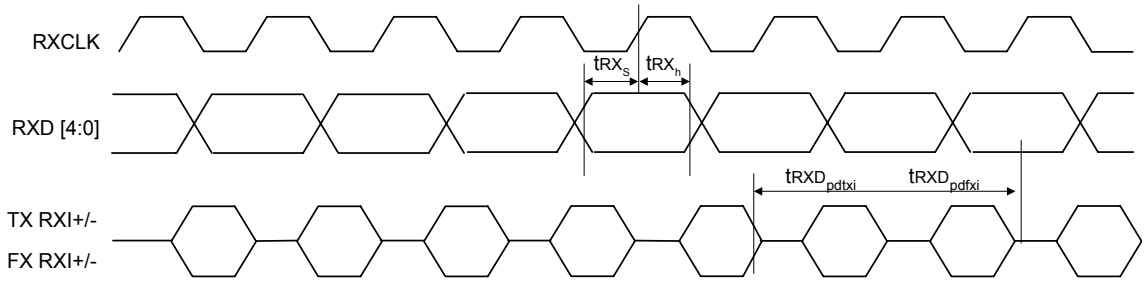
5-Bit Symbol 100Base-TX/FX Transmit Timing Diagram



5-Bit Symbol 100Base-TX/FX Transmit Timing Parameters

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Conditions
tTX_s	TXD[4:0] Setup To TX_CLK High	11	-	-	ns	
tTX_h	TXD[4:0] Hold From TX_CLK High	0	-	-	ns	
$tTXD_{pdtpo}$	TXD[4:0] Sampled To TPTXO (TXD to TP Latency)	-	-	6	BT	
$tTXD_{pdfxo}$	TXD[4:0] Sampled To PECLTXO (TXD to FX Latency)	-	-	4	BT	
$tTX_{r/f}$	100TX Driver Rise/Fall Time	3	4	5	ns	90% To 10%, Into 100ohm Differential
1. Typical values are at 25and are for design aid only; not guaranteed and not subject to production testing.						

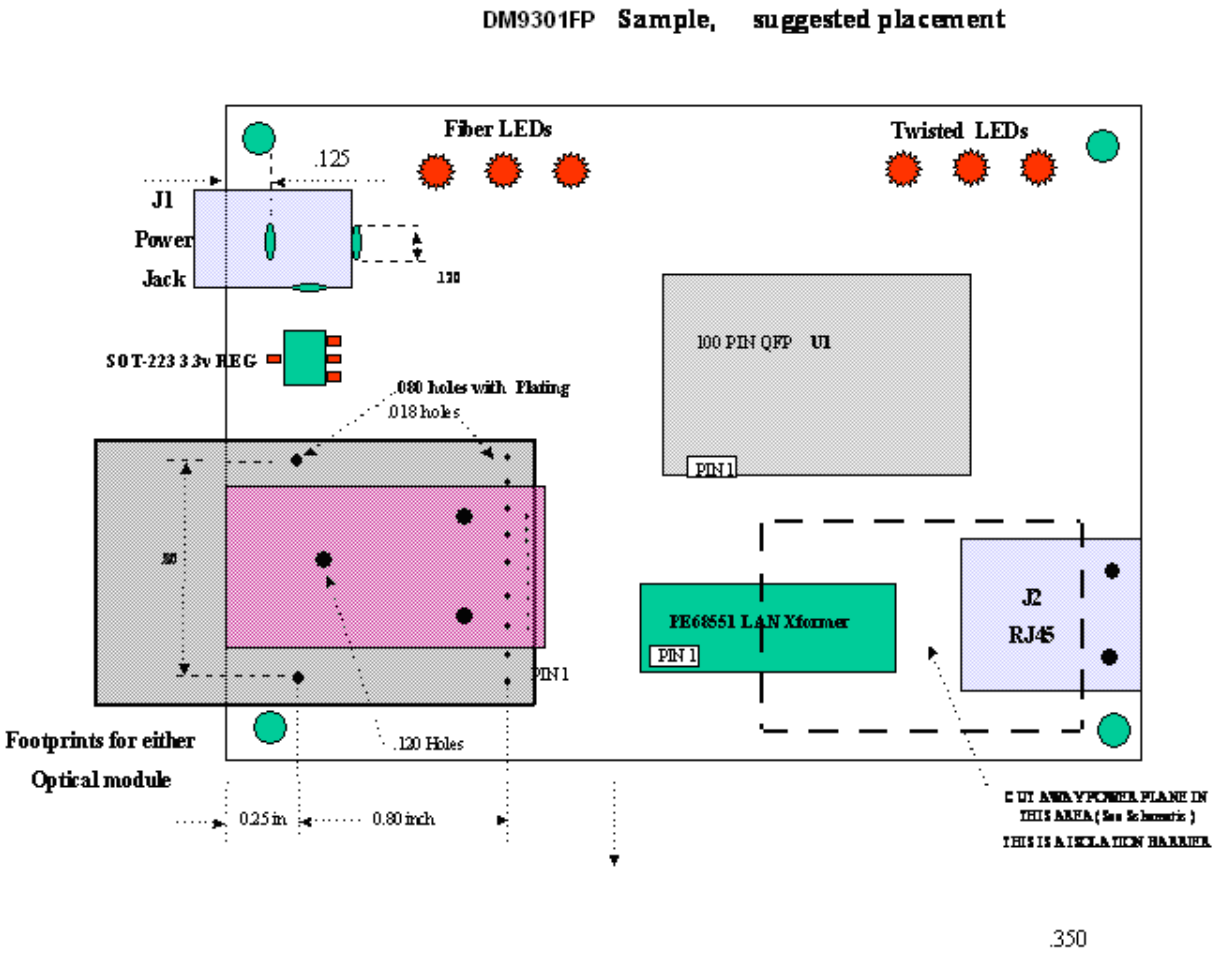
5-Bit Symbol 100Base-TX/FX Receive Timing Diagram



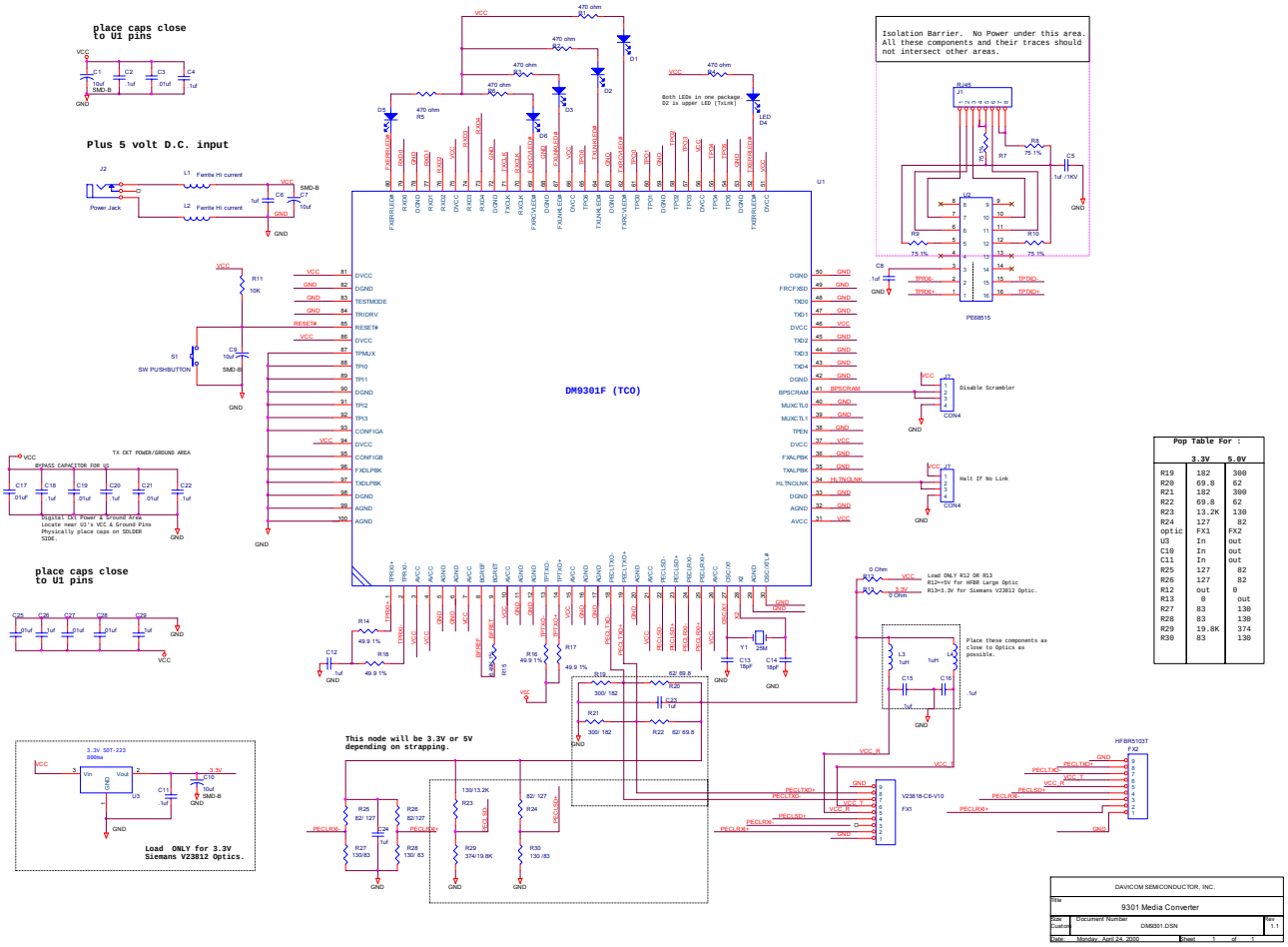
5-Bit Symbol 100Base-TX/FX Receive Timing Parameter

Symbol	Parameter	Min.	Typ[1].	Max.	Unit	Conditions
tRX_s	RXD[4:0) Setup To RX_CLK High	10	-	-	ns	
tRX_h	RXD[4:0]Hold From RX_CLK High	10	-	-	ns	
$tRXD_{pdtxi}$	TXRXI In To RXD[0:3] Out (Rx Latency)	-	-	6	BT	
$tRXD_{pdfxi}$	PECLRDI In To RXD[4:0] Out (Rx Latency)	-	-	4	BT	

MII Application Circuit: DM9301FP QFP (For Reference Only)

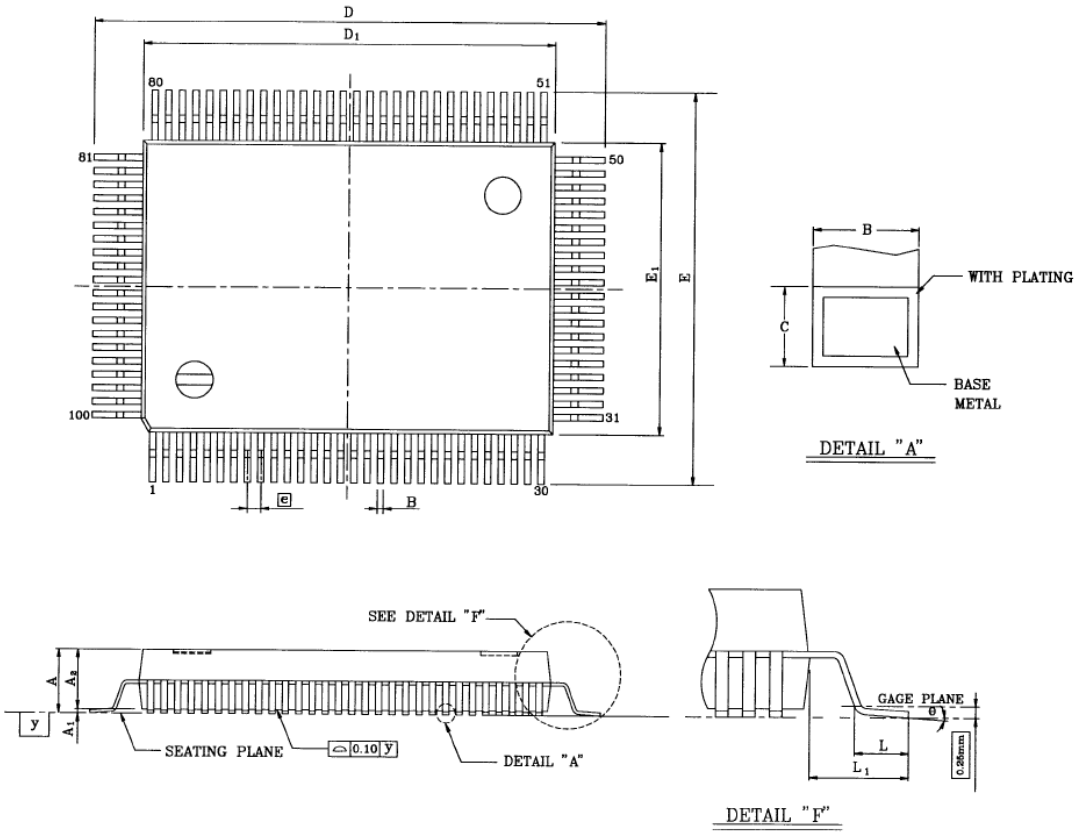


MII Application Circuit: DM9301FP QFP (For Reference Only)



Package Information

100 Pins QFP Package Outline Information:



Symbol	Dimension in mm				Dimension in inch		
	Min	Nom	Max		Min	Nom	Max
A	—	—	3.40		—	—	0.134
A_1	0.25	—	—		0.010	—	—
A_2	2.73	2.85	2.97		0.107	0.112	0.117
B	0.25	0.30	0.38		0.010	0.012	0.015
C	0.13	0.15	0.23		0.005	0.006	0.009
D	23.00	23.20	23.40		0.906	0.913	0.921
D_1	19.90	20.00	20.10		0.783	0.787	0.791
E	17.00	17.20	17.40		0.669	0.677	0.685
E_1	13.90	14.00	14.10		0.547	0.551	0.555
e	0.65 BSC				0.026 BSC		
L	0.73	0.88	1.03		0.029	0.035	0.041
L_1	1.60 BSC				0.063 BSC		
y	—	—	0.10		—	—	0.004
θ	0^o	—	7^o		0^o	—	7^o

1. Dimension D_1 and E_1 do not include resin fin.
2. All dimensions are base on metric system.
3. General appearance spec should base on its final visual inspection spec.

Ordering Information

Part Number	Pin Count	Package
DM9301FP	100	QFP (Pb-Free)

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WARNING

Conditions beyond those listed for the absolute maximum may destroy or damage the products. In addition, conditions for sustained periods at near the limits of the operating ranges will stress and may temporarily (and permanently) affect and damage structure, performance and/or function.