ANALOG DEVICES

DSP Microcomputer

Preliminary Technical Data ADSP-21161N

SUMMARY

- High performance 32-bit DSP—applications in audio, medical, military, wireless communications, graphics, imaging, motor-control, and telephony
- Super Harvard Architecture—four independent buses for dual data fetch, instruction fetch, and nonintrusive, zero-overhead I/O
- Code-compatible to all other SHARC Family DSPs
- Single-Instruction-Multiple-Data (SIMD) computational architecture—two 32-bit IEEE floating-point computation units, each with a multiplier, ALU, shifter, and register file
- Serial ports offer I^2S support via 8 programmable and simultaneous receive and transmit pins, which supports up to 16 transmit or 16 receive channels of audio
- Integrated peripherals—integrated I/O processor, 1 Mbit on-chip dual-ported SRAM, SDRAM controller, glueless multiprocessing features, and I/O ports (serial, link, external bus, SPI, & JTAG)
- ADSP-21161N supports 32-bit fixed, 32-bit float, and 40-bit floating point formats.

KEY FEATURES

- 100 MHz (10 ns) core instruction rate
- Single-cycle instruction execution, including SIMD operations in both computational units
- 600 MFLOPS peak and 400 MFLOPs sustained performance
- 225-ball 17x17mm PBGA package
- 1 Mbit on-chip dual-ported SRAM (0.5 Mbit block 0, 0.5 Mbit block 1) for independent access by core processor and DMA

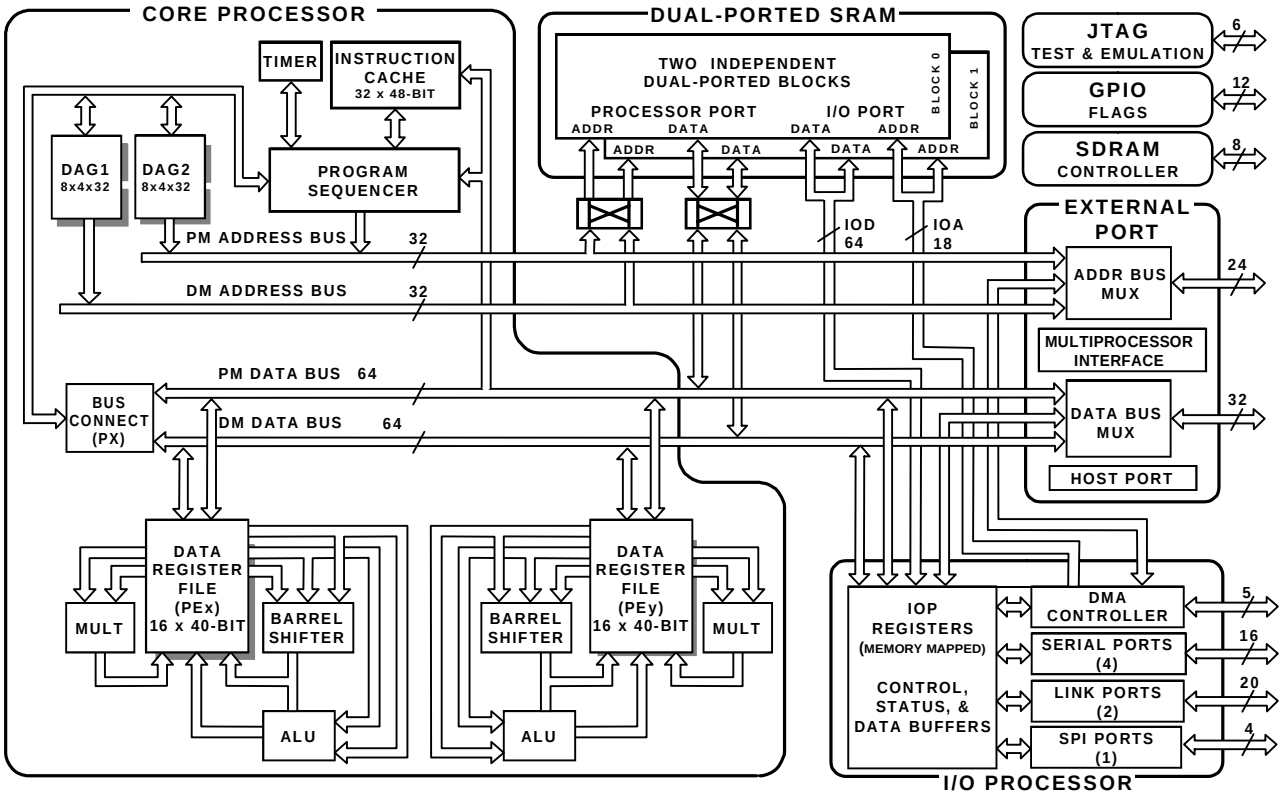

Figure 1 ADSP-21161N Functional Block Diagram

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KEY FEATURES (continued)

- 400 million fixed-point MACs sustained performance
- Dual Data Address Generators (DAGs) with modulo and bit-reverse addressing
- Zero-overhead looping with single-cycle loop setup, providing efficient program sequencing
- IEEE 1149.1 JTAG standard test access port and on-chip emulation
- Single Instruction Multiple Data (SIMD) architecture provides:
  - Two computational processing elements
  - Concurrent execution--Each processing element executes the same instruction, but operates on different data
  - Code compatibility--At assembly level, uses the same instruction set as other SHARC DSPs
- Parallelism in busses and computational units allows:
  - Single-cycle execution (with or without SIMD) of: a multiply operation, an ALU operation, a dual memory read or write, and an instruction fetch
  - Transfers between memory and core at up to four 32-bit floating- or fixed-point words per cycle, sustained 1.6 Gigabytes/second bandwidth
  - Accelerated FFT butterfly computation through a multiply with add and subtract
- DMA Controller supports:
  - 14 zero-overhead DMA channels for transfers between ADSP-21161N internal memory and external memory, external peripherals, host processor, serial ports, link ports or Serial Peripheral Interface (SPI) interface
  - 64-bit background DMA transfers at core clock speed, in parallel with full-speed processor execution
  - 800 Mbytes/s transfer rate over IOP bus
  - Host processor interface to 8-, 16- and 32-bit microprocessors, the host can directly read/write ADSP-21161N IOP registers.
- 32-bit (or up to 48-bit) wide synchronous External Port provides:
  - Glueless connection to asynchronous, SBSRAM and SDRAM external memories
  - Memory interface supports programmable wait state generation and wait mode for off-chip memory
  - Up to 50 MHz operation for non-SDRAM accesses
  - 1:2, 1:3, 1:4, 1:6, 1:8 clock in to Core Clock frequency multiply ratios
  - 24-bit address, 32-bit data bus. 16 additional data lines via multiplexed link port data pins allow complete 48-bit wide data bus for single-cycle external instruction execution
  - Direct reads and writes of IOP registers from host or other 21161N DSPs
  - 64 Mega-word address range for off-chip SRAM and SBSRAM memories
  - 32-48, 16-48, 8-48 execution packing for executing instruction directly from 32-bit, 16-bit, or 8-bit wide external memories
  - 32-48, 16-48, 8-48, 32-32/64, 16-32/64, 8-32/64, data packing for DMA transfers directly from 32-bit, 16-bit, or 8-bit wide external memories to and from internal 32-, 48-, or 64-bit internal memory
  - Can be configured to have 48-bit wide external data bus possible, if link ports are not

used. The link port data lines are multiplexed with the data lines D0 to D15 and is enabled through control bits in SYSCON

- SDRAM Controller for glueless interface to low cost external memory
  - Zero wait state, 100 MHz operation for most accesses
  - Extended external memory banks (64 M-words) for SDRAM accesses
  - Page sizes up to 2048 words
  - An SDRAM controller supports SDRAM in any and all memory banks
  - Support for interface to run at core clock & half the core clock frequency
  - Support for 16 Mbits, 64 Mbits, 128 Mbits, and 256 Mbits with SDRAM data bus configurations of x4, x8 and x16
  - 254 Mega-word address range for off-chip SDRAM memory
- Multiprocessing support provides:
  - Glueless connection for scalable DSP multiprocessing architecture
  - Distributed on-chip bus arbitration for parallel bus connect of up to six ADSP-21161Ns, global memory and a host
  - Two 8-bit wide link ports for point-to-point connectivity and array multiprocessing between ADSP-21161Ns
  - 400 Mbytes/s transfer rate over parallel bus
  - 200 Mbytes/s transfer rate over link ports
- Serial Ports provide:
  - Four 50 Mbit/s synchronous serial ports with companding hardware
  - 8 bi-directional serial data pins, configurable as either a transmitter or receiver
  - I^2S Support, programmable direction for 8 simultaneous Receive and Transmit channels, or up to either 16 Transmit channels or 16 Receive channels.
  - TDM support for T1 and E1 interfaces, and 128 TDM channel support for newer telephony interfaces such as H.100/H.110
  - Companding selection on a per channel basis in TDM mode
- Serial Peripheral Interface (SPI)
  - Slave Serial boot through SPI from a Master SPI device
  - Full-duplex operation
  - Master-Slave mode multi-master support
  - Open drain outputs
  - Programmable baud rates, clock polarities and phases
- 12 Programmable I/O pins

GENERAL DESCRIPTION

The ADSP-21161N SHARC DSP is the first low-cost derivative of the ADSP-21160 featuring Analog Devices' Super Harvard Architecture. Easing portability, the ADSP-21161N is source code compatible with the ADSP-21160 and with first generation ADSP-2106x SHARCs in SISD (Single Instruction, Single Data) mode. Like other SHARCs, the ADSP-21161N is a 32-bit processor that is optimized for high performance DSP applications. The ADSP-21161N includes a 100 MHz core, a dual-ported on-chip SRAM, an integrated I/O processor with multiprocessing support, and multiple internal busses to eliminate I/O bottlenecks.

The ADSP-21161N offers a Single-Instruction-Multiple-Data (SIMD) architecture, which was first offered in the ADSP-21160. Using two computational units (ADSP-2106x SHARCs have one), the ADSP-21161N can double cycle performance versus the ADSP-2106x on a range of DSP algorithms.

Fabricated in a state of the art, high speed, low power CMOS process, the ADSP-21161N has a 10 ns instruction cycle time. With its SIMD computational hardware running at 100 MHz, the ADSP-21161N can perform 600 million math operations per second. Table 1 shows performance benchmarks for the ADSP-21161N.

Table 1 ADSP-21161N Benchmarks (at 100 MHz)

Benchmark Algorithm	Speed (at 100 MHz)
1024 Point Complex FFT (Radix 4, with reversal)	92 µs
FIR Filter (per tap)	5 ns
IIR Filter (per biquad)	20 ns
Matrix Multiply (pipelined) [3x3] * [3x1] [4x4] * [4x1]	 45 ns 80 ns
Divide (y/x)	30 ns
Inverse Square Root	45 ns

The ADSP-21161N continues SHARC's industry leading standards of integration for DSPs, combining a high performance 32-bit DSP core with integrated, on-chip system features. These features include a 1 Mbit dual ported SRAM memory, host processor interface, I/O processor that supports 14 DMA channels, four serial ports, two link ports, SDRAM controller, SPI interface, external parallel bus, and glueless multiprocessing.

Figure 1 on page 1 shows a block diagram of the ADSP-21161N, illustrating the following architectural features:

- Two processing elements, each made up of an ALU, Multiplier, Shifter and Data Register File
- Data Address Generators (DAG1, DAG2)
- Program sequencer with instruction cache
- PM and DM buses capable of supporting four 32-bit data transfers between memory and the core every core processor cycle
- Interval timer

- On-Chip SRAM (1 Mbit)
- SDRAM Controller for glueless interface to SDRAMs
- External port that supports:
  - Interfacing to off-chip memory peripherals
  - Glueless multiprocessing support for six ADSP-21161N SHARCs
  - Host port read/write of IOP registers
- DMA controller
- Four serial ports
- Two link ports
- SPI-compatible interface
- JTAG test access port
- 12 General Purpose I/O Pins

Figure 2 shows a typical single-processor system. A multi-processing system appears in Figure 5 on page 11.

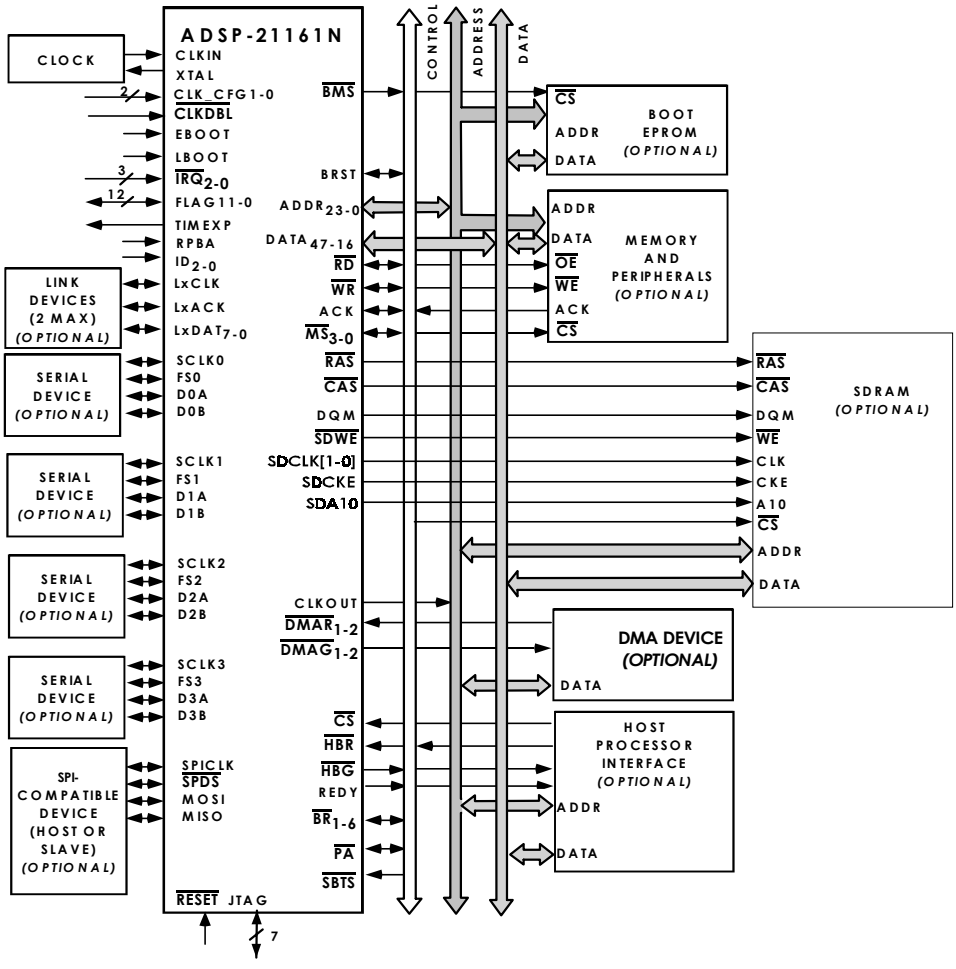


Figure 2 ADSP-21161N System

ADSP-21161N Family Core Architecture

The ADSP-21161N includes the following architectural features of the ADSP-21100 family core. The ADSP-21161N is code compatible at the assembly level with the ADSP-21160, ADSP-21060, ADSP-21061, and ADSP-21062 and ADSP-21065L.

SIMD Computational Engine

The ADSP-21161N contains two computational processing elements that operate as a Single Instruction Multiple Data (SIMD) engine. The processing elements are referred to as PEX and PEY and each contains an ALU, multiplier, shifter and register file. PEX is always active, and PEY may be enabled by setting the PEYEN mode bit in the MODE1 register. When this mode is enabled, the same instruction is executed in both processing elements, but each processing element operates on different data. This architecture is efficient at executing math intensive DSP algorithms.

Entering SIMD mode also has an effect on the way data is transferred between memory and the processing elements. When in SIMD mode, twice the data bandwidth is required to sustain computational operation in the processing elements. Because of this requirement, entering SIMD mode also doubles the bandwidth between memory and the processing elements. When using the DAGs to transfer data in SIMD mode, two data values are transferred with each access of memory or the register file.

Independent, Parallel Computation Units

Within each processing element is a set of computational units. The computational units consist of an arithmetic/logic unit (ALU), multiplier and shifter. These units perform single-cycle instructions. The three units within in each processing element are arranged in parallel, maximizing computational throughput. Single multi-function instructions execute parallel ALU and multiplier operations. In SIMD mode, the parallel ALU and multiplier operations occur in both processing elements. These computation units support IEEE 32-bit single-precision floating-point, 40-bit extended precision floating-point, and 32-bit fixed-point data formats.

Data Register File

A general purpose data register file is contained in each processing element. The register files transfer data between the computation units and the data buses, and store intermediate results. These 10-port, 32-register (16 primary, 16 secondary) register files, combined with the ADSP-21100 enhanced Harvard architecture, allow unconstrained data flow between computation units and internal memory. The registers in PEX are referred to as R0-R15 and in PEY as S0-S15.

Single-Cycle Fetch of Instruction and Four Operands

The ADSP-21161N features an enhanced Harvard architecture in which the data memory (DM) bus transfers data and the program memory (PM) bus transfers both instructions and data (see Figure 1 on page 1). With the ADSP-21161N's separate program and data memory buses and on-chip instruction cache, the processor can simultaneously fetch four operands (two over each data bus) and an instruction (from the cache), all in a single cycle.

Instruction Cache

The ADSP-21161N includes an on-chip instruction cache that enables three-bus operation for fetching an instruction and four data values. The cache is selective—only the instructions whose fetches conflict with PM bus data accesses are cached. This cache allows full-speed execution of core, looped operations such as digital filter multiply-accumulates and FFT butterfly processing.

Data Address Generators With Hardware Circular Buffers

The ADSP-21161N's two data address generators (DAGs) are used for indirect addressing and let you implement circular data buffers in hardware. Circular buffers allow efficient programming of delay lines and other data structures required in digital signal processing, and are commonly used in digital filters and Fourier transforms. The two DAGs of the ADSP-21161N contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets, 16 secondary). The DAGs automatically handle address pointer wrap-around, reducing overhead, increasing performance, and simplifying implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set

The 48-bit instruction word accommodates a variety of parallel operations, for concise programming. For example, the ADSP-21161N can conditionally execute a multiply, an add, and a subtract in both processing elements, while branching, all in a single instruction.

ADSP-21161N Memory and I/O Interface Features

Augmenting the ADSP-21100 family core, the ADSP-21161N adds the following architectural features:

Dual-Ported On-Chip Memory

The ADSP-21161N contains one megabit of on-chip SRAM, organized as two blocks of 0.5 Mbits each, which can be configured for different combinations of code and data storage. Each memory block is dual-ported for single-cycle, independent accesses by the core processor and I/O processor. The dual-ported memory in combination with three separate on-chip buses allow two data transfers from the core and one from the I/O processor, in a single cycle. On the ADSP-21161N, the memory can be configured as a maximum of 32K words of 32-bit data, 64K words of 16-bit data, 21.25K words of 48-bit instructions (or 40-bit data), or combinations of different word sizes up to one megabit. All of the memory can be accessed as 16-bit, 32-bit, 48-bit, or 64-bit words. A 16-bit floating-point storage format is supported that effectively doubles the amount of data that may be stored on-chip. Conversion between the 32-bit floating-point and 16-bit floating-point formats is done in a single instruction. While each memory block can store combinations of code and data, accesses are most efficient when one block stores data, using the DM bus for transfers, and the other block stores instructions and data, using the PM bus for transfers. Using the DM bus and PM bus in this way, with one dedicated to each memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache.

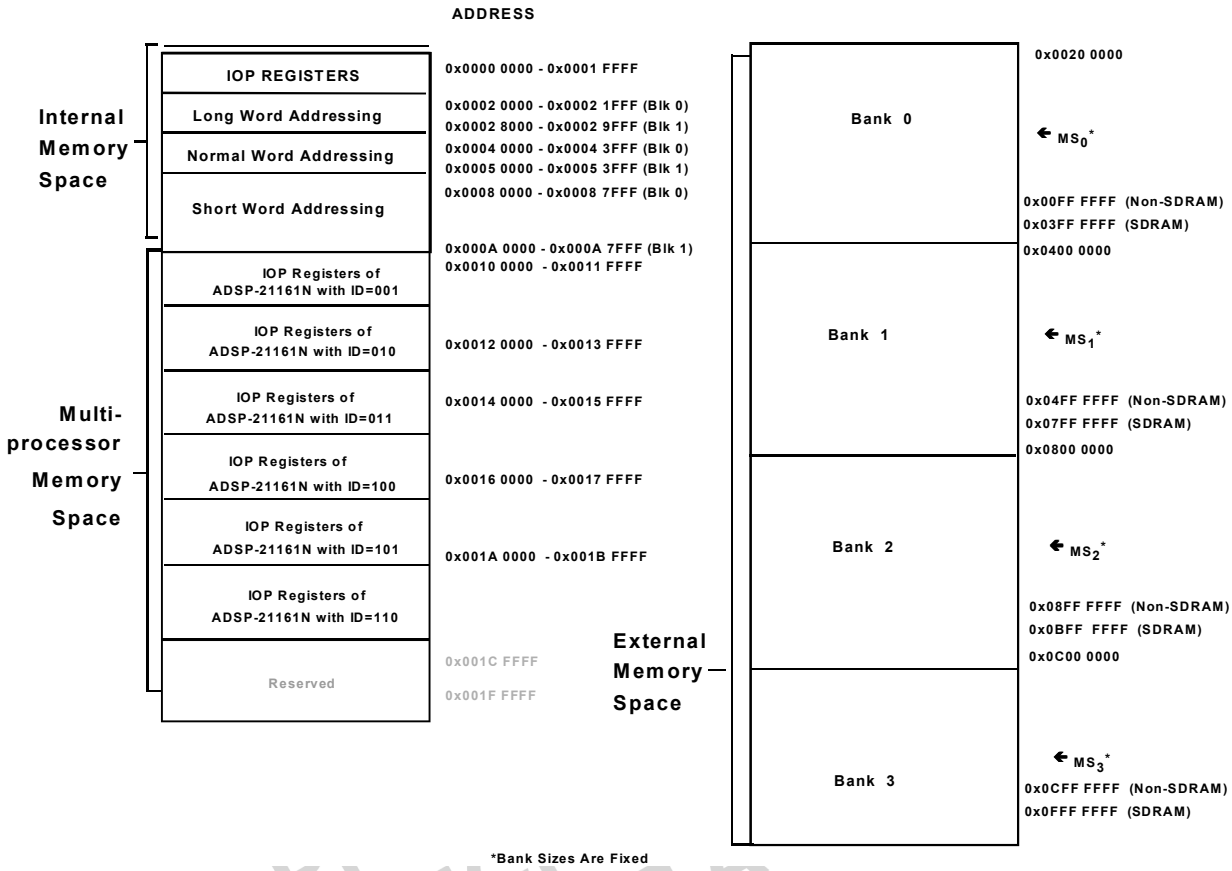


Figure 3 ADSP-21161N Memory Map

Off-Chip Memory and Peripherals Interface

The ADSP-21161N's external port provides the processor's interface to off-chip memory and peripherals. The 64-megaword off-chip address space (254-megaword if all SDRAM) is included in the ADSP-21161N's unified address space. The separate on-chip buses—for PM addresses, PM data, DM addresses, DM data, I/O addresses, and I/O data—are multiplexed at the external port to create an external system bus with a single 24-bit address bus and a single 32-bit data bus. Every access to external memory is based on an address that fetches a 32-bit word. When fetching an instruction from external memory, two 32-bit data locations are being accessed for packed instructions. Unused link port lines can also be used as additional data lines DATA[0]-DATA[15], allowing single cycle execution of instructions from external memory at up to 100 MHz. Figure 4 on page 10 shows the alignment of various accesses to external memory.

The external port supports asynchronous, synchronous, and synchronous burst accesses. Synchronous burst SRAM can be interfaced gluelessly. The ADSP-21161N also can interface gluelessly to SDRAM. Addressing of external memory devices is facilitated by on-chip decoding of high-order address lines to generate memory bank select signals. Separate control lines are also generated for simplified addressing of page-mode DRAM. The ADSP-21161N provides programmable memory wait states and external memory acknowledge controls to allow interfacing to memory and peripherals with variable access, hold, and disable time requirements.

SDRAM Interface

The SDRAM interface enables the ADSP-21161N to transfer data to and from synchronous DRAM (SDRAM) at the core clock frequency or one-half the core clock frequency. The synchronous approach, coupled with the core clock frequency, supports data transfer at a high throughput—up to 400 Mbytes/sec. for x32 transfers and 600 Mbytes/sec. for x48 transfers.

The SDRAM interface provides a glueless interface with standard SDRAMs—16 Mb, 64 Mb, 128 Mb, and 256 Mb—and includes options to support additional buffers between the ADSP-21161N and SDRAM. The SDRAM interface is extremely flexible and provides capability for connecting SDRAMs to any one of the ADSP-21161N's four external memory banks, with up to all four banks mapped to SDRAM.

Systems with several SDRAM devices connected in parallel may require buffering to meet overall system timing requirements. The ADSP-21161N supports pipelining of the address and control signals to enable such buffering between itself and multiple SDRAM devices.

DMA Controller

The ADSP-21161N's on-chip DMA controller allows zero-overhead data transfers without processor intervention. The DMA controller operates independently and invisibly to the processor core, allowing DMA operations to occur while the core is simultaneously executing its program instructions. DMA transfers can occur between the ADSP-21161N's internal memory and external memory, external peripherals, or a host processor. DMA transfers can also occur between the ADSP-21161N's internal memory and its serial ports, link ports, or the Serial Peripheral Interface (SPI)-compatible port. External bus packing and unpacking of 16-, 32-, 48-, or 64-bit words in internal memory is performed during DMA transfers from either 8-, 16-, or 32-bit wide external memory. Fourteen channels of DMA are available on the ADSP-21161N—two are shared between the SPI interface and the link ports, eight via the serial ports, and four via the processor's external port (for either host processor, other ADSP-21161Ns, memory or I/O transfers). Programs can be downloaded to the ADSP-21161N using DMA transfers. Asynchronous off-chip peripherals can control two DMA channels using DMA Request/Grant lines ($\overline{\text{DMAR}}_{1\text{-}2}$, $\overline{\text{DMAG}}_{1\text{-}2}$). Other DMA features include interrupt generation upon completion of DMA transfers, two-dimensional DMA, and DMA chaining for automatic linked DMA transfers.

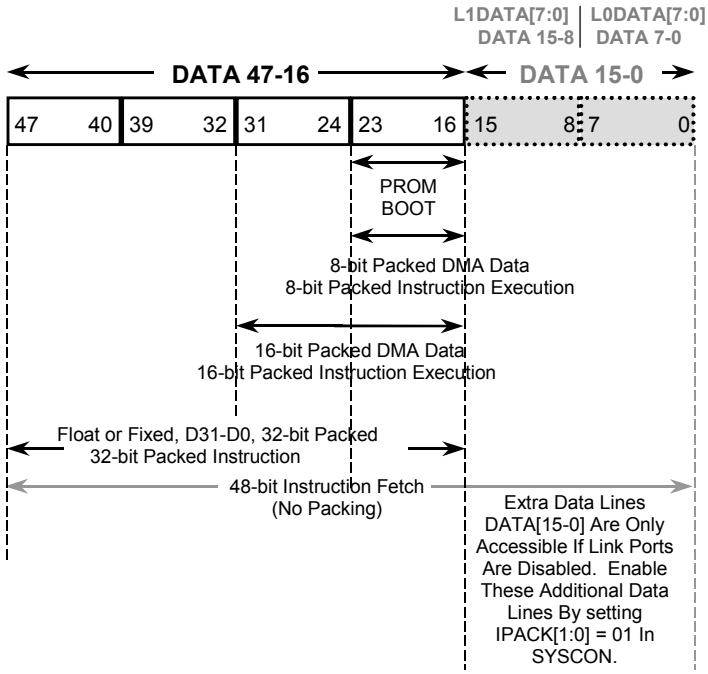


Figure 4 ADSP-21161N External Data Alignment Options

Multiprocessing

The ADSP-21161N offers powerful features tailored to multi-processing DSP systems. The external port and link ports provide integrated glueless multiprocessing support.

The external port supports a unified address space (see Figure 3 on page 8) that allows direct interprocessor accesses of each ADSP-21161N's internal memory-mapped (I/O processor) registers. All other internal memory can be indirectly accessed via DMA transfers initiated via the programming of the IOP DMA parameter and control registers. Distributed bus arbitration logic is included on-chip for simple, glueless connection of systems containing up to six ADSP-21161Ns and a host processor. Master processor change over incurs only one cycle of overhead. Bus arbitration is selectable as either fixed or rotating priority. Bus lock allows indivisible read-modify-write sequences for semaphores. A vector interrupt is provided for interprocessor commands. Maximum throughput for interprocessor data transfer is 400 Mbytes/s over the external port.

Two link ports provide for a second method of multiprocessing communications. Each link port can support communications to another ADSP-21161N. A large multiprocessor system can be constructed in a 2D fashion, using the link ports. The ADSP-21161N running at 100 MHz has a maximum throughput for interprocessor communications over the links of 200 Mbytes per second. You can use the link ports and cluster multiprocessing concurrently or independently.

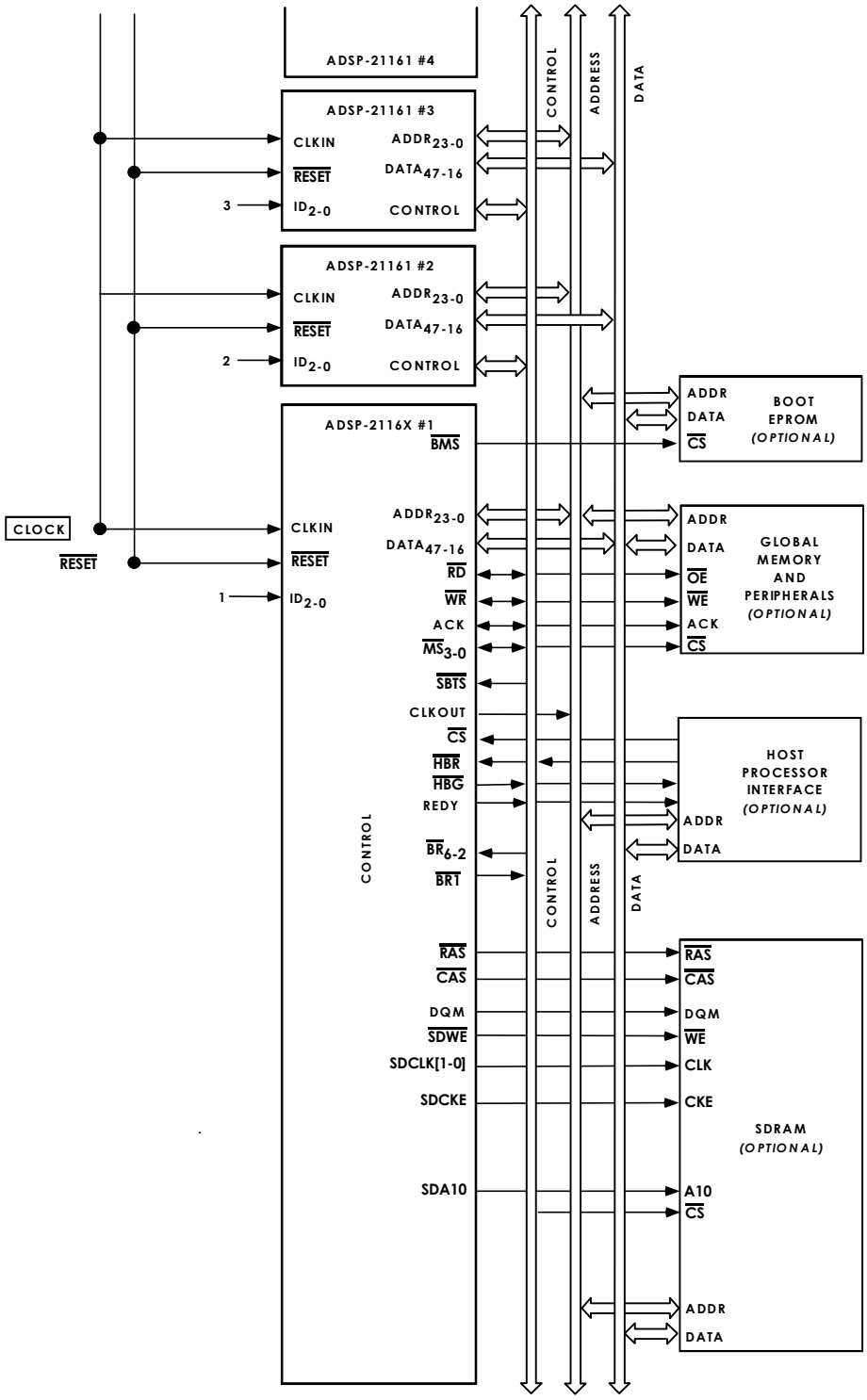


Figure 5 ADSP-21161N Shared Memory Multiprocessing System

Link Ports

The ADSP-21161N features two 8-bit link ports that provide additional I/O capabilities. With the capability of running at 100 MHz rates, each link port can support 100 Mbytes/s. Link port I/O is especially useful for point-to-point interprocessor communication in multiprocessing systems. The link ports can operate independently and simultaneously, with a maximum data throughput of 200 Mbytes/s. Link port data is packed into 48- or 32-bit words and can be directly read by the core processor or DMA-transferred to on-chip memory. Each link port has its own double-buffered input and output registers. Clock/acknowledge handshaking controls link port transfers. Transfers are programmable as either transmit or receive.

Serial Ports

The ADSP-21161N features four synchronous serial ports that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices. Each serial port is made up of two data lines, a clock and frame sync. The data lines can be programmed to be either transmit or receive.

The serial ports can operate up to half the clock rate of the core, providing each with a maximum data rate of 50 Mbit/s. The serial data pins can be programmable as either a transmitter or receiver, providing greater flexibility for serial communications. Serial port data can be automatically transferred to and from on-chip memory via a dedicated DMA. Each of the serial ports offers a Time Division Multiplex (TDM) multichannel mode, where two serial ports are TDM transmitters and two serial ports are TDM receivers (SPORT0 RX paired with SPORT2 TX, SPORT1 RX paired with SPORT3 TX). Each of the serial ports also support the I^2S protocol (an industry standard interface commonly used by audio codecs, ADCs and DACs), with two data pins, allowing four I^2S channels (using 2 I^2S stereo devices) per serial port, with a maximum of up to 16 I^2S channels. The serial ports can operate with little-endian or big-endian transmission formats, with word lengths selectable from 3 bits to 32 bits. For I^2S mode, data-word lengths are selectable between 8 bits and 32 bits. They offer selectable synchronization and transmit modes as well as optional µ-law or A-law companding. Serial port clocks and frame syncs can be internally or externally generated.

Serial Peripheral (Compatible) Interface

Serial Peripheral Interface (SPI) is an industry standard synchronous serial link, enabling the ADSP-21161N SPI-compatible port to communicate with other SPI-compatible devices. SPI is a 4-wire interface consisting of two data pins, one device select pin, and one clock pin. It is a full-duplex synchronous serial interface, supporting both master and slave modes. It can operate in a multi-master environment by interfacing with up to 4 other SPI-compatible devices, either acting as a master or slave device. The ADSP-21161N SPI-compatible peripheral implementation also supports programmable baud rate and clock phase/polarities. The ADSP-21161N SPI-compatible port supports the use of open drain drivers to support the multi-master scenario and to avoid data contention.

Host Processor Interface

The ADSP-21161N host interface allows easy connection to standard microprocessor buses, either 8-bit, 16-bit, or 32-bit, with little additional hardware required. The host interface is accessed through the ADSP-21161N's external port and is memory-mapped into the unified address space. Four channels of DMA are available for the host interface; code and data transfers are accomplished with low software overhead. The host processor requests the ADSP-21161N's external bus with the host bus request ($\overline{\text{HBR}}$), host bus grant ($\overline{\text{HBG}}$), and ready (REDY) signals. The host can directly read and write the internal IOP registers of the ADSP-21161N, and can access the DMA channel setup and mailbox registers. DMA setup via a host would allow it to access any internal memory address via DMA transfers. Vector interrupt support provides efficient execution of host commands.

General Purpose I/O Ports

The ADSP-21161N also contains twelve programmable, general purpose I/O pins that can function as either input or output. As output, these pins can signal peripheral devices; as input, these pins can provide the test for conditional branching.

Program Booting

The internal memory of the ADSP-21161N can be booted at system power-up from either an 8-bit EPROM, a host processor, the SPI interface, or through one of the link ports. Selection of the boot source is controlled by the Boot Memory Select ($\overline{BMS}$), EBOOT (EPROM Boot), and Link/Host Boot (LBOOT) pins. 8-, 16-, or 32-bit host processors can also be used for booting.

Phased Locked Loop and CLKIN Double Enable

The ADSP-21161N uses an on-chip Phase Locked Loop (PLL) to generate the internal clock for the core. The CLK_CFG[1:0] pins are used to select ratios of 2:1, 3:1, and 4:1. In addition to the PLL ratios, an additional $\overline{CLKDBL}$ pin can be used for additional clock ratio options. The (1x/2x CLKIN) rate set by the $\overline{CLKDBL}$ pin determines the rate of the PLL input clock and the rate at which the synchronous external port operates. With the combination of CLK_CFG[1:0] and $\overline{CLKDBL}$, ratios of 2:1, 3:1, 4:1, 6:1, and 8:1 between the core and CLKIN are supported. See also Figure 8 on page 28.

Power Supplies

The ADSP-21161N has separate power supply connections for the internal (VDDINT), external (VDDEXT), and analog (AVDD/AGND) power supplies. The internal and analog supplies must meet the 1.8V requirement. The external supply must meet the 3.3V requirement. All external supply pins must be connected to the same supply

Note that the analog supply (AV_{DD}) powers the ADSP-21161N's clock generator PLL. To produce a stable clock, you must provide an external circuit to filter the power input to the AV_{DD} pin. Place the filter as close as possible to the pin. For an example circuit, see Figure 6. To prevent noise coupling, use a wide trace for the analog ground (AGND) signal and install a decoupling capacitor as close as possible to the pin.

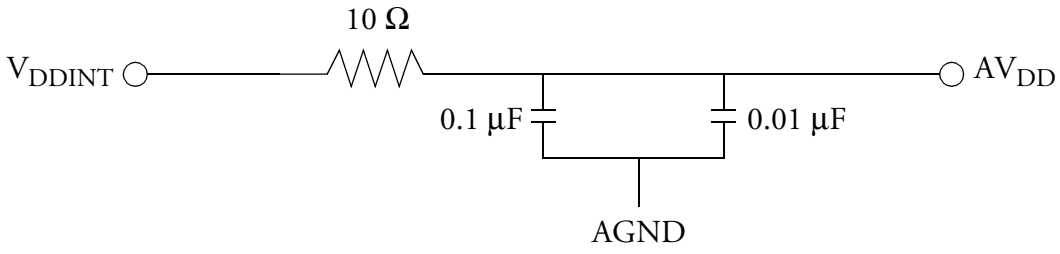


Figure 6 Analog Power (AV_{DD}) Filter Circuit

Development Tools

The ADSP-21161N is supported by a complete set of VisualDSP® software and hardware development tools, including the Analog Devices White Mountain line of JTAG emulator and development software. The same Analog Devices White Mountain line of JTAG emulator hardware that you use for the ADSP-21060/62/61/65L and ADSP-21160, also fully emulates the ADSP-21161N.

Both the SHARC Development Tools family and the VisualDSP integrated project management and debugging environment support the ADSP-21161N. The VisualDSP project management environment enables you to develop and debug an application from within a single, integrated program.

The SHARC Development Tools include an easy to use Assembler that is based on an algebraic syntax; an Assembly library/librarian; a linker; a loader; a cycle-accurate, instruction-level simulator; a C compiler; and a C run-time library that includes DSP and mathematical functions.

Debugging both C and Assembly programs with the Visual DSP debugger, enables you to:

- View mixed C and Assembly code
- Insert break points
- Set conditional breakpoints on registers, memory, and stacks
- Trace instruction execution
- Profile program execution
- Fill and dump memory
- Perform source-level debugging
- Create custom debugger windows

The VisualDSP IDE lets you define and manage DSP software development. Its dialog boxes and property pages enable you to configure and manage all of the SHARC Development Tools, including the syntax highlighting in the VisualDSP editor. This capability lets you:

- Control how the development tools process inputs and generate outputs.
- Maintain a one-to-one correspondence with the tool's command line switches.

Analog Devices White Mountain line of JTAG emulators use the IEEE 1149.1 JTAG test access port of the ADSP-21161N processor to monitor and control the target board processor during emulation. JTAG emulators provide emulation at full processor speed, allowing inspection and modification of memory, registers, and processor stacks. The processor's JTAG interface ensures the emulator will not affect target system loading or timing.

In addition to the software and hardware development tools available from Analog Devices, third parties provide a wide range of tools supporting the SHARC processor family. Hardware tools include SHARC PC plug-in cards, multiprocessor SHARC VME boards, a daughter board, and modules with multiple SHARCs and additional memory. Third Party software tools include DSP libraries, real-time operating systems, and block diagram design tools.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-21161N architecture and functionality. For detailed information on the ADSP-21100 Family core architecture and instruction set, refer to the *ADSP-21161N Technical Specification*.

PIN FUNCTION DESCRIPTIONS

ADSP-21161N pin definitions are listed below. Inputs identified as synchronous (S) must meet timing requirements with respect to CLKIN (or with respect to TCK for TMS, TDI). Inputs identified as asynchronous (A) can be asserted asynchronously to CLKIN (or to TCK for $\overline{\text{TRST}}$).

Unused inputs should be tied or pulled to VDDINT or GND, except for $\text{ADDR}_{23\text{-}0}$, $\text{DATA}_{47\text{-}16}$, $\text{FLAG}_{11\text{-}0}$, and inputs that have internal pull-up or pull-down resistors ($\overline{\text{PA}}$, ACK, BRST, CLKOUT,

$\overline{MS}_{3-0}$, $\overline{RD}$, $\overline{WR}$, $\overline{DMAR}_x$, $\overline{DMAG}_x$, DxA, DxB, SCLKx, $LxDAT_{7-0}$, LxCLK, LxACK, TMS, $\overline{TRST}$ and TDI)--these pins can be left floating. These pins have a logic-level hold circuit (only enabled on the ADSP-21161N with ID2-0=00x) that prevents input from floating internally.

The following symbols appear in the Type column of Table 2: A = Asynchronous, G = Ground, I = Input, O = Output, P = Power Supply, S = Synchronous, (A/D) = Active Drive, (O/D) = Open Drain, and T = Three-State (when $\overline{SBTS}$ is asserted or when the ADSP-21161N is a bus slave).

Table 2 Pin Descriptions

Pin	Type	Function
$ADDR_{23-0}$	I/O/T	**External Bus Address**. The ADSP-21161N outputs addresses for external memory and peripherals on these pins. In a multiprocessor system the bus master outputs addresses for read/writes of the IOP registers of other ADSP-21161Ns while all other internal memory resources can be accessed indirectly via DMA control (that is, accessing IOP DMA parameter registers). The ADSP-21161N inputs addresses when a host processor or multiprocessing bus master is reading or writing its IOP registers. A keeper latch on the DSP's $ADDR_{23-0}$ pins maintains the input at the level it was last driven (only enabled on the ADSP-21161N with ID2-0=00x).
$DATA_{47-16}$	I/O/T	**External Bus Data**. The ADSP-21161N inputs and outputs data and instructions on these pins. Pull-up resistors on unused data pins are not necessary. A keeper latch on the DSP's $DATA_{47-16}$ pins maintains the input at the level it was last driven (only enabled on the ADSP-21161N with ID2-0=00x). **Note:** *DATA[15:8] pins (multiplexed with L1DATA[7:0]) can also be used to extend the data bus if the link ports are disabled and will not be used. In addition, DATA[7:0] pins (multiplexed with L0DATA[7:0]) can also be used to extend the data bus if the link ports are not used. This allows execution of 48-bit instructions from external SBSRAM (system clock speed-external port), SRAM (system clock speed-external port) and SDRAM (core clock or one-half the core clock speed). The IPACKx Instruction Packing Mode Bits in SYSCON should be set correctly ($IPACK_{1-0}$ = 0x1) to enable this full instruction Width/No-packing Mode of operation.*
$\overline{MS}_{3-0}$	I/O/T	**Memory Select Lines**. These outputs are asserted (low) as chip selects for the corresponding banks of external memory. Memory bank sizes are fixed to 16 Mwords for non-SDRAM and 64 Mwords for SDRAM. The $\overline{MS}_{3-0}$ outputs are decoded memory address lines. In asynchronous access mode, the $\overline{MS}_{3-0}$ outputs transition with the other address outputs. In synchronous access modes, the $\overline{MS}_{3-0}$ outputs assert with the other address lines; however, they de-assert after the first CLKIN cycle in which ACK is sampled asserted. In a multiprocessor systems, the $\overline{MS}_x$ signals are tracked by slave SHARCs.

Table 2 Pin Descriptions (Continued)

Pin	Type	Function
$\overline{RD}$	I/O/T	**Memory Read Strobe.** $\overline{RD}$ is asserted whenever ADSP-21161N reads a word from external memory or from the IOP registers of other ADSP-21161Ns. External devices, including other ADSP-21161Ns, must assert $\overline{RD}$ for reading from a word of the ADSP-21161N IOP register memory. In a multiprocessing system, $\overline{RD}$ is driven by the bus master.
$\overline{WR}$	I/O/T	**Memory Write Low Strobe.** $\overline{WR}$ is asserted when ADSP-21161N writes a word to external memory or IOP registers of other ADSP-21161Ns. External devices must assert $\overline{WR}$ for writing to ADSP-21161N's IOP registers. In a multiprocessing system, $\overline{WR}$ is driven by the bus master.
BRST	I/O/T	**Sequential Burst Access.** BRST is asserted by ADSP-21161N to indicate that data associated with consecutive addresses is being read or written. A slave device samples the initial address and increments an internal address counter after each transfer. The incremented address is not pipelined on the bus. A master ADSP-21161N in a multiprocessor environment can read slave external port buffers (EPBx) using the burst protocol. BRST is asserted after the initial access of a burst transfer. It is asserted for every cycle after that, except for the last data request cycle (denoted by $\overline{RD}$ or $\overline{WR}$ asserted and BRST negated). A keeper latch on the DSP's BRST pin maintains the input at the level it was last driven (only enabled on the ADSP-21161N with ID2-0=00x).
ACK	I/O/S	**Memory Acknowledge**. External devices can de-assert ACK (low) to add wait states to an external memory access. ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access. The ADSP-21161N deasserts ACK as an output to add wait states to a synchronous access of its IOP registers.
$\overline{SBTS}$	I/S	**Suspend Bus & Three-State**. External devices can assert $\overline{SBTS}$ (low) to place the external bus address, data, selects, and strobes in a high impedance state for the following cycle. If the ADSP-21161N attempts to access external memory while $\overline{SBTS}$ is asserted, the processor will halt and the memory access will not be completed until $\overline{SBTS}$ is de-asserted. $\overline{SBTS}$ should only be used to recover from host processor/ADSP-21161N deadlock.
$\overline{CAS}$	I/O/T	**SDRAM Column Access Strobe.** In conjunction with $\overline{RAS}$, $\overline{MS}$x, $\overline{SDWE}$, SDCLKx, and sometimes SDA10, defines the operation for the SDRAM to perform.
$\overline{RAS}$	I/O/T	**SDRAM Row Access Strobe.** In conjunction with $\overline{CAS}$, $\overline{MS}$x, $\overline{SDWE}$, SDCLKx, and sometimes SDA10, defines the operation for the SDRAM to perform.
SDWE	I/O/T	**SDRAM Write Enable.** In conjunction with $\overline{CAS}$, $\overline{RAS}$, $\overline{MS}$x, SDCLKx, and sometimes SDA10, defines the operation for the SDRAM to perform.

Table 2 Pin Descriptions (Continued)

Pin	Type	Function
DQM	O/T	**SDRAM Data Mask.** In write mode, DQM has a latency of zero and is used during a precharge command and during SDRAM power-up initialization.
SDCLK0	I/O/S/T	**SDRAM Clock Output 0.** Clock for SDRAM devices.
SDCLK1	O/S/T	**SDRAM Clock Output 1.** Additional clock for SDRAM devices. For systems with multiple SDRAM devices, handles the increased clock load requirements, eliminating need of off-chip clock buffers. Either SDCLK1 or both SDCLKx pins can be three-stated.
SDCKE	I/O/T	**SDRAM Clock Enable.** Enables and disables the CLK signal. For details, see the data sheet supplied with your SDRAM device.
SDA10	O/T	**SDRAM A10 Pin.** Enables applications to refresh an SDRAM in parallel with a non-SDRAM accesses or host accesses.
IRQ2-0	I/A	**Interrupt Request Lines.** These are sampled on the rising edge of CLKIN and may be either edge-triggered or level-sensitive.
FLAG11-0	I/O/A	**Flag Pins**. Each is configured via control bits as either an input or output. As an input, it can be tested as a condition. As an output, it can be used to signal external peripherals.
TIMEXP	O	**Timer Expired**. Asserted for four CLKIN cycles when the timer is enabled and TCOUNT decrements to zero.
$\overline{\text{HBR}}$	I/A	**Host Bus Request**. Must be asserted by a host processor to request control of the ADSP-21161N's external bus. When $\overline{\text{HBR}}$ is asserted in a multiprocessing system, the ADSP-21161N that is bus master will relinquish the bus and assert $\overline{\text{HBG}}$. To relinquish the bus, the ADSP-21161N places the address, data, select, and strobe lines in a high impedance state. $\overline{\text{HBR}}$ has priority over all ADSP-21161N bus requests ($\overline{\text{BR6-1}}$) in a multiprocessing system.
$\overline{\text{HBG}}$	I/O	**Host Bus Grant**. Acknowledges an $\overline{\text{HBR}}$ bus request, indicating that the host processor may take control of the external bus. $\overline{\text{HBG}}$ is asserted (held low) by the ADSP-21161N until $\overline{\text{HBR}}$ is released. In a multiprocessing system, $\overline{\text{HBG}}$ is output by the ADSP-21161N bus master and is monitored by all others.
$\overline{\text{CS}}$	I/A	**Chip Select**. Asserted by host processor to select the ADSP-21161N.
REDY	O (O/D)	**Host Bus Acknowledge**. The ADSP-21161N de-asserts REDY (low) to add waitstates to a host access of its IOP registers when $\overline{\text{CS}}$ and $\overline{\text{HBR}}$ inputs are asserted.
$\overline{\text{DMAR1}}$	I/A	**DMA Request 1** (DMA Channel 11). Asserted by external port devices to request DMA services.

Table 2 Pin Descriptions (Continued)

Pin	Type	Function
$\overline{\text{DMAR2}}$	I/A	**DMA Request 2** (DMA Channel 12). Asserted by external port devices to request DMA services.
$\overline{\text{DMAG1}}$	O/T	**DMA Grant 1** (DMA Channel 11). Asserted by ADSP-21161N to indicate that the requested DMA starts on the next cycle. Driven by bus master only.
$\overline{\text{DMAG2}}$	O/T	**DMA Grant 2** (DMA Channel 12). Asserted by ADSP-21161N to indicate that the requested DMA starts on the next cycle. Driven by bus master only.
$\overline{\text{BR}}_{6\text{-}1}$	I/O/S	**Multiprocessing Bus Requests**. Used by multiprocessing ADSP-21161Ns to arbitrate for bus mastership. An ADSP-21161N only drives its own $\overline{\text{BR}}$x line (corresponding to the value of its ID2-0 inputs) and monitors all others. In a multiprocessor system with less than six ADSP-21161Ns, the unused $\overline{\text{BR}}$x pins should be pulled high; the processor's own $\overline{\text{BR}}$x line must not be pulled high or low because it is an output.
$\overline{\text{BMSTR}}$	O	**Bus Master Output.** In a multiprocessor system, indicates whether the ADSP-21161N is current bus master of the shared external bus. The ADSP-21161N drives $\overline{\text{BMSTR}}$ high only while it is the bus master. In a single-processor system (ID = 000), the processor drives this pin high.
ID2-0	I	**Multiprocessing ID**. Determines which multiprocessing bus request (BR1 - BR6) is used by ADSP-21161N. ID = 001 corresponds to BR1, ID = 010 corresponds to BR2, and so on. Use ID = 000 or ID = 001 in single-processor systems. These lines are a system configuration selection that should be hardwired or only changed at reset.
RPBA	I/S	**Rotating Priority Bus Arbitration Select**. When RPBA is high, rotating priority for multiprocessor bus arbitration is selected. When RPBA is low, fixed priority is selected. This signal is a system configuration selection that must be set to the same value on every ADSP-21161N. If the value of RPBA is changed during system operation, it must be changed in the same CLKIN cycle on every ADSP-21161N.
$\overline{\text{PA}}$	I/O/T	**Priority Access**. Asserting its $\overline{\text{PA}}$ pin allows an ADSP-21161N bus slave to interrupt background DMA transfers and gain access to the external bus. $\overline{\text{PA}}$ is connected to all ADSP-21161Ns in the system. If access priority is not required in a system, the $\overline{\text{PA}}$ pin should be left unconnected.
DxA	I/O	**Data Transmit or Receive Channel A** (Serial Ports 0, 1, 2, 3). Each DxA pin has a 50 kΩ internal pull-up resistor. Bidirectional data pin. This signal can be configured as an output to transmit serial data, or as an input to receive serial data.
DxB	I/O	**Data Transmit or Receive Channel B** (Serial Ports 0, 1, 2, 3). Each DxB pin has a 50 kΩ internal pull-up resistor. Bidirectional data pin. This signal can be configured as an output to transmit serial data, or as an input to receive serial data.

Table 2 Pin Descriptions (Continued)

Pin	Type	Function
SCLKx	I/O	**Transmit/Receive Serial Clock** (Serial Ports 0, 1, 2, 3). Each SCLK pin has a 50 kΩ internal pull-up resistor. This signal can be either internally or externally generated.
FSx	I/O	**Transmit or Receive Frame Sync** (Serial Ports 0, 1, 2, 3). The frame sync pulse initiates shifting of serial data. This signal is either generated internally or externally. It can be active high or low or an early or a late frame sync, in reference to the shifting of serial data.
SPICLK	I/O	**Serial Peripheral Interface Clock Signal**. Driven by the master, this signal controls the rate at which data is transferred. The master may transmit data at a variety of baud rates. SPICLK cycles once for each bit transmitted. SPICLK is a gated clock that is active during data transfers, only for the length of the transferred word. Slave devices ignore the serial clock if the slave select input is driven inactive (HIGH). SPICLK is used to shift out and shift in the data driven on the MISO and MOSI lines. The data is always shifted out on one clock edge of the clock and sampled on the opposite edge of the clock. Clock polarity and clock phase relative to data are programmable into the SPICTL control register and define the transfer format.
$\overline{\text{SPIDS}}$	I	**Serial Peripheral Interface Slave Device Select.** An active low signal used to enable slave devices. This input signal behaves like a chip select, and is provided by the master device for the slave devices. In multi-master mode $\overline{\text{SPIDS}}$ signal can be asserted to a master device to signal that an error has occurred, as some other device is also trying to be the master device. If asserted low when the device is in master mode, it is considered a multi-master error. For a Single-Master, Multiple-Slave configuration where $\text{FLAG}_{3\text{-}0}$ are used, this pin must be tied high to VDDINT. For ADSP-21161N to ADSP-21161N SPI interaction, any of the master ADSP-21161N's $\text{FLAG}_{3\text{-}0}$ pins can be used to drive the $\overline{\text{SPIDS}}$ signal on the ADSP-21161N SPI slave device.
MOSI	I/O	**SPI Master Out Slave.** If the ADSP-21161N is configured as a master, the MOSI pin becomes a data transmit (output) pin, transmitting output data. If the ADSP-21161N is configured as a slave, the MOSI pin becomes a data receive (input) pin, receiving input data. In an ADSP-21161N SPI interconnection, the data is shifted out from the MOSI output pin of the master and shifted into the MOSI input(s) of the slave(s).
MISO	I/O	**SPI Master In Slave Out.** If the ADSP-21161N is configured as a master, the MISO pin becomes a data receive (input) pin, receiving input data. If the ADSP-21161N is configured as a slave, the MISO pin becomes a data transmit (output) pin, transmitting output data. In an ADSP-21161N SPI interconnection, the data is shifted out from the MISO output pin of the slave and shifted into the MISO input pin of the master. Note: *Only one slave is allowed to transmit data at any given time.*

Table 2 Pin Descriptions (Continued)

Pin	Type	Function
LxDAT7-0 [DATA15-0]	I/O [I/O/T]	**Link Port Data** (Link Ports 0-1). Each LxDAT pin has a 50 kΩ internal pull-down resistor that is enabled or disabled by the LPDRD bit of the LCTL0-1 register. **Note:** *L1DATA[7:0] are multiplexed with the DATA[15:8] pinsL0DATA[7:0] are multiplexed with the DATA[7:0] pins. If link ports are disabled and are not be used, then these pins can be used as additional data lines for executing instructions at up to the full clock rate from external memory. See* $DATA_{47:16}$ *on page 15 for more information.*
LxCLK	I/O	**Link Port Clock** (Link Ports 0-1). Each LxCLK pin has a 50 kΩ internal pull-down resistor that is enabled or disabled by the LPDRD bit of the LCTL register.
LxACK	I/O	**Link Port Acknowledge** (Link Ports 0-1). Each LxACK pin has a 50 kΩ internal pull-down resistor that is enabled or disabled by the LPDRD bit of the LCOM register.
EBOOT	I	**EPROM Boot Select**. For a description of how this pin operates, see the table in the $\overline{\text{BMS}}$ pin description. This signal is a system configuration selection that should be hardwired.
LBOOT	I	**Link Boot**. For a description of how this pin operates, see the table in the $\overline{\text{BMS}}$ pin description. This signal is a system configuration selection that should be hardwired.
$\overline{\text{BMS}}$	I/O/T	**Boot Memory Select**. Serves as an output or input as selected with the EBOOT and LBOOT pins; see table below. This input is a system configuration selection that should be hardwired. EBOOT / LBOOT / BMS / Booting Mode 1 / 0 / Output / EPROM (Connect BMS to EPROM chip select.) 0 / 0 / 1 (Input) / Host Processor 0 / 1 / 0 (Input) / Serial Boot via SPI 0 / 1 / 1 (Input) / Link Port 0 / 0 / 0 (Input) / No Booting. Processor executes from external memory. 1 / 1 / x (Input) / Reserved For Host and PROM boot, DMA channel 10 (EPB0) is used. For Link Boot and SPI boot, DMA channel 8 is used. *Three-statable only in EPROM boot mode (when $\overline{\text{BMS}}$ is an output).

Table 2 Pin Descriptions (Continued)

Pin	Type	Function
CLKIN	I	**Local Clock In.** Used in conjunction with XTAL. CLKIN is the ADSP-21161N clock input. It configures the ADSP-21161N to use either its internal clock generator or an external clock source. Connecting the necessary components to CLKIN and XTAL enables the internal clock generator. Connecting the external clock to CLKIN while leaving XTAL unconnected configures the ADSP-21161N to use the external clock source such as an external clock oscillator.The ADSP-21161N external port cycles at the frequency of CLKIN. The instruction cycle rate is a multiple of the CLKIN frequency; it is programmable at power-up via the CLK_CFG1-0 pins. CLKIN may not be halted, changed, or operated below the specified frequency.
XTAL	O	**Crystal Oscillator Terminal 2.** Used in conjunction with CLKIN to enable the ADSP-21161N's internal clock generator or to disable it to use an external clock source. *See* CLKIN.
CLK_CFG1-0	I	**Core/CLKIN Ratio Control.** ADSP-21161N core clock (instruction cycle) rate is equal to n x PLLICLK where n is user selectable to 2, 3, or 4, using the CLK_CFG1-0 inputs. These pins can also be used in combination with the CLKDBL pin to generate additional core clock rates of 6 x CLKIN and 8 x CLKIN (*see* Table 3- Clock Rate Ratios below).

Table 2 Pin Descriptions (Continued)

Pin	Type	Function
$\overline{\text{CLKDBL}}$	I	**Clock Double Mode Enable.** This pin is used to enable the 2x clock double circuitry, where CLKOUT can be configured as either 1x or 2x the rate of CLKIN. The 2x clock mode is enabled (during $\overline{\text{RESET}}$ low) by tying $\overline{\text{CLKDBL}}$ to GND, otherwise it is connected to VDDEXT for 1x clock mode. This is mainly intended for external crystals to increase external port clock rate operation. For example, this allows the use of a 25 MHz crystal to enable 100 MHz core clock rates and a 50 MHz external port operation when CLK_CFG1='0', CLK_CFG1 = '0' and $\overline{\text{CLKDBL}}$ = '0'. This pin can also be used to generate different clock rate ratios for external clock oscillators as well. The possible clock rate ratio options (up to 100 MHz) for either CLKIN (external clock oscillator) or XTAL (crystal input) are as follows: Table 3 **Clock Rate Ratios** $\overline{\text{CLKDBL}}$ / CLK_CFG1 / CLK_CFG0 / Core Clock Ratio / EP Clock Ratio 1 / 0 / 0 / 2:1 / 1x 1 / 0 / 1 / 3:1 / 1x 1 / 1 / 0 / 4:1 / 1x 0 / 0 / 0 / 4:1 / 2x 0 / 0 / 1 / 6:1 / 2x 0 / 1 / 0 / 8:1 / 2x An 8:1 ratio allows the use of a 12.5 MHz crystal to generate a 100 MHz core (instruction clock) rate and a 25 MHz CLKOUT (external port) clock rate. See also Figure 8 on page 28. **Note:** *When using an external crystal, the maximum crystal frequency cannot exceed 25 Mhz. For all other external clock sources, the maximum CLKIN frequency is 50 MHz.*
CLKOUT	O/T	**Local Clock Out.** CLKOUT is 1x or 2x and is driven at either 1x or 2x the frequency of CLKIN frequency by the current bus master. The frequency is determined by the $\overline{\text{CLKDBL}}$ pin. This output is three-stated when the ADSP-21161N is not the bus master or when the host controls the bus ($\overline{\text{HBG}}$ asserted). A keeper latch on the DSP's CLKOUT pin maintains the output at the level it was last driven (only enabled on the ADSP-21161N with ID2-0=00x). If $\overline{\text{CLKDBL}}$ enabled, CLKOUT = 2xCLKIN If $\overline{\text{CLKDBL}}$ disabled, CLKOUT = 1xCLKIN **Note:** *CLKOUT is only controlled by the $\overline{\text{CLKDBL}}$ pin and operates at either 1xCLKIN or 2xCLKIN.*
$\overline{\text{RESET}}$	I/A	**Processor Reset**. Resets the ADSP-21161N to a known state and begins execution at the program memory location specified by the hardware reset vector address. The $\overline{\text{RESET}}$ input must be asserted (low) at power-up.

Table 2 Pin Descriptions (Continued)

Pin	Type	Function
TCK	I	**Test Clock (JTAG)**. Provides a clock for JTAG boundary scan.
TMS	I/S	**Test Mode Select (JTAG)**. Used to control the test state machine. TMS has a 20 kΩ internal pull-up resistor.
TDI	I/S	**Test Data Input (JTAG)**. Provides serial data for the boundary scan logic. TDI has a 20 kΩ internal pull-up resistor.
TDO	O	**Test Data Output (JTAG)**. Serial scan output of the boundary scan path.
$\overline{\text{TRST}}$	I/A	**Test Reset (JTAG)**. Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the ADSP-21161N. $\overline{\text{TRST}}$ has a 20 kΩ internal pull-up resistor.
$\overline{\text{EMU}}$	O (O/D)	**Emulation Status**. Must be connected to the ADSP-21161N Analog Devices White Mountain line of JTAG emulators target board connector only. $\overline{\text{EMU}}$ has a 50 kΩ internal pullup resistor.
VDDINT	P	**Core Power Supply.** Nominally +1.8 V dc and supplies the DSP's core processor (14 pins).
VDDEXT	P	**I/O Power Supply**; Nominally +3.3 V dc. (13 pins).
AVDD	P	**Analog Power Supply**; Nominally +1.8 V dc and supplies the DSP's internal PLL (clock generator). This pin has the same specifications as VDDINT, except that added filtering circuitry is required. For more information, see "Power Supplies" on page 13.
AGND	G	**Analog Power Supply Return**.
GND	G	**Power Supply Return** (26 pins).
NC		**Do Not Connect**. Reserved pins that must be left open and unconnected. (5 pins).

CLOCK SIGNALS

The ADSP-21161N can use an external clock or a crystal. See CLKIN pin description. You can configure the ADSP-21161N to use its internal clock generator by connecting the necessary components to CLKIN and XTAL. Figure 7 shows the component connections used for a crystal operating in fundamental mode.

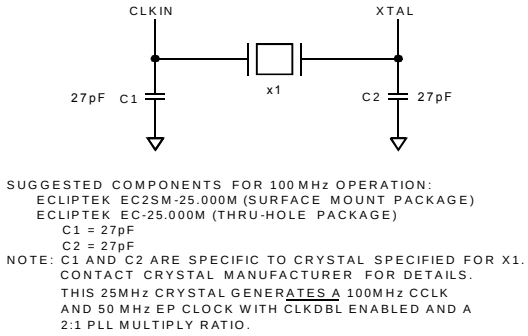


Figure 7 100 MHz Operation (Fundamental Mode Crystal)

Target Board JTAG Emulator Connector

Analog Devices White Mountain line of JTAG emulators uses the IEEE 1149.1 JTAG test access port of the ADSP-21161N processor to monitor and control the target board processor during emulation. Analog Devices White Mountain line of JTAG emulators provides emulation at full processor speed, allowing inspection and modification of memory, registers, and processor stacks. The processor's JTAG interface ensures that the emulator will not affect target system loading or timing.

For complete information on SHARC Analog Devices White Mountain line of JTAG emulator operation, see the appropriate "ICE™ Emulator Hardware User's Guide". For detailed information on the interfacing of Analog Devices JTAG emulators with Analog Devices DSP products with JTAG emulation ports, please refer to Engineer to Engineer Note EE-68, "Analog Devices JTAG Emulation Technical Reference". Both of these documents can be found on the Analog Devices web-site:

http://www.analog.com/dsp/tech_docs.html

ADSP-21161N-Specifications

Note that component specifications are subject to change without notice.

Table 4 Recommended Operating Conditions

Signal	K Grade Parameter	Min	Max	Units
V_{DDINT}	Internal (Core) Supply Voltage	1.71	1.89	V
AV_{DD}	Analog (PLL) Supply Voltage	1.71	1.89	V
V_{DDEXT}	External (I/O) Supply Voltage	3.13	3.47	V
V_{IH1}	High Level Input Voltage[1], @ VDDEXT = max	2.0	V_{DDEXT}+0.5	V
V_{IH2}	High Level Input Voltage[2], @ VDDEXT = max	2.2	V_{DDEXT}+0.5	V
V_{IL}	Low Level Input Voltage[1,2], @ VDDEXT = min	-0.5	0.8	V
T_{CASE}	Case Operating Temperature[3]	0	+85	°C

1. Applies to input and bidirectional pins: $DATA_{47-16}$, $ADDR_{23-0}$, $\overline{MS}_{3-0}$, $\overline{RD}$, $\overline{WR}$, ACK, $\overline{SBTS}$, $\overline{IRQ}_{2-0}$, $FLAG_{11-0}$, $\overline{HBG}$, $\overline{CS}$, $\overline{DMAR}_1$, $\overline{DMAR}_2$, $\overline{BR}_{6-1}$, ID_{2-0}, RPBA, $\overline{PA}$, BRST, FSx, DxA, DxB, SCLKx, $\overline{RAS}$, $\overline{CAS}$, $\overline{SDWE}$, $SDCLK_0$, LxDAT3-0, LxCLK, Lx-ACK, SPICLK, MOSI, MISO, $\overline{SPIDS}$, EBOOT, LBOOT, $\overline{BMS}$, TDO, $\overline{EMU}$.
2. Applies to input pins: CLKIN, $\overline{RESET}$, $\overline{TRST}$.
3. See "Environmental Conditions" on page 72 for information on thermal specifications.

Table 5 Electrical Characteristics

Parameter		Test Conditions	Min	Max	Units
V_{OH}	High Level Output Voltage[1]	@ V_{DDEXT} = min, I_{OH} = -2.0 mA[2]	2.4		V
V_{OL}	Low Level Output Voltage[1]	@ V_{DDEXT} = min, I_{OL} = 4.0 mA[2]		0.4	V
I_{IH}	High Level Input Current[3,4]	@ V_{DDEXT} = max, V_{IN} = V_{DDEXT} max		10	µA
I_{IL}	Low Level Input Current[3]	@ V_{DDEXT} = max, V_{IN} = 0 V		10	µA
I_{ILP}	Low Level Input Current[4]	@ V_{DDEXT} = max, V_{IN} = 0 V		150	µA
I_{OZH}	Three-State Leakage Current[5,6,7,8]	@ V_{DDEXT}= max, V_{IN} = V_{DDEXT} max		10	µA
I_{OZL}	Three-State Leakage Current[5,9]	@ V_{DDEXT} = max, V_{IN} = 0 V		10	µA
I_{OZHP}	Three-State Leakage Current[9]	@ V_{DDEXT} = max, V_{IN} = V_{DDEXT} max		350	µA
I_{OZLAR}	Three-State Leakage Current[8]	@ V_{DDEXT} = max, V_{IN} = 0 V		4.2	mA

Table 5 Electrical Characteristics (Continued)

Parameter		Test Conditions	Min	Max	Units
I_{OZLA}	Three-State Leakage Current[10]	@ V_{DDEXT} = max, V_{IN} = 1.5 V		350	µA
I_{OZLS}	Three-State Leakage Current[6]	@ V_{DDEXT} = max, V_{IN} = 0 V		150	µA
$I_{DD-INPEAK}$	Supply Current (Internal)[11]	t_{CCLK} = 10.0 ns, V_{DDINT} = max		TBD	mA
$I_{DD-INHIGH}$	Supply Current (Internal)[12]	t_{CCLK} = 10.0 ns, V_{DDINT} = max		TBD	mA
$I_{DD-INLOW}$	Supply Current (Internal)[13]	t_{CCLK} = 10.0 ns, V_{DDINT} = max		TBD	mA
$I_{DD-IDLE}$	Supply Current (Idle)[14]	V_{DDINT} = max		TBD	mA
AI_{DD}	Supply Current (Analog)[15]	@AV_{DD} = max		10	mA
C_{IN}	Input Capacitance[16,17]	f_{IN}=1 MHz, T_{CASE}=25°C, V_{IN}=1.8V		4.7	pF

1. Applies to output and bidirectional pins: $DATA_{47-16}$, $ADDR_{23-0}$, $\overline{MS}_{3-0}$, $\overline{RD}$, $\overline{WR}$, ACK, $FLAG_{11-0}$, TIMEXP, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR6-1}$, $\overline{PA}$, BRST, LxDAT7-0, LxCLK, LxACK, SPICLK, MOSI, MISO, $\overline{BMS}$, TDO, $\overline{EMU}$.
2. See "Output Drive Currents" on page 67 for typical drive current capabilities.
3. Applies to input pins: ACK, $\overline{SBTS}$, $\overline{IRQ}_{2-0}$, $\overline{HBR}$, $\overline{CS}$, $\overline{DMAR}_1$, $\overline{DMAR}_2$, ID2-0, RPBA, EBOOT, $\overline{SPIDS}$, LBOOT, CLKIN, RESET, TCK.
4. Applies to input pins with internal pull-ups: $\overline{TRST}$, TMS, TDI.
5. Applies to three-statable pins: $DATA_{47-16}$, $ADDR_{24-0}$, $\overline{MS}_{3-0}$, $\overline{RD}$, $\overline{WR}$, CLKOUT, ACK, $FLAG_{11-0}$, REDY, $\overline{HBG}$, $\overline{DMAG}_1$, $\overline{DMAG}_2$, $\overline{BMS}$, $\overline{BR}_{6-1}$, TDO, $\overline{EMU}$. (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when ID2-0 = 001 and another ADSP-21161N is not requesting bus mastership.)
6. Applies to three-statable pins with internal pull-ups: DxA, DxB, SCLKx, SPICLK.
7. Applies to $\overline{PA}$ pin.
8. Applies to ACK pin when pulled up. (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when ID2-0 = 001 and another ADSP-21161N is not requesting bus mastership).
9. Applies to three-statable pins with internal pull-downs: LxDAT7-0, LxCLK, LxACK.
10. Applies to ACK pin when keeper latch enabled.
11. The test program used to measure $I_{DDINPEAK}$ represents worst case processor operation and is not sustainable under normal application conditions. Actual internal power measurements made using typical applications are less than specified. For more information, see "Power Dissipation" on page 67.
12. $I_{DDINHIGH}$ is a composite average based on a range of high activity code. For more information, see "Power Dissipation" on page 67.
13. $I_{DDINLOW}$ is a composite average based on a range of low activity code. For more information, see "Power Dissipation" on page 67.
14. Idle denotes ADSP-21161N state during execution of IDLE instruction. For more information, see "Power Dissipation" on page 67.
15. Characterized, but not tested.
16. Applies to all signal pins.
17. Guaranteed, but not tested.

Table 6 Absolute Maximum Ratings[1]

Parameter	Absolute Maximum Rating
Internal (Core) Supply Voltage (V_{DDINT})	-0.3 V to +2.2 V
Analog (PLL) Supply Voltage (AV_{DD})	-0.3 V to +2.2 V
External (I/O) Supply Voltage (V_{DDEXT})	-0.3 V to +4.6 V
Input Voltage	-0.5 V to V_{DDEXT} + 0.5 V **TBD**
Output Voltage Swing	-0.5 V to V_{DDEXT} + 0.5 V **TBD**
Load Capacitance	200 pF
Storage Temperature Range	-65°C to +150°C
Lead Temperature (5 seconds)	+185°C

1. Stresses greater than those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Sensitivity

CAUTION: ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADSP-21161N features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Timing Specifications

The ADSP-21161N's internal clock switches at higher frequencies than the system input clock (CLKIN). To generate the internal clock, the DSP uses an internal phase-locked loop (PLL). This PLL-based clocking minimizes the skew between the system clock (CLKIN) signal and the DSP's internal clock (the clock source for the external port logic and I/O pads).

The ADSP-21161N's internal clock (a multiple of CLKIN) provides the clock signal for timing internal memory, processor core, link ports, serial ports, and external port (as required for read/write strobes in asynchronous access mode). During reset, program the ratio between the DSP's internal clock frequency and external (CLKIN) clock frequency with the CLK_CFG1-0 and $\overline{\text{CLKDBL}}$ pins. Even though the internal clock is the clock source for the external port, it is behaves as described on the Clock Rate Ratio chart in $\overline{\text{CLKDBL}}$ pin description (see the $\overline{\text{CLKDBL}}$ description on page 22). To determine switching frequencies for the serial and link ports, divide down the internal clock, using the programmable divider control of each port (DIVx for the serial ports and LxCLKD1-0 for the link ports).

Note the following definitions of various clock periods that are a function of CLKIN and the appropriate ratio control.

Figure 8, "Core Clock and System Clock Relationship to CLKIN" allows Core-to-CLKIN ratios of 1:1, 2:1, 3:1, 4:1, 6:1, and 8:1 with external oscillator or crystal:

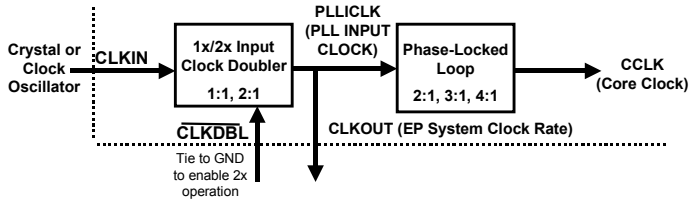


Figure 8 Core Clock and System Clock Relationship to CLKIN

Table 7 ADSP-21161N CLKOUT and CCLK Clock Generation Operation

Timing Requirements		Calculation		Description
CLKIN	=	$1/t_{CKIN}$	=	Input Clock
CLKOUT	=	$1/t_{TCK}$	=	External Port System Clock
PLLICLK	=	$1/t_{PLLIN}$	=	PLL Input Clock
CCLK	=	$1/t_{CCLK}$	=	Core Clock

Notes:

1. *If $\overline{CLKDBL}$ is enabled (tied low at reset), then CLKOUT = PLLICLK = 2xCLKIN. Otherwise, CLKOUT = PLLICLK = CLKIN.*
2. *CCLK = Core Clock = PLLICLK x PLL Multiply Ratio (determined by CLK_CFG pins).*

Table 8 Clock Relationships

Timing Requirements		Description[1]
t_{CK}	=	CLKOUT Clock Period
t_{CCLK}	=	(Processor) Core Clock Period
t_{LCLK}	=	Link Port Clock Period = (t_{CCLK}) * LR
t_{SCLK}	=	Serial Port Clock Period = (t_{CCLK}) * SR
t_{SDK}	=	SDRAM Clock Period = (t_{CCLK}) * SDCKR
t_{SPICLK}	=	SPI Clock Period = (t_{CCLK}) * SPIR

1. where:
   LR = link port-to-core clock ratio (1, 2, 3, or 1:4, determined by LxCLKD)
   SR = serial port-to-core clock ratio (wide range, determined by CLKDIV)
   SDCKR = SDRAM-to-Core Clock Ratio (1:1 or 1:2, determined by SDCTL register)
   SPIR = SPI-to-Core Clock Ratio (wide range, determined by SPICTL register)
   LCLK = Link Port Clock
   SCLK = Serial Port Clock
   SDK = SDRAM Clock
   SPICLK = SPI Clock

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, it is not meaningful to add parameters to derive longer times.

See Figure 37 on page 70 under Test Conditions for voltage reference levels.

Switching Characteristics specify how the processor changes its signals. Circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics describe what the processor will do in a given circumstance. Use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing Requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

Table 9 Clock Input

Parameter		100 MHz		
		Min	Max	Units
Timing Requirements				
t_{CK}	CLKIN Period	20	TBD	ns
t_{CKL}	CLKIN Width Low	8	40	ns
t_{CKH}	CLKIN Width High	8	40	ns
t_{CKRF}	CLKIN Rise/Fall (0.4V-2.0V)		3	ns

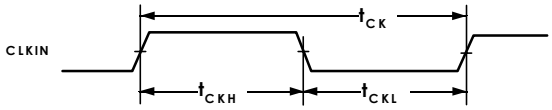


Figure 9 Clock Input

Table 10 Reset

Parameter		Min	Max	Units
Timing Requirements				
t_{WRST}	$\overline{\text{RESET}}$ Pulse Width Low[1]	$4t_{CK}$		ns
t_{SRST}	$\overline{\text{RESET}}$ Setup Before CLKIN High[2]	7.3		ns

1. Applies after the power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 100 µs while $\overline{\text{RESET}}$ is low, assuming stable VDD and CLKIN (not including start-up time of external clock oscillator).
2. Only required if multiple ADSP-21161Ns must come out of reset synchronous to CLKIN with program counters (PC) equal. Not required for multiple ADSP-21161Ns communicating over the shared bus (through the external port), because the bus arbitration logic synchronizes itself automatically after reset.

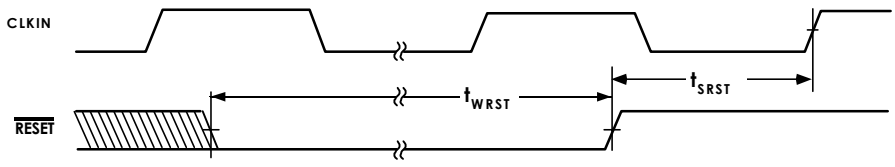


Figure 10 Reset

Table 11 Interrupts

Parameter		Min	Max	Units
Timing Requirements				
t_{SIR}	$\overline{IRQ}_{2-0}$ Setup Before CLKOUT High[1]	8.3		ns
t_{HIR}	$\overline{IRQ}_{2-0}$ Hold After CLKOUT High[1]	-1.6		ns
t_{IPW}	$\overline{IRQ}_{2-0}$ Pulse Width[2]	2 + t_{CK}		ns

1. Only required for $\overline{IRQ}_x$ recognition in the following cycle.
2. Applies only if t_{SIR} and t_{HIR} requirements are not met.

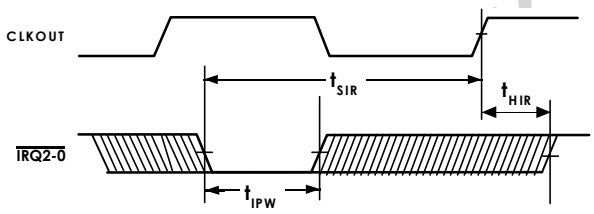


Figure 11 Interrupts

Timer

Table 12 Timer

Parameter		Min	Max	Units
Switching Characteristic				
t_{DTEX}	CLKOUT High to TIMEXP	-0.9	5.2	ns

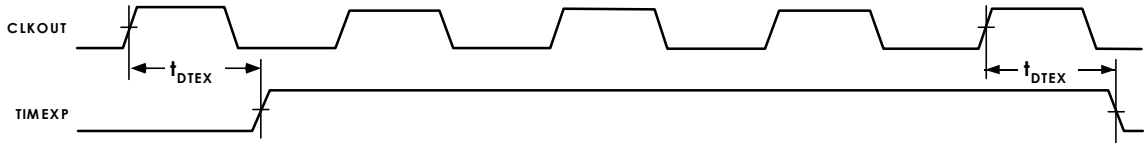


Figure 12 Timer

Table 13 Flags

Parameter		Min	Max	Units
Timing Requirement				
t_{SFI}	FLAG11-0IN Setup Before CLKOUT High[1]	6.3		ns
t_{HFI}	FLAG11-0IN Hold After CLKOUT High[1]	-0.6		ns
t_{DWRFI}	FLAG11-0IN Delay After $\overline{RD}/\overline{WR}$ Low[1]		TBD	ns
t_{HFIWR}	FLAG11-0IN Hold After $\overline{RD}/\overline{WR}$ Deasserted[1]	TBD		ns
Switching Characteristics				
t_{DFO}	FLAG11-0OUT Delay After CLKOUT High		7.2	ns
t_{HFO}	FLAG11-0OUT Hold After CLKOUT High	-0.9		ns
t_{DFOE}	CLKOUT High to FLAG11-0OUT Enable	-0.9		ns
t_{DFOD}	CLKOUT High to FLAG11-0OUT Disable		3.2	ns

1. Flag inputs meeting these setup and hold times for instruction cycle N will affect conditional instructions in instruction cycle N+2.

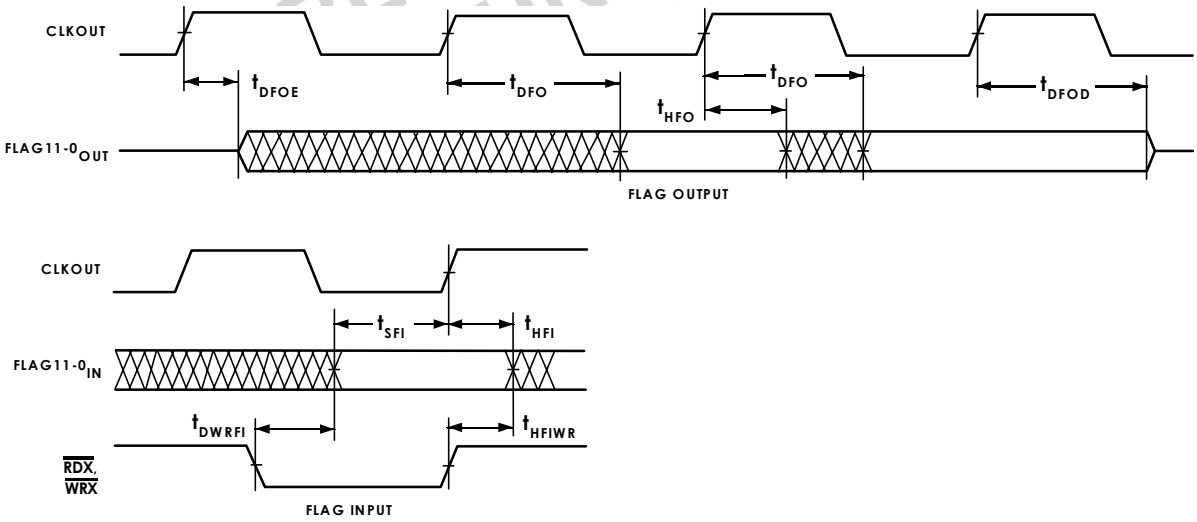


Figure 13 Flags

Memory Read--Bus Master

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) without reference to CLKOUT. These specifications apply when the ADSP-21161N is the bus master accessing external memory space in asynchronous access mode. Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and $\overline{DMAG}$ strobe timing parameters only apply to asynchronous access mode.

Table 14 Memory Read--Bus Master

Parameter		Min	Max	Units
Timing Requirements:				
t_{DAD}	Address, Selects Delay to Data Valid[1,2]		t_{CK}–.25t_{CCLK}–11+W	ns
t_{DRLD}	$\overline{RD}$ Low to Data Valid[1,3]		.75t_{CK}–11+W	ns
t_{HDA}	Data Hold from Address, Selects[4]	0		ns
t_{SDS}	Data Setup to $\overline{RD}$ High	2		ns
t_{HDRH}	Data Hold from $\overline{RD}$ High[3,4]	1		ns
t_{DAAK}	ACK Delay from Address, Selects[2,5]		t_{CK}–.5t_{CCLK}–12+W	ns
t_{DSAK}	ACK Delay from $\overline{RD}$ Low[3,5]		t_{CK}–.75t_{CCLK}–11+W	ns
t_{SAKC}	ACK Setup to CLKOUT[3,5]	.5t_{CCLK}+5.3		ns
t_{HAKC}	ACK Hold After CLKOUT[3]	-0.6		ns
Switching Characteristics				
t_{DRHA}	Address Selects Hold After $\overline{RD}$ High[3]	.25t_{CCLK}–1+H		ns
t_{DARL}	Address Selects to $\overline{RD}$ Low[2]	.25t_{CCLK}–1		ns
t_{RW}	$\overline{RD}$ Pulse Width[3]	t_{CK}–.5t_{CCLK}–1+W		ns
t_{RWR}	$\overline{RD}$ High to $\overline{WR}$, $\overline{RD}$, $\overline{DMAG}_x$ Low[3]	.5t_{CCLK}–1+HI		ns

W = (number of wait states specified in WAIT register) × t_{CK}.
HI = t_{CK} (if an address hold cycle or bus idle cycle occurs, as specified in WAIT register; otherwise HI = 0).
H = t_{CK} (if an address hold cycle occurs as specified in WAIT register; otherwise H = 0).

1. Data Delay/Setup: User must meet t_{DAD}, t_{DRLD}, or t_{SDS}.
2. The falling edge of $\overline{MS}_x$, $\overline{BMS}$ is referenced.
3. Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and $\overline{DMAG}$ strobe timing parameters only apply to asynchronous access mode.

4. Data Hold: User must meet t_{HDA} or t_{HDRH} in asynchronous access mode. See "Example System Hold Time Calculation" on page 69 for the calculation of hold times given capacitive and dc loads.
5. ACK Delay/Setup: User must meet t_{DAAK}, t_{DSAK}, or t_{SAKC} for deassertion of ACK (Low), all three specifications must be met for assertion of ACK (High).

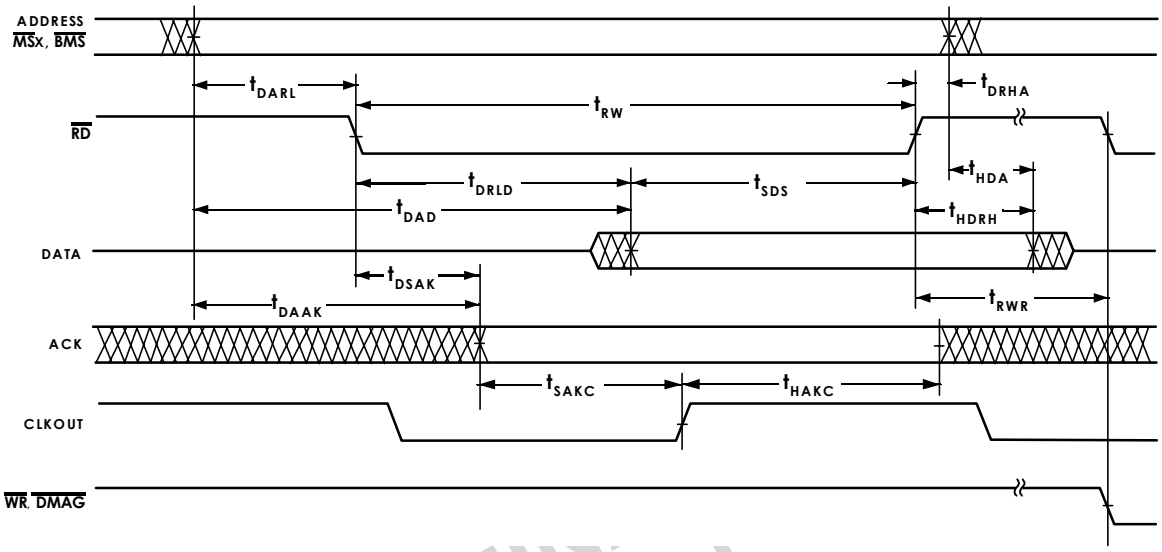


Figure 14 Memory Read--Bus Master

Memory Write--Bus Master

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) without reference to CLKOUT. These specifications apply when the ADSP-21161N is the bus master accessing external memory space in asynchronous access mode. Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and $\overline{DMAG}$ strobe timing parameters only apply to asynchronous access mode.

Table 15 Memory Write--Bus Master

Parameter		Min	Max	Units
Timing Requirements				
t_{DAAK}	ACK Delay from Address, Selects[1,2]		t_{CK}–.5t_{CCLK}–12+W	ns
t_{DSAK}	ACK Delay from $\overline{WR}$ Low[1,3]		t_{CK}–.75t_{CCLK}–11+W	ns
t_{SAKC}	ACK Setup to CLKOUT[1,3]	.5t_{CCLK}+5.3		ns
t_{HAKC}	ACK Hold After CLKOUT[1,3]	-0.6		ns
Switching Characteristics				
t_{DAWH}	Address Selects to $\overline{WR}$ Deasserted[2,3]	t_{CK}–.25t_{CCLK}–2+W		ns
t_{DAWL}	Address Selects to $\overline{WR}$ Low[2]	.25t_{CCLK}–2		ns
t_{WW}	$\overline{WR}$ Pulse Width[3]	t_{CK}–.5t_{CCLK}–1+W		ns
t_{DDWH}	Data Setup before $\overline{WR}$ High[3]	t_{CK}–.25t_{CCLK}– 12.5+W		ns
t_{DWHA}	Address Hold after $\overline{WR}$ Deasserted[3]	.25t_{CCLK}–1+H		ns
t_{DWHD}	Data Hold after $\overline{WR}$ Deasserted[3]	.25t_{CCLK}–1+H		ns
t_{DATRWH}	Data Disable after $\overline{WR}$ Deasserted[3,4]	.25t_{CCLK}–1+H	.25t_{CCLK}+2+H	ns
t_{WWR}	$\overline{WR}$ High to $\overline{WR}$, $\overline{RD}$, $\overline{DMAGx}$ Low[3]	.5t_{CCLK}–1+HI		ns
t_{DDWR}	Data Disable before $\overline{WR}$ or $\overline{RD}$ Low	.25t_{CCLK}–1+I		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	–.25t_{CCLK}–1		ns

Table 15 Memory Write--Bus Master

Parameter	Min	Max	Units
W = (number of wait states specified in WAIT register) × t_{CK}. H = t_{CK} (if an address hold cycle occurs, as specified in WAIT register; otherwise H = 0). HI = t_{CK} (if an address hold cycle or bus idle cycle occurs, as specified in WAIT register; otherwise HI = 0). I = t_{CK} (if a bus idle cycle occurs, as specified in WAIT register; otherwise I = 0).			

1. ACK Delay/Setup: User must meet t_{DAAK} or t_{DSAK} or t_{SAKC} for deassertion of ACK (Low), all three specifications must be met for assertion of ACK (High).
2. The falling edge of $\overline{MS}_x$, $\overline{BMS}$ is referenced.
3. Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and $\overline{DMAG}$ strobe timing parameters only apply to asynchronous access mode.
4. See "Example System Hold Time Calculation" on page 69 for calculation of hold times given capacitive and dc loads.

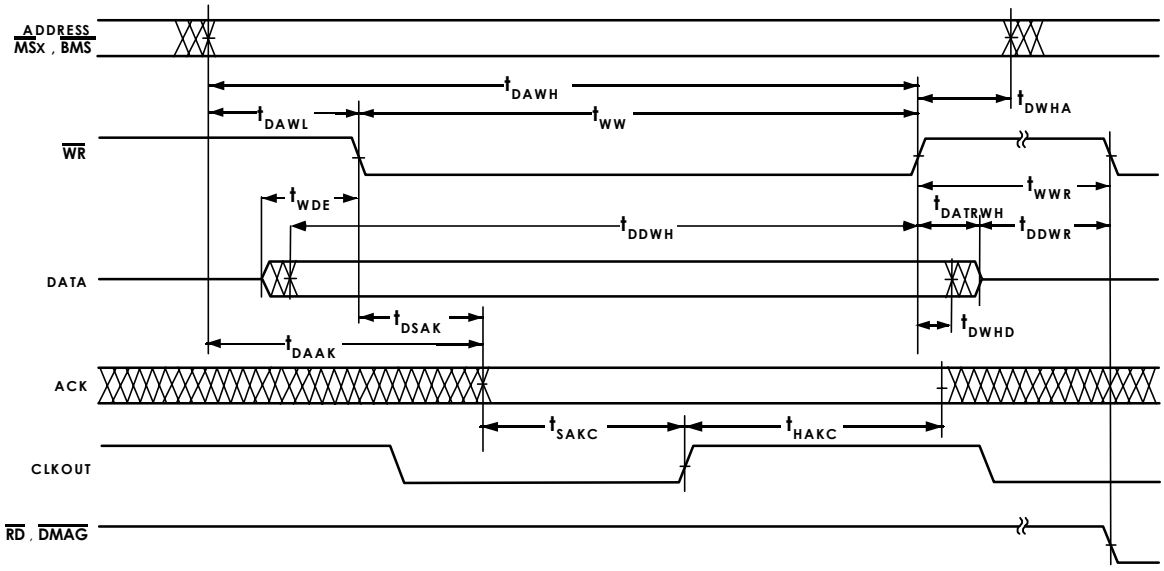


Figure 15 Memory Write--Bus Master

Synchronous Read/Write--Bus Master

Use these specifications for interfacing to external memory systems that require CLKOUT, relative to timing or for accessing a slave ADSP-21161N (in multiprocessor memory space). These synchronous switching characteristics are also valid during asynchronous memory reads and writes except where noted (see "Memory Read--Bus Master" on page 33 and "Memory Write--Bus Master" on page 35). When accessing a slave ADSP-21161N, these switching characteristics must meet the slave's timing requirements for synchronous read/writes (see "Synchronous Read/Write--Bus Slave" on page 39). The slave ADSP-21161N must also meet these (bus master) timing requirements for data and acknowledge setup and hold times.

Table 16 Synchronous Read/Write--Bus Master

Parameter		Min	Max	Units
Timing Requirements				
t_{SSDATI}	Data Setup Before CLKOUT [1]	6.8		ns
t_{HSDATI}	Data Hold After CLKOUT [1]	-0.6		ns
t_{SACKC}	ACK Setup Before CLKOUT [1]	$.5t_{CCLK}$+5.3		ns
t_{HACKC}	ACK Hold After CLKOUT [1]	-0.6		ns
Switching Characteristics				
t_{DADDO}	Address, $\overline{MS}$x, $\overline{BMS}$, BRST, Delay After CLKIN		8.2	ns
t_{HADDO}	Address, $\overline{MS}$x, $\overline{BMS}$, BRST, Hold After CLKIN	-0.4		ns
t_{DRDO}	$\overline{RD}$ High Delay After CLKOUT [1]	$.25t_{CCLK}$–2.9	$.25t_{CCLK}$+7.2	ns
t_{DWRO}	$\overline{WR}$ High Delay After CLKOUT [1]	$.25t_{CCLK}$–2.9	$.25t_{CCLK}$+7.2	ns
t_{DRWL}	$\overline{RD}$/$\overline{WR}$ Low Delay After CLKOUT	$.25t_{CCLK}$–2.9	$.25t_{CCLK}$+7.2	ns
t_{DDATO}	Data Delay After CLKOUT		10.7	ns
t_{HDATO}	Data Hold After CLKOUT	-0.4		ns
t_{DACKMO}	ACK Delay After CLKOUT [2]	$.25t_{CCLK}$+1.1	$.25t_{CCLK}$+7.2	ns
t_{ACKMTR}	ACK Disable Before CLKOUT [2]	$.25t_{CCLK}$–4.9		ns
t_{DCKOO}	CLKOUT Delay After CLKIN	1.6	2.3	ns
t_{CKOP}	CLKOUT Period	t_{CK}	t_{CK} [3]	ns
t_{CKWH}	CLKOUT Width High	$t_{CK}/2$ - 2	$t_{CK}/2 + 2$ [3]	ns
t_{CKWL}	CLKOUT Width Low	$t_{CK}/2$ - 2	$t_{CK}/2 + 2$ [3]	ns

1. Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and $\overline{DMAG}$ strobe timing parameters only applies to synchronous access mode.
2. Applies to broadcast write, master precharge of ACK.
3. Applies only when the DSP drives a bus operation; CLKOUT held inactive or three-state otherwise, For more information, see the System Design chapter in the ADSP-21160 or ADSP-21161N SHARC DSP Technical Reference.

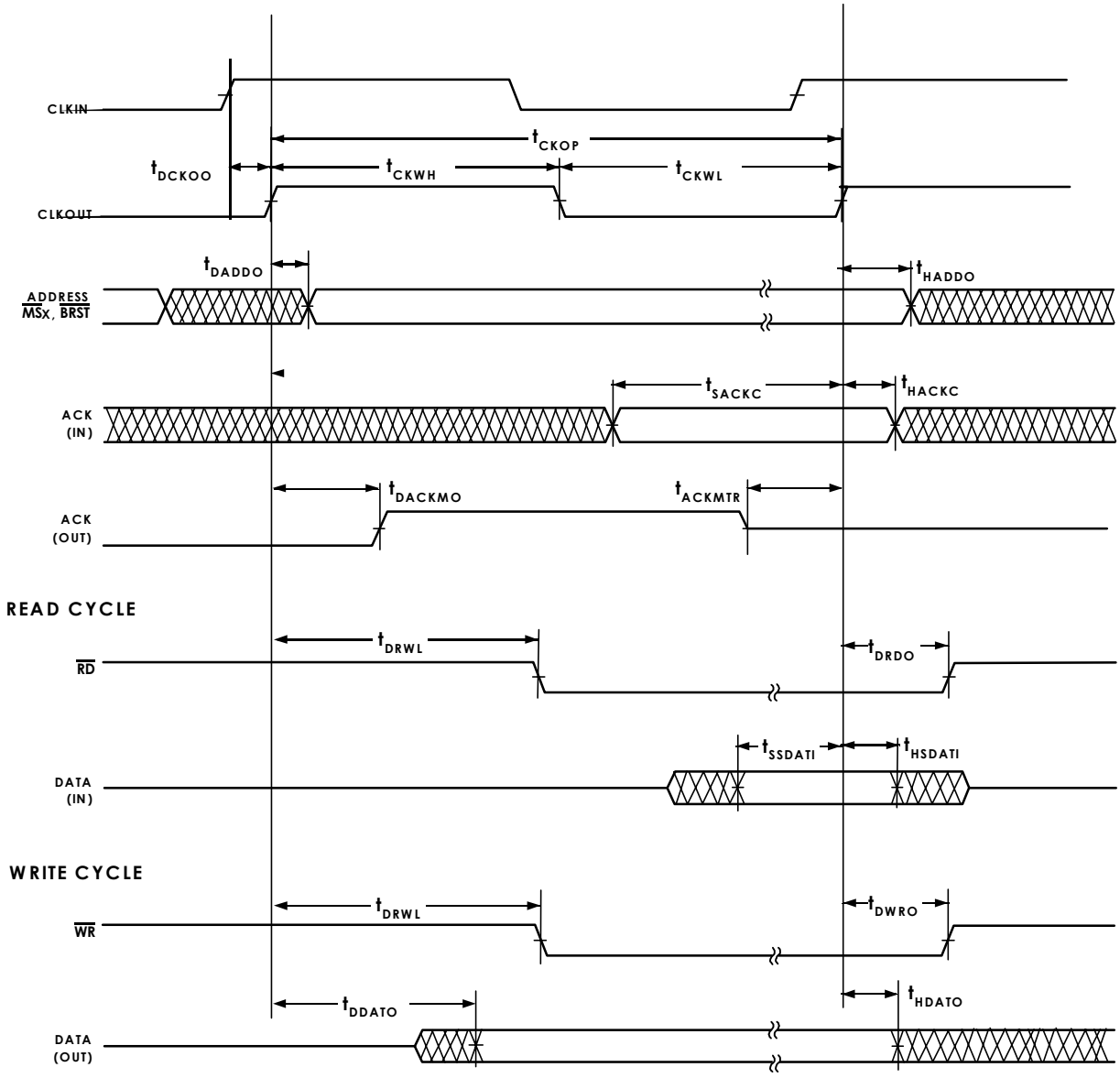


Figure 16 Synchronous Read/Write--Bus Master

Synchronous Read/Write--Bus Slave

Use these specifications for ADSP-21161N bus master accesses of a slave's IOP registers in multiprocessor memory space. The bus master must meet these (bus slave) timing requirements.

Table 17 Synchronous Read/Write--Bus Slave

Parameter		Min	Max	Units
Timing Requirements:				
t_{SADDI}	Address, BRST Setup Before CLKOUT	7.3		ns
t_{HADDI}	Address, BRST Hold After CLKOUT	-0.6		ns
t_{SRWI}	$\overline{RD}/\overline{WR}$ Setup Before CLKOUT	7.3		ns
t_{HRWI}	$\overline{RD}/\overline{WR}$ Hold After CLKOUT	-0.6		ns
t_{SSDATI}	Data Setup Before CLKOUT	6.8		ns
t_{HSDATI}	Data Hold After CLKOUT	-0.6		ns
Switching Characteristics				
t_{DDATO}	Data Delay After CLKOUT		10.7	ns
t_{HDATO}	Data Hold After CLKOUT	-0.4		ns
t_{DACKC}	ACK Delay After CLKOUT		8.2	ns
t_{HACKO}	ACK Hold After CLKOUT	-0.4		ns

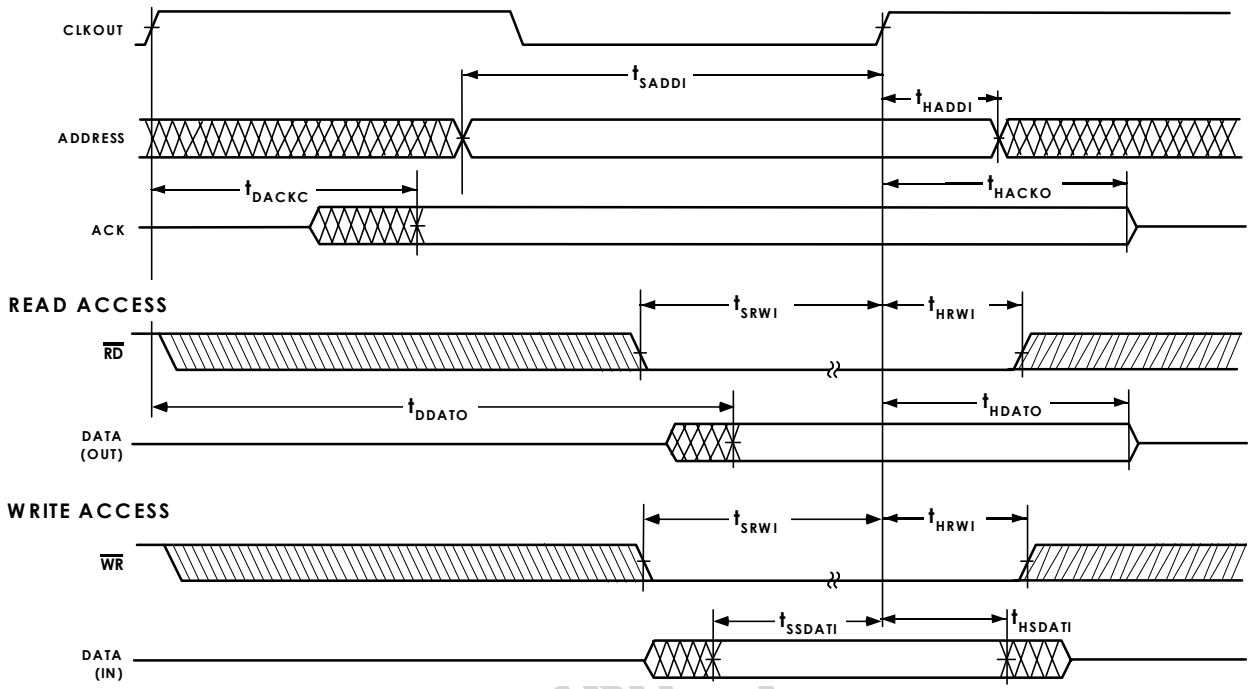


Figure 17 Synchronous Read/Write--Bus Slave

Multiprocessor Bus Request and Host Bus Request

Use these specifications for passing of bus mastership between multiprocessing ADSP-21161Ns ($\overline{BRx}$) or a host processor ($\overline{HBR}$, $\overline{HBG}$).

Table 18 Multiprocessor Bus Request and Host Bus Request

Parameter		Min	Max	Units
Timing Requirements:				
$t_{HBGRCSV}$	$\overline{HBG}$ Low to $\overline{RD}$/$\overline{WR}$/$\overline{CS}$ Valid[1]	TBD	TBD	ns
t_{SHBRI}	$\overline{HBR}$ Setup Before CLKOUT [2]	8.3		ns
t_{HHBRI}	$\overline{HBR}$ Hold After CLKOUT [2]	-0.6		ns
t_{SHBGI}	$\overline{HBG}$ Setup Before CLKOUT	8.3		ns
t_{HHBGI}	$\overline{HBG}$ Hold After CLKOUT High	-0.6		ns
t_{SBRI}	$\overline{BR}_x$, $\overline{PA}$ Setup Before CLKOUT	11.3		ns
t_{HBRI}	$\overline{BR}_x$, $\overline{PA}$ Hold After CLKOUT High	-0.6		ns
t_{SPAI}	$\overline{PA}$ Setup Before CLKOUT	11.3		ns
t_{HPAI}	$\overline{PA}$ Hold After CLKOUT High	-0.6		ns
t_{SRPBAI}	RPBA Setup Before CLKOUT	8.3		ns
t_{HRPBAI}	RPBA Hold After CLKOUT	0.4		ns
Switching Characteristics				
t_{DHBGO}	$\overline{HBG}$ Delay After CLKOUT		TBD	ns
t_{HHBGO}	$\overline{HBG}$ Hold After CLKOUT	TBD		ns
t_{DBRO}	$\overline{BRx}$ Delay After CLKOUT		7.2	ns
t_{HBRO}	$\overline{BR}_x$ Hold After CLKOUT	-0.4		ns
t_{DPASO}	$\overline{PA}$ Delay After CLKOUT, Slave		7.2	ns
t_{TRPAS}	$\overline{PA}$ Disable After CLKOUT, Slave	-0.4		ns
t_{DPAMO}	$\overline{PA}$ Delay After CLKOUT, Master		$.25t_{CCLK}+7.2$	ns
t_{PATR}	$\overline{PA}$ Disable Before CLKOUT, Master	$.25t_{CCLK}+0.6$		ns
t_{DRDYCS}	REDY (O/D) or (A/D) Low from $\overline{CS}$ and $\overline{HBR}$ Low[3]		TBD	ns
t_{TRDYHG}	REDY (O/D) Disable or REDY (A/D) High from $\overline{HBG}$[3]	TBD		ns

See note on page 42.

Table 18 Multiprocessor Bus Request and Host Bus Request

Parameter		Min	Max	Units
t_{ARDYTR}	REDY (A/D) Disable from $\overline{CS}$ or $\overline{HBR}$ High[3]		TBD	ns
See note on page 42.				

1. For first asynchronous access after $\overline{HBR}$ and $\overline{CS}$ asserted, $ADDR_{23-0}$ must be a non-MMS value (TBD) before $\overline{RD}$ or $\overline{WR}$ goes low or by $t_{HBGRCSV}$ after $\overline{HBG}$ goes low. This is easily accomplished by driving an upper address signal high when $\overline{HBG}$ is asserted.
2. Only required for recognition in the current cycle.
3. (O/D) = open drain, (A/D) = active drive.

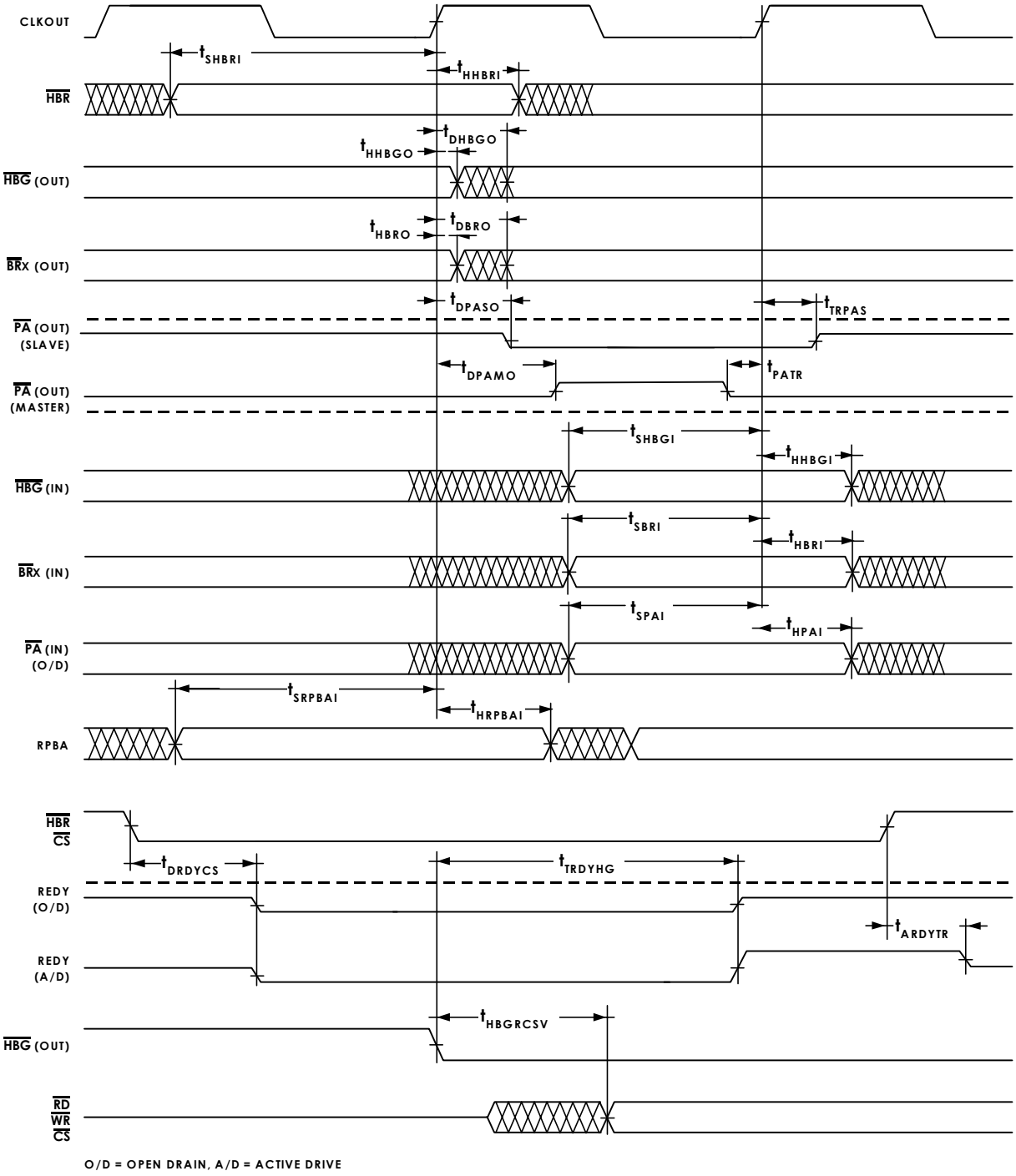


Figure 18 Multiprocessor Bus Request and Host Bus Request

Asynchronous Read/Write--Host to ADSP-21161N

Use these specifications (continued on page 45 and page 46) for asynchronous host processor accesses of an ADSP-21161N, after the host has asserted $\overline{CS}$ and $\overline{HBR}$ (low). After $\overline{HBG}$ is returned by the ADSP-21161N, the host can drive the $\overline{RD}$ and $\overline{WR}$ pins to access the ADSP-21161N's IOP register. $\overline{HBR}$ and $\overline{HBG}$ are assumed low for this timing.

Note: *Host internal memory access is not supported.*

Table 19 Write Cycle (Synchronous READY)

Parameter		Min	Max	Units
Switching Characteristics				
t_{SRDYCK}	REDY (O/D) or (A/D) Disable to CLKOUT	TBD	TBD	ns

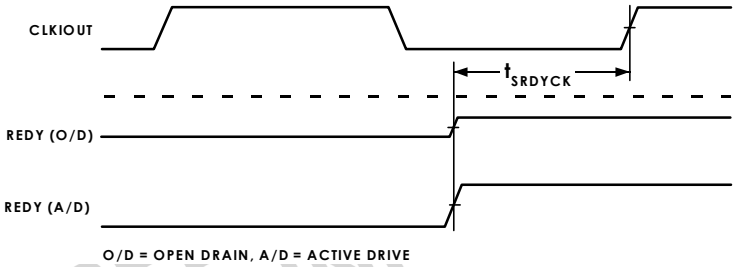


Figure 19 Synchronous READY Timing

Table 20 Read Cycle

Parameter		Min	Max	Units
Timing Requirements				
t_{SADRDL}	Address Setup $\overline{CS}$ Low Before $\overline{RD}$ Low[1]	0		ns
t_{HADRDH}	Address Hold $\overline{CS}$ Hold Low After $\overline{RD}$	0		ns
t_{WRWH}	$\overline{RD}$/$\overline{WR}$ High Width	5		ns
$t_{DRDHRDY}$	$\overline{RD}$ High Delay After REDY (O/D) Disable	0		ns
$t_{DRDHRDY}$	$\overline{RD}$ High Delay After REDY (A/D) Disable	0		ns
Switching Characteristics				
$t_{SDATRDY}$	Data Valid Before REDY Disable from Low	2		ns
$t_{DRDYRDL}$	REDY (O/D) or (A/D) Low Delay After $\overline{RD}$ Low		10	ns
t_{RDYPRD}	REDY (O/D) or (A/D) Low Pulse Width for Read	$2t_{CK}$		ns
t_{HDARWH}	Data Disable After $\overline{RD}$ High	2	TBD	ns

1. Not required if $\overline{RD}$ and address are valid $t_{HBGRCSV}$ after $\overline{HBG}$ goes low. For first access after $\overline{HBR}$ asserted, $ADDR_{23-0}$ must be a non-MMS value (TBD) before $\overline{RD}$ or $\overline{WR}$ goes low or by $t_{HBGRCSV}$ after $\overline{HBG}$ goes low. This is easily accomplished by driving an upper address signal high when $\overline{HBG}$ is asserted.

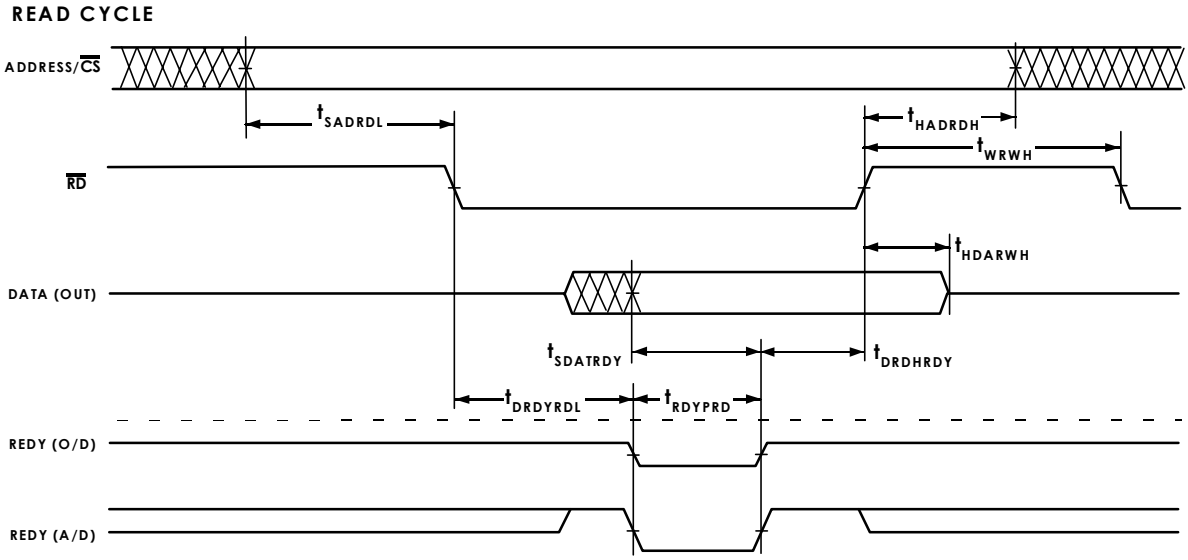


Figure 20 Asynchronous Read--Host to ADSP-21161N

Table 21 Write Cycle

Parameter		Min	Max	Units
Timing Requirements				
t_{SCSWRL}	$\overline{CS}$ Low Setup Before $\overline{WR}$ Low	0		ns
t_{HCSWRH}	$\overline{CS}$ Low Hold After $\overline{WR}$ High	0		ns
t_{SADWRH}	Address Setup Before $\overline{WR}$ High	5		ns
t_{HADWRH}	Address Hold After $\overline{WR}$ High	2		ns
t_{WWRL}	$\overline{WR}$ Low Width	7		ns
t_{WRWH}	$\overline{RD}$/$\overline{WR}$ High Width	5		ns
$t_{DWRHRDY}$	$\overline{WR}$ High Delay After REDY (O/D) or (A/D) Disable	0		ns
t_{SDATWH}	Data Setup Before $\overline{WR}$ High	5		ns
t_{HDATWH}	Data Hold After $\overline{WR}$ High	1		ns
Switching Characteristics				
$t_{DRDYWRL}$	REDY (O/D) or (A/D) Low Delay After $\overline{WR}$/$\overline{CS}$ Low		10	ns
t_{RDYPWR}	REDY (O/D) or (A/D) Low Pulse Width for Write	TBD		ns

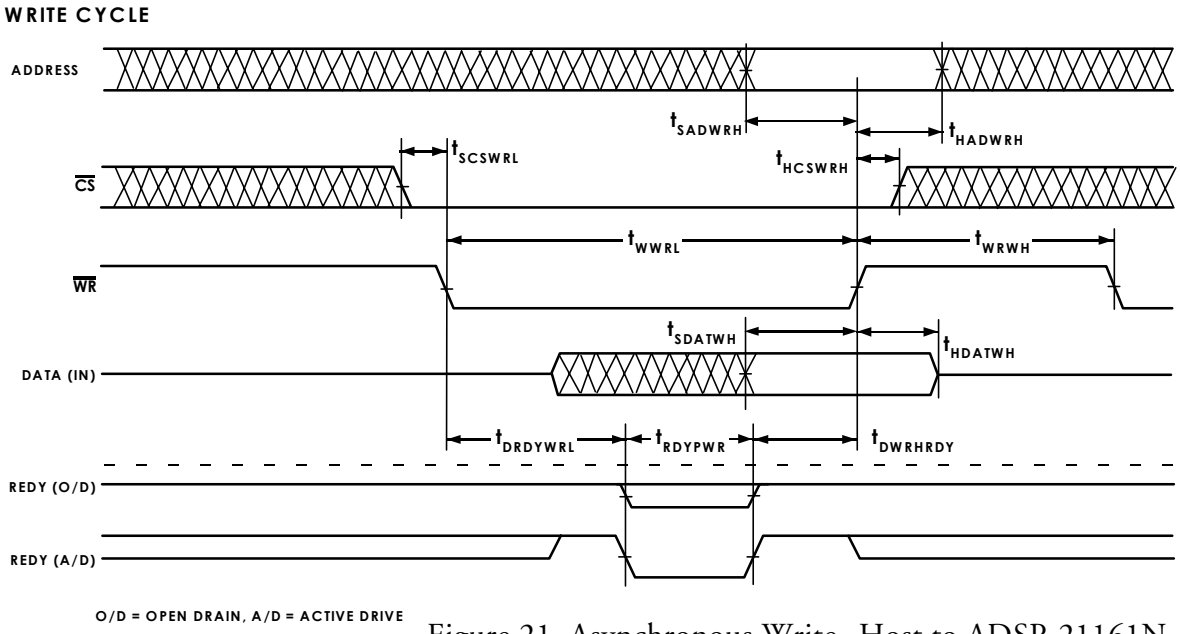


Figure 21 Asynchronous Write--Host to ADSP-21161N

Three-State Timing--Bus Master, Bus Slave, HBR, SBTS

These specifications show how the memory interface is disabled (stops driving) or enabled (resumes driving) relative to CLKOUT and the $\overline{SBTS}$ pin. This timing is applicable to bus master transition cycles (BTC) and host transition cycles (HTC) as well as the $\overline{SBTS}$ pin.

Table 22 Three-State Timing--Bus Slave, $\overline{HBR}$, $\overline{SBTS}$

Parameter		Min	Max	Units
Timing Requirements				
t_{STSCK}	$\overline{SBTS}$ Setup Before CLKOUT	8.3		ns
t_{HTSCK}	$\overline{SBTS}$ Hold After CLKOUT	-0.6		ns
Switching Characteristics				
t_{MIENA}	Address/Select Enable After CLKOUT	-0.4	7.2	ns
t_{MIENS}	Strobes Enable After CLKOUT[1]	-0.4	3.2	ns
t_{MIENHG}	HBG Enable After CLKOUT	-0.4	7.2	ns
t_{MITRA}	Address/Select Disable After CLKOUT	$.5t_{CK}$-0.9	$.5t_{CK}$+3.2	ns
t_{MITRS}	Strobes Disable After CLKOUT[1]	t_{CK}–$.25t_{CCLK}$-1.9	t_{CK}– $.25t_{CCLK}$+3.2	ns
t_{MITRHG}	HBG Disable After CLKOUT	-0.4	3.2	ns
t_{DATEN}	Data Enable After CLKOUT [2]	-0.4	7.2	ns
t_{DATTR}	Data Disable After CLKOUT[2]	-0.4	3.2	ns
t_{ACKEN}	ACK Enable After CLKOUT[2]	-0.4	7.2	ns
t_{ACKTR}	ACK Disable After CLKOUT[2]	1.5	5	ns
t_{CDCEN}	CLKOUT Enable After CLKIN	-0.4	7.2	ns
t_{CDCTR}	CLKOUT Disable After CLKIN	$.5t_{CK}$-0.9	$.5t_{CK}$+3.2	ns
t_{MTRHBG}	Memory Interface Disable Before $\overline{HBG}$ Low[3]	$.5t_{CK}$–4	TBD	ns
t_{MENHBG}	Memory Interface Enable After $\overline{HBG}$ High[3]	t_{CK}–5	TBD	ns

1. Strobes = $\overline{RD}$, $\overline{WR}$, $\overline{DMAG}$x.
2. In addition to bus master transition cycles, these specs also apply to bus master and bus slave synchronous read/write.
3. Memory Interface = Address, $\overline{RD}$, $\overline{WR}$, $\overline{MSx}$, $\overline{DMAG_x}$, $\overline{BMS}$ (in EPROM boot mode).

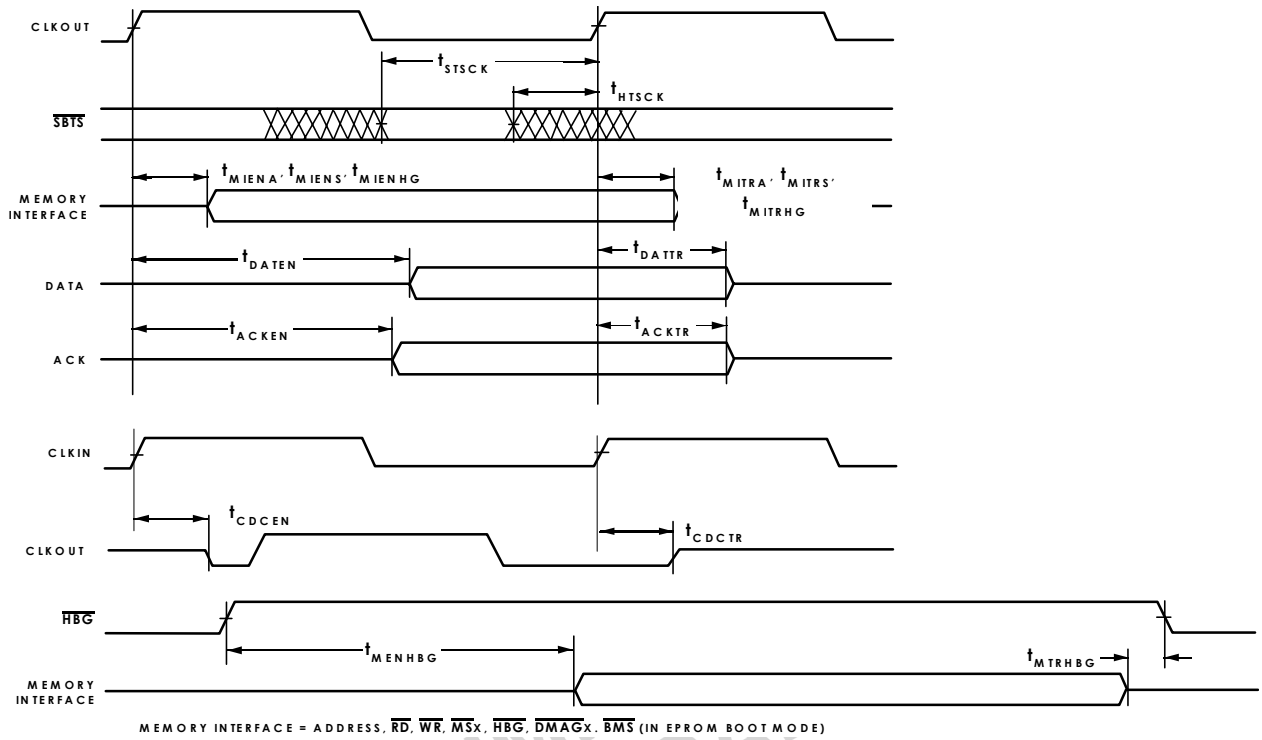


Figure 22 Three-State Timing

DMA Handshake

These specifications describe the three DMA handshake modes. In all three modes $\overline{\text{DMAR}}$ is used to initiate transfers. For handshake mode, $\overline{\text{DMAG}}$ controls the latching or enabling of data externally. For external handshake mode, the data transfer is controlled by the $\text{ADDR}_{24\text{-}0}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{MS}}_{3\text{-}0}$, ACK, and $\overline{\text{DMAG}}$ signals. For Paced Master mode, the data transfer is controlled by $\text{ADDR}_{24\text{-}0}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{MS}}_{3\text{-}0}$, and ACK (not $\overline{\text{DMAG}}$). For Paced Master mode, the Memory Read-Bus Master, Memory Write-Bus Master, and Synchronous Read/Write-Bus Master timing specifications for $\text{ADDR}_{23\text{-}0}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{MS3-0}}$, $\text{DATA}_{47\text{-}16}$, and ACK also apply.

Table 23 DMA Handshake

Parameter		Min	Max	Units
Timing Requirements				
t_{SDRC}	$\overline{\text{DMARx}}$ Setup Before CLKOUT [1]	5.3		ns
t_{WDR}	$\overline{\text{DMARx}}$ Width Low (Nonsynchronous)	$.5t_{CK}+1$		ns
$t_{SDATDGL}$	Data Setup After $\overline{\text{DMAGx}}$ Low[2]		$.75t_{CK}–7$	ns
$t_{HDATIDG}$	Data Hold After $\overline{\text{DMAGx}}$ High	2		ns

Table 23 DMA Handshake (Continued)

Parameter		Min	Max	Units
t_{DATDRH}	Data Valid After $\overline{DMAR}_x$ High[2]		TBD	ns
t_{DMARLL}	$\overline{DMAR}_x$ Low Edge to Low Edge[3]	t_{CK}		ns
t_{DMARH}	$\overline{DMAR}_x$ Width High	$.5t_{CK}+1$		ns
Switching Characteristics				
t_{DDGL}	$\overline{DMAG}_x$ Low Delay After CLKOUT	$.25t_{CCLK}-0.9$	$.25t_{CCLK}+7.2$	ns
t_{WDGH}	$\overline{DMAG}_x$ High Width	$.5t_{CCLK}-1+HI$		ns
t_{WDGL}	$\overline{DMAG}_x$ Low Width	$t_{CK}-.5t_{CCLK}-1$		ns
t_{HDGC}	$\overline{DMAG}_x$ High Delay After CLKOUT	$t_{CK}-.25t_{CCLK}-0.4$	$t_{CK}-.25t_{CCLK}+7.2$	ns
$t_{VDATDGH}$	Data Valid Before $\overline{DMAG}_x$ High[4]	$t_{CK}-.25t_{CCLK}-8$	$t_{CK}-.25t_{CCLK}+5$	ns
$t_{DATRDGH}$	Data Disable After $\overline{DMAG}_x$ High[5]	$.25t_{CCLK}+1.5$	$.25t_{CCLK}+1.5$	ns
t_{DGWRL}	$\overline{WR}$ Low Before $\overline{DMAG}_x$ Low	–1	1	ns
t_{DGWRH}	$\overline{DMAG}_x$ Low Before $\overline{WR}$ High	$t_{CK}-.5t_{CCLK}-2+W$		ns
t_{DGWRR}	$\overline{WR}$ High Before $\overline{DMAG}_x$ High[6]	–1	1	ns
t_{DGRDL}	$\overline{RD}$ Low Before $\overline{DMAG}_x$ Low	–1	1	ns
t_{DRDGH}	$\overline{RD}$ Low Before $\overline{DMAG}_x$ High	$t_{CK}-.5t_{CCLK}-2+W$		ns
t_{DGRDR}	$\overline{RD}$ High Before $\overline{DMAG}_x$ High[6]	–1	1	ns
t_{DGWR}	$\overline{DMAR}_x$ High to $\overline{WR}$, $\overline{RD}$, $\overline{DMAG}_x$ Low	$.5t_{CCLK}-1+HI$		ns
t_{DADGH}	Address/Select Valid to $\overline{DMAG}_x$ High	TBD		ns
t_{DDGHA}	Address/Select Hold after $\overline{DMAG}_x$ High	TBD		ns
W = (number of wait states specified in WAIT register) × t_{CK}. HI = t_{CK} (if data bus idle cycle occurs, as specified in WAIT register; otherwise HI = 0).				

1. Only required for recognition in the current cycle.
2. $t_{SDATDGL}$ is the data setup requirement if $\overline{DMAR}_x$ is not being used to hold off completion of a write. Otherwise, if $\overline{DMAR}_x$ low holds off completion of the write, the data can be driven t_{DATDRH} after $\overline{DMAR}_x$ is brought high.

3. Use t_{DMARLL} if $\overline{DMAR}_x$ transitions synchronous with CLKOUT. Otherwise, use t_{WDR} and t_{DMARH}.
4. $t_{VDATDGH}$ is valid if $\overline{DMAR}_x$ is not being used to hold off completion of a read. If $\overline{DMAR}_x$ is used to prolong the read, then $t_{VDATDGH} = t_{CK} - .25t_{CCLK} - 8 + (n \times t_{CK})$ where n equals the number of extra cycles that the access is prolonged.
5. See "Example System Hold Time Calculation" on page 69 for calculation of hold times given capacitive and dc loads.
6. This parameter applies for synchronous access mode only.

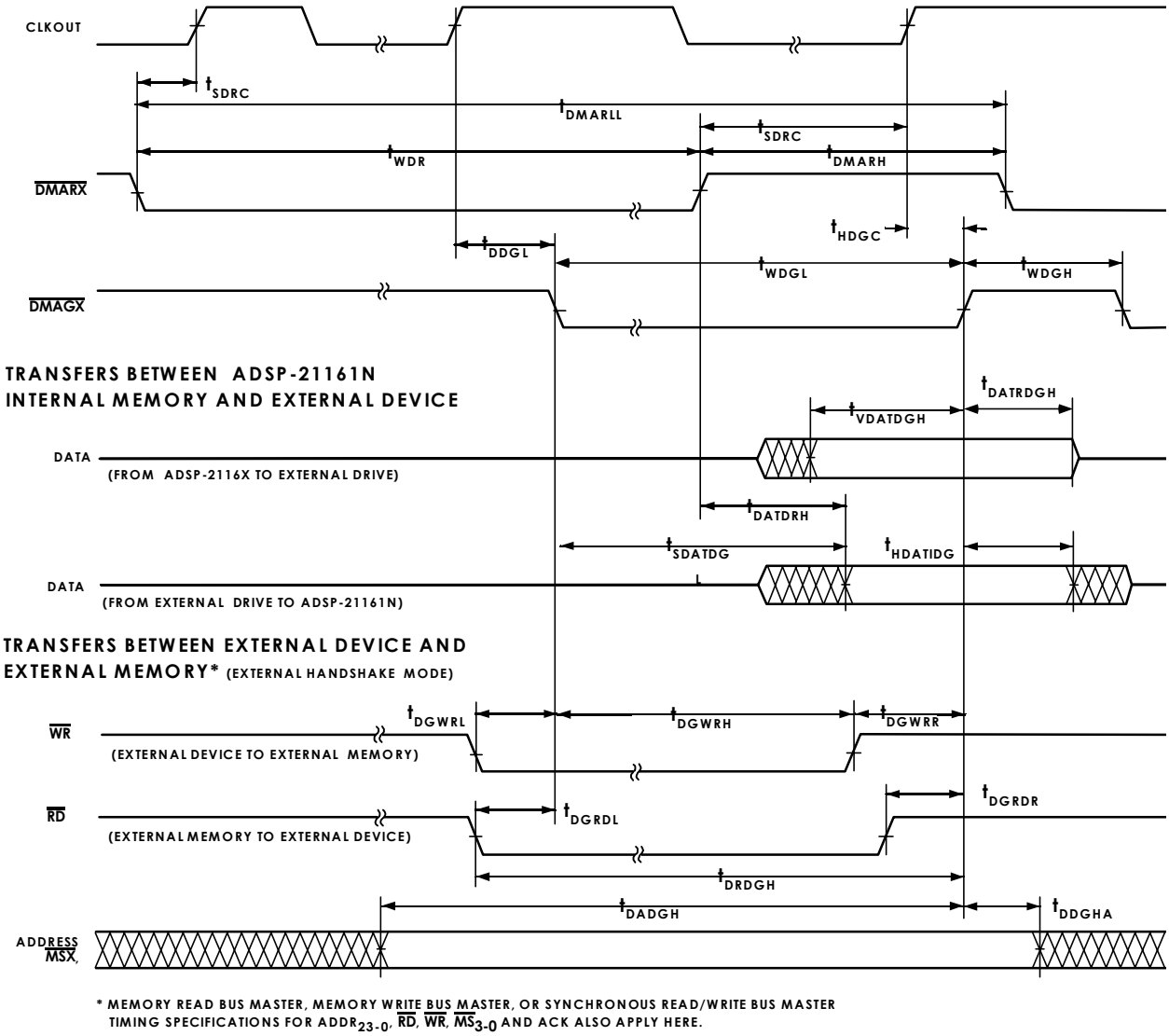


Figure 23 DMA Handshake Timing

SDRAM Interface – Bus Master

Use these specifications for ADSP-21161N bus master accesses of SDRAM:

Parameter		Min	Max	Units
Timing Requirements:				
t_{SDSDK}	Data Setup before SDCLK	2.0		ns
t_{HDSDK}	Data Hold after SDCLK	1.5		ns
Switching Characteristics:				
t_{DSDK1}	First SDCLK Rise Delay after CLKOUT[1, 2]	SDCKR x t_{CCLK} -0.25 x t_{CCLK} - 0.4	SDCKR x t_{CCLK} -0.25 x t_{CCLK} + 1.7	ns
t_{SDK}	SDCLK Period	10.0	2 x t_{CCLK}	ns
t_{SDKH}	SDCLK Width High	4.0		ns
t_{SDKL}	SDCLK Width Low	4.0		ns
$t_{DCADSDK}$	Command, Address, Data, Delay after SDCLK[3]		.25 x t_{CCLK} + 2.0	ns
$t_{HCADSDK}$	Command, Address, Data, Hold after SDCLK[3]	1.3		ns
$t_{SDTRSDK}$	Data Three-State after SDCLK		0.5 x t_{CCLK} + 2.0	ns
$t_{SDENSDK}$	Data Enable After SDCLK[4]	0.75 x t_{CCLK}		ns
t_{SDCTR}	Command Three-State After CLKOUT[3]	0.5 x t_{CCLK} - 0.4	0.5 x t_{CCLK} + 1.7	ns
t_{SDCEN}	Command Enable After CLKOUT[3]	-0.4	1.7	ns
$t_{SDSDKTR}$	SDCLK Three-State after CLKOUT	-0.4	1.7	ns
$t_{SDSDKEN}$	SDCLK Enable after CLKOUT	-0.4	1.7	ns
t_{SDATR}	Address Three-State after CLKOUT	0.5 x t_{CK} - 0.9	0.5 x t_{CK} + 3.2	ns
t_{SDAEN}	Address Enable after CLKOUT	-0.4	7.2	ns

1. For the second, third, and forth rising edges of SDCLK delay from CLKOUT, add appropriate number of SDCLK period to the t_{DSDK1} and t_{SSDKC1} values, depending upon the SDCKR value and the Core clk to CLKOUT ratio.
2. SDCKR = 1 for SDCLK equal to core clock frequency and SDCKR = 2 for SDCLK equal to half core clock frequency.
3. Command = SDCKE, $\overline{RAS}$, $\overline{CAS}$, and $\overline{SDWE}$.
4. SDRAM Controller adds one SDRAM CLK three-stated cycle delay on a read followed, by a write.

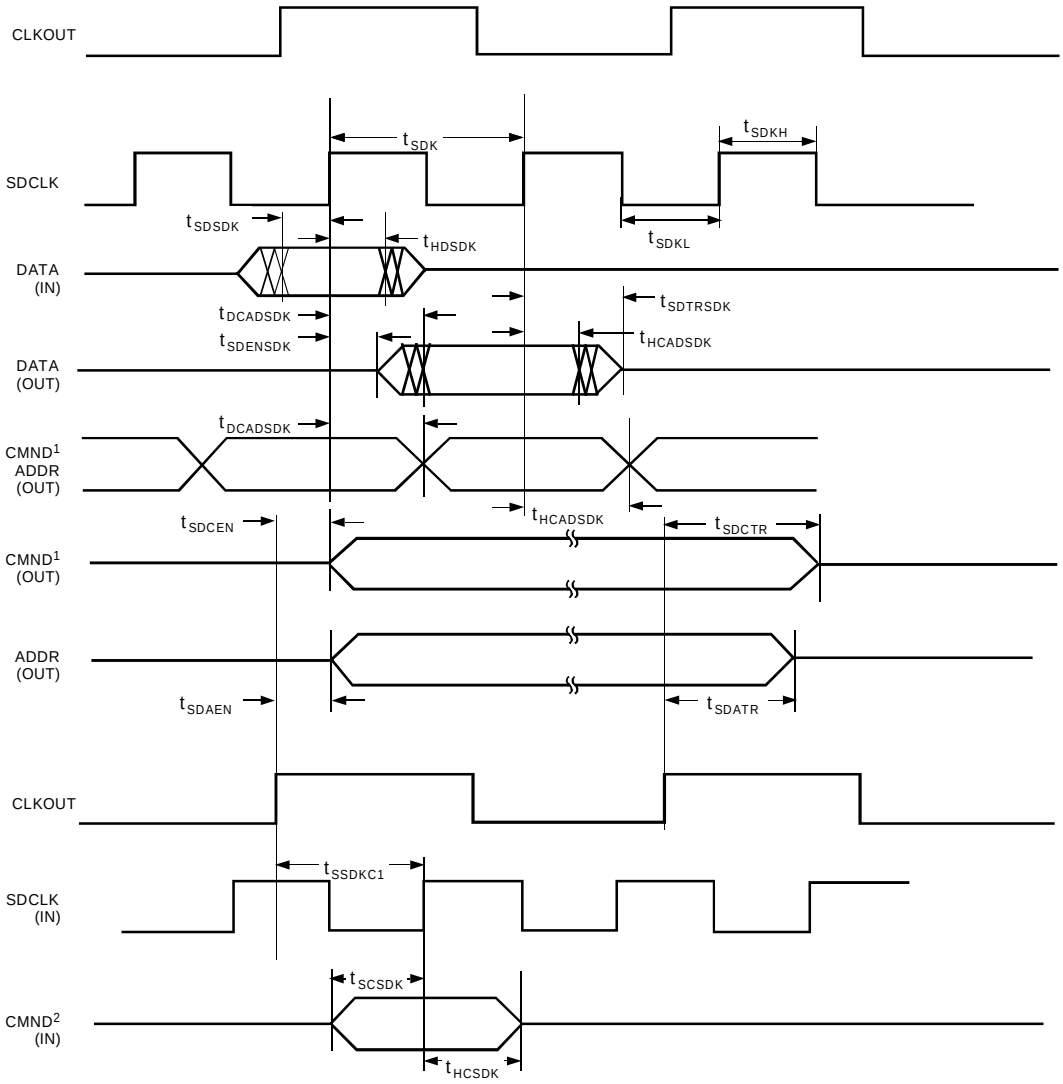
SDRAM Interface – Bus Slave

These timing requirements allow a bus slave to sample the bus master's SDRAM command and detect when a refresh occurs.

Parameter		Min	Max	Unit
Timing Requirements:				
t_{SSDKC1}	First SDCLK Rise After CLKOUT[1, 2]	SDCKR x tCCLK -0.5 x t_{CCLK} -1.4	SDCKR x tCCLK -0.25 x t_{CCLK} + 2.7	ns
t_{SCSDK}	Command Setup Before SDCLK[3]	0.0		ns
t_{HCSDK}	Command Hold After SDCLK[3]	2.0		ns

NOTES

1. For the second, third, and forth rising edges of SDCLK delay from CLKOUT, add appropriate number of SDCLK period to the t_{DSDK1} and t_{SSDKC1} values, depending upon the SDCKR value and the Core clk to CLKOUT ratio.
2. SDCKR = 1 for SDCLK equal to core clock frequency and SDCKR = 2 for SDCLK equal to half core clock frequency.
3. Command = SDCKE, $\overline{RAS}$, $\overline{CAS}$, and $\overline{SDWE}$.



NOTES
[1]COMMAND = SDCKE, $\overline{MS_X}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{SDWE}$, $\overline{DQM}$ and SDA10.
[2]SDRAM CONTROLLER ADDS ONE SDRAM CLK THREE-STATED CYCLE DELAY ON A READ FOLLOWED BY A WRITE.

Figure 24 SDRAM Interface

Link Ports

Calculation of link receiver data setup and hold relative to link clock is required to determine the maximum allowable skew that can be introduced in the transmission path between LDATA and LCLK. Setup skew is the maximum delay that can be introduced in LDATA relative to LCLK, (setup skew = $t_{LCLKTWH}$ min – t_{DLDCH} – t_{SLDCL}). Hold skew is the maximum delay that can be introduced in LCLK relative to LDATA, (hold skew = $t_{LCLKTWL}$ min – t_{HLDCH} – t_{HLDCL}). Calculations made directly from speed specifications will result in unrealistically small skew times because they include multiple tester guardbands. The setup and hold skew times shown below are calculated to include only one tester guardband.

ADSP-21161N Setup Skew = TBD ns max

ADSP-21161N Hold Skew = TBD ns max

Note that there is a two-cycle effect latency between the link port enable instruction and the DSP enabling the link port.

Table 24 Link Ports Receive

Parameter		Min	Max	Units
Timing Requirements				
t_{SLDCL}	Data Setup Before LCLK Low	2		ns
t_{HLDCL}	Data Hold After LCLK Low	2		ns
t_{LCLKIW}	LCLK Period	t_{LCLK}		ns
$t_{LCLKRWL}$	LCLK Width Low	3.5		ns
$t_{LCLKRWH}$	LCLK Width High	3.5		ns
Switching Characteristics				
t_{DLALC}	LACK Low Delay After LCLK High[1]	TBD	TBD	ns

1. LACK goes low with t_{DLALC} relative to rise of LCLK after first nibble, but doesn't go low if the receiver's link buffer is not about to fill.

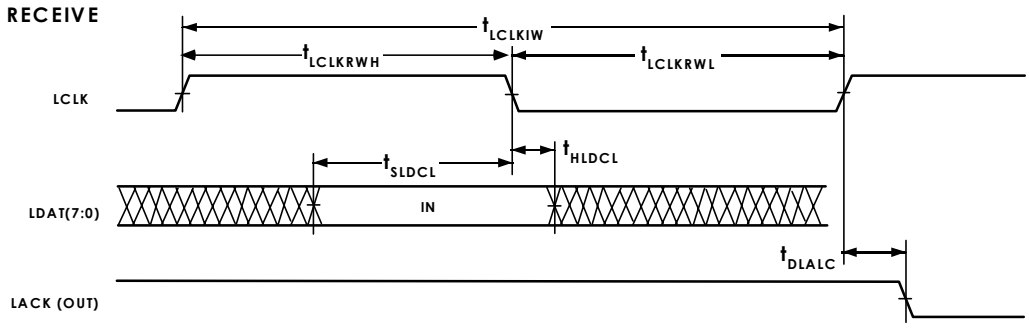


Figure 25 Link Ports—Receive

Table 25 Link Ports Transmit

Parameter		Min	Max	Units
Timing Requirements				
t_{SLACH}	LACK Setup Before LCLK High	15		ns
t_{HLACH}	LACK Hold After LCLK High	–2		ns
Switching Characteristics				
t_{DLDCH}	Data Delay After LCLK High		2	ns
t_{HLDCH}	Data Hold After LCLK High	–2		ns
$t_{LCLKTWL}$	LCLK Width Low	$.5t_{LCLK}$–1	$.5t_{LCLK}$+1	ns
$t_{LCLKTWH}$	LCLK Width High	$.5t_{LCLK}$–1	$.5t_{LCLK}$+1	ns
t_{DLACLK}	LCLK Low Delay After LACK High	$.5t_{LCLK}$+5	$3t_{LCLK}$+11	ns

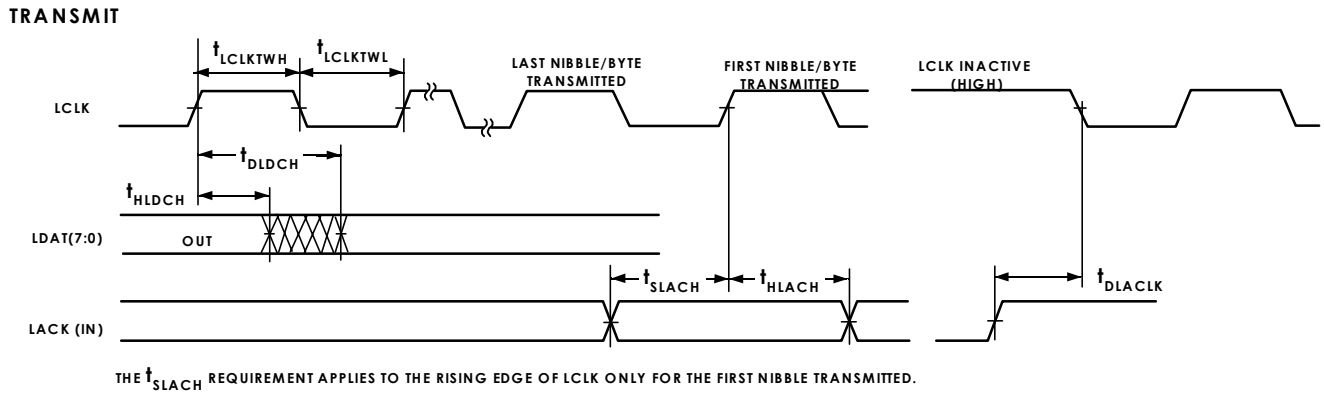


Figure 26 Link Ports—Transmit

Serial Ports

To determine whether communication is possible between two devices at clock speed n, the following specifications must be confirmed: 1) frame sync delay & frame sync setup and hold, 2) data delay & data setup and hold, and 3) SCLK width.

Table 26 Serial Ports—External Clock

Parameter		Min	Max	Units
Timing Requirements				
t_{SFSE}	Transmit/Receive FS Setup Before Transmit/Receive SCLK[1]	3.5		ns
t_{HFSE}	Transmit/Receive FS Hold After Transmit/Receive SCLK[1, 2]	4		ns
t_{SDRE}	Receive Data Setup Before Receive SCLK[1, 3]	1.5		ns
t_{HDRE}	Receive Data Hold After SCLK[1, 4]	4		ns
t_{SCLKW}	SCLKx Width	9		ns
t_{SCLK}	SCLKx Period	$2t_{CCLK}$		ns

1. Referenced to sample edge.
2. FSx hold after Receive SCLK when MCE = 1, MFD = 0 is 0 ns minimum from drive edge. Transmit FS hold after Transmit SCLK for late external Transmit FS is 0 ns minimum from drive edge.
3. SCLK/FS Configured as a receive clock/frame sync with the DDIR bit = 0 in SPCTLx register.
4. SCLK/FS Configured as a transmit clock/frame sync with the DDIR bit = 1 in SPCTLx register.

Table 27 Serial Ports—Internal Clock

Parameter		Min	Max	Units
Timing Requirements				
t_{SFSI}	FS Setup Time Before SCLK[1, 2]	8		ns
t_{HFSI}	FS Hold After SCLK[1, 2, 3]	1		ns
t_{SDRI}	Receive Data Setup Before SCLK[1]	3		ns
t_{HDRI}	Receive Data Hold After SCLK[1]	3		ns

1. Referenced to sample edge.
2. SCLK/FS configured as a receive clock/frame sync with the DDIR bit = 0 in SPCTLx register.
3. FSx hold after Receive SCLK when MCE = 1, MFD = 0 is 0 ns minimum from drive edge. Transmit FS hold after Transmit SCLK for late external Transmit FS is 0 ns minimum from drive edge.

Table 28 Serial Ports—External or Internal Clock

Parameter		Min	Max	Units
Switching Characteristics				
t_{DFSE}	FS Delay After SCLK ([1]) (Internally Generated FS) [2]		13	ns
t_{HOFSE}	FS Hold After Receive SCLK ([1]) (Internally Generated FS)[1]	3		ns

1. SCLK/FS Configured as a receive clock/frame sync with the DDIR bit = 0 in SPCTLx register.
2. Referenced to drive edge.

Table 29 Serial Ports—External Clock

Parameter		Min	Max	Units
Switching Characteristics				
t_{DFSE}	FS Delay After Transmit SCLK (Internally Generated Transmit FS) [1, 2]		13	ns
t_{HOFSE}	FS Hold After Transmit SCLK (Internally Generated Transmit FS [1, 2]	3		ns
t_{DDTE}	Transmit Data Delay After Transmit SLCK [1, 2]		16	ns
t_{HODTE}	Transmit Data Hold After Transmit SCLK [1, 2]	0		ns

1. Referenced to drive edge.
2. SCLK/FS Configured as a transmit clock/frame sync with the DDIR bit = 1 in SPCTLx register.

Table 30 Serial Ports—Internal Clock

Parameter		Min	Max	Units
Switching Characteristics				
t_{DFSI}	Transmit FS Delay After SCLK (Internally Generated Transmit FS)[1, 2]		4.5	ns
t_{HOFSI}	Transmit FS Hold After SCLK (Internally Generated Transmit FS)[1, 2]	-1.5		ns

Table 30 Serial Ports—Internal Clock

Parameter		Min	Max	Units
t_{DDTI}	Transmit Data Delay After SCLK[1, 2]		7.5	ns
t_{HDTI}	Transmit Data Hold After SCLK[1, 2]	0		ns
t_{SCLKIW}	Transmit or Receive SCLK Width[2]	$.5t_{SCLK}$–2.5	$.5t_{SCLK}$+2	ns

1. Referenced to drive edge.
2. SCLK/FS Configured as a transmit clock/frame sync with the DDIR bit = 1 in SPCTLx register.

Table 31 Serial Ports—Enable and Three-State

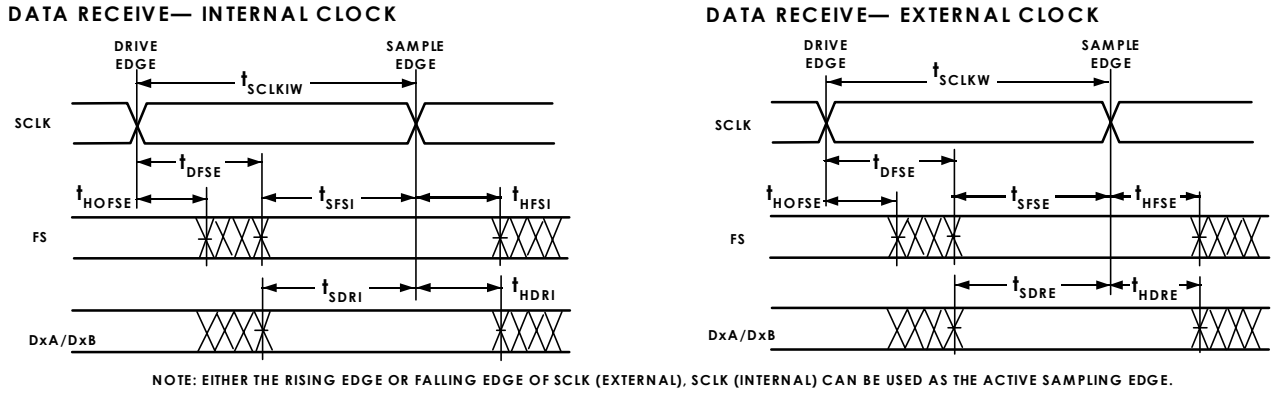
Parameter		Min	Max	Units
Switching Characteristics				
t_{DDTEN}	Data Enable from External Transmit SCLK[1, 2]	4		ns
t_{DDTTE}	Data Disable from External Transmit SCLK[1]		10	ns
t_{DDTIN}	Data Enable from Internal Transmit SCLK[1]	0		ns
t_{DDTTI}	Data Disable from Internal Transmit SCLK[1]		3	ns

1. Referenced to drive edge.
2. SCLK/FS Configured as a transmit clock/frame sync with the DDIR bit = 1 in SPCTLx register.

Table 32 Serial Ports—External Late Frame Sync

Parameter		Min	Max	Units
Switching Characteristics				
$t_{DDTLFSE}$	Data Delay from Late External Transmit FS or External Receive FS with MCE = 1, MFD = 0[1]		13	ns
$t_{DDTENFS}$	Data Enable from Late FS or MCE = 1, MFD = 0[1]	3.5		ns

1. MCE = 1, Transmit FS enable and Transmit FS valid follow $t_{DDTLFSE}$ and $t_{DDTENFS}$.



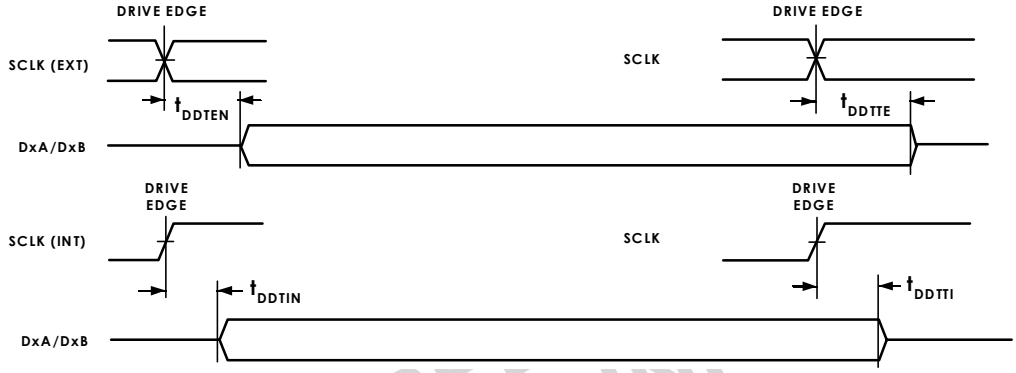


Figure 27 Serial Ports

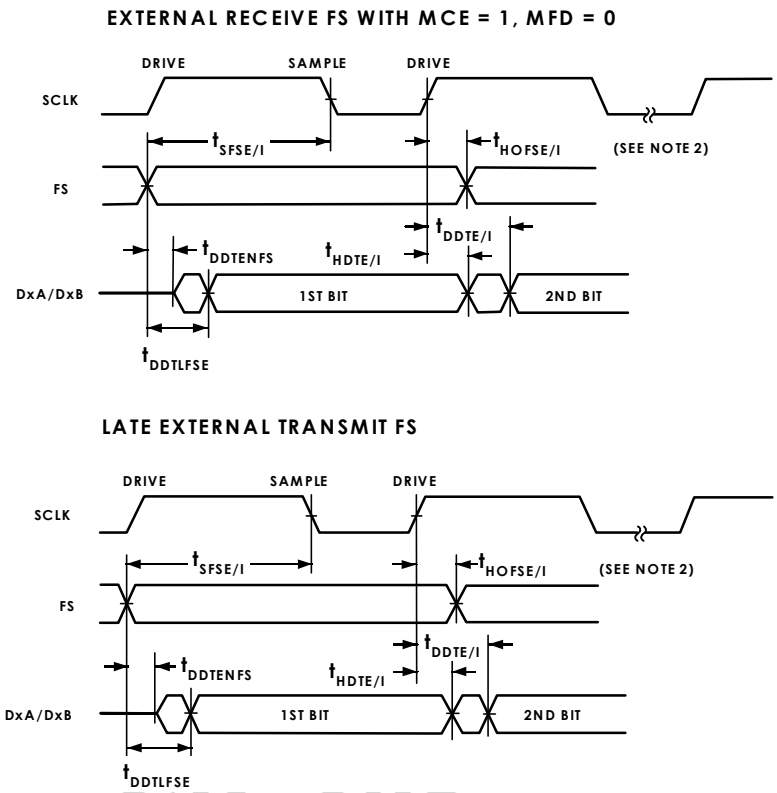


Figure 28 External Late Frame Sync

SPI INTERFACE SPECIFICATIONS

Table 33 SPI Interface Protocol — Timing Specifications

Name	Parameter	Mode	Min	Max	Units
t_{SPICLK}	Minimum serial clock cycle	Master	TBD		ns
t_{SPICHM}	Serial clock high period	Master	TBD		ns
t_{SPICHS}	Serial clock low period	Slave	TBD		ns
t_{SPICLM}	Serial clock low period	Master	TBD		ns
t_{SPICLS}	Serial clock high period	Slave	TBD		ns
t_{SDSCO}	$\overline{SPIDS}$ assertion to first SPICLK edge CPHASE=0 CPHASE=1 t_{SDSCI} CP0=1	Slave Slave	TBD TBD		ns
t_{HDS}	Last SPICLK edge to $\overline{SPIDS}$ not asserted	Slave	TBD		ns
t_{SSPID}	Data input valid to SPICLK edge (data input set-up time)	Master/ Slave	TBD		ns
t_{HSPID}	SPICLK last sampling edge to data input not valid	Master/ Slave	TBD		ns
t_{DSOE} ($t_{SPIDSOE}$)	$\overline{SPIDS}$ assertion to data out active	Slave	TBD		ns
t_{DSDHI}	$\overline{SPIDS}$ deassertion to data high impedance	Slave		TBD	ns
t_{DDSPID}	SPICLK edge to data out valid (data out delay time)	Master/ Slave		TBD	ns
t_{HDSPID}	SPICLK edge to data out not valid (data out hold time)	Master/ Slave	TBD		ns
t_{DSOV}	$\overline{SPIDS}$ assertion to data out valid (CPHASE=0)	Slave		TBD	ns
t_{SDPPW}	$\overline{SPIDS}$ deassertion pulse width (CPHASE=0)	Slave	TBD		ns

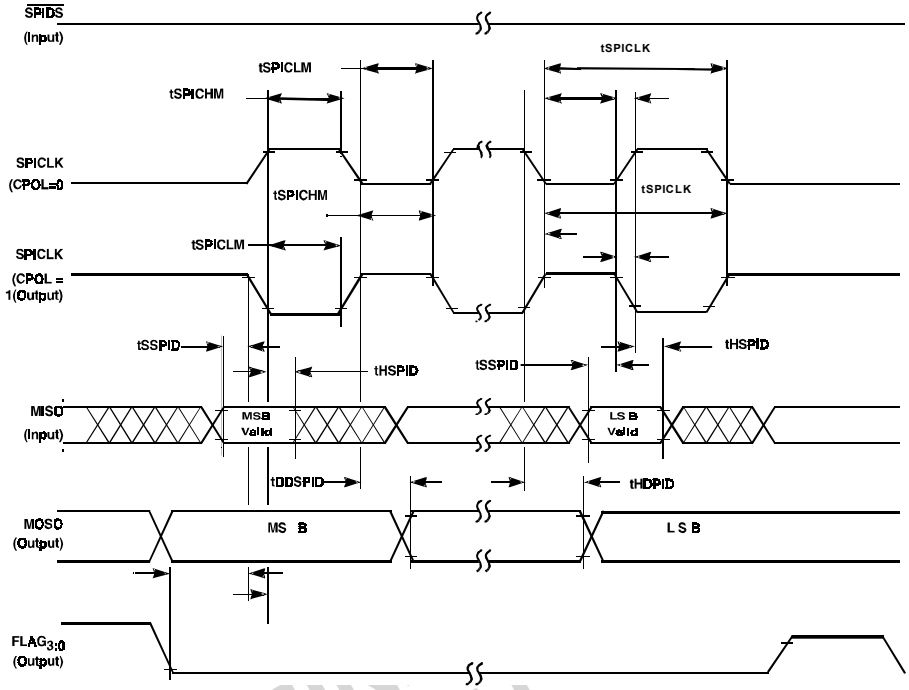


Figure 29 SPI Master Timing (CPHA=0)

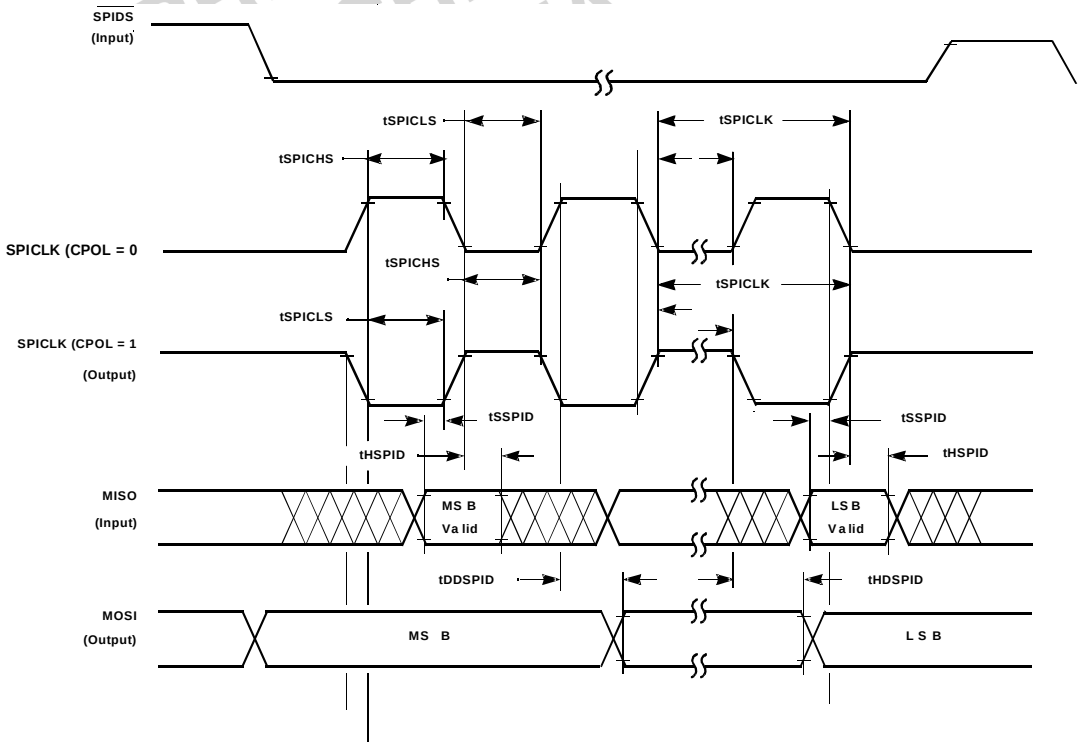


Figure 30 SPI Slave Timing (CPHA=0)

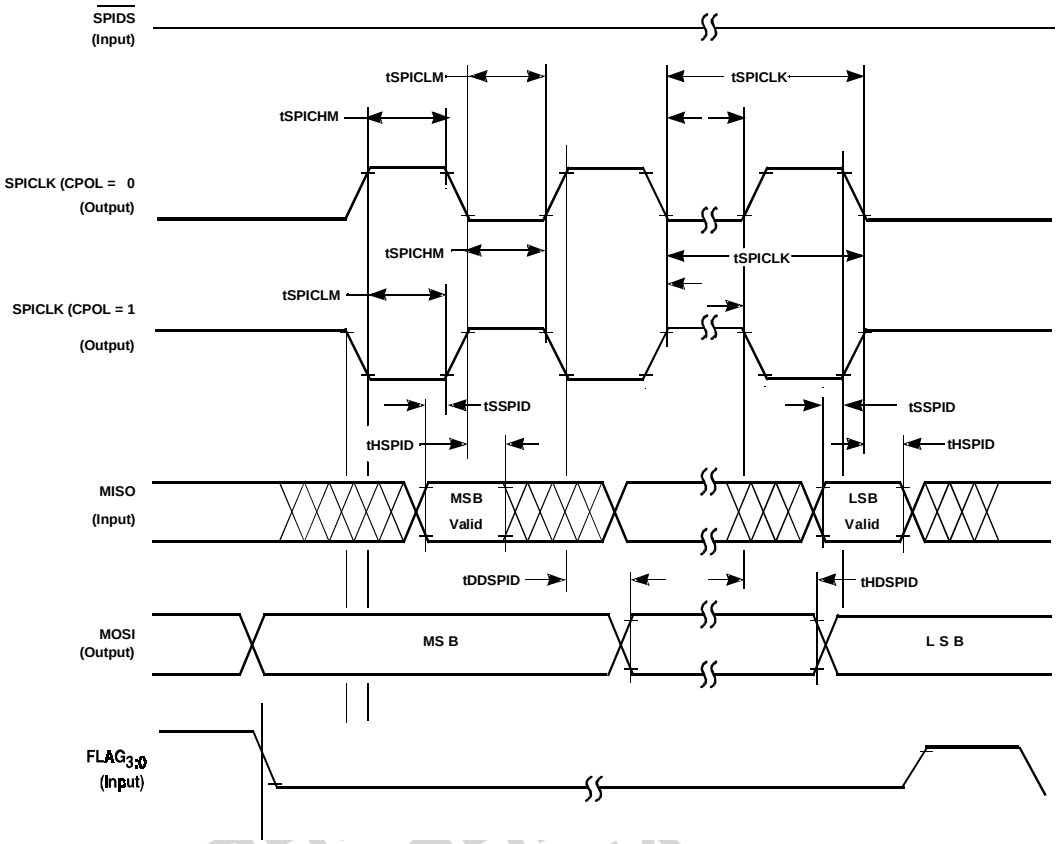


Figure 31 SPI Master Timing (CPHA=1)

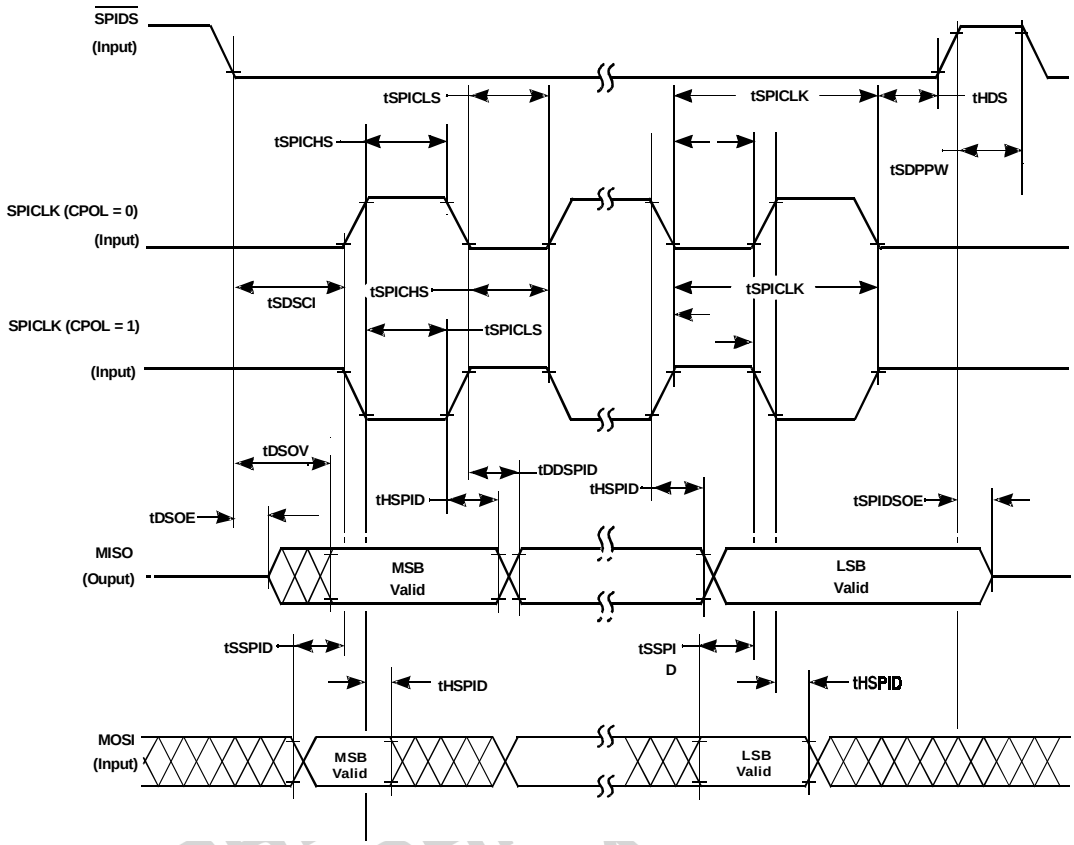


Figure 32 SPI Slave Timing (CPHA=0)

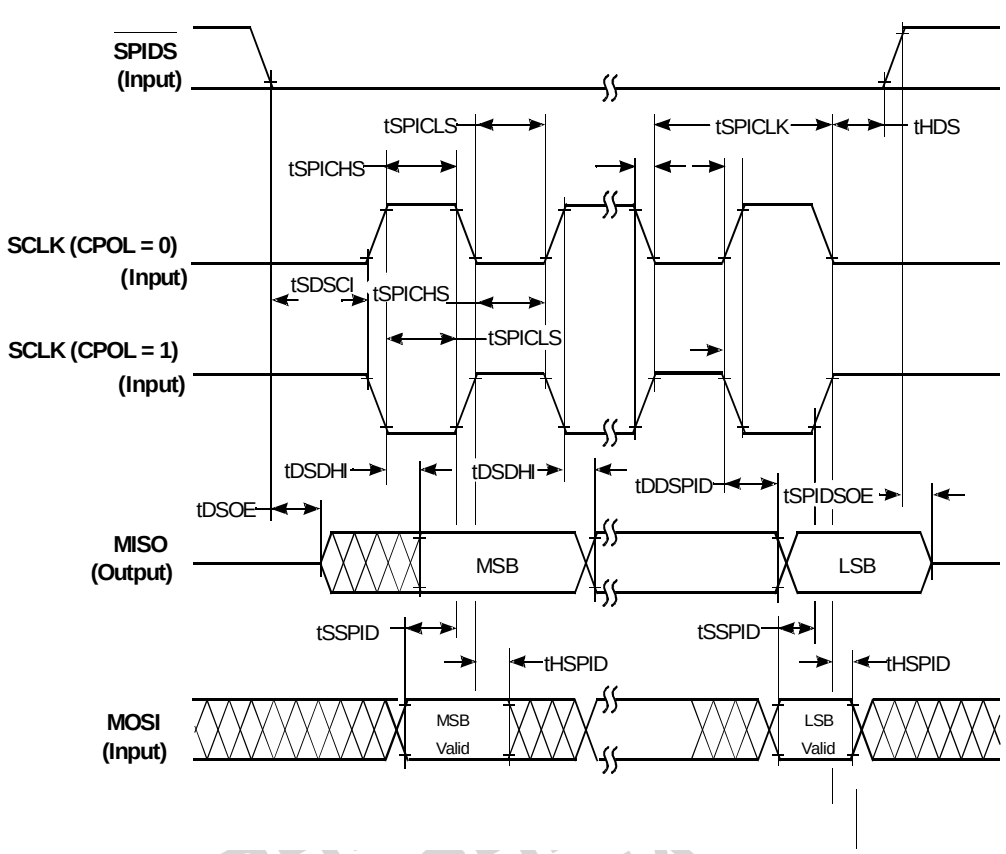


Figure 33 SPI Slave Timing (CPHA=1)

Table 34 JTAG Test Access Port and Emulation

Parameter		Min	Max	Units
Timing Requirements				
t_{TCK}	TCK Period	t_{CK}		ns
t_{STAP}	TDI, TMS Setup Before TCK High	5		ns
t_{HTAP}	TDI, TMS Hold After TCK High	6		ns
t_{SSYS}	System Inputs Setup Before TCK Low[1]	7		ns
t_{HSYS}	System Inputs Hold After TCK Low[1]	18		ns
t_{TRSTW}	$\overline{TRST}$ Pulse Width	$4t_{CK}$		ns
Switching Characteristics				
t_{DTDO}	TDO Delay from TCK Low		13	ns
t_{DSYS}	System Outputs Delay After TCK Low[2]		18	ns

1. System Inputs = $DATA_{47-16}$, $ADDR_{23-0}$, $\overline{RD}$, $\overline{WR}$, ACK, RPBA, $\overline{SPIDS}$, EBOOT, LBOOT, $\overline{DMAR}_{2-1,}$ CLK_CFG_{1-0}, $\overline{CLKDBL}$, $\overline{CS}$, $\overline{HBR}$, $\overline{SBTS}$, ID_{2-0}, $\overline{IRQ}_{2-0}$, $\overline{RESET}$, $\overline{BMS}$, MISO, MOSI, SPICLK, DxA, DxB, SCLKx, FSx, $LxDAT_{7-0}$, LxCLK, LxACK, $\overline{SDWE}$, $\overline{HBG}$, $\overline{RAS}$, $\overline{CAS}$, SDCLK0, SDCKE, BRST, $\overline{BR}_{6-1}$, $\overline{PA}$, $\overline{MS}_{3-0}$, $FLAG_{11-0}$
2. System Outputs = $\overline{BMS}$, MISO, MOSI, SPICLK, DxA, DxB, SCLKx, FSx, $LxDAT_{7-0}$, LxCLK, LxACK, $DATA^{47-16}$, $\overline{SDWE}$, ACK, $\overline{HBG}$, $\overline{RAS}$, $\overline{CAS}$, $SDCLK_{1-0}$, SDCKE, $\overline{BRST}$, $\overline{RD}$, $\overline{WR}$, $\overline{BR}_{6-1}$, $\overline{PA}$, $\overline{MS}_{3-0}$, $ADDR_{23-0}$, $FLAG_{11-0}$, $\overline{DMAG}_{2-1}$, DQM, REDY, CLKOUT, SDA10, TIMEXP, $\overline{EMU}$, $\overline{BMSTR}$.

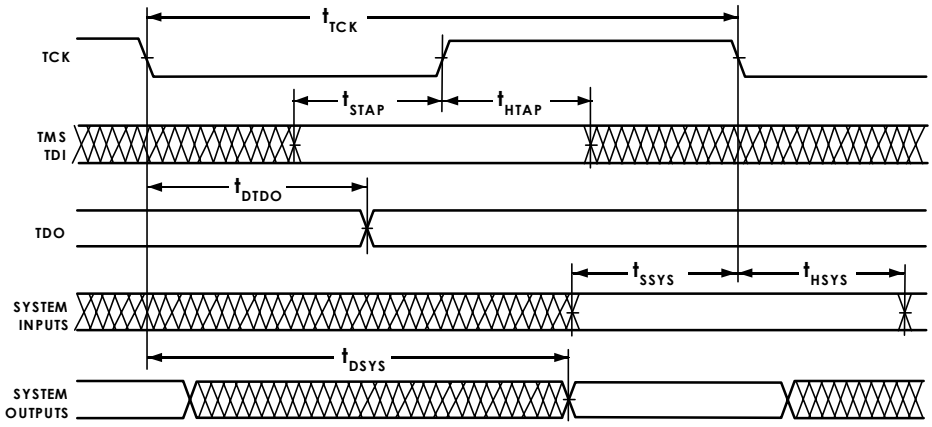


Figure 34 IEEE 11499.1 JTAG Test Access Port

OUTPUT DRIVE CURRENTS

Figure 38 on page 70 shows typical I-V characteristics for the output drivers of the ADSP-21161N. The curves represent the current drive capability of the output drivers as a function of output voltage.

POWER DISSIPATION

Total power dissipation has two components: one due to internal circuitry and one due to the switching of external output drivers.

Internal power dissipation is dependent on the instruction execution sequence and the data operands involved. Using the current specifications ($I_{DDINPEAK}$, $I_{DDINHIGH}$, $I_{DDINLOW}$, I_{DDIDLE}) from Table 5 on page 25 and the current-versus-operation information in Table 35, you can estimate the ADSP-21161N's internal power supply (V_{DDINT}) input current for a specific application, according to the following formula:

$$I_{DDINT} = \frac{\%Peak \times I_{DDINPEAK} + \%High \times I_{DDINHIGH} + \%Low \times I_{DDINLOW} + \%Idle \times I_{DDIDLE}}{}$$

Table 35 ADSP-21161N Operation Types Versus Input Current

Operation	**Peak Activity**[1] **($I_{DDINPEAK}$)**	**High Activity**[1] **($I_{DDINHIGH}$)**	**Low Activity**[1] **($I_{DDINLOW}$)**
Instruction Type	Multifunction	Multifunction	Single Function
Instruction Fetch	Cache	Internal Memory	Internal Memory
Core Memory Access[2]	2 per t_{CK} cycle (DM×64 and PM×64)	1 per t_{CK} cycle (DM×64)	None
Internal Memory DMA	1 per 2 t_{CCLK} cycles	1 per 2 t_{CCLK} cycles	N/A
External Memory DMA	1 per external port cycle (×32)	1 per external port cycle (×32)	N/A
Data bit pattern for core memory access and DMA	Worst case	Random	N/A

1. The state of the PEYEN bit (SIMD versus SISD mode) does not influence these calculations.
2. These assume a 2:1 core clock ratio. For more information on ratios and clocks (t_{CK} and t_{CCLK}), see the timing ratio definitions on page 27.

The external component of total power dissipation is caused by the switching of output pins. Its magnitude depends on:

- The number of output pins that switch during each cycle (O)
- The maximum frequency at which they can switch (f)

- Their load capacitance (C)
- Their voltage swing (VDD)

and is calculated by:

$$PEXT = O \times C \times VDD^2 \times f$$

The load capacitance should include the processors package capacitance (Cin). The switching frequency includes driving the load high and then back low. Address and data pins can drive high and low at a maximum rate of 1_{tck} while writing to a SDDRAM Memory.

Example:

Estimate Pext with the following assumptions:

- A system with one bank of external memory (32 bit)
- Two 1M x 16 SDRAM chips are used, each with a load of 10pF
- External Data Memory writes can occur every cycle at a rate of 1/tck, with 50% of the pins switching
- The bus cycle time is 50Mhz
- The external SDRAM clock rate is 100Mhz

The PEXT equation is calculated for each class of pins that can drive:

Table 36 External Power Calculations (3.3 V Device)

Pin Type	**# of Pins**	**% Switching**	**× C**	**× f**	**× VDD^2**	**= P_{EXT}**
Address	11	50	× 44.7 pF	50 MHz	× 10.9 V	= 0.134 W
MSx	4	0	× 44.7 pF	-	× 10.9 V	= 0.000 W
$\overline{SDWE}$	1	1	× 44.7 pF	-	× 10.9 V	= 0.024 W
Data	32	50	× 14.7 pF	50 MHz	× 10.9 V	= 0.128 W
SDCLK0	1	-	× 10.7 pF	100 MHz	× 10.9 V	= 0.012 W
						P_{EXT} = 0.298 W

A typical power consumption can now be calculated for these conditions by adding a typical internal power dissipation:

$$P_{TOTAL} = P_{EXT} + P_{INT} + P_{PLL}$$

Where:

P_{EXT} is from Table 36

P_{INT} is I_{DDINT} × 1.8V, using the calculation I_{DDINT} listed in "Power Dissipation" on page 67

P_{PLL} is AI_{DD} × 1.8V, using the value for AI_{DD} listed in Table 5 on page 25

Note that the conditions causing a worst-case PEXT are different from those causing a worst-case PINT. Maximum PINT cannot occur while 100% of the output pins are switching from all ones to all

zeros. Note also that it is not common for an application to have 100% or even 50% of the outputs switching simultaneously.

TEST CONDITIONS

Output Disable Time

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The time for the voltage on the bus to decay by –V is dependent on the capacitive load, CL and the load current, IL. This decay time can be approximated by the following equation:

$$t_{DECAY} = (C_L \Delta V)/I_L$$

The output disable time t_{DIS} is the difference between $t_{MEASURED}$ and t_{DECAY} as shown in Figure 25. The time $t_{MEASURED}$ is the interval from when the reference signal switches to when the output voltage decays –V from the measured output high or output low voltage. t_{DECAY} is calculated with test loads CL and IL, and with –V equal to 0.5 V.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high impedance state to the point when they start driving. The output enable time t_{ENA} is the interval from the point when a reference signal reaches a high or low voltage level to the point when the output has reached a specified high or low trip point, as shown in the Output Enable/Disable diagram (Figure 35). If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given above. Choose –V to be the difference between the ADSP-21161N's output voltage and the input threshold for the device requiring the hold time. A typical –V will be 0.4 V. CL is the total bus capacitance (per data line), and IL is the total leakage or three-state current (per data line). The hold time will be t_{DECAY} plus the minimum disable time (i.e., t_{DATRWH} for the write cycle).

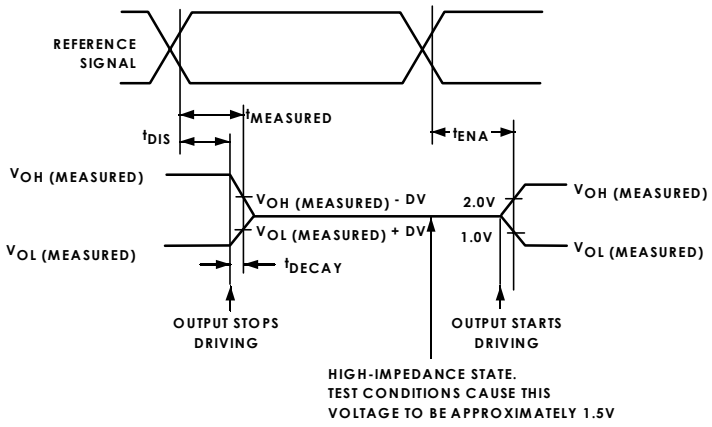


Figure 35 Output Enable/Disable

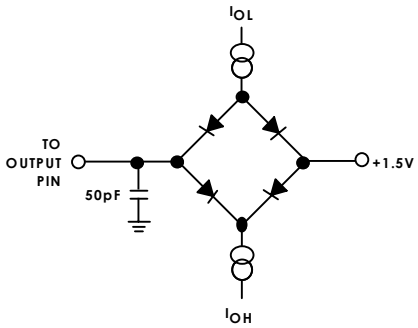


Figure 36 Equivalent Device Loading for AC Measurements (Includes All Fixtures)

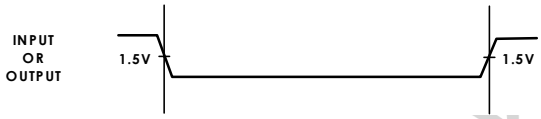


Figure 37 Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Capacitive Loading

Output delays and holds are based on standard capacitive loads: 50 pF on all pins (see Figure 36 on page 70). The delay and hold specifications given should be derated by a factor of 1.5 ns/50 pF for loads other than the nominal value of 50 pF. Figures 31-32, 34-35 show how output rise time varies with capacitance. Figures 33, 37 show graphically how output delays and holds vary with load capacitance (Note that this graph or derating does not apply to output disable delays; see "Output Disable Time" on page 69.). The graphs of Figures 31, 32 and 33 may not be linear outside the ranges shown.

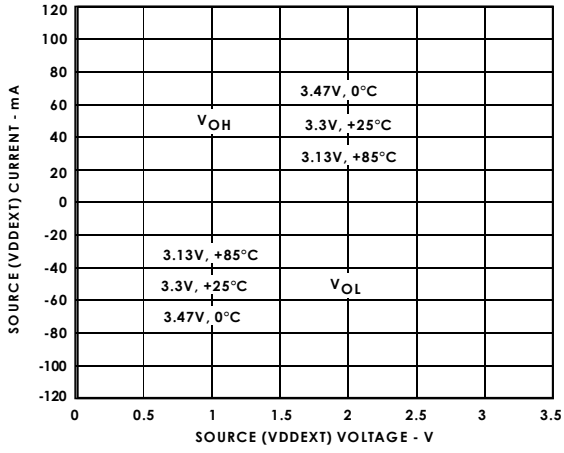


Figure 38 ADSP-21161N Typical Drive Currents

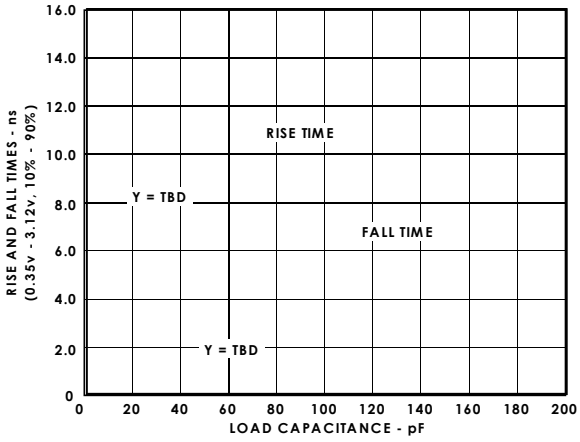


Figure 39 Typical Output Rise Time (10%-90%, V_{DDEXT}=Max) vs. Load Capacitance

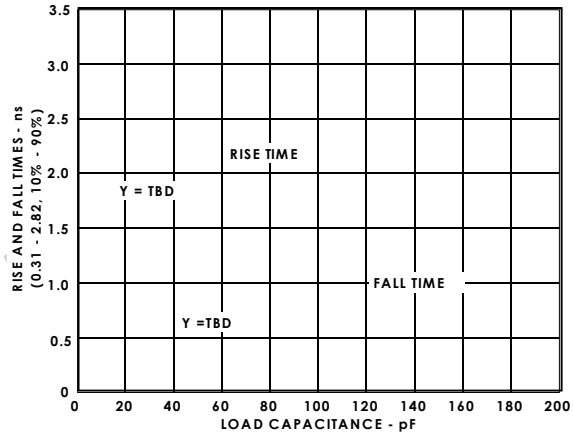


Figure 40 Typical Output Rise Time (10%-90%, V_{DDEXT}=Min) vs. Load Capacitance

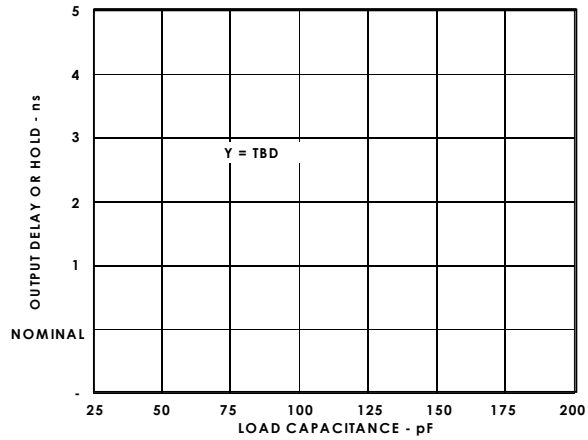


Figure 41 Typical Output Delay or Hold vs. Load Capacitance (at Max Case Temperature)

ENVIRONMENTAL CONDITIONS

Thermal Characteristics

The ADSP-21161N is packaged in a 225-lead Plastic Ball Grid Array (PBGA). The ADSP-21161N is specified for a case temperature (T_{CASE}). To ensure that the T_{CASE} data sheet specification is not exceeded, a heatsink and/or an air flow source may be used. Use the center block of ground pins (PBGA balls: F6-10, G6-10, H6-10, J6-10, K6-10) to provide thermal pathways to your printed circuit board's ground plane. A heatsink should be attached to the ground plane (as close as possible to the thermal pathways) with a thermal adhesive.

$T_{CASE} = T_{AMB} + (PD \times \theta_{CA})$

T_{CASE} = Case temperature (measured on top surface of package)

PD = Power dissipation in W (this value depends upon the specific application; a method for calculating PD is shown under Power Dissipation).

θ_{CA} = Value from table below.

Airflow (Linear Ft./Min.)	TBD	TBD	TBD	TBD	TBD
Airflow (Meters/Second)	TBD	TBD	TBD	TBD	TBD
θ_{CA} (°C/W)[1]	TBD	TBD	TBD	TBD	TBD

1. These are preliminary estimates.

θ_{JB} = **TBD** °C/W

NOTES

- This represents thermal resistance at total power of **TBD** W.
- With air flow, no variance is seen in θ_{CA} with power.
- θ_{CA} at 0 LFM varies with power: At [**DATA NOT AVAILABLE- TBD.**].
- θ_{JC} = **TBD** °C/W

225-BALL METRIC PBGA PIN CONFIGURATIONS

Table 37 225-Lead Metric PBGA Pin Assignments

Pin Name	PBGA Pin#	Pin Name	PBGA Pin#	Pin Name	PBGA Pin#	Pin Name	PBGA Pin#
NC	A01	TRST_B	B01	TMS	C01	TDO	D01
BMSTR	A02	TDI	B02	EMU_B	C02	TCK	D02
BMS_B	A03	RPBA	B03	GND	C03	FLAG11	D03
SPIDS	A04	MOSI	B04	SPICLK	C04	MISO	D04
EBOOT	A05	SFS0	B05	SD0B	C05	SCLK0	D05
LBOOT	A06	SCLK1	B06	SD1A	C06	SD1B	D06
SCLK2	A07	SD2B	B07	SD2A	C07	SFS1	D07
SD3B	A08	SD3A	B08	SFS2	C08	VDDINT	D08
L0DAT[4]	A09	L0DAT[7]	B09	SFS3	C09	SCLK3	D09
L0ACK	A10	L0CLK	B10	L0DAT[6]	C10	L0DAT[5]	D10
L0DAT[2]	A11	L0DAT[1]	B11	L1DAT[7]	C11	L0DAT[3]	D11
L1DAT[6]	A12	L1DAT[4]	B12	L1DAT[3]	C12	L1DAT[5]	D12
L1CLK	A13	L1ACK	B13	L1DAT[1]	C13	DATA[42]	D13
L1DAT[2]	A14	L1DAT[0]	B14	DATA[45]	C14	DATA[46]	D14
NC	A15	NC	B15	DATA[47]	C15	DATA[44]	D15
FLAG10	E01	FLAG5	F01	FLAG1	G01	FLAG0	H01
RESET_B	E02	FLAG7	F02	FLAG2	G02	IRQ0_B	H02
FLAG8	E03	FLAG9	F03	FLAG4	G03	VDDINT	H03
SD0A	E04	FLAG6	F04	FLAG3	G04	IRQ1_B	H04
VDDEXT	E05	VDDINT	F05	VDDEXT	G05	VDDINT	H05
VDDINT	E06	GND	F06	GND	G06	GND	H06
VDDEXT	E07	GND	F07	GND	G07	GND	H07
VDDINT	E08	GND	F08	GND	G08	GND	H08
VDDEXT	E09	GND	F09	GND	G09	GND	H09
VDDINT	E10	GND	F10	GND	G10	GND	H10
VDDEXT	E11	VDDINT	F11	VDDEXT	G11	VDDINT	H11
L0DAT[0]	E12	DATA[37]	F12	DATA[34]	G12	DATA[29]	H12
DATA[39]	E13	DATA[40]	F13	DATA[35]	G13	DATA[28]	H13
DATA[43]	E14	DATA[38]	F14	DATA[33]	G14	DATA[30]	H14

Table 37 225-Lead Metric PBGA Pin Assignments (Continued)

Pin Name	PBGA Pin#	Pin Name	PBGA Pin#	Pin Name	PBGA Pin#	Pin Name	PBGA Pin#
DATA[41]	E15	DATA[36]	F15	DATA[32]	G15	DATA[31]	H15
IRQ2_B	J01	TIMEXP	K01	ADDR[19]	L01	ADDR[16]	M01
ID1	J02	ADDR[22]	K02	ADDR[17]	L02	ADDR[12]	M02
ID2	J03	ADDR[20]	K03	ADDR[21]	L03	ADDR[18]	M03
ID0	J04	ADDR[23]	K04	ADDR[2]	L04	ADDR[6]	M04
VDDEXT	J05	VDDINT	K05	VDDEXT	L05	ADDR[0]	M05
GND	J06	GND	K06	VDDINT	L06	MS1_B	M06
GND	J07	GND	K07	VDDEXT	L07	BR6_B	M07
GND	J08	GND	K08	VDDINT	L08	VDDEXT	M08
GND	J09	GND	K09	VDDEXT	L09	WRL_B	M09
GND	J10	GND	K10	VDDINT	L10	SDA10	M10
VDDEXT	J11	VDDINT	K11	VDDEXT	L11	RAS_B	M11
DATA[26]	J12	DATA[22]	K12	CAS_B	L12	ACK	M12
DATA[24]	J13	DATA[19]	K13	DATA[20]	L13	DATA[17]	M13
DATA[25]	J14	DATA[21]	K14	DATA[16]	L14	DMAG2_B	M14
DATA[27]	J15	DATA[23]	K15	DATA[18]	L15	DMAG1_B	M15
ADDR[14]	N01	ADDR[13]	P01	NC	R01		
ADDR[15]	N02	ADDR[9]	P02	ADDR[11]	R02		
ADDR[10]	N03	ADDR[8]	P03	ADDR[7]	R03		
ADDR[5]	N04	ADDR[4]	P04	ADDR[3]	R04		
ADDR[1]	N05	MS2_B	P05	MS3_B	R05		
MS0_B	N06	SBTS_B	P06	PA_B	R06		
BR5_B	N07	BR4_B	P07	BR3_B	R07		
BR2_B	N08	BR1_B	P08	RDL_B	R08		
BRST	N09	SDCLK1	P09	CLKOUT	R09		
SDCKE	N10	SDCLK0	P10	HBR_B	R10		
CS_B	N11	REDY	P11	HBG_B	R11		
CLK_CFG1	N12	CLKIN	P12	$\overline{\text{CLKDBL}}$	R12		
CLK_CFG0	N13	DQM	P13	XTAL	R13		
AVDD	N14	AVSS	P14	SDWE_B	R14		
DMAR1_B	N15	DMAR2_B	P15	NC	R15		

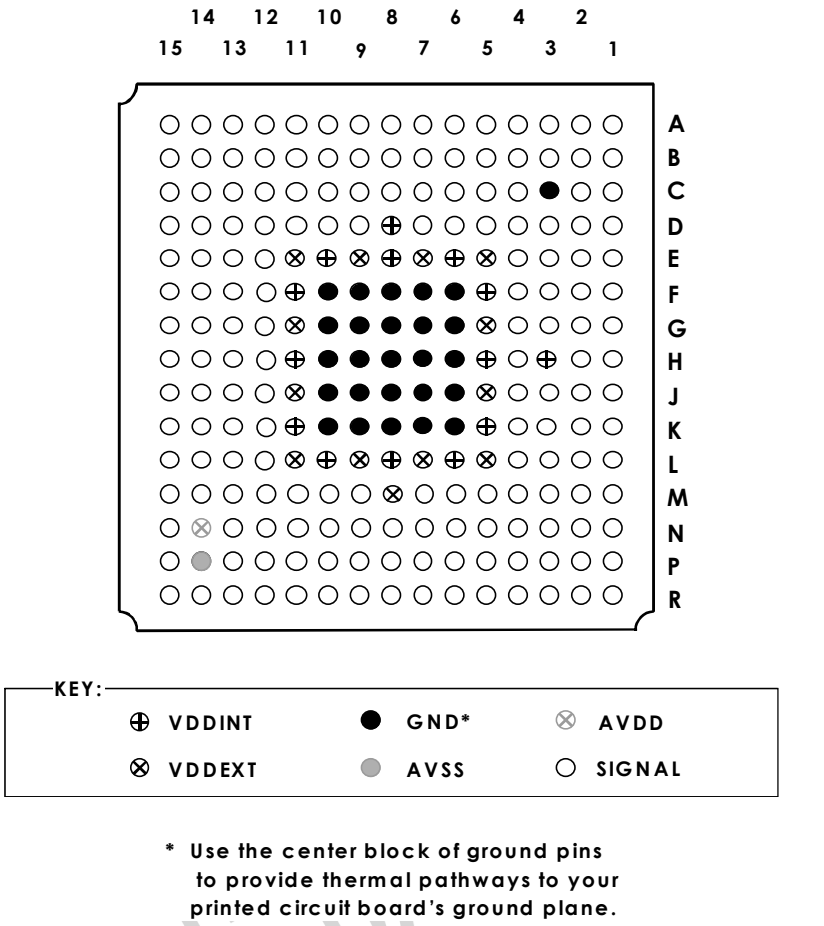


Figure 42 225-Lead Metric PBGA Pin Assignments (Bottom View, Summary)

PACKAGE DIMENSIONS

The ADSP-21161N comes in a 17mm × 17mm, 225 ball PBGA package with 15 rows of balls. All dimensions in Figure 43 are in millimeters (mm).

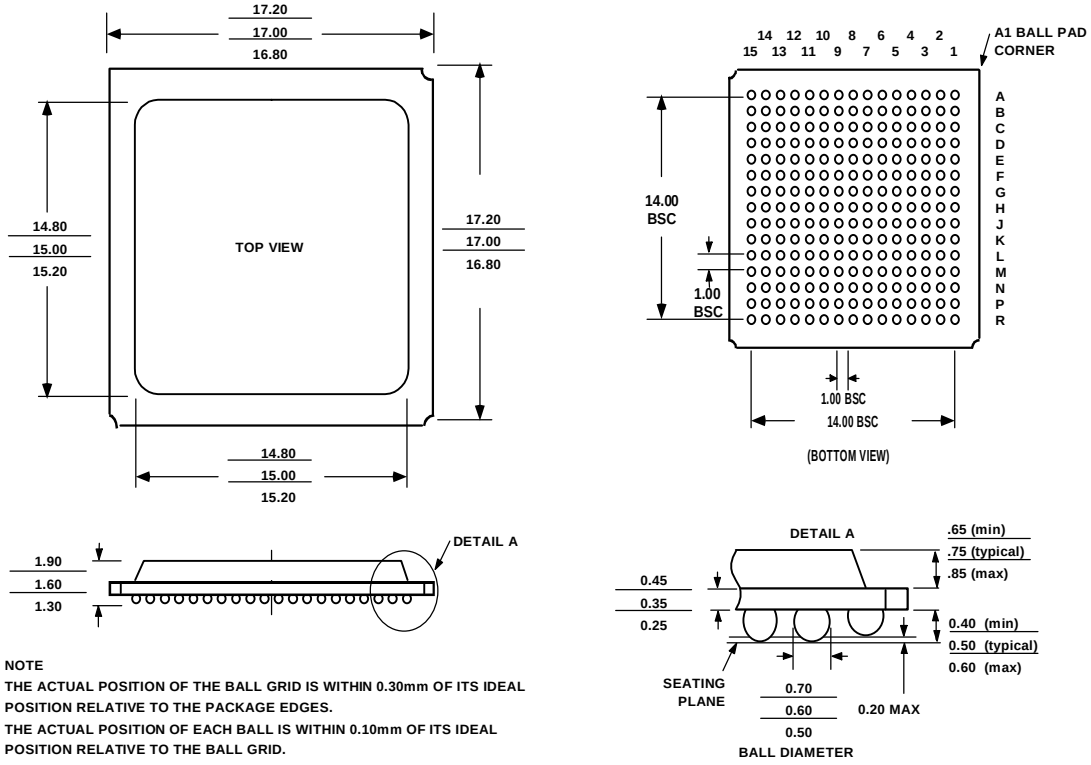


Figure 43 Package Dimensions Metric 17mm × 17mm, 225 ball PBGA

ORDERING GUIDE

Part Number[1]	Case Temperature Range[2]	Instruction Rate	On-Chip SRAM	Operating Voltage
ADSP-21161N-KB-100X	0°C to +85°C	100 MHz	1 Mbit	1.8 INT/3.3 EXT V

1. These parts are packaged in a 225-lead Plastic Ball Grid Array (PBGA).
2. Parts for the industrial temperature ranges will be available in 2000.