SHARC® Processor Data Sheet Addendum

Preliminary Technical Data

ADSP-21367/ADSP-21368/ADSP-21369

SUMMARY

High performance 32-bit/40-bit floating point processor optimized for high performance audio processing

Single-instruction, multiple-data (SIMD) computational architecture

On-chip memory—2M bit of on-chip SRAM and 6M bit of on-chip mask programmable ROM

400 MHz maximum core clock frequency

1.3 V core V_{DD}/3.3 V I/O

Code compatible with all other members of the SHARC family

The ADSP-21367/ADSP-21368/ADSP-21369 are available with a 400 MHz core instruction rate with unique audio-centric peripherals such as the digital audio interface, S/PDIF transceiver, serial ports, 8-channel asynchronous sample rate converter, precision clock generators, and more. For complete ordering information, see Ordering Guide on Page 11.

At 400 MHz (2.5 ns) core instruction rate, the processors perform 2.4 GFLOPS/800 MMACS

Transfers between memory and core at a sustained 6.4G bytes/s bandwidth at 400 MHz core instruction rate

GENERAL DESCRIPTION

This data sheet addendum introduces the 400 MHz ADSP-21367/ADSP-21368/ADSP-21369 SHARC processors. This addendum provides the frequency benchmark, as well as ac and dc specifications that differ from the 333 MHz ADSP-21367/ADSP-21368/ADSP-21369 SHARC processors. All other specifications and timing data as well as package information for these devices can be found in the ADSP-21367/ADSP-21368/ADSP-21369 SHARC Processor Data Sheet, Rev A. The products listed in the addendum are engineering grade and have not been fully characterized. For complete ordering information, see the Ordering Guide on Page 11.

Rev. PrA

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TABLE OF CONTENTS

PERFORMANCE BENCHMARKS

The processors use two computational units to deliver a significant performance increase over the previous SHARC processors on a range of DSP algorithms. Fabricated in a state-of-the-art, high speed, CMOS process, the ADSP-21367/ADSP-21368/ADSP-21369 processors achieve an instruction cycle time of up to 2.5 ns at 400 MHz. With its SIMD computational hardware, the processors can perform 2.4 GFLOPS running at 400 MHz.

Table 1 shows performance benchmarks for these devices.

Table 1. Processor Benchmarks (at 400 MHz)

Benchmark Algorithm	Speed (at 400 MHz)
1024 Point Complex FFT (Radix 4, with reversal)	23.2 µs
FIR Filter (per tap)[1]	1.25 ns
IIR Filter (per biquad)[1]	5.0 ns
Matrix Multiply (pipelined)	
[3×3] × [3×1]	11.25 ns
[4×4] × [4×1]	20.0 ns
Divide (y/×)	8.75 ns
Inverse Square Root	13.5 ns

[1] Assumes two files in multichannel SIMD mode.

POWER SUPPLIES

The processors have separate power supply connections for the internal (V_{DDINT}), external (V_{DDEXT}), and analog (A_{VDD}/A_{VSS}) power supplies. The internal and analog supplies must meet the 1.3 V requirement for the 400 MHz device. The external supply must meet the 3.3 V requirement. All external supply pins must be connected to the same power supply.

SPECIFICATIONS

OPERATING CONDITIONS

Parameter[1]	Description	Min	Max	Unit
V_{DDINT}	Internal (Core) Supply Voltage	1.25	1.35	V
A_{VDD}	Analog (PLL) Supply Voltage	1.25	1.35	V
V_{DDEXT}	External (I/O) Supply Voltage	3.13	3.47	V
V_{IH}[2]	High Level Input Voltage @ V_{DDEXT} = max	2.0	V_{DDEXT} + 0.5	V
V_{IL}[2]	Low Level Input Voltage @ V_{DDEXT} = min	–0.5	+0.8	V
V_{IH_CLKIN}[3]	High Level Input Voltage @ V_{DDEXT} = max	1.74	V_{DDEXT} + 0.5	V
V_{IL_CLKIN}[3]	Low Level Input Voltage @ V_{DDEXT} = min	–0.5	+1.1	V
T_J	Junction Temperature, 256-Ball SBGA @ $T_{AMBIENT}$ 0°C to +70°C	0	+105	°C

[1] Specifications subject to change without notice.
[2] Applies to input and bidirectional pins: DATAx, ACK, RPBA, $\overline{BRx}$, IDx, FLAGx, DAI_Px, DPI_Px, BOOT_CFGx, CLK_CFGx, $\overline{RESET}$, TCK, TMS, TDI, $\overline{TRST}$.
[3] Applies to input pin CLKIN.

ELECTRICAL CHARACTERISTICS

Parameter[1]	Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}[2]	High Level Output Voltage	@ V_{DDEXT} = min, I_{OH} = –1.0 mA[3]	2.4			V
V_{OL}[2]	Low Level Output Voltage	@ V_{DDEXT} = min, I_{OL} = 1.0 mA[3]			0.4	V
I_{IH}[4, 5]	High Level Input Current	@ V_{DDEXT} = max, V_{IN} = V_{DDEXT} max			10	µA
I_{IL}[4, 6, 7]	Low Level Input Current	@ V_{DDEXT} = max, V_{IN} = 0 V			10	µA
I_{IHPD}[6]	High Level Input Current Pull-down	@ V_{DDEXT} = max, V_{IN} = 0 V			250	µA
I_{ILPU}[5]	Low Level Input Current Pull-up	@ V_{DDEXT} = max, V_{IN} = 0 V			200	µA
I_{OZH}[8, 9]	Three-State Leakage Current	@ V_{DDEXT} = max, V_{IN} = V_{DDEXT} max			10	µA
I_{OZL}[8, 10]	Three-State Leakage Current	@ V_{DDEXT} = max, V_{IN} = 0 V			10	µA
I_{OZLPU}[9]	Three-State Leakage Current Pull-up	@ V_{DDEXT} = max, V_{IN} = 0 V			200	µA
$I_{DD-INTYP}$[11]	Supply Current (Internal)	t_{CCLK} = 2.5 ns, V_{DDINT} = 1.3 V, 25°C		1.4		A
AI_{DD}[12]	Supply Current (Analog)	A_{VDD} = max			10	mA
C_{IN}[13, 14]	Input Capacitance	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 1.3 V			4.7	pF

[1] Specifications subject to change without notice.
[2] Applies to output and bidirectional pins: ADDRx, DATAx, $\overline{RD}$, $\overline{WR}$, $\overline{MSx}$, $\overline{BRx}$, FLAGx, DAI_Px, DPI_Px, $\overline{SDRAS}$, $\overline{SDCAS}$, $\overline{SDWE}$, SDCKE, SDA10, SDCLKx, $\overline{EMU}$, TDO, CLKOUT.
[3] See Output Drive Currents on Page 10 for typical drive current capabilities.
[4] Applies to input pins without internal pull-ups: BOOT_CFGx, CLK_CFGx, CLKIN, $\overline{RESET}$, TCK.
[5] Applies to input pins with internal pull-ups: ACK, RPBA, TMS, TDI, TRST.
[6] Applies to input pins with internal pull-downs: IDx.
[7] Applies to input pins with internal pull-ups disabled: ACK, RPBA.
[8] Applies to three-statable pins without internal pull-ups: FLAGx, SDCLKx, TDO.
[9] Applies to three-statable pins with internal pull-ups: ADDRx, DATAx, $\overline{RD}$, $\overline{WR}$, $\overline{MSx}$, $\overline{BRx}$, DAI_Px, DPI_Px, $\overline{SDRAS}$, $\overline{SDCAS}$, $\overline{SDWE}$, SDCKE, SDA10, $\overline{EMU}$.
[10] Applies to three-statable pins with internal pull-ups disabled: ADDRx, DATAx, $\overline{RD}$, $\overline{WR}$, $\overline{MSx}$, $\overline{BRx}$, DAI_Px, DPI_Px, $\overline{SDRAS}$, $\overline{SDCAS}$, $\overline{SDWE}$, SDCKE, SDA10
[11] See Engineer-to-Engineer Note 299 for further information.
[12] Characterized, but not tested.
[13] Applies to all signal pins.
[14] Guaranteed, but not tested.

TIMING SPECIFICATIONS

The processor's internal clock (a multiple of CLKIN) provides the clock signal for timing internal memory, processor core, and serial ports. During reset, program the ratio between the processor's internal clock frequency and external (CLKIN) clock frequency with the CLK_CFG1–0 pins. To determine switching frequencies for the serial ports, divide down the internal clock, using the programmable divider control of each port (DIVx for the serial ports).

The processor's internal clock switches at higher frequencies than the system input clock (CLKIN). To generate the internal clock, the processor uses an internal phase-locked loop (PLL). This PLL-based clocking minimizes the skew between the system clock (CLKIN) signal and the processor's internal clock.

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, it is not meaningful to add parameters to derive longer times.

Switching Characteristics specify how the processor changes its signals. Circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics describe what the processor will do in a given circumstance. Use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing Requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

Power-Up Sequencing

The timing requirements for processor startup are given in Table 2.

Table 2. Power-Up Sequencing Timing Requirements (Processor Startup)

Parameter		Min	Max	Unit
Timing Requirements				
t_{RSTVDD}	$\overline{\text{RESET}}$ Low Before V_{DDINT}/V_{DDEXT} On	0		ns
$t_{IVDDEVDD}$	V_{DDINT} On Before V_{DDEXT}	–50	+200	ms
t_{CLKVDD} [1]	CLKIN Valid After V_{DDINT}/V_{DDEXT} Valid	0	+200	ms
t_{CLKRST}	CLKIN Valid Before $\overline{\text{RESET}}$ Deasserted	10^{2}		µs
t_{PLLRST}	PLL Control Setup Before $\overline{\text{RESET}}$ Deasserted	20		µs
Switching Characteristic				
$t_{CORERST}$	Core Reset Deasserted After $\overline{\text{RESET}}$ Deasserted	$4096t_{CK} + 2\ t_{CCLK}$ [3, 4]		

[1] Valid V_{DDINT}/V_{DDEXT} assumes that the supplies are fully ramped to their 1.3 volt rails and 3.3 volt rails. Voltage ramp rates can vary from microseconds to hundreds of milliseconds depending on the design of the power supply subsystem.

[2] Assumes a stable CLKIN signal, after meeting worst-case startup timing of crystal oscillators. Refer to your crystal oscillator manufacturer's data sheet for start-up time. Assume a 25 ms maximum oscillator start-up time if using the XTAL pin and internal oscillator circuit in conjunction with an external crystal.

[3] Applies after the power-up sequence is complete. Subsequent resets require $\overline{\text{RESET}}$ to be held low a minimum of four CLKIN cycles in order to properly initialize and propagate default states at all I/O pins.

[4] The 4096 cycle count depends on t_{srst} specification. If setup time is not met, 1 additional CLKIN cycle may be added to the core reset time, resulting in 4097 cycles maximum.

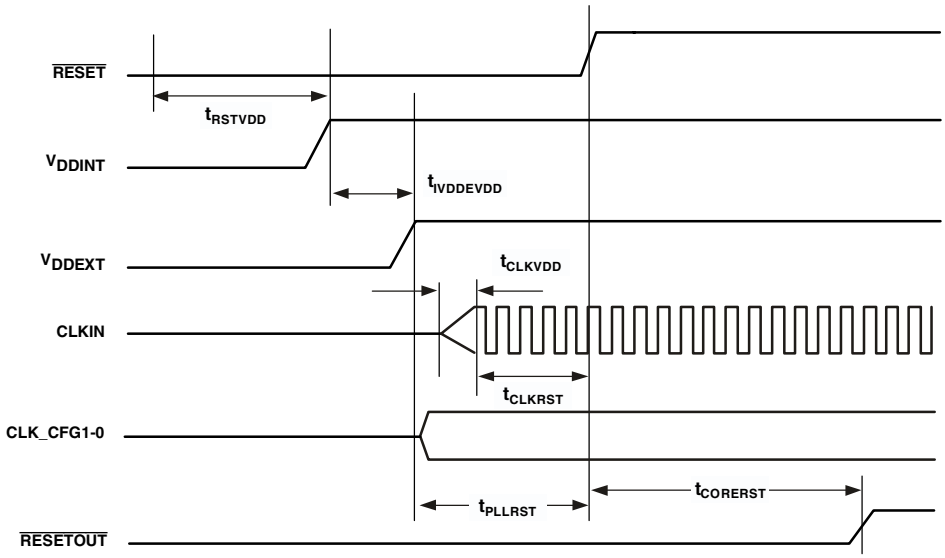

Figure 1. Power-Up Sequencing

Clock Input

Table 3. Clock Input

Parameter		400 MHz Min	400 MHz Max	Unit
Timing Requirements				
t_{CK}	CLKIN Period	18[1]	100[2]	ns
t_{CKL}	CLKIN Width Low	8[1]	45[2]	ns
t_{CKH}	CLKIN Width High	8[1]	45[2]	ns
t_{CKRF}	CLKIN Rise/Fall (0.4 V to 2.0 V)		3	ns
t_{CCLK}[3]	CCLK Period	2.5[1]	10	ns
t_{CKJ}[4, 5]	CLKIN Jitter Tolerance	–250	+250	ps

[1] Applies only for CLK_CFG1–0 = 00 and default values for PLL control bits in PMCTL.

[2] Applies only for CLK_CFG1–0 = 10 and default values for PLL control bits in PMCTL.

[3] Any changes to PLL control bits in the PMCTL register must meet core clock timing specification t_{CCLK}.

[4] Actual input jitter should be combined with ac specifications for accurate timing analysis.

[5] Jitter specification is maximum peak-to-peak time interval error (TIE) jitter.

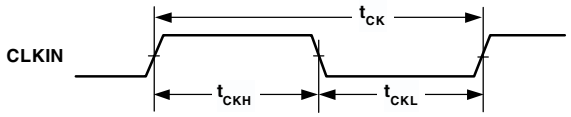

Figure 2. Clock Input

Clock Signals

The processors can use an external clock or a crystal. See the CLKIN pin description. Programs can configure the processor to use its internal clock generator by connecting the necessary components to CLKIN and XTAL. Figure 3 shows the component connections used for a crystal operating in fundamental mode. Note that the clock rate is achieved using a 25 MHz crystal and a PLL multiplier ratio 16:1 (CCLK:CLKIN achieves a clock speed of 400 MHz). To achieve the full core clock rate, programs need to configure the multiplier bits in the PMCTL register.

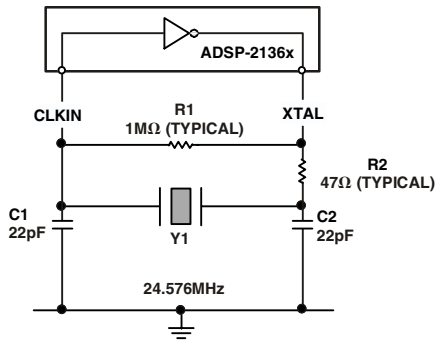

Figure 3. 400 MHz Operation (Fundamental Mode Crystal)

SDRAM Interface Timing (133 MHz SDCLK)

The 133 MHz access speed is for a single processor. When multiple ADSP-21368 processors are connected in a shared memory system, the access speed is 100 MHz.

Table 4. SDRAM Interface Timing[1]

Parameter		Min	Max	Unit
Timing Requirements				
t_{SSDAT}	DATA Setup Before SDCLK	0.78		ns
t_{HSDAT}	DATA Hold After SDCLK	1.23		ns
Switching Characteristics				
t_{SDCLK}	SDCLK Period	7.5		ns
t_{SDCLKH}	SDCLK Width High	3.65		ns
t_{SDCLKL}	SDCLK Width Low	3.65		ns
t_{DCAD}	Command, ADDR, Data Delay After SDCLK[2]		4.8	ns
t_{HCAD}	Command, ADDR, Data Hold After SDCLK[2]	1.2		ns
t_{DSDAT}	Data Disable After SDCLK		5.3	ns
t_{ENSDAT}	Data Enable After SDCLK	1.2		ns

[1] For F_{CCLK} = 400 MHz (SDCLK ratio = 1:2.5).
[2] Command pins include: $\overline{SDCAS}$, $\overline{SDRAS}$, $\overline{SDWE}$, $\overline{MSx}$, SDA10, SDCKE.

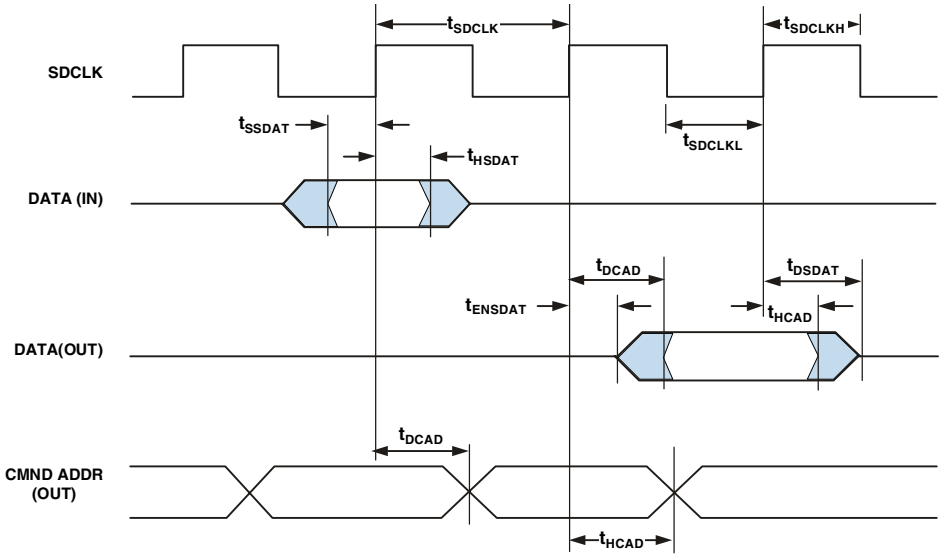

Figure 4. SDRAM Interface Timing

SDRAM Interface Enable/Disable Timing (133 MHz SDCLK)

Table 5. SDRAM Interface Enable/Disable Timing[1]

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DSDC}	Command Disable After CLKIN Rise		$2 \times t_{PCLK} + 1$	ns
t_{ENSDC}	Command Enable After CLKIN Rise	4.0		ns
t_{DSDCC}	SDCLK Disable After CLKIN Rise		8.5	ns
t_{ENSDCC}	SDCLK Enable After CLKIN Rise	3.8		ns
t_{DSDCA}	Address Disable After CLKIN Rise		9.2	ns
t_{ENSDCA}	Address Enable After CLKIN Rise	$2 \times t_{PCLK} - 4$	$4 \times t_{PCLK}$	ns

[1] For F_{CCLK} = 400 MHz (SDCLK ratio = 1:2.5).

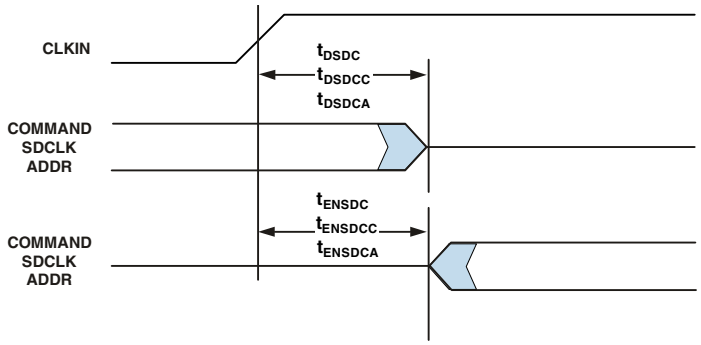

Figure 5. SDRAM Interface Enable/Disable Timing

Pin to Pin Direct Routing (DAI and DPI)

For direct pin connections only (for example, DAI_PB01_I to DAI_PB02_O).

Table 6. DAI Pin to Pin Routing

Parameter		Min	Max	Unit
Timing Requirement				
t_{DPIO}	Delay DAI Pin Input Valid to DAI Output Valid	1.5	12	ns

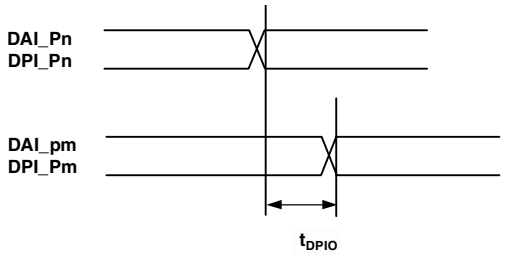

Figure 6. DAI Pin to Pin Direct Routing

Memory Read – Bus Master to Memory Read

Use these specifications for asynchronous interfacing to memories. These specifications apply when the processors are the bus master accessing external memory space in asynchronous access mode. Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and strobe timing parameters only apply to asynchronous access mode.

Table 7. Memory Read—Bus Master

Parameter		Min	Max	Unit
Timing Requirements				
t_{DAD}	Address, Selects Delay to Data Valid[1, 2]		$W+t_{SDCLK}-5.12$	ns
t_{DRLD}	$\overline{RD}$ Low to Data Valid[1]		W– 2.9	ns
t_{SDS}	Data Setup to $\overline{RD}$ High	2.2		ns
t_{HDRH}	Data Hold from $\overline{RD}$ High[3, 4]	0		ns
t_{DAAK}	ACK Delay from Address, Selects[2, 5]		$t_{SDCLK}-9.5+W$	ns
t_{DSAK}	ACK Delay from $\overline{RD}$ Low[4]		W – 7.0	ns
Switching Characteristics				
t_{DRHA}	Address Selects Hold After $\overline{RD}$ High	RH + 0.18		ns
t_{DARL}	Address Selects to $\overline{RD}$ Low[2]	$t_{SDCLK}-3.3$		ns
t_{RW}	$\overline{RD}$ Pulse Width	W – 1.2		ns
t_{RWR}	$\overline{RD}$ High to $\overline{WR}$, $\overline{RD}$ Low	HI $+t_{SDCLK}$ – 0.8		ns

W = (number of wait states specified in AMICTLx register) × t_{SDCLK}.
HI =RHC + IC (RHC = number of read hold cycles specified in AMICTLx register) × t_{SDCLK}
IC = (number of idle cycles specified in AMICTLx register) × t_{SDCLK}.
H = (number of hold cycles specified in AMICTLx register) × t_{SDCLK}.

[1] Data delay/setup: system must meet t_{DAD}, t_{DRLD}, or t_{SDS}.
[2] The falling edge of $\overline{MS}$x is referenced.
[3] Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and strobe timing parameters only apply to asynchronous access mode.
[4] Data hold: User must meet t_{HDA} or t_{HDRH} in asynchronous access mode.
[5] ACK Delay/Setup: User must meet t_{DAAK}, or t_{DSAK}, for deassertion of ACK (low). For asynchronous assertion of ACK (high) user must meet t_{DAAK} or t_{DSAK}.

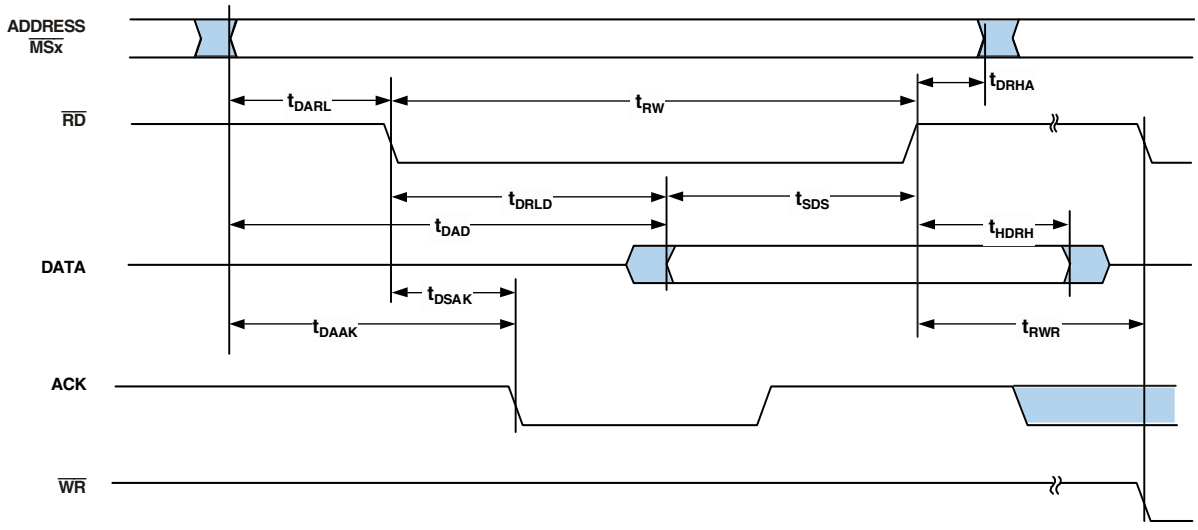

Figure 7. Memory Read—Bus Master

OUTPUT DRIVE CURRENTS

Figure 8 shows typical I-V characteristics for the output drivers of the ADSP-21367/ADSP-21368/ADSP-21369. The curves represent the current drive capability of the output drivers as a function of output voltage.

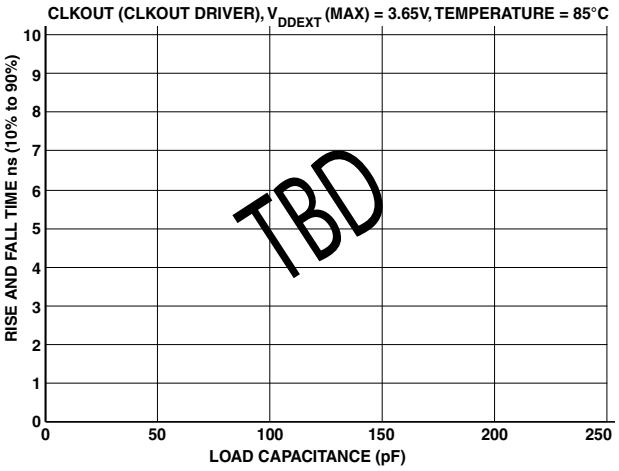

Figure 8. Typical Drive at Junction temperature

CAPACITIVE LOADING

Output delays and holds are based on standard capacitive loads: 30 pF on all pins. Figure 11 shows graphically how output delays and holds vary with load capacitance. The graphs of Figure 9, Figure 10, and Figure 11 may not be linear outside the ranges shown for Typical Output Delay vs. Load Capacitance and Typical Output Rise Time (20% to 80%, V = Min) vs. Load Capacitance.

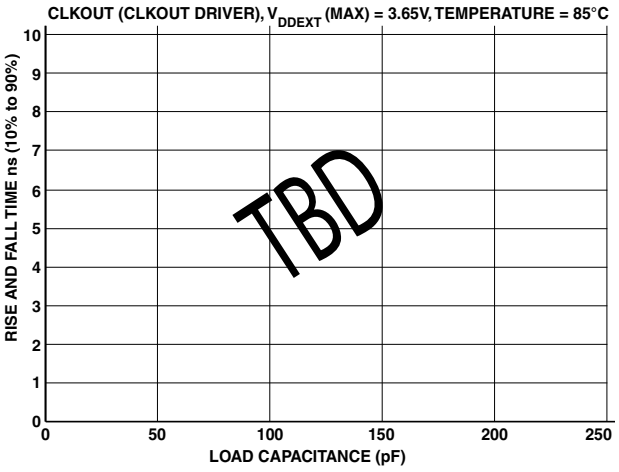

Figure 9. Typical Output Rise/Fall Time (20% to 80%, V_{DDEXT} = Max)

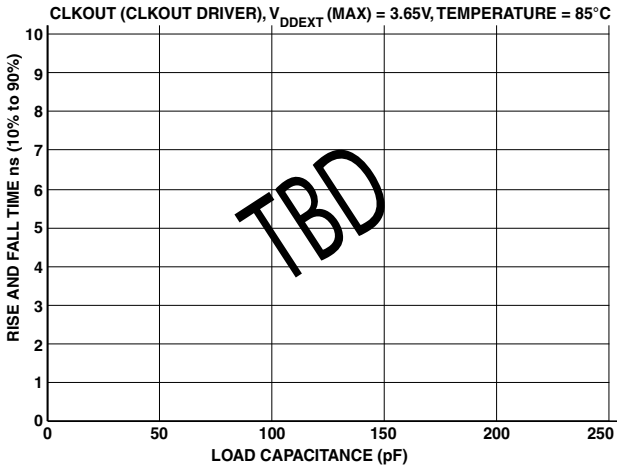

Figure 10. Typical Output Rise/Fall Time (20% to 80%, V_{DDEXT} = Min)

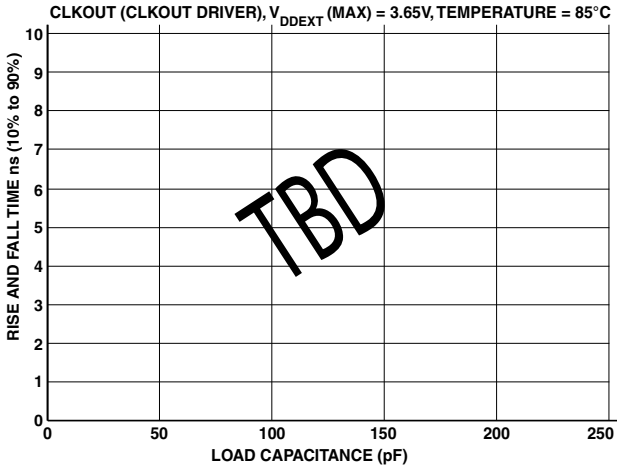

Figure 11. Typical Output Delay or Hold vs. Load Capacitance (at Junction Temperature)

ORDERING GUIDE

Part Number	Temperature Range	Instruction Rate	On-Chip SRAM	ROM	Operating Voltage Internal/External	Package Description	Package Option
ADSP-21367KBP-3A[1]	0°C to +70°C	400 MHz	2M bit	6M bit	1.3 V/3.3 V	256-Ball SBGA	BP-256
ADSP-21367KBPZ-3A[2]	0°C to +70°C	400 MHz	2M bit	6M bit	1.3 V/3.3 V	256-Ball SBGA	BP-256
ADSP-21368KBP-3A	0°C to +70°C	400 MHz	2M bit	6M bit	1.3 V/3.3 V	256-Ball SBGA	BP-256
ADSP-21368KBPZ-3A[2]	0°C to +70°C	400 MHz	2M bit	6M bit	1.3 V/3.3 V	256-Ball SBGA	BP-256
ADSP-21369KBP-3A	0°C to +70°C	400 MHz	2M bit	6M bit	1.3 V/3.3 V	256-Ball SBGA	BP-256
ADSP-21369KBPZ-3A[2]	0°C to +70°C	400 MHz	2M bit	6M bit	1.3 V/3.3 V	256-Ball SBGA	BP-256

[1] Available with a wide variety of audio algorithm combinations sold as part of a chipset and bundled with necessary software. For a complete list, visit our website at www.analog.com/SHARC.
[2] Z = RoHS Compliant Part.

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