ANALOG DEVICES

Concurrent Signal Processor

ADSP-21csp01

FEATURES

Performance
20 ns Instruction Cycle Time from 25 MHz Crystal @ 5.0 V
50 MIPS Sustained Performance
24-Bit Address Bus with a Unified 16M Address Space
32 Flexible Data Registers Provide Local Variable Storage
64 Data Addressing Registers Support 16 Data Structures
Background Registers Provide Single-Cycle Context Switch
Multifunction Instructions Combine Memory Read or Write with Arithmetic Operation
Single-Cycle Linked-List Update
64-Word, Selective Instruction Cache Provides Three Bus Performance
Single-Cycle Arithmetic Execution
Two 40-Bit Accumulators
Power-Down Mode Featuring Low CMOS Standby Power Dissipation with Fast Recovery from Power-Down Condition
Low Power Dissipation in Idle Mode
Low Three-Cycle Interrupt Latency

Integration
20K Bytes of On-Chip RAM, Configured as:
4K Words of On-Chip Program or Data RAM (24 Bits)
4K Words of On-Chip Data RAM (16 Bits)
Five Channel DMA Controller
Dual Purpose Program Memory for Both Instruction and Data Storage
Independent ALU, Multiplier/Accumulator, & Barrel Shifter Computational Units
Two Independent Data Address Generators Provide:
Pre-Modify and Post-Modify Addressing
Modification with a Constant
Circular/Modulo Addressing
Powerful Program Sequencer Provides:
Zero Overhead Looping
Conditional Instruction Execution
Programmable 16-Bit Interval Timer with Prescaler

System Interface
16-Bit Internal DMA Port for High Speed Access to On-Chip Memory
Four Memory Strobes & Separate I/O Memory Space Permits "Glueless" System Design
Programmable Wait State Generation
Acknowledge Pin Supports Asynchronous Memory Interface
Two Synchronous Serial Ports with Companding Hardware, Four 8-Word FIFOs, Separate Receive and Transmit Clocks, DMA, and TDM Multichannel Support
Automatic Booting of On-Chip Program Memory from Byte-Wide External Memory (e.g., EPROM) or through Internal DMA Port
12 Programmable Flag Pins (6 Input and 6 Output) Provide Flexible System Signaling
Four External Interrupts (Plus 12 Internal and Software Interrupts for a Total of 16)
IEEE JTAG Standard 1149.1 Test Access Port
160-Lead PQFP

GENERAL DESCRIPTION

The ADSP-21csp01 is a single chip DSP optimized for concurrent signal processing (CSP) and other high speed numeric processing applications. The ADSP-21csp01 combines high performance, high bandwidth, 16M address space, DMA ports, and fast task switching support to provide efficient multisignal or multichannel processing. The ADSP-21csp01 processor is based on the architecture used for the ADSP-2100 Family. Although this architecture has been modified to improve the processor's performance and add new features, the ADSP-2100 Family code can be ported easily to the ADSP-21csp01.

The ADSP-21csp01's flexible architecture and comprehensive instruction set supports a high degree of parallelism. In one cycle the ADSP-21csp01 can perform all of the following operations:

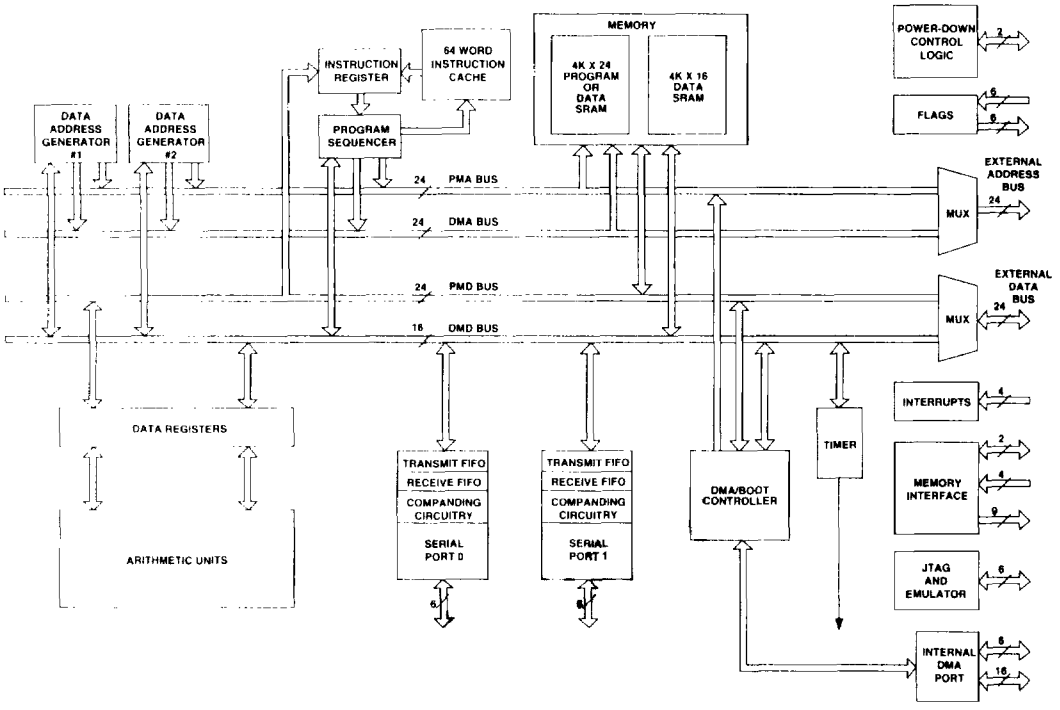
- perform a computation
- perform one or two data moves
- update one or two data address pointers
- generate a program address
- fetch an instruction
- decode an instruction

These operations take place while the processor continues to complete the following tasks:

- receive and transmit data through one or two serial ports
- receive or transmit data through the IDMA port
- decrement the timer

25

FUNCTIONAL BLOCK DIAGRAM



This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.