

**Amplifier, Power, 1.2W  
8.5—10.5 GHz**
**M/A-COM Products  
RoHS Compliant**
**Features**

- ◆ 1.2 Watt Saturated Output Power Level
- ◆ Variable Drain Voltage (6-8V) Operation
- ◆ MSAG™ Process
- ◆ 5x5 mm 20 Lead MLP Package

**Description**

The MAAP-000038-PKG003 is a packaged, 3-stage, 1.2 W power amplifier with on-chip bias networks in a 20 lead MLP package, allowing easy assembly. This product is fully matched to 50 ohms on both the input and output. It can be used as a power amplifier stage or as a driver stage in high power applications.

Each device is 100% RF tested to ensure performance compliance. The part is fabricated using M/A-COM's GaAs Multifunction Self-Aligned Gate (MSAG) Process.

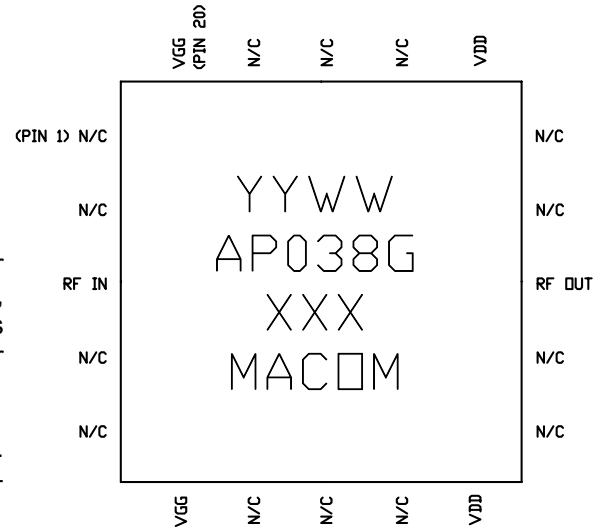
The 5 mm PQFN package has a lead-free lead finish that is RoHS compliant and compatible with a 260°C reflow temperature. The package also features low lead inductance and an excellent thermal path. The MTTF is 1,000,000 hours at 170°C.

**Ordering Information**

Description	Die	Ceramic Pkg	Tape & Reel (500)	Tape & Reel (1000)	Plastic Pkg Sample Brd
Part Number	MAAPGM0038-DIE	MAAPGM0038	MAAP-000038-TR0500	MAAP-000038-TR1000	MAAP-000038-SMB003

**Electrical Characteristics:  $T_C = 40^\circ\text{C}^1$ ,  $Z_0 = 50\ \Omega$ ,  $V_{DD} = 8\text{V}$ ,  $I_{DQ} \approx 710\text{mA}^2$ ,  $P_{in} = 16\text{dBm}$ ,  $R_G \approx 30\ \Omega$** 

Parameter	Symbol	Typical*	Units
Bandwidth	f	8.5-10.5	GHz
Output Power	POUT	31.5	dBm
Power Added Efficiency	PAE	17	%
1-dB Compression Point	P1dB	30	dBm
Small Signal Gain	G	17	dB
Gate Supply Current	$I_{GG}$	<10	mA
Drain Supply Current	$I_{DD}$	0.9	A
Input VSWR	VSWR	2.5:1	—
Output VSWR	VSWR	2:1	—
Output Third Order Intercept	OTOI	41	dBm
3 <sup>rd</sup> Order Intermodulation Distortion, Single Carrier Level = 21 dBm	IM3	42	dBc

**1.  $T_C$  = Case Temperature**
**2. Adjust  $V_{GG}$  between -2.5 to -1.2V to achieve indicated  $I_{DQ}$ .**

**Primary Applications**

- ◆ Weather Radar
- ◆ Airborne Radar

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### Maximum Ratings<sup>3</sup>

Parameter	Symbol	Absolute Maximum	Units
Input Power	$P_{IN}$	21.0	dBm
Drain Supply Voltage	$V_{DD}$	+12.0	V
Gate Supply Voltage	$V_{GG}$	-3.0	V
Quiescent Drain Current (No RF)	$I_{DQ}$	1.15	A
Quiescent DC Power Dissipated (No RF)	$P_{DISS}$	11.5	W
Junction Temperature	$T_J$	170	°C
Storage Temperature	$T_{STG}$	-55 to +150	°C

3. Operation beyond these limits may result in permanent damage to the part.

### Recommended Operating Conditions<sup>4</sup>

Characteristic	Symbol	Min	Typ	Max	Unit
Drain Supply Voltage	$V_{DD}$	6.0	8.0	8.0	V
Gate Supply Voltage	$V_{GG}$	-2.5	-2.0	-1.2	V
Input Power	$P_{IN}$		16.0	19.0	dBm
Thermal Resistance	$\Theta_{JC}$		16.9		°C/W
Case Temperature	$T_C$			Note 5	°C

4. Operation outside of these ranges may reduce product reliability.

5. Maximum Case Temperature =  $170^{\circ}\text{C} - \Theta_{JC} * V_{DD} * I_{DQ}$

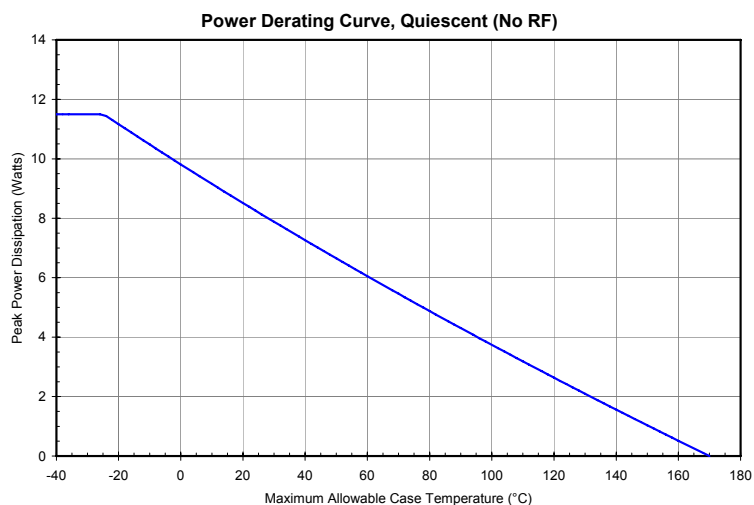


### Operating Instructions

This device is static sensitive. Please handle with care.

To operate the device, follow these steps.

1. Apply  $V_{GG} = -2.7\text{ V}$ ,  $V_{DD} = 0\text{ V}$ .
2. Ramp  $V_{DD}$  to desired voltage, typically 8.0 V.
3. Adjust  $V_{GG}$  to set  $I_{DQ}$ , (approximately @ -2 V).
4. Set RF input.
5. Power down sequence in reverse. Turn  $V_{GG}$  off last.



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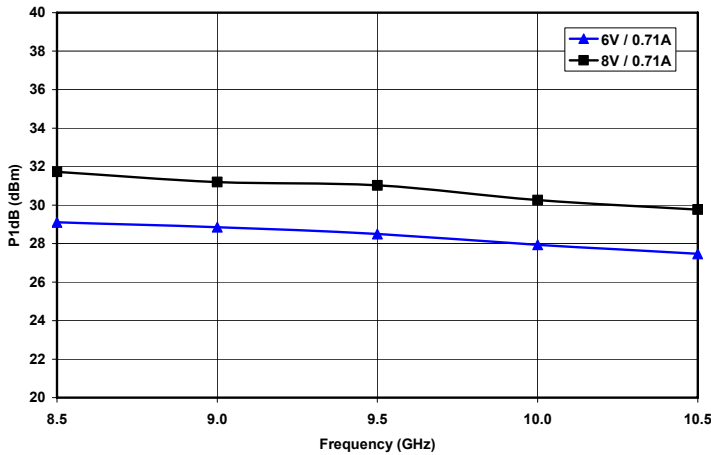


Figure 1. P1dB vs. Frequency and Quiescent Bias Condition (VDD / IDQ)

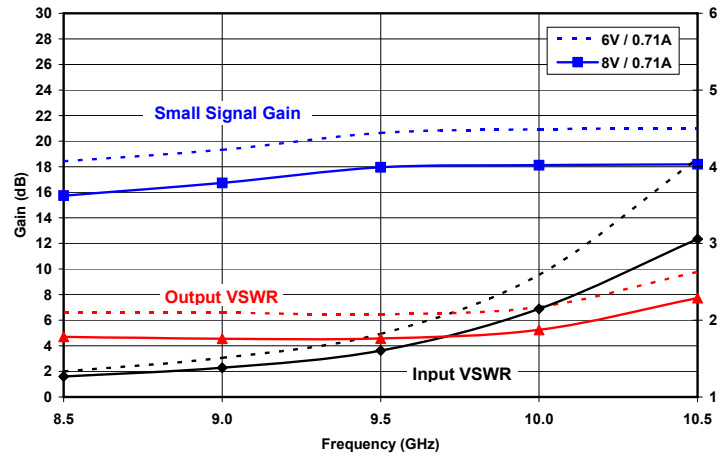


Figure 2. Small Signal Gain and Input & Output VSWR vs. Frequency and Quiescent Bias Condition (VDD / IDQ)

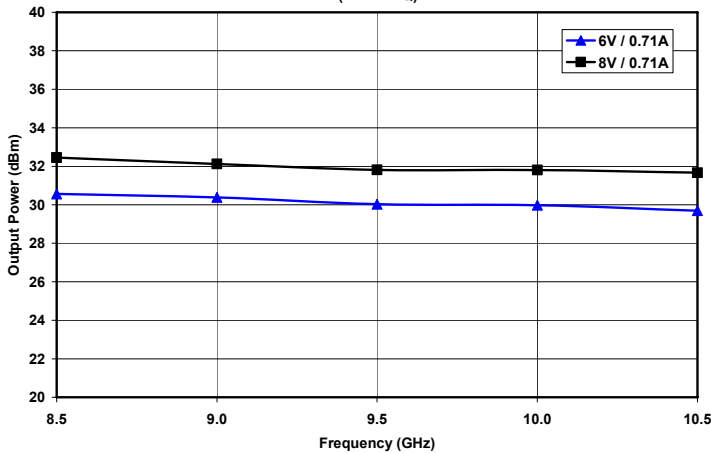


Figure 3. Saturated Output Power vs. Frequency and Quiescent Bias Condition (VDD / IDQ)

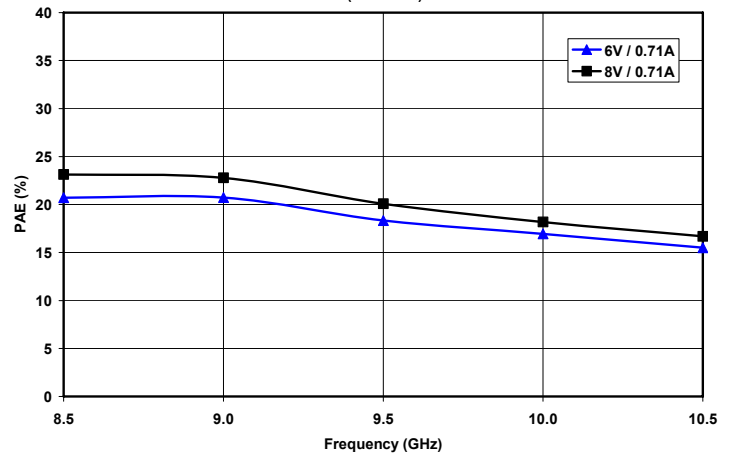


Figure 4. Saturated Power Added Efficiency vs. Frequency and Quiescent Bias Condition (VDD / IDQ)

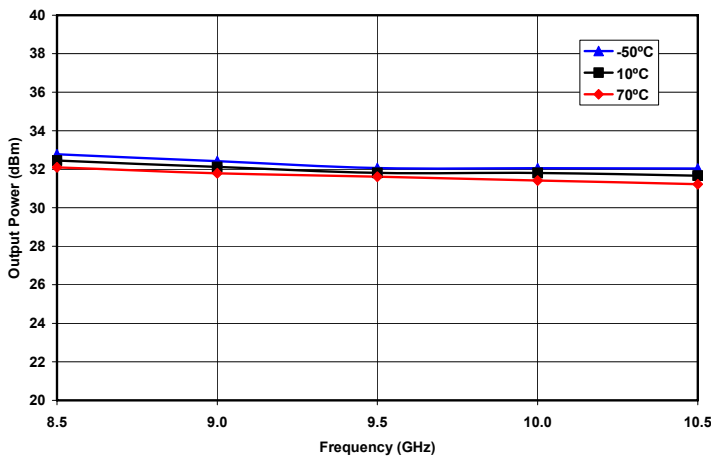


Figure 5. Saturated Output Power vs. Frequency and Case Temperature at VD = 8V and IDQ = 0.71A

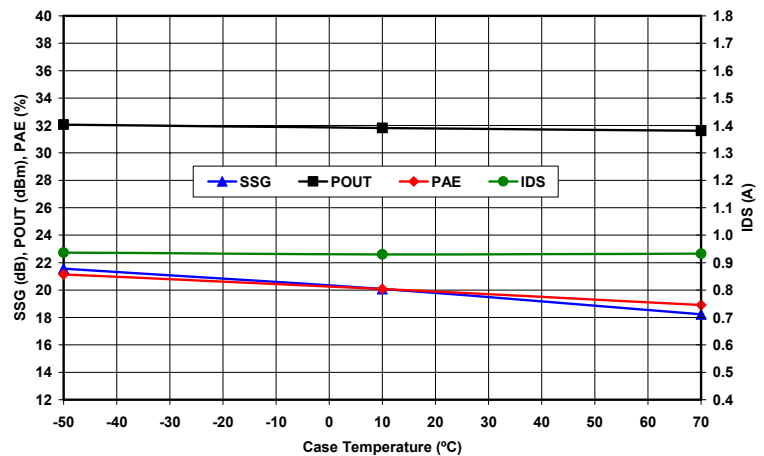


Figure 6. Small Signal Gain & Saturated Output Power, Power Added Efficiency and Drain Current vs. Case Temperature at 9.5GHz, VD = 8V, and IDQ = 0.71A

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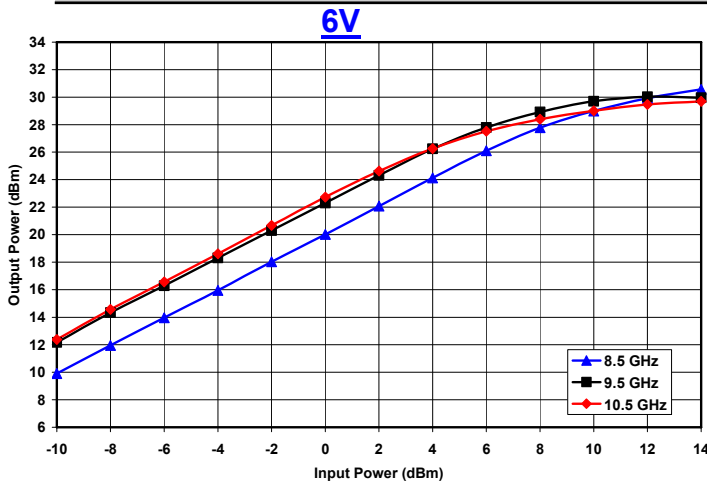


Figure 7. Output Power vs. Input Power and Frequency  
at  $V_D = 6V$  and  $ID_Q = 0.71A$

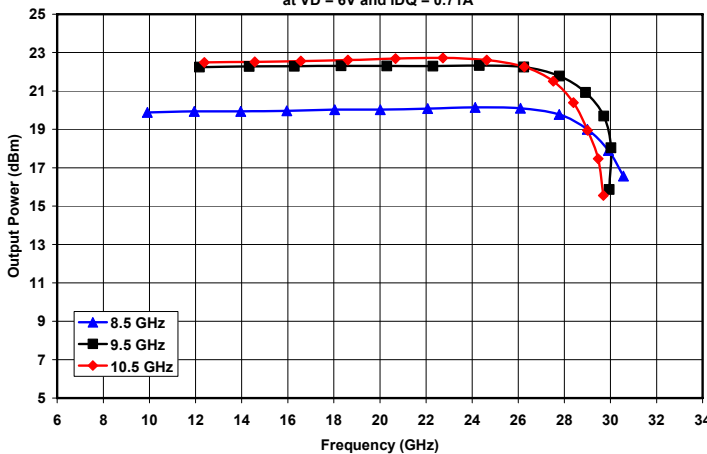


Figure 9. Gain vs. Output Power and Frequency  
at  $V_D = 6V$  and  $ID_Q = 0.71A$

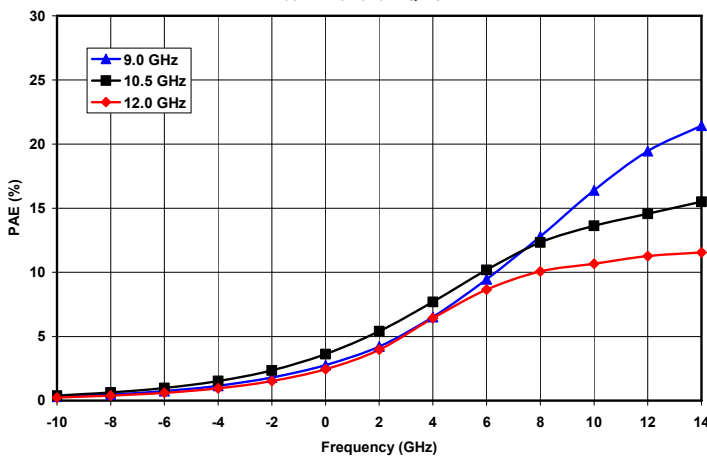


Figure 11. Power Added Efficiency vs. Input Power and Frequency  
at  $V_D = 6V$  and  $ID_Q = 0.71A$

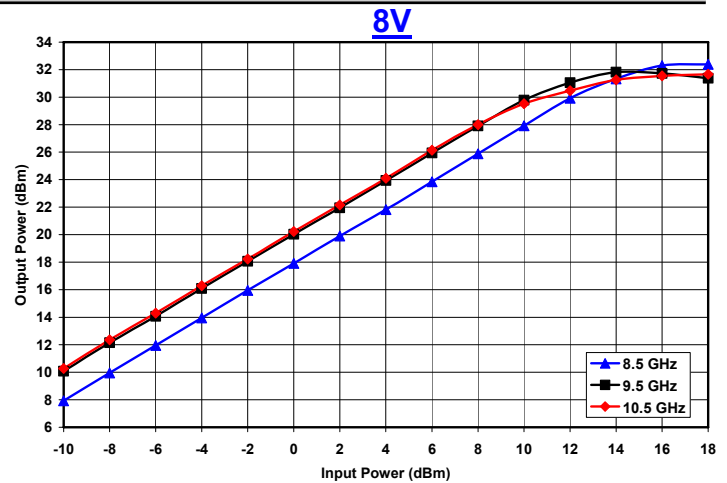


Figure 8. Output Power vs. Input Power and Frequency  
at  $V_D = 8V$  and  $ID_Q = 0.71A$

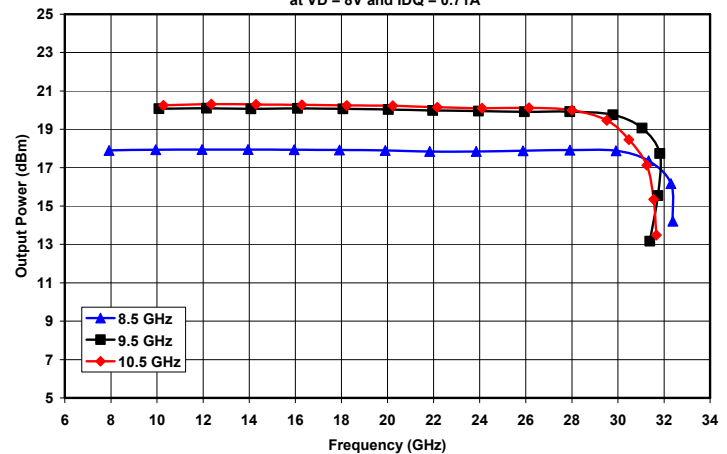


Figure 10. Gain vs. Output Power and Frequency  
at  $V_D = 8V$  and  $ID_Q = 0.71A$

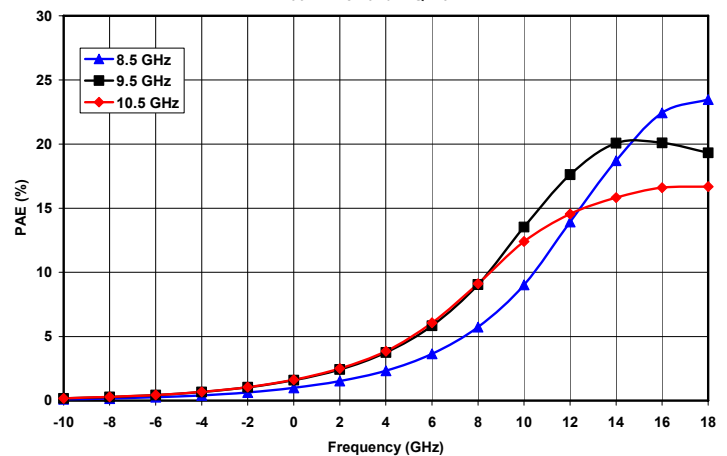


Figure 12. Power Added Efficiency vs. Input Power and Frequency  
at  $V_D = 8V$  and  $ID_Q = 0.71A$

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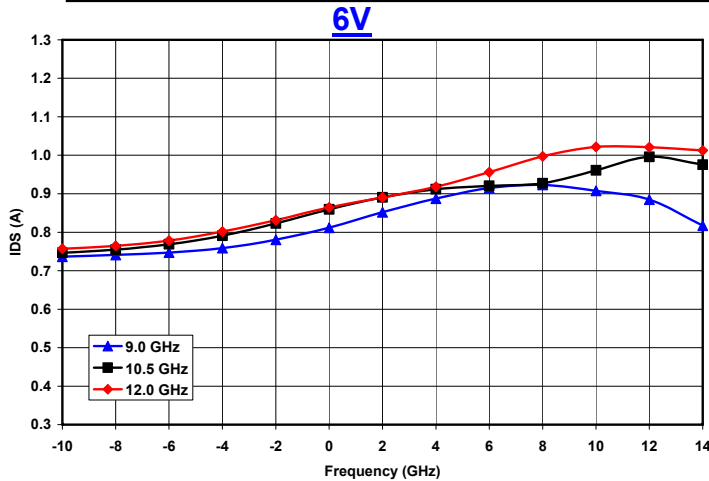


Figure 13. Drain Current vs. Input Power and Frequency  
at  $V_D = 6V$  and  $I_{DQ} = 0.71A$

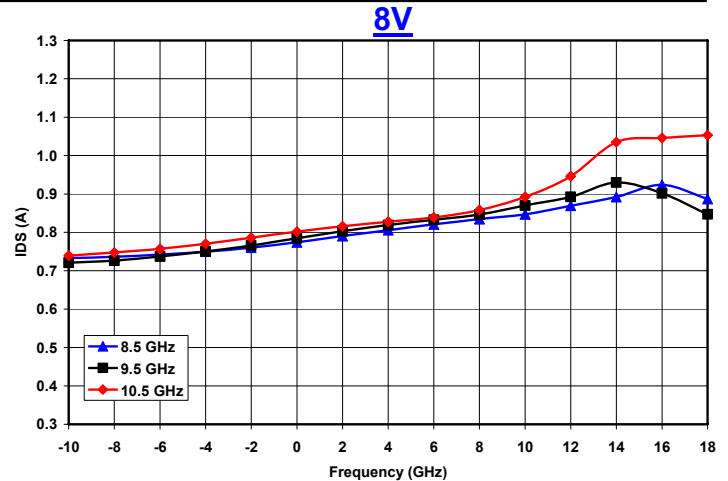


Figure 14. Drain Current vs. Input Power and Frequency  
at  $V_D = 8V$  and  $I_{DQ} = 0.71A$

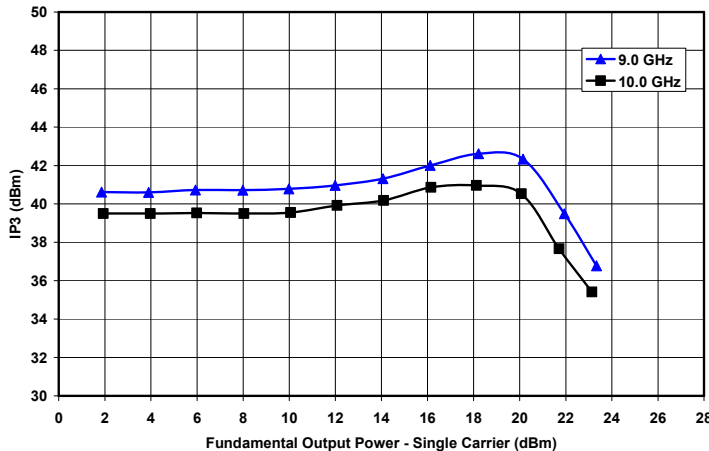


Figure 15. Third Order Intercept vs. Output Power and Frequency  
at  $V_D = 6V$  and  $I_{DQ} = 0.71A$

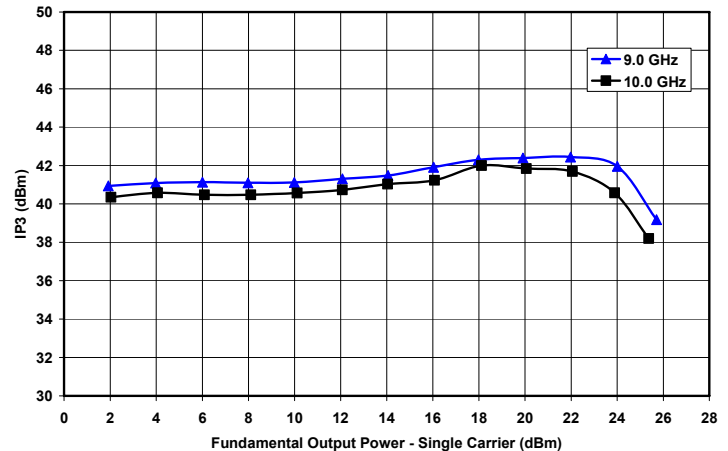


Figure 16. Third Order Intercept vs. Output Power and Frequency  
at  $V_D = 8V$  and  $I_{DQ} = 0.71A$

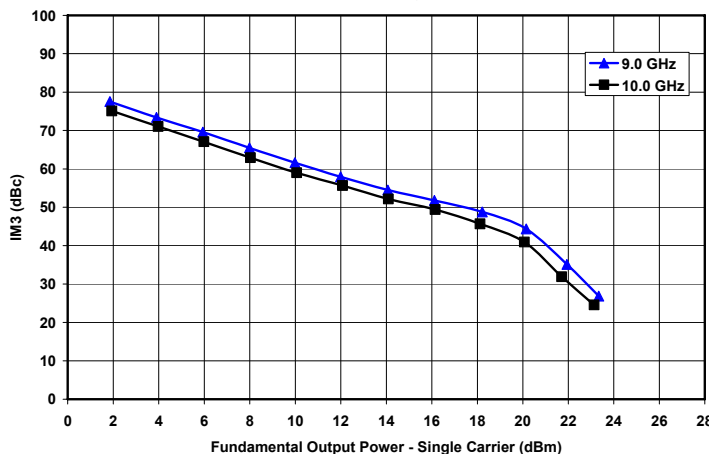


Figure 17. Third Order Intermod vs. Output Power and Frequency  
at  $V_D = 6V$  and  $I_{DQ} = 0.71A$

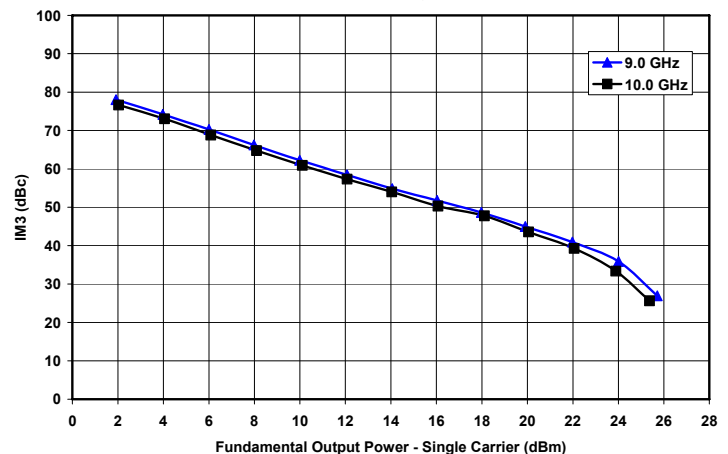


Figure 18. Third Order Intermod vs. Output Power and Frequency  
at  $V_D = 8V$  and  $I_{DQ} = 0.71A$

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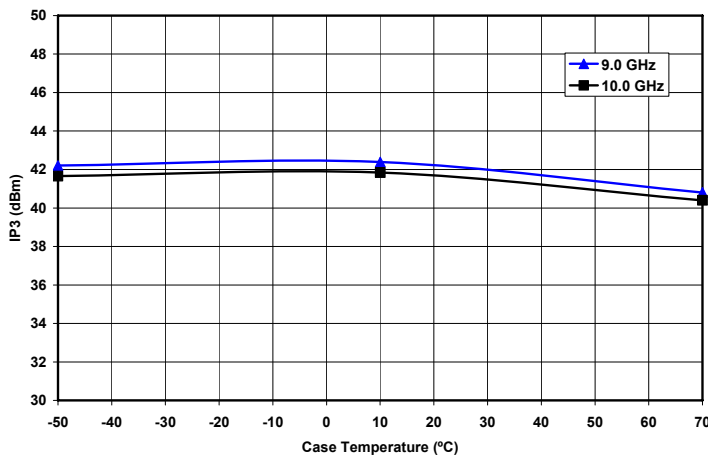


Figure 19. Third Order Intercept vs. Case Temperature and Frequency at Single Carrier Output Power Level = 20dBm, VD = 8V and IDQ = 0.71A

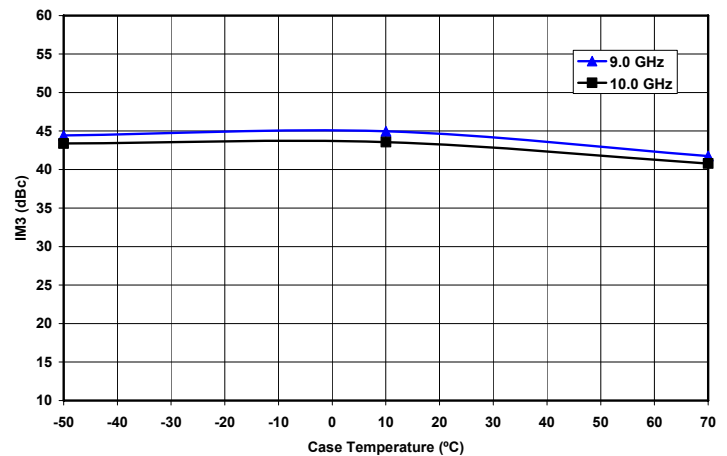
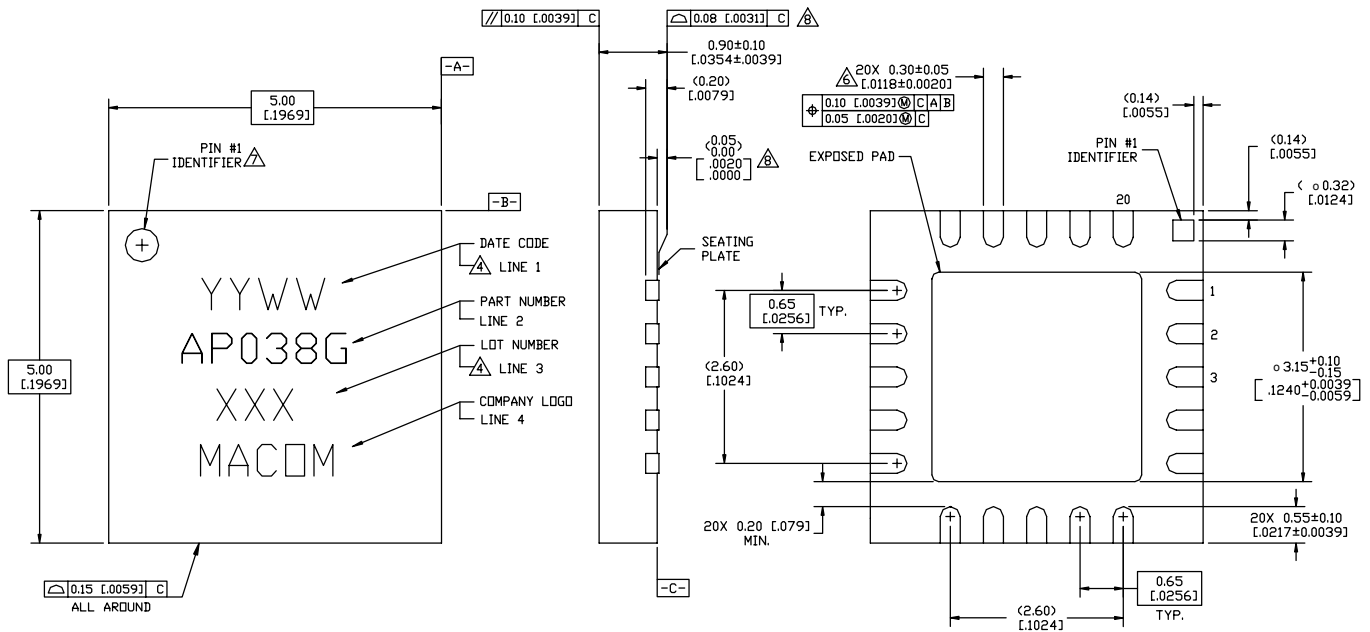


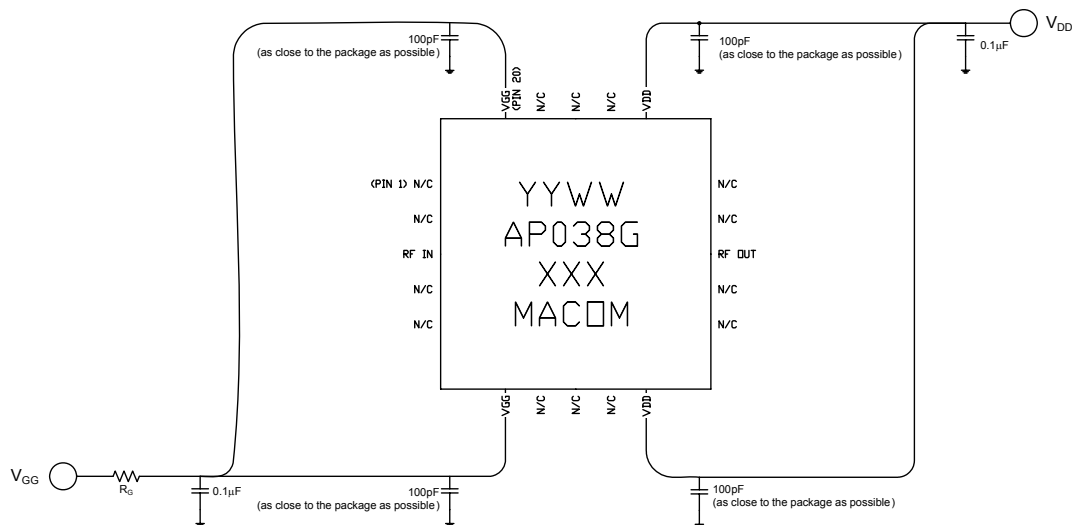
Figure 20. Third Order Intermod vs. Case Temperature and Frequency at Single Carrier Output Power Level = 20 dBm, VD = 8V and IDQ = 0.71A

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**Figure 21. 5x5 mm 20-Lead MLP.**



**Figure 22. Recommended Bias Configuration.**

Note: The exposed pad centered on the package bottom must be connected to RF and dc ground for proper electrical and thermal operation.

Refer to M/A-COM Application Note **Surface Mounting Instructions for PQFN Packages #S2083\*** for assembly guidelines.

**Additional Precaution: All parts must receive a bake-out of 125°C for 24 hours prior to any solder reflow operation.**

\*Application Notes can be found by going to the Site Search Page of M/A-COM's web page (<http://www.macom.com/search/search.jsp>) and searching for the required Application Note.

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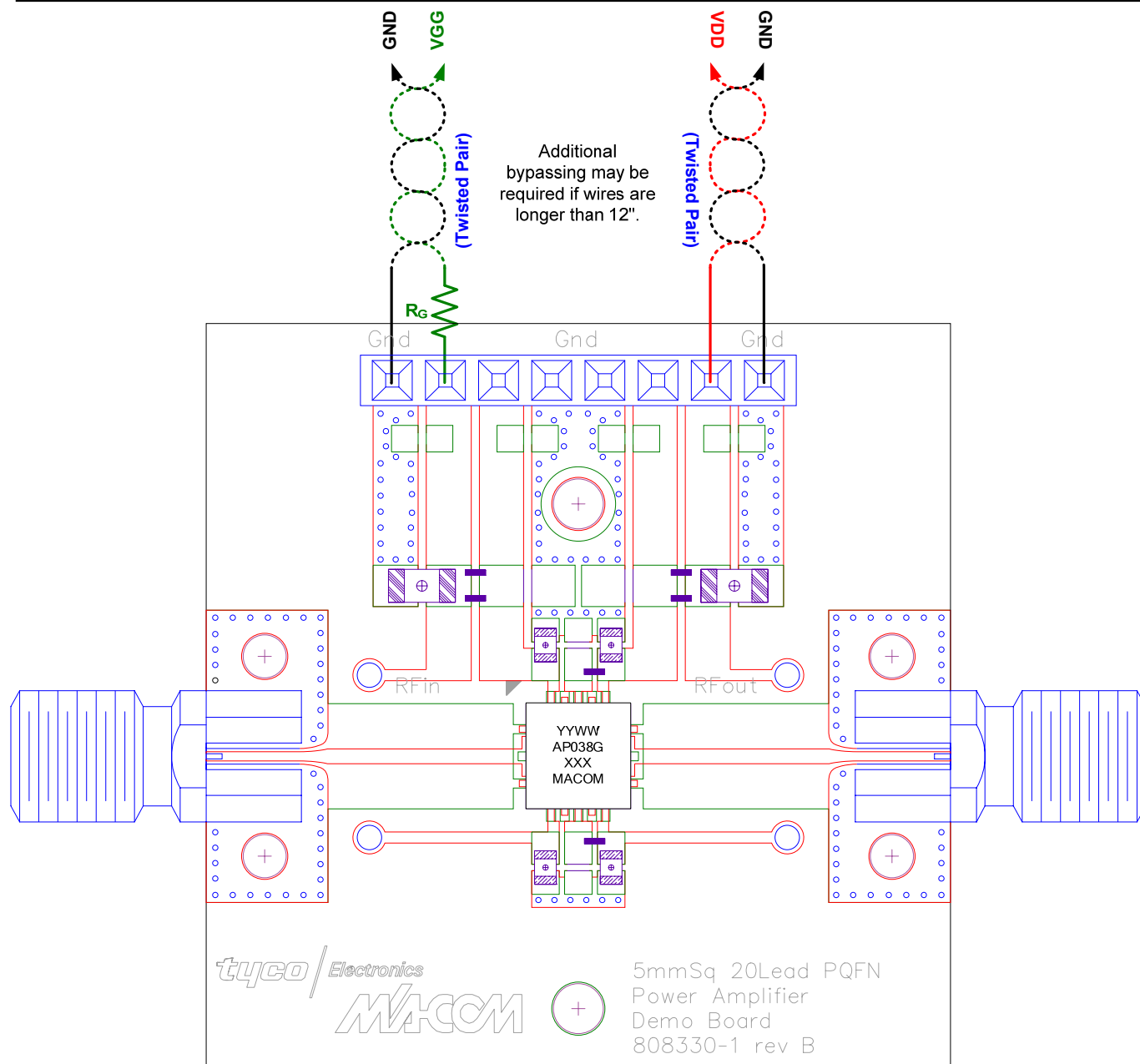


Figure 23. Demonstration Board PN MAAP-000038-PKG-SMB (available upon request).