FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-21336-2E

ASSP

Single Serial Input PLL Frequency Synthesizer

On-Chip 2.5 GHz Prescaler

MB15E06

■ DESCRIPTION

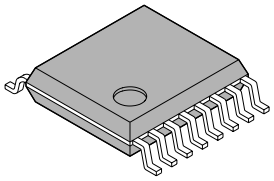
The Fujitsu MB15E06 is serial input Phase Locked Loop (PLL) frequency synthesizers with a 2.5 GHz prescaler. A 64/65 or a 128/129 can be selected for the prescaler that enables pulse swallow operation.
The latest BiCMOS process technology is used, resultantly a supply current is limited as low as 8 mA typ. This operates with a supply voltage of 3.0 V (typ.) .
Furthermore, a super charger circuit is included to get a fast tuning as well as low noise performance. As a result of this, MB15E06 is ideally suitable for digital mobile communications, such as GPS (Global Positioning System) , Wireless LAN, CATV (CAble TeleVision) etc.

■ FEATURES

- High frequency operation : 2.5 GHz max
- Low power supply voltage : V_{CC} = 2.7 to 3.6 V
- Very Low power supply current : I_{CC} = 8.0 mA typ. (V_{CC} = 3 V)
- Power saving function : I_{PS} = 10 µA max.
- Pulse swallow function : 64/65 or 128/129
- Serial input 14-bit programmable reference divider : R = 5 to 16, 383
- Serial input 18-bit programmable divider consisting of:
  - Binary 7-bit swallow counter : 0 to 127
  - Binary 11-bit programmable counter : 5 to 2, 047
- Wide operating temperature : Ta = –40 to 85 °C
- Plastic 16-pin SSOP package (FPT-16P-M05)

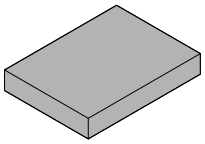
■ PACKAGE

16-pin plastic SSOP



(FPT-16P-M05)

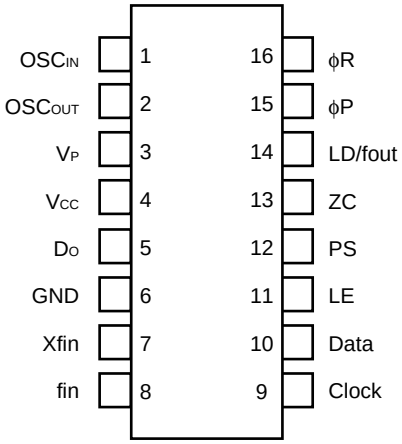
16-pad plastic BCC



(LCC-16P-M06)

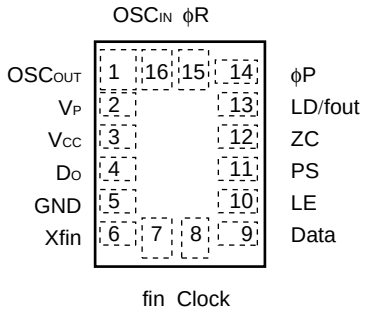
■ PIN ASSIGNMENT

(TOP VIEW)



(FPT-16P-M05)

(TOP VIEW)



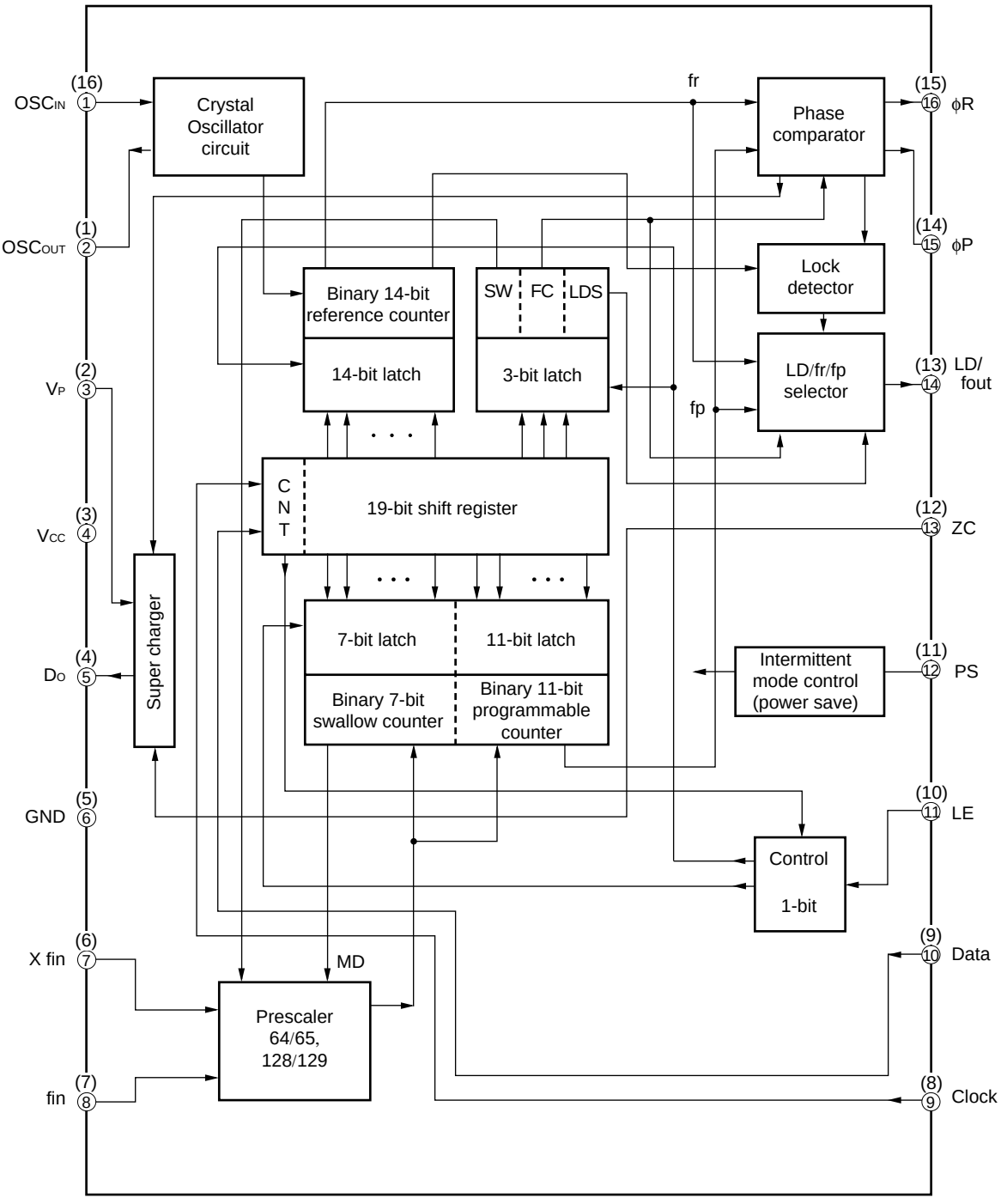
(LCC-16P-M06)

■ PIN DESCRIPTIONS

Pin No.	Pin Name	I/O	Descriptions
1 (16)	OSC_{IN}	I	Programmable reference divider input. Oscillator input connection to a TCXO.
2 (1)	OSC_{OUT}	O	Oscillator output.
3 (2)	V_P	—	Power supply voltage input for the charge pump.
4 (3)	V_{CC}	—	Power supply voltage input.
5 (4)	D_O	O	Charge pump output. Phase of the charge pump can be reversed by FC input.
6 (5)	GND	—	Ground.
7 (6)	Xfin	I	Prescaler complementary input, and should be grounded via a capacitor.
8 (7)	fin	I	Prescaler input. Connection with an external VCO should be done with AC coupling.
9 (8)	Clock	I	Clock input for the 19-bit shift register. Data is shifted into the shift register on the rising edge of the clock. *(Open is prohibited.)*
10 (9)	Data	I	Serial data input using binary code. The last bit of the data is a control bit. *(Open is prohibited.)* Control bit = “H” ; Data is transmitted to the programmable reference counter. Control bit = “L” ; Data is transmitted to the programmable counter.
11 (10)	LE	I	Load enable signal input *(Open is prohibited.)* When LE is high, the data in the shift register is transferred to a latch, according to the control bit in the serial data.
12 (11)	PS	I	Power saving mode control. This pin must be set at “L” at Power-ON. *(Open is prohibited.)* PS = “H” ; Normal mode PS = “L” ; Power saving mode
13 (12)	ZC	I	Forced high-impedance control for the charge pump (with internal pull up resistor.) ZC = “H” ; Normal Do output. ZC = “L” ; Do becomes high impedance.
14 (13)	LD/fout	O	Lock detect signal output (LD) /phase comparator monitoring output (fout) . The output signal is selected by LDS bit in the serial data. LDS = “H” ; outputs fout (fr/fp monitoring output) LDS = “L” ; outputs LD (“H” at locking, “L” at unlocking.)
15 (14)	ϕP	O	Phase comparator output for an external charge pump.
16 (15)	ϕR	O	Phase comparator output for an external charge pump.

( ) : for Bcc Package.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RAGINGS

Parameter	Symbol	Rating		Unit	Remark
		Min.	Max.		
Power supply voltage	V_{CC}	–0.5	+4.0	V	
	V_P	V_{CC}	+6.0	V	
Output voltage	V_O	–0.5	V_{CC} +0.5	V	
Input voltage	V_I	–0.5	V_{CC} +0.5	V	
Output current	I_O	–10	+10	mA	
Open drain withstand voltage	V_{OOP}	–0.5	+7.0	V	
Storage temperature	T_{stg}	–55	+125	°C	

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Remark
		Min.	Typ.	Max.		
Power supply voltage	V_{CC}	2.7	3.0	3.6	V	
	V_P	V_{CC}	—	6.0	V	
Input voltage	V_I	GND	—	V_{CC}	V	
Operating temperature	Ta	–40	—	+85	°C	

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

Parameter		Symbol	Condition	Value			Unit
				Min.	Typ.	Max.	
Power supply current*1		I_{CC}	fin_{IF} = 2500 MHz, fosc = 12 MHz	—	8.0	—	mA
Power saving current*2		Ips	Vcc current at PS = "L" and ZC = "H"	—	—	10	µA
Operating frequency		fin	—	100	—	2500	MHz
Crystal oscillator operating frequency		f_{OSC}	min. 500 mVp–p	3	—	40	MHz
Input sensitivity	fin	$Vfin_{IF}$	50 Ω termination (Refer to the test circuit.)	–10	—	+2	dBm
	OSCin	V_{OSC}	—	500	—	V_{CC}	mVp–p
Input voltage	Data, Clock, LE, PS, ZC	V_{IH}	—	$V_{CC} \times 0.7$	—	—	V
		V_{IL}	—	—	—	$V_{CC} \times 0.3$	
Input current	Data, Clock, LE, PS	I_{IH}	—	–1.0	—	+1.0	µA
		I_{IL}	—	–1.0	—	+1.0	
	ZC	I_{IH}	—	–1.0	—	+1.0	µA
		I_{IL}	Pull up input	–100	—	0	
	OSCin	I_{IH}	—	0	—	+100	µA
		I_{IL}	—	–100	—	0	
Output voltage	ϕP	V_{OL}	Open drain output	—	—	0.4	V
	ϕR, LD/fout	V_{OH}	—	V_{CC} – 0.4	—	–	V
		V_{OL}	—	—	—	0.4	
	Do	V_{DOH}	—	V_P – 0.4	—	–	V
		V_{DOL}	—	—	—	0.4	
High impedance cutoff current	Do	I_{OFF}	—	—	—	1.1	µA
Output current	ϕP	I_{OL}	Open drain output	1.0	—	—	mA
	ϕR, LD/fou	I_{OH}	—	—	—	–1.0	mA
		I_{OL}	—	1.0	—	—	
	Do	I_{DOH}	V_{CC} = 3.0 V, Vp = 5 V, V_{DOH} = 4.0 V	—	–10.0*2	—	mA
		I_{DOL}	V_{CC} = 3.0 V, Vp = 5 V, V_{DOL} = 1.0 V	—	10.0*2	—	

*1 : Conditions ; V_{CC} = 3.0 V, Ta = 25 °C, in locking state.

*2 : Conditions ; Ta = 25 °C

■ FUNCTION DESCRIPTIONS

Pulse Swallow Function

The divide ratio can be calculated using the following equation :

$f_{VCO} = [(M \times N) + A] \times f_{OSC} \div R \quad (A < N)$

- f_{VCO} : Output frequency of external voltage controlled oscillator (VCO)
- N : Preset divide ratio of binary 11-bit programmable counter (5 to 2,047)
- A : Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$)
- f_{OSC} : Output frequency of the reference frequency oscillator
- R : Preset divide ratio of binary 14-bit programmable reference counter (5 to 16,383)
- M : Preset divide ratio of modules prescaler (64 or 128)

Serial Data Input

Serial data is processed using the Data, Clock, and LE pins. Serial data controls the programmable reference divider and the programmable divider separately.
Binary serial data is entered through the Data pin.
One bit of data is shifted into the shift register on the rising edge of the clock. When the load enable pin is high, stored data is latched according to the control bit data as follows:

Table.1 Control Bit

Control bit (CNT)	Destination of serial data
H	17 bit latch (for the programmable reference divider)
L	18 bit latch (for the programmable divider)

Shift Register Configuration

Programmable Reference Counter

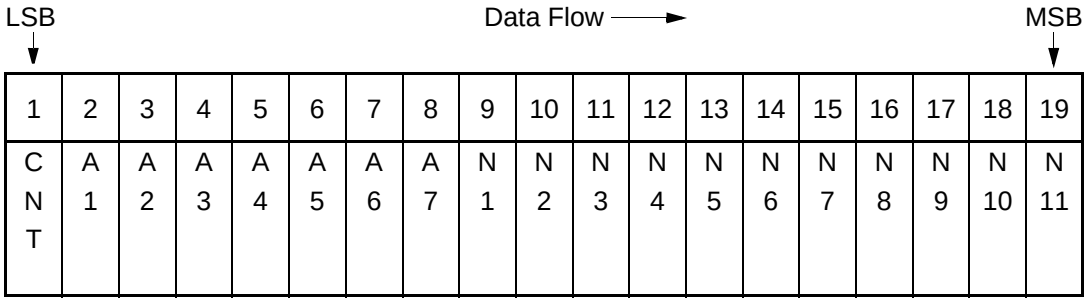
LSB ← Data Flow → MSB

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
CNT	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	SW	FC	LDS

CNT : Control bit [Table. 1]
R1 to R14 : Divide ratio setting bit for the programmable reference counter (5 to 16,383) [Table. 2]
SW : Divide ratio setting bit for the prescaler (64/65 or 128/129) [Table. 5]
FC : Phase control bit for the phase comparator [Table. 7]
LDS : LD/fout signal select bit [Table. 6]

Note : Start data input with MSB first

Programmable Reference Counter



1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
CNT	A1	A2	A3	A4	A5	A6	A7	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11

CNT : Control bit [Table. 1]
N1 to N11 : Divide ratio setting bits for the programmable counter (5 to 2,047) [Table. 3]
A1 to A7 : Divide ratio setting bits for the swallow counter (0 to 127) [Table. 4]

Note : Start data input with MSB first

Table2. Binary 14-bit Programmable Reference Counter Data Setting

Divide ratio (R)	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1
5	0	0	0	0	0	0	0	0	0	0	0	1	0	1
6	0	0	0	0	0	0	0	0	0	0	0	1	1	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note : • Divide ratio less than 5 is prohibited.

Table.3 Binary 11-bit Programmable Counter Data Setting

Divide ratio (N)	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1
5	0	0	0	0	0	0	0	0	1	0	1
6	0	0	0	0	0	0	0	0	1	1	0
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

Note : • Divide ratio less than 5 is prohibited.
• Divide ratio (N) range = 5 to 2,047

Table.4 Binary 7-bit Swallow Counter Data Setting

Divide ratio (A)	A 7	A 6	A 5	A 4	A 3	A 2	A 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

Note : • Divide ratio (A) range = 0 to 127

Table. 5 Prescaler Data Setting

SW	Prescaler Divide ratio
H	64/65
L	128/129

Table. 6 LD/fout Output Select Data Setting

LDS	LD/fout output signal
H	fout signal
L	LD signal

Relation between the FC input and phase characteristics

The FC bit changes the phase characteristics of the phase comparator. Both the internal charge pump output level (D_O) and the phase comparator output (ϕR, ϕP) are reversed according to the FC bit. Also, the monitor pin (f_{OUT}) output is controlled by the FC bit. The relationship between the FC bit and each of D_O, ϕR, and ϕP is shown below.

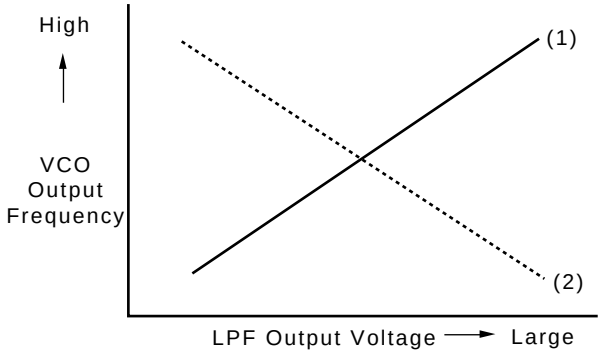
Table. 7 FC Bit Data Setting (LDS = "H")

	FC = High				FC = Low			
	Do	ϕR	ϕP	LD/fout	Do	ϕR	ϕP	LD/fout
$f_r > f_p$	H	L	L	(fr)	L	H	Z*	(fp)
$f_r < f_p$	L	H	Z*	(fr)	H	L	L	(fp)
$f_r = f_p$	Z*	L	Z*	(fr)	Z*	L	Z*	(fp)

* : High impedance

When designing a synthesizer, the FC pin setting depends on the VCO and LPF characteristics.

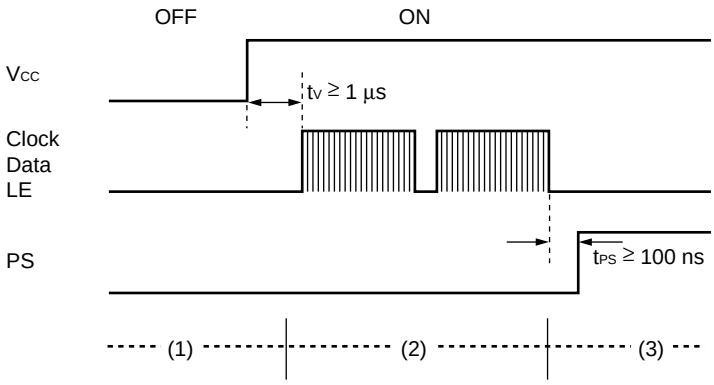
* : When the LPF and VCO characteristics are similar to (1) , set FC bit high.
* : When the VCO characteristics are similar to (2) , set FC bit low.



3. Power Saving Mode (Intermittent Mode Control Circuit)

Setting a PS pin to Low, the IC enters into power saving mode resultaly current sonsumption can be limited to 10 µA (max.) . Setting PS pin to High, power saving mode is released so that the IC works normally.
In addition, the intermittent operation control circuit is included which helps smooth start up from the power saving mode. In general, the power consumption can be saved by the intermittent operation that powering down or waking up the synthesizer. Such case, if the PLL is powered up uncontrolled, the resulting phase comparator output signal is unpredictable due to an undefined phase relation between reference frequency (f_r) and comparison frequency (f_p) and may in the worst case take longer time for lock up of the loop.
To prevent this, the intermittent operation control circuit enforces a limited error signal output of the phase detector during power up, thus keeping the loop locked.
During the power saving mode, the corresponding section except for indispensable circuit for the power saving function stops working, then current consumption is reduced to 10 µA (max.) .

Note : • While the power saving mode is executed, ZC pin should be set at “H” or open. If ZC is set at “L” during power saving mode, approximately 10 µA current flows.
• PS pin must be set “L” at Power-ON.
• The power saving mode can be released (PS : L → H) 1 µs later after power supply remains stable.
• During the power saving mode, it is possible to input the serial data.



(1) PS = L (power saving mode) at Power ON
(2) Set serial data 1 µs later after power supply remains stable ($V_{CC} \geq 2.2$ V) .
(3) Release power saving mode (PS : L → H) 100 ns later after setting serial data.

Table.8 PS Pin Setting

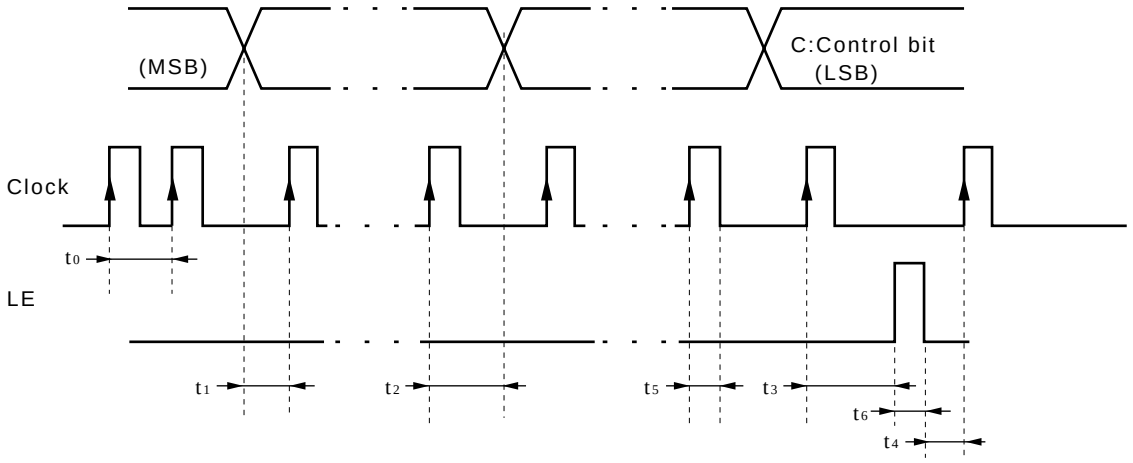
PS pin	Status
H	Normal mode
L	Power saving mode

Table.9 ZC Pin Setting

ZC pin	Do output
H	Normal output
L	High impedance

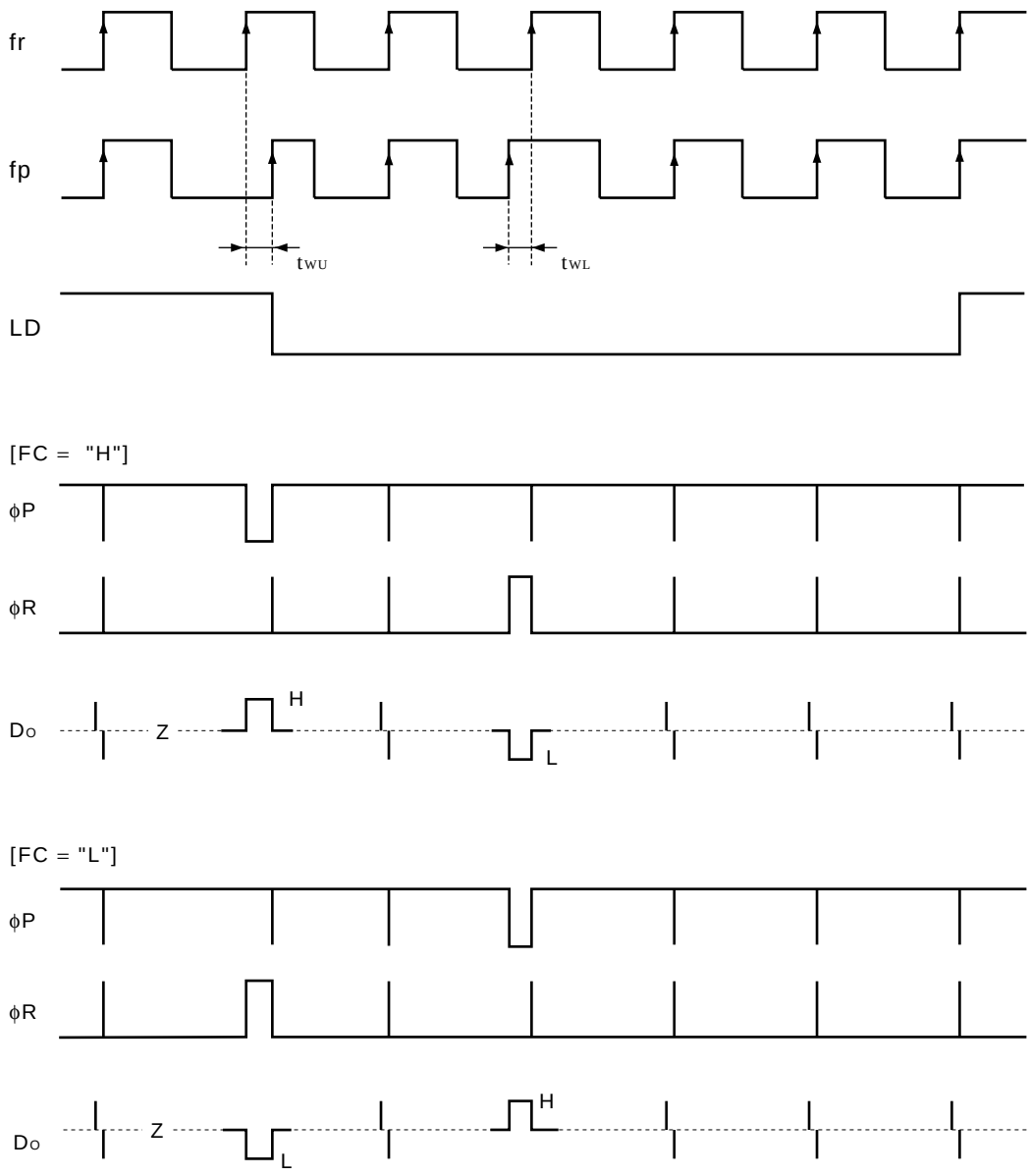
■ SERIAL DATA INPUT TIMING

$t_0 \geq 100$ ns, t_1, t_2, $t_4 \geq 20$ ns, t_3, $t_5 \geq 30$ ns, $t_6 \geq 100$ ns



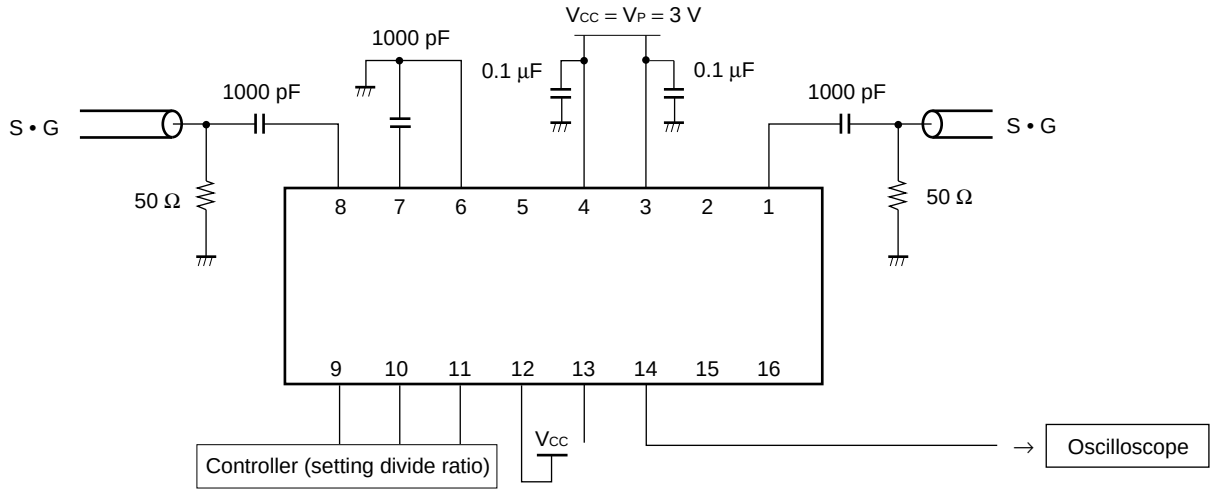
On rising edge of the clock, one bit of the data is transferred into the shift register.

■ PHASE COMPARATOR OUTPUT WAVEFORM



Note : 1. Phase error detection range : -2π to $+2\pi$
2. Pulses on Do output signal during locked state are output to prevent dead zone.
3. LD output becomes low when phase is t_{WU} or more. LD output becomes high when phase error is t_{WL} or less and continues to be so for three cysles or more.
4. t_{WU} and t_{WL} depend on OSCin input frequency.
   $t_{WU} \geq 8/fosc$ (e. g. $t_{WU} \geq 625ns$, foscin = 12.8 MHz)
   $t_{WL} \leq 16/fosc$ (e. g. $t_{WL} \leq 1250ns$, foscin = 12.8 MHz)
5. LD becomes high during the power saving mode (PS = “L”.)

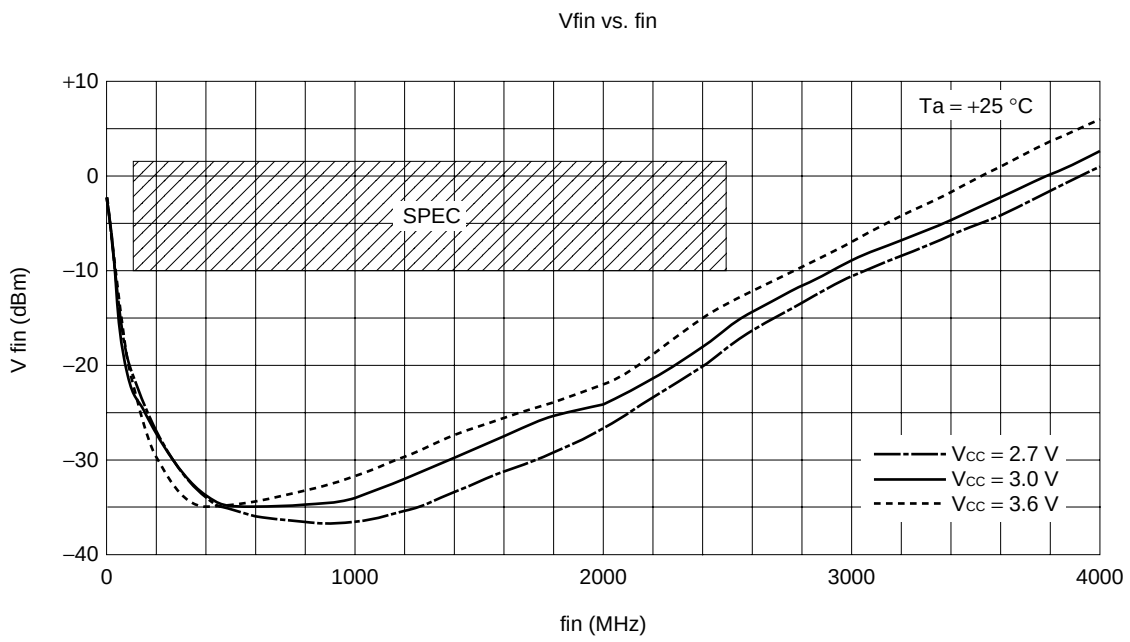
■ TEST CIRCUIT (for Measuring Input Sensitivity fin/OSCin)



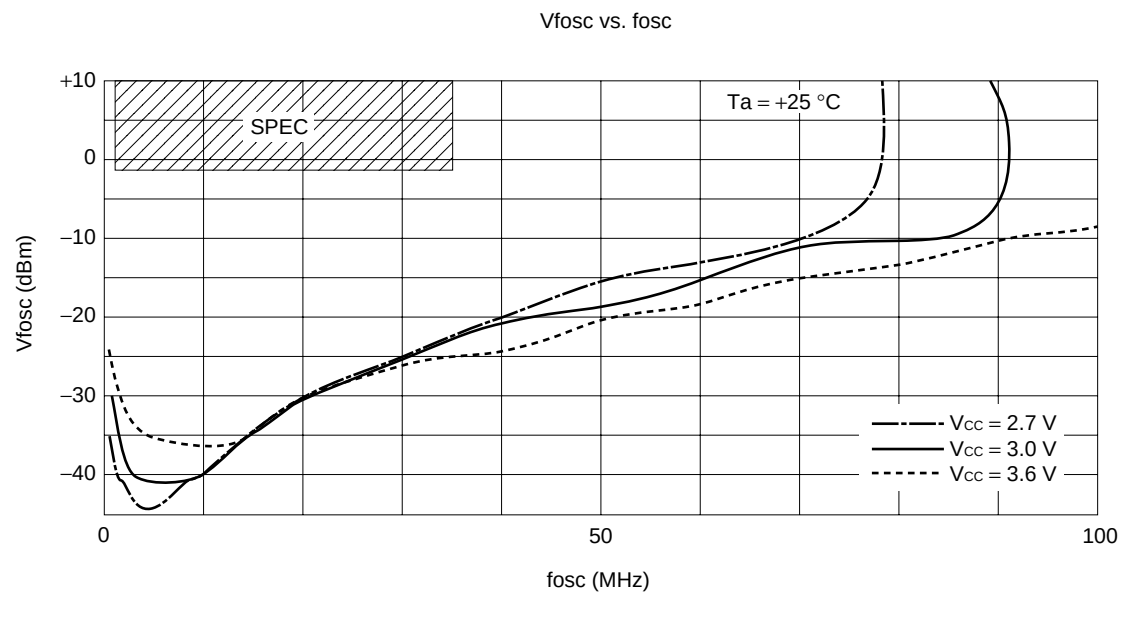
Note : SSOP

■ TYPICAL CHARACTERISTICS

1. fin Input Sensitivity

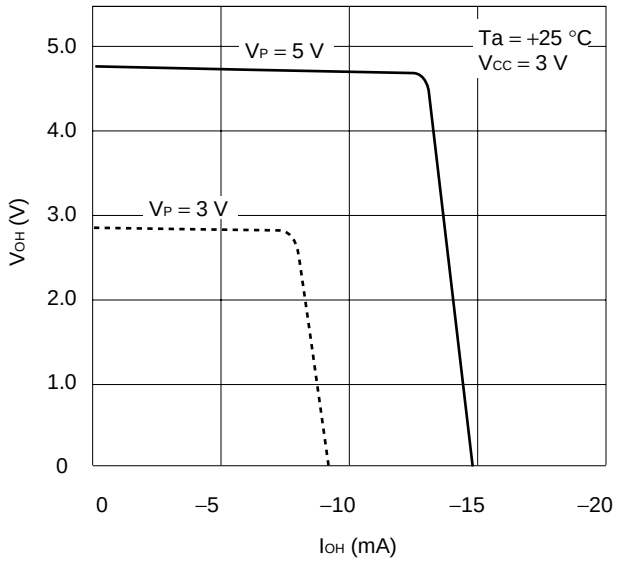


2. OSCin Input Sensitivity

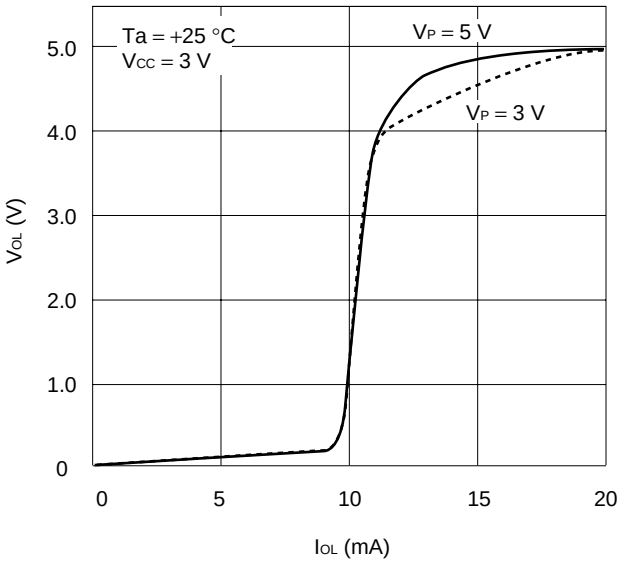


3. Do Output Current

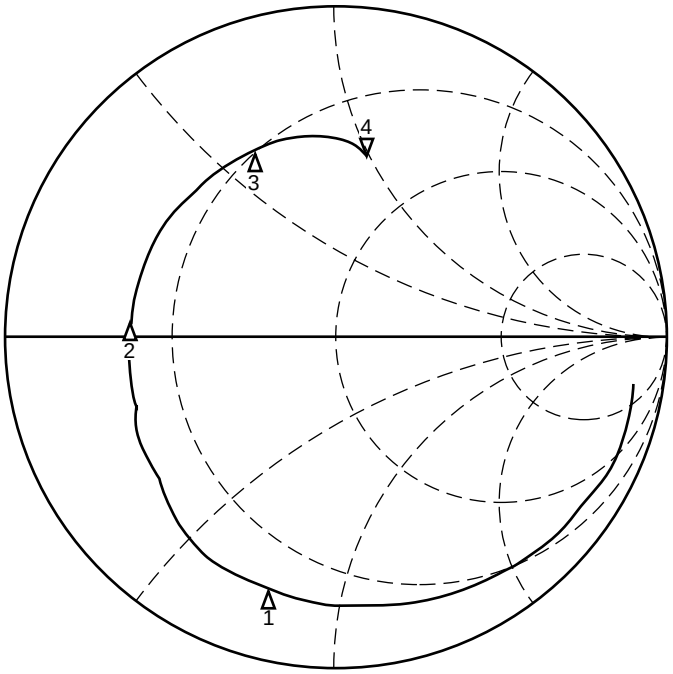
V_{OH} vs. I_{OH}



V_{OL} vs. I_{OL}



4. fin Input Impedance



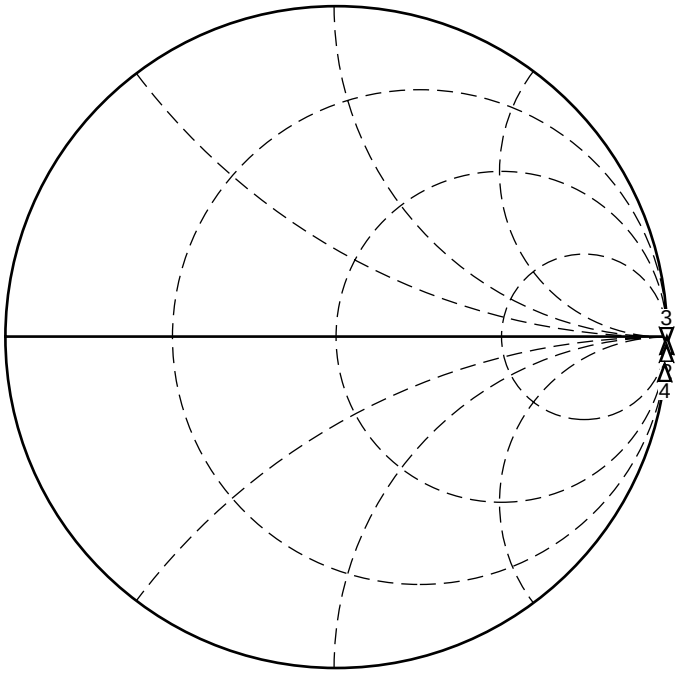
1; 10.188 Ω
–36.666 Ω
1 GHz

2; 10.731 Ω
1.4438 Ω
1.5 GHz

3; 16.474 Ω
31.454 Ω
2 GHz

4; 29.314 Ω
50.516 Ω
2.5 GHz

5. OSCin Input Impedance



1; 3.516 kΩ
–43.99 kΩ
1 MHz

2; 150.5 Ω
–4.8388 kΩ
10 MHz

3; 30.13 Ω
–2.389 kΩ
20 MHz

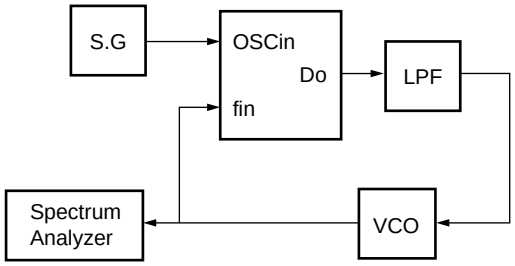
4; 12.844 Ω
–948.37 Ω
50 MHz

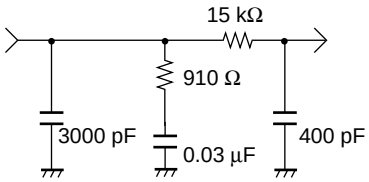
■ REFERENCE INFORMATION

Typical plots measured with the test circuit are shown below. Each plot shows lock up time, phase noise and reference leakage.

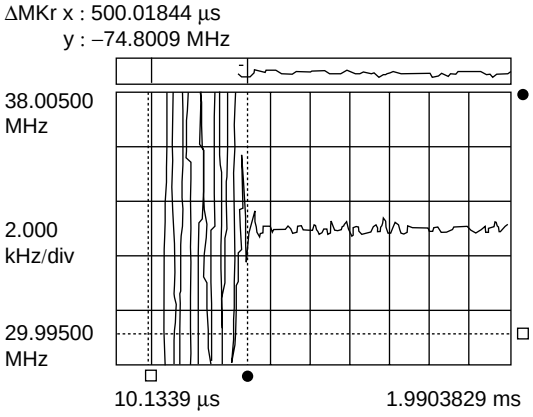
- fvco = 1835 MHz
- Kv = 87 MHz/v
- fr = 200 kHz
- fosc = 13 MHz
- LPF :

Test Circuit

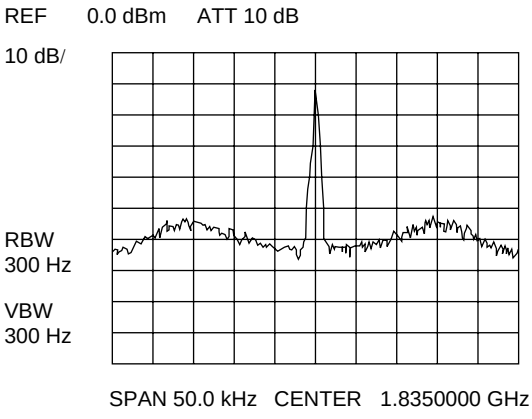


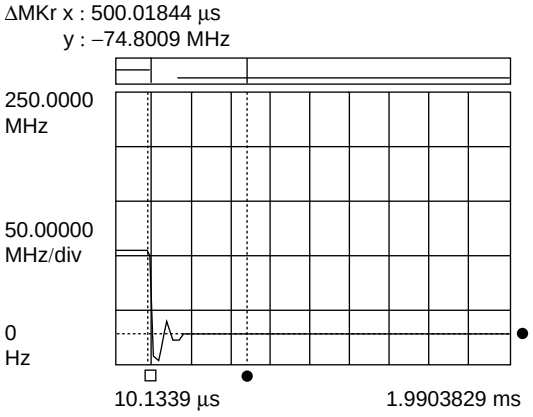


PLL Lock Up Time = 500 µs
(1797.6 MHz → 1872.4 MHz, within ± 1kHz)

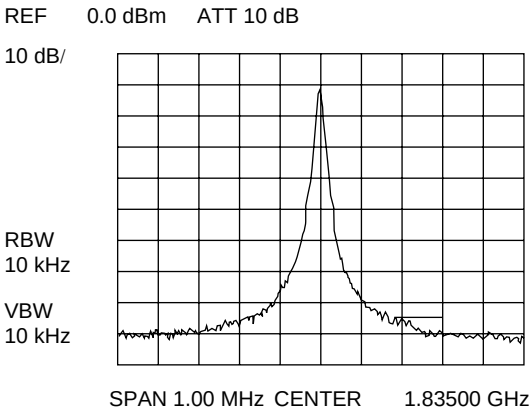


PLL Phase Noise
@ within loop band = 69.4 dBc/H

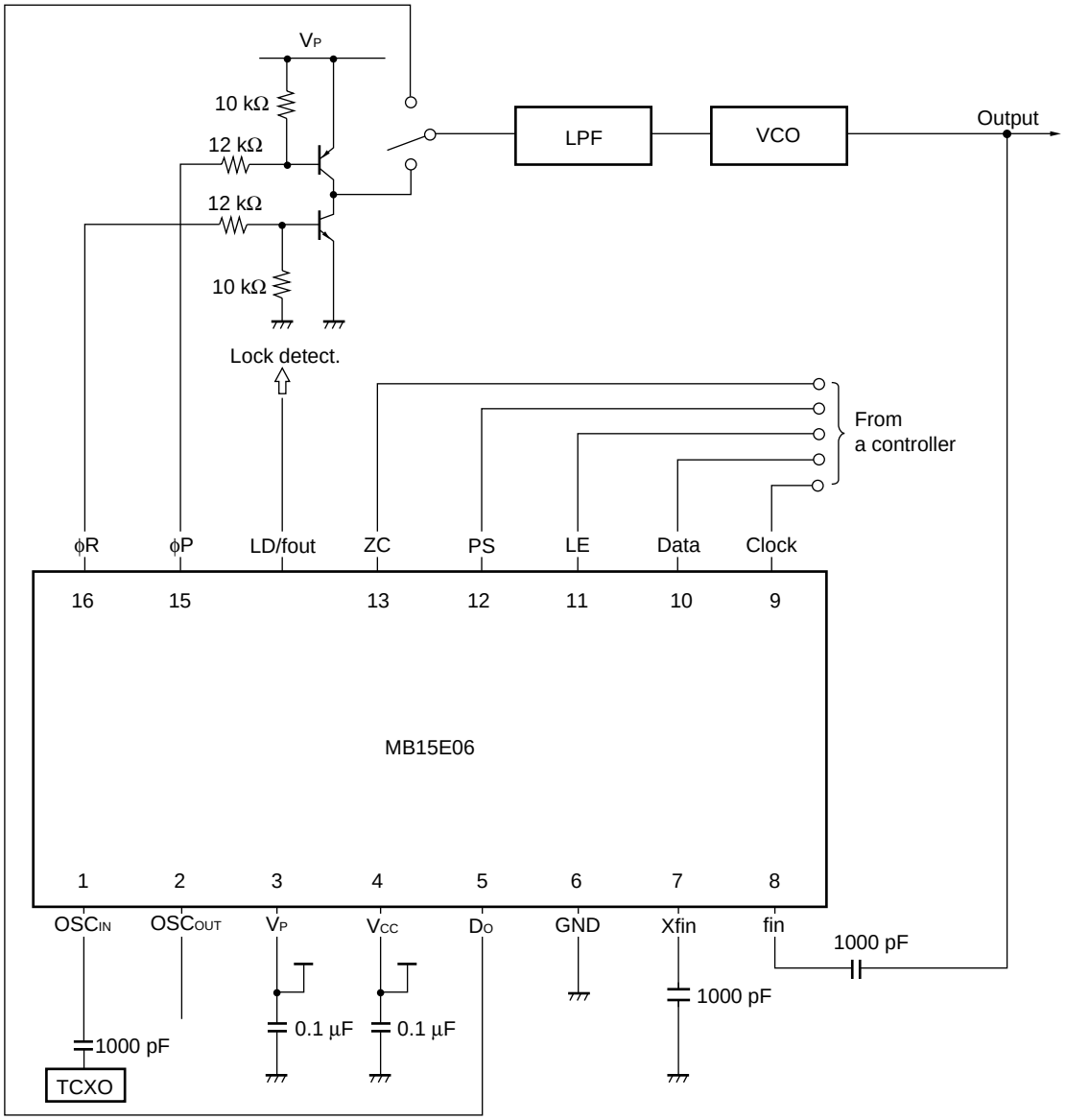




PLL Reference Leakage
@ 200 kHz offset = 74.6 dBc



■ APPLICATION EXAMPLE



Vp : 5.5 V Max

Note : 1. SSOP-16

2. In case of using a crystal resonator, it is necessary to optimize matching between the crystal and this LSI, and perform detailed system evaluation. It is recommended to consult with a supplier of the crystal resonator. (Reference oscillator circuit provides its own bias, feedback resistor is 100 kΩ (typ) .)

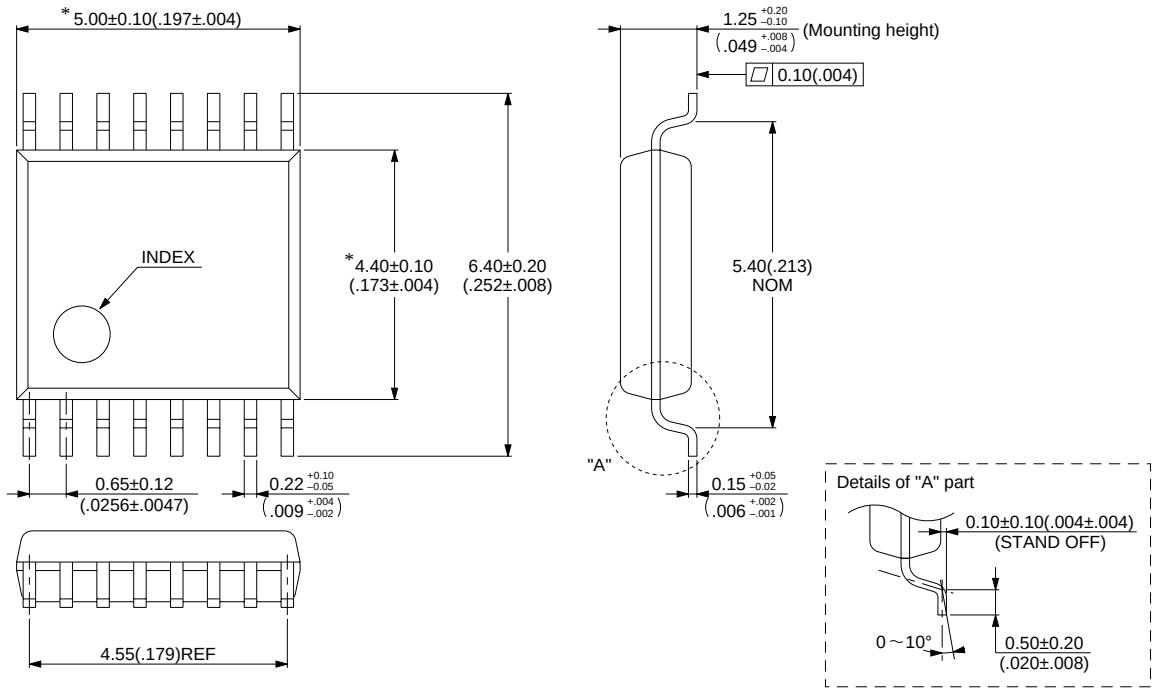
■ ORDERING INFORMATION

Part number	Package	Remarks
MB15E06PFV1	16-pin Plastic SSOP (FPT-16P-M05)	
MB15E06PV1	16-pad plastic BCC (LCC-16P-M06)	

■ PACKAGE DIMENSION

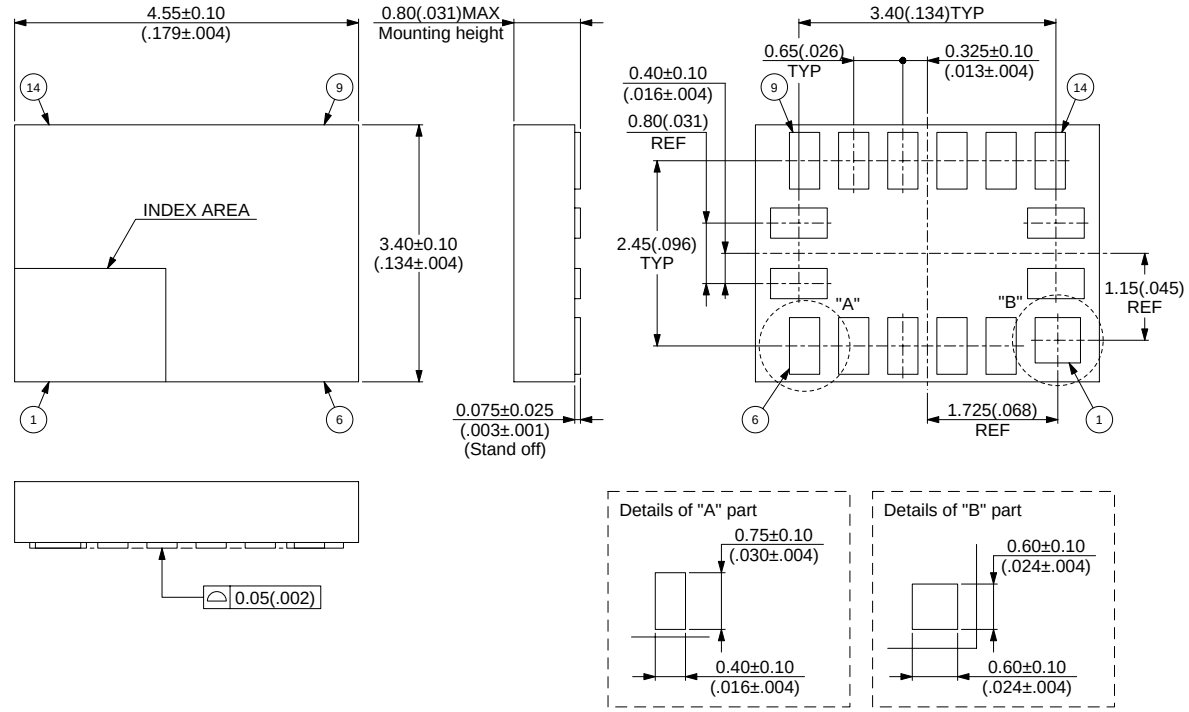
16-pin Plastic SSOP
(FPT-16P-M05)

* : These dimensions do not include resin protrusion.



Dimensions in : mm (inches)

16-pad Plastic BCC
(LCC-16P-M06)



Dimensions in : mm (inches)

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