5. PRELIMINARY ELECTRICAL SPECIFICATIONS

5.1 WHEN SUPPLY VOLTAGE V_{DD} = 5 V±10%

Absolute Maximum Rating (T_a = 25°C)

Parameter	Symbol	Conditions	Rating	Units
Power supply	V_{DD}		−0.5 to +7.0	V
Input voltage	V_I	V_{DD} = 5 V±10%	−0.5 to V_{DD}+0.3	V
Clock input voltage	V_K		−0.5 to V_{DD}+1.0	V
Output voltage	V_O		−0.5 to V_{DD}+0.3	V
Operating temperature	T_{opt}		−40 to +85	°C
Storage temperature	T_{stg}		−65 to +150	°C

DC Characteristics (T_a = −40 to +85°C, V_{DD} = 5 V+10%)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Units
High-level input voltage	V_{IH1} V_{IH2}	•1 •2		2.2 0.7V_{DD}		V_{DD}+0.3	V
Low-level input voltage	V_{IL1} V_{IL2}	•1 •2		−0.5		+0.8 0.2V_{DD}	V
High-level clock input voltage	V_{KH}			3.9		V_{DD}+1.0	V
Low-level clock input voltage	V_{KL}			-0.5		+0.6	V
High-level output voltage	V_{OH}	I_{OH} = −100μA		0.7V_{DD}			V
Low-level output voltage	V_{OL}	I_{OL} = 1.6mA				0.4	V
High-level input leakage current	I_{LIH}	V_I = V_{DD}				10	μA
Low-level input leakage current	I_{LIL}	V_I = 0V				−10	μA
High-level output leakage current	I_{LOH}	V_O = V_{DD}				10	μA
Low-level output leakage current	I_{LOL}	V_O = 0V				−10	μA
Power supply current	I_{DD}	When operating				150	mA
		When clock input stopped	After HALT instruction executed			50	μA
			Other than the above			5	mA

•1 : Each pin of AD0-AD15, SD0-SD7, DMARQ1-DMARQ3, INTP2-INTP7, ADBIOS, HDINS, KEYLOCK, TCLK.

•2 : Pins other than the above

Capacitance (T_a = 25°C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Units
Input capacitance	C_I	fc=1MHz			15	pF
I/O capacitance	C_{IO}	Other than measurement pins : 0 V			15	pF
Output capacitance	C_O				15	pF

AC Characteristics (Ta = −40 to + 85°C, V_{DD} = 5 V±10%)

(1) CPU Timing (1/3)

Parameter	Symbol		Conditions	MIN.	MAX.	Units
X1 input cycle	1	t_{CYX}		31.25	DC	ns
X1 input width, high	2	t_{XXH}		12		ns
X1 input width, low	3	t_{XXL}		12		ns
X1 input rise	4	t_{XR}			5	ns
X1 input fall	5	t_{XF}			5	ns
CPUCLK output cycle	6	t_{CYCK}		62.5	DC	ns
CPUCLK output width, high	7	t_{CKCKH}		t_{CYCK}/2-15		ns
CPUCLK output width, low	8	t_{CKCKL}		t_{CYCK}/2-15		ns
CPUCLK output rise	9	t_{CKR}			15	ns
CPUCLK output fall	10	t_{CKF}			15	ns
CPUCLK output delay (for X1)	11	t_{DXCK}			20	ns
SYSCLK output cycle	12	t_{CYSK}		62.5	DC	ns
SYSCLK output width, high	13	t_{SKSKH}		t_{CYSK}/2-15		ns
SYSCLK output width, low	14	t_{SKSKL}	3-time division	2t_{CYSK}-15		ns
			1, 2, 4-time division	t_{CYSK}/2-15		
SYSCLK output rise	15	t_{SKR}			15	ns
SYSCLK output fall	16	t_{SKF}			15	ns
SYSCLK output delay (for X1)	17	t_{DXSK}			20	ns
TCLK input cycle	18	t_{CYTK}		62.5	DC	ns
TCLK input width, high	19	t_{TKTKH}		30		ns
TCLK input width, low	20	t_{TKTKL}		30		ns
TCLK input rise	21	t_{TKR}			25	ns
TCLK input fall	22	t_{TKF}			25	ns
PWRGOOD set (for CPUCLK↓)	23	t_{SPGCK}		20		ns
PWRGOOD hold (for CPUCLK↓)	24	t_{HCKPG}		15		ns
CPUCLK↓→RESOUT output delay	25	t_{DCKRSO}		5	30	ns
CPUCLK↑→MA address delay	26	t_{DCKMA}			25	ns
X1↑→MA address hold	27	t_{HXMA}		0		ns
X1↑→MA address delay	28	t_{DXMA}			25	ns
CPUCLK↑→MA address hold	29	t_{HCKMA}		0		ns
X1↑→$\overline{WR}$ active delay	30	t_{DXWRL}			40	ns
CPUCLK↓→$\overline{WR}$ inactive delay	31	t_{DCKWRH}			35	ns
X1↑→$\overline{RAS}$ active delay	32	t_{DXRASL}			25	ns

Remarks : Figures in the symbol column correspond to figures in the timing chart.

(1) CPU Timing (2/3)

Parameter	Symbol		Conditions	MIN.	MAX.	Units
CPUCLK↓→$\overline{RAS}$ inactive delay	33	$t_{DCKRASH}$			25	ns
X1↑→$\overline{CAS}$ active delay	34	t_{DXCASL}			25	ns
CPUCLK↑→$\overline{CAS}$ active delay	35	$t_{DCKCASL}$			25	ns
X1↓→$\overline{CAS}$ inactive delay	36	t_{DXCASH}			25	ns
CPUCLK↓→$\overline{CAS}$ inactive delay	37	$t_{DCKCASH}$		5	25	ns
CPUCLK↓→AD data output delay	38	t_{DCKD}		5	30	ns
CPUCLK↑→AD data floating delay	39	t_{FCKD}		5	30	ns
AD data input set (for CPUCLK↓)	40	t_{SDCK}		20		ns
AD data input hold (for CPUCLK↓)	41	t_{HCKD}		10		ns
CPUCLK↑→BS↓delay	42	t_{DKBL}		0	55	ns
CPUCLK↓→BS↑delay	43	t_{DKBH}		0	55	ns
SYSCLK→MA address delay	44	t_{DSKMA}			25	ns
SYSCLK→MA address hold	45	t_{HSKMA}		0		ns
SYSCLK↑→$\overline{WR}$↓delay	46	t_{DSKWRL}			25	ns
SYSCLK↑→$\overline{WR}$↑delay	47	t_{DSKWRH}			40	ns
SYSCLK↑→$\overline{RAS}$↓delay	48	$t_{DSKRASL}$			25	ns
SYSCLK↑→$\overline{RAS}$↑delay	49	$t_{DSKRASH}$			40	ns
SYSCLK↑→$\overline{CAS}$↓delay	50	$t_{DSKCASL}$			25	ns
SYSCLK↑→$\overline{CAS}$↑delay	51	$t_{DSKCASH}$			40	ns
AD data set (for SYSCLK↑)	52	t_{SDSK}		15		ns
AD data hold (for SYSCLK↑)	53	t_{HSKD}		10		ns
SYSCLK↑→AD data output delay	54	t_{DSKDO}		10		ns
SYSCLK↓→AD data valid output delay	55	t_{DSKD}		15		ns
SYSCLK↑→AD data floating delay	56	t_{FSKD}		10		ns
CPUCLK↓→SA address delay	57	t_{DCKSA}			25	ns
CPUCLK↓→SA address hold	58	t_{HCKSA}		0		ns
CPUCLK→control output delay	59	t_{DCKCT}			25	ns
X1↑→control output delay	60	t_{DXCT}			25	ns
SYSCLK↑→SA address delay	61	t_{DSKSA}			25	ns
SYSCLK↑→SA address hold	62	t_{HSKSA}		0		ns
SYSCLK↓→SA address delay	63	t_{DSKSA}			30	ns
SYSCLK↓→SA address hold	64	t_{HSKSA}		0		ns
SYSCLK↓→PCS delay	65	t_{DSKCS}			35	ns
SYSCLK↓→PCS hold	66	t_{HSKCS}		0		ns
Address set (for ALE↓)	67	t_{DSAST}		t_{SKSKL}-10		ns

Remarks : Figures in the symbol column correspond to figures in the timing chart.

(1) CPU Timing (3/3)

Parameter	Symbol		Conditions	MIN.	MAX.	Units
SYSCLK↓→ALE↑delay	68	$t_{DSKSTH1}$			25	ns
SYSCLK↑→ALE↑delay	69	$t_{DSKSTH2}$			35	ns
SYSCLK↑→ALE↓delay	70	t_{DSKSTL}			25	ns
SYSCLK→control 1*1 delay	71	t_{DSKCT1}		5	25	ns
SYSCLK→control 2*1 delay	72	t_{DSKDT2}			40	ns
SD data set (for SYSCLK↓)	73	t_{SSDSK}		30		ns
SD data hold (for $\overline{SMRD}$, $\overline{SIORD}$↑)	74	t_{HRDSD}		0		ns
SYSCLK↑→SD data output delay	75	t_{DSKSDO}			25	ns
SYSCLK↑→SD data valid output delay	76	t_{DSKSD}			25	ns
SYSCLK↑→SD data floating delay	77	t_{FSKSD}		5	30	ns
IOCHRDY set (for SYSCLK↑)	78	t_{SRYSK}		15		ns
IOCHRDY hold (for SYSCLK↑)	79	t_{HSKRY}		5		ns
DMARQn set (for SYSCLK↓)	80	t_{SDQSK}		15		ns
SYSCLK→AEN output delay	81	t_{DSKAE}		5	55	ns
SYSCLK↓→$\overline{DMAAK}$n output delay	82	t_{DSKLDA}		5	55	ns
SYSCLK↑→TC active output delay	83	t_{DSKTCH}			35	ns
SYSCLK↑→TC inactive output delay	84	t_{DSKTCL}			35	ns
TC width, high	85	t_{DTCTC}		t_{SKSKL}-20		ns
NMIIN set (for CPUCLK↓)	86	t_{SNICK}		20		ns
NMIIN hold (for CPUCLK↓)	87	t_{HCKNI}		20		ns
NMIOUT output delay (for CPUCLK↓)	88	t_{DCKNO}			25	ns
$\overline{IOCHCK}$→NMIOUT output delay	89	t_{DCINI}			40	ns
$\overline{IOCHCK}$ set (for CPUCLK)	90	t_{SICK}		20		ns
INTPn width, low	91	t_{IPIPL}			80	ns
KCLK input cycle	92	t_{CYKK}		100		ns
KCLK input width, low	93	t_{TKKKKL}		45		ns
KCLK input width, high	94	t_{TKKKKH}		45		ns
Keyboard data*2 set (for keyboard clock*3 ↑)	95	t_{SKDKK}		15		ns
Keyboard data*2 hold (for keyboard clock*3 ↑)	96	t_{HKKKD}		10		ns
Keyboard data*2 delay (for keyboard clock*3 ↑)	97	t_{DKKKD}			35	ns

*1 : $\overline{SMRD}$, $\overline{SMWR}$, $\overline{SIORD}$, and $\overline{SIOWR}$ signals when other than DMA transfer

*2 : Keyboard data indicate KDAT or MDAT.

*3 : Keyboard clocks indicate KCLK or MCLK.

Remarks 1 : Relationships between keyboard data and keyboard clocks are as follows.

- When checking KDAT, KCLK is used
- When checking MDAT, MCLK is used

2 : Figures in the symbol column correspond to figures in the timing chart.

(2) DRAM Access Timing (Other Than DMA Transfer)

Parameter	Symbol	Conditions	MIN.	MAX.	Units
Random read/write cycle	(201) t_{RC}		$4(1+n)t_{CYCK}-25$		ns
$\overline{RAS}$ access	(202) t_{RAC}			$2.25(1+n)t_{CYCK}-35$	ns
$\overline{CAS}$ access	(203) t_{CAC}			$1.25(1+n)t_{CYCK}-35$	ns
Access from column address	(204) t_{AA}			$1.75(1+n)t_{CYCK}-35$	ns
Output buffer turn-off delay	(205) t_{OFF}			$t_{CYCK}-25$	ns
$\overline{RAS}$ precharge	(206) t_{RP}		$1.75t_{CYCK}-20$		ns
$\overline{RAS}$ pulse width (when random read/write cycle)	(207) t_{RAS}		$2.25(1+n)t_{CYCK}-25$		ns
$\overline{RAS}$ hold	(208) t_{RSH}		$(1+n)t_{CYCK}-25$		ns
$\overline{CAS}$ pulse width	(209) t_{CAS}		$1.25(1+n)t_{CYCK}-25$		ns
$\overline{CAS}$ hold	(210) t_{CSH}		$2.25(1+n)t_{CYCK}-25$		ns
$\overline{RAS}$-$\overline{CAS}$ delay width	(211) t_{RCD}			$t_{CYCK}-25$	ns
$\overline{CAS}$-$\overline{RAS}$ precharge	(212) t_{CRP}		$1.25t_{CYCK}-45$		ns
$\overline{CAS}$ precharge	(213) t_{CPN}		$2.25t_{CYCK}-45$		ns
Low address set-up	(214) t_{ASR}		0		ns
Low address hold	(215) t_{RAH}		$0.5t_{CYCK}-15$		ns
Column address set-up	(216) t_{ASC}		$0.5t_{CYCK}-25$		ns
Column address hold	(217) t_{CAH}		$2.5(1+n)t_{CYCK}-25$		ns
Column address hold for $\overline{RAS}$	(218) t_{AR}		$3.75(1+n)t_{CYCK}-25$		ns
Column address delay for $\overline{RAS}$	(219) t_{RAD}			$0.5t_{CYCK}-25$	ns
Column address read for $\overline{RAS}$	(220) t_{RAL}		$1.75(1+n)t_{CYCK}-25$		ns
Read command set-up	(221) t_{RCS}		$2.75t_{CYCK}-55$		ns
Read command hold for $\overline{RAS}$	(222) t_{RRH}		$1.75t_{CYCK}-45$		ns
Read command hold	(223) t_{RCH}		$1.75t_{CYCK}-45$		ns
Write command hold	(224) t_{WCH}		$(1+n)t_{CYCK}-25$		ns
Write command hold for $\overline{RAS}$	(225) t_{WCR}		$2.25(1+n)t_{CYCK}-25$		ns
Write command pulse width	(226) t_{WP}		$2.25(1+n)t_{CYCK}-40$		ns
Data input set-up	(227) t_{DS}		$t_{CYCK}-30$		ns
Data input hold	(228) t_{DH}		$2(1+n)t_{CYCK}-25$		ns
Data input hold for $\overline{RAS}$	(229) t_{DHR}		$3.25(1+n)t_{CYCK}-25$		ns
$\overline{WE}$ command set-up	(230) t_{WCS}		$1.25t_{CYCK}-40$		ns

Remarks : Figures in the symbol column correspond to figures in the timing chart.

(3) DRAM Access Timing (DMA Transfer)

Parameter	Symbol		Conditions	MIN.	MAX.	Units
Random read/write cycle	(201)	t_{RC}		3.5(1+n)t_{CYSK}-25		ns
$\overline{RAS}$ access	(202)	t_{RAC}			2(1+n)t_{CYSK}-25	ns
$\overline{CAS}$ access	(203)	t_{CAC}			(1+n)t_{CYSK}-35	ns
Access from column address	(204)	t_{AA}			1.5(1+n)t_{CYSK}-35	ns
Output buffer turn-off delay	(205)	t_{OFF}			1.5t_{CYSK}	ns
$\overline{RAS}$ precharge	(206)	t_{RP}		1.5t_{CYSK}		ns
$\overline{RAS}$ pulse width (when random read/write cycle)	(207)	t_{RAS}		2(1+n)t_{CYSK}-25		ns
$\overline{RAS}$ hold	(208)	t_{RSH}	read cycle	(1+n)t_{CYSK}-25		ns
			write cycle	t_{CYSK}-25		
$\overline{CAS}$ pulse width	(209)	t_{CAS}	read cycle	(1+n)t_{CYSK}-25		ns
			write cycle	t_{CYSK}-25		
$\overline{CAS}$ hold	(210)	t_{CSH}		2(1+n)t_{CYSK}-25		ns
$\overline{RAS}$-$\overline{CAS}$ delay width	(211)	t_{RCD}			t_{CYSK}-25	ns
$\overline{CAS}$-$\overline{RAS}$ precharge	(212)	t_{CRP}		2t_{CYSK}-40		ns
$\overline{CAS}$ precharge	(213)	t_{CPN}		1.5t_{CYSK}		ns
Low address set-up	(214)	t_{ASR}		t_{CYCK}-25		ns
Low address hold	(215)	t_{RAH}		0.5t_{CYSK}-15		ns
Column address set-up	(216)	t_{ASC}		0.5t_{CYSK}-25		ns
Column address hold	(217)	t_{CAH}		2(1+n)t_{CYSK}-25		ns
Column address hold for $\overline{RAS}$	(218)	t_{AR}		3(1+n)t_{CYSK}-25		ns
Column address delay for $\overline{RAS}$	(219)	t_{RAD}			0.5t_{CYSK}+25	ns
Column address read for $\overline{RAS}$	(220)	t_{RAL}		1.5(1+n)t_{CYSK}-25		ns
Read command set-up	(221)	t_{RCS}		3t_{CYSK}-40		ns
Read command hold for $\overline{RAS}$	(222)	t_{RRH}		1.5t_{CYSK}		ns
Read command hold	(223)	t_{RCH}		1.5t_{CYSK}		ns
Write command hold	(224)	t_{WCH}		t_{CYSK}-25		ns
Write command hold for $\overline{RAS}$	(225)	t_{WCR}		2(1+n)t_{CYSK}-25		ns
Write command pulse width	(226)	t_{WP}		2(1+n)t_{CYSK}-25		ns
Data input set-up	(227)	t_{DS}		(1+n)t_{CYSK}-30		ns
Data input hold	(228)	t_{DH}		2t_{CYSK}-25		ns
Data input hold for $\overline{RAS}$	(229)	t_{DHR}		3(1+n)t_{CYSK}-25		ns
$\overline{WE}$ command set-up	(230)	t_{WCS}		(1+n)t_{CYSK}-25		ns

Remarks : Figures in the symbol column correspond to figures in the timing chart.

(4) DRAM Access Timing (Refresh Cycle)

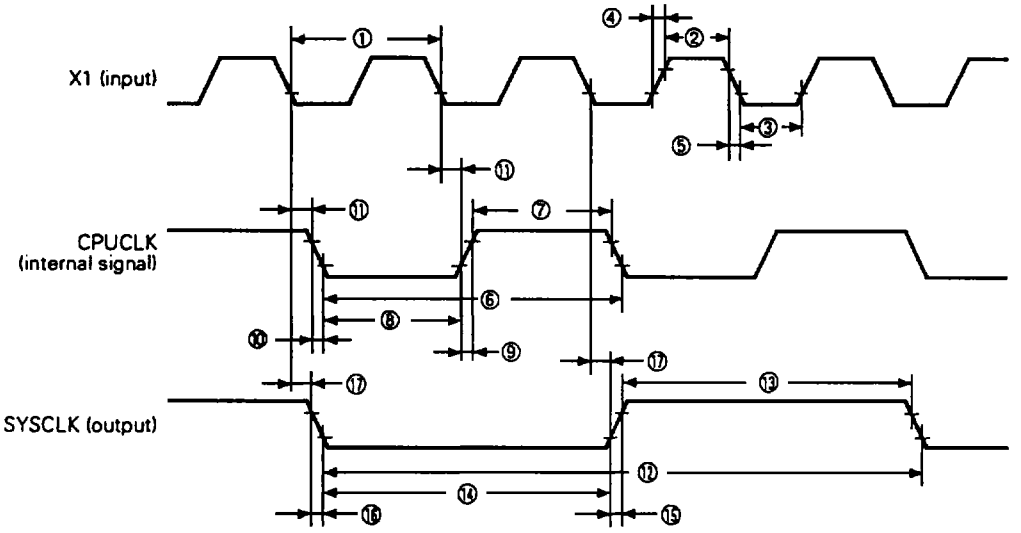
Parameter	Symbol		Conditions	MIN.	MAX.	Units
Random read/write cycle	(301)	t_{RC}		3.5(1+n)t_{CYSK}-25		ns
$\overline{RAS}$ precharge	(302)	t_{RP}		2t_{CYSK}-40		ns
$\overline{RAS}$ pulse width (when random read/write cycle time)	(303)	t_{RAS}		2(1+n)t_{CYSK}-25		ns
$\overline{RAS}$ precharge/$\overline{CAS}$ hold	(304)	t_{RPC}		t_{CYSK}-40		ns
$\overline{CAS}$ set-up	(305)	t_{CSR}		t_{CYSK}-25		ns
$\overline{CAS}$ hold ($\overline{CAS}$ before $\overline{RAS}$ refresh)	(306)	t_{CHR}		2(1+n)t_{CYSK}-25		ns

Remarks : Figures in the symbol column correspond to figures in the timing chart.

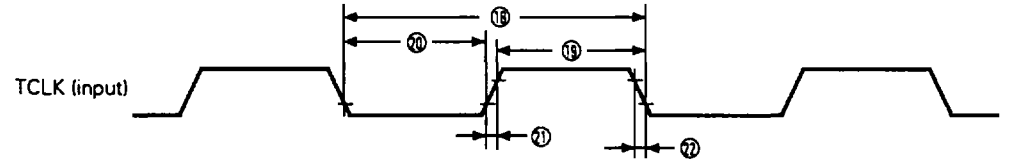
5.2 WHEN SUPPLY VOLTAGE V_{DD} = 3 V±10%

Under evaluation

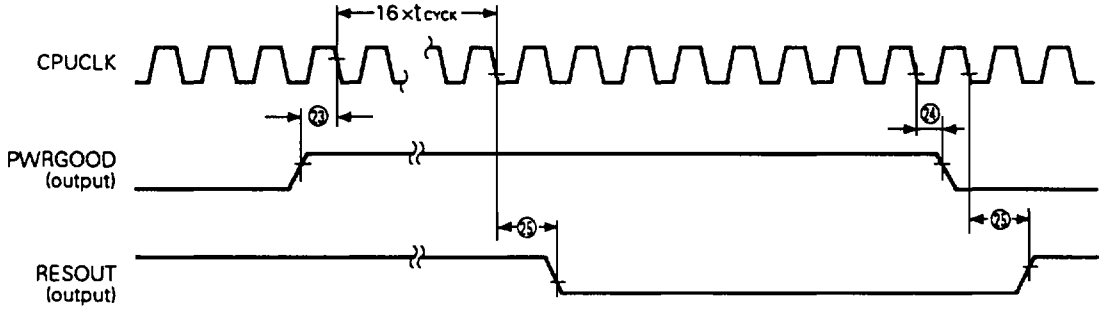
Clock Timing



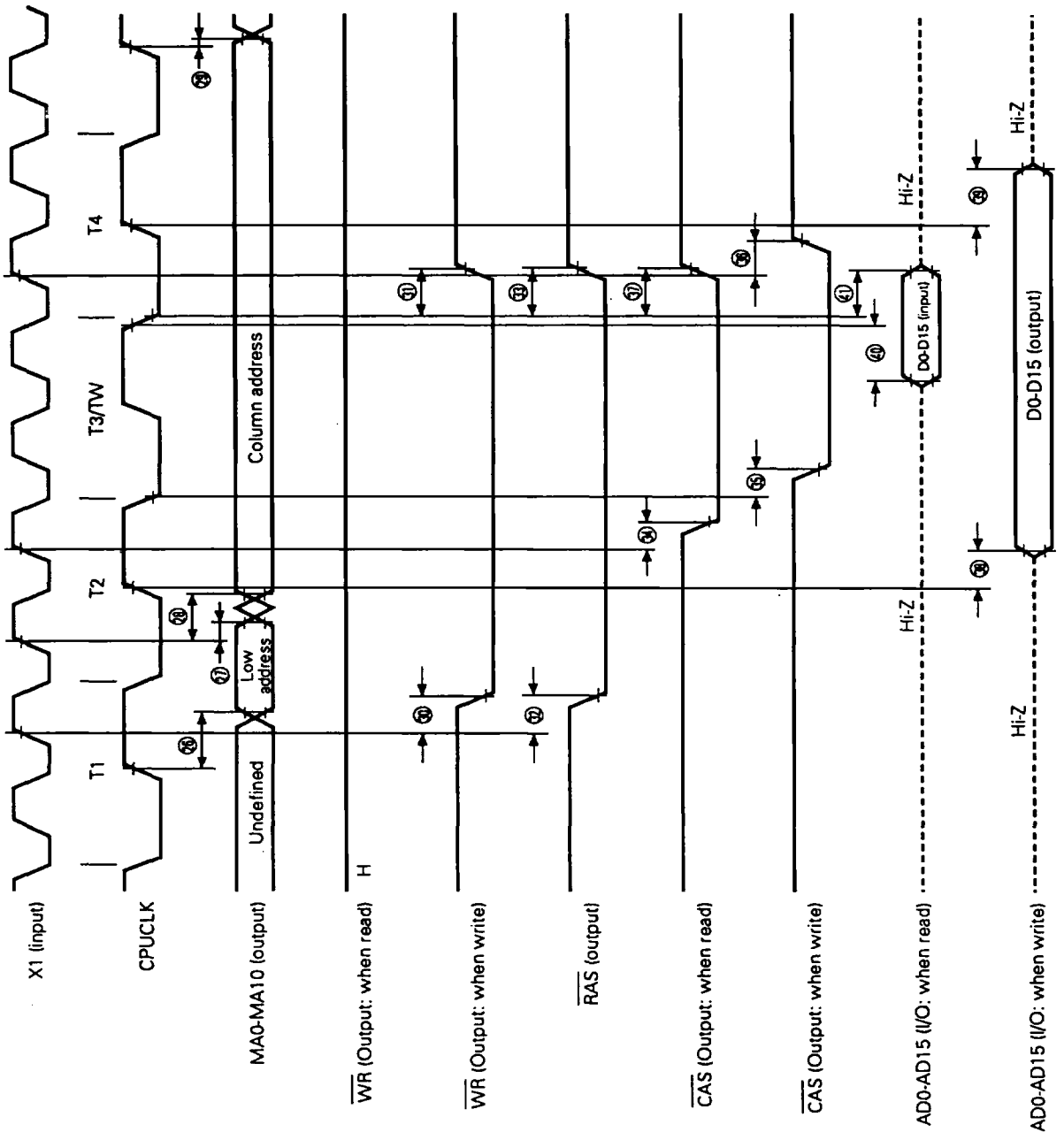
Timer Clock Timing



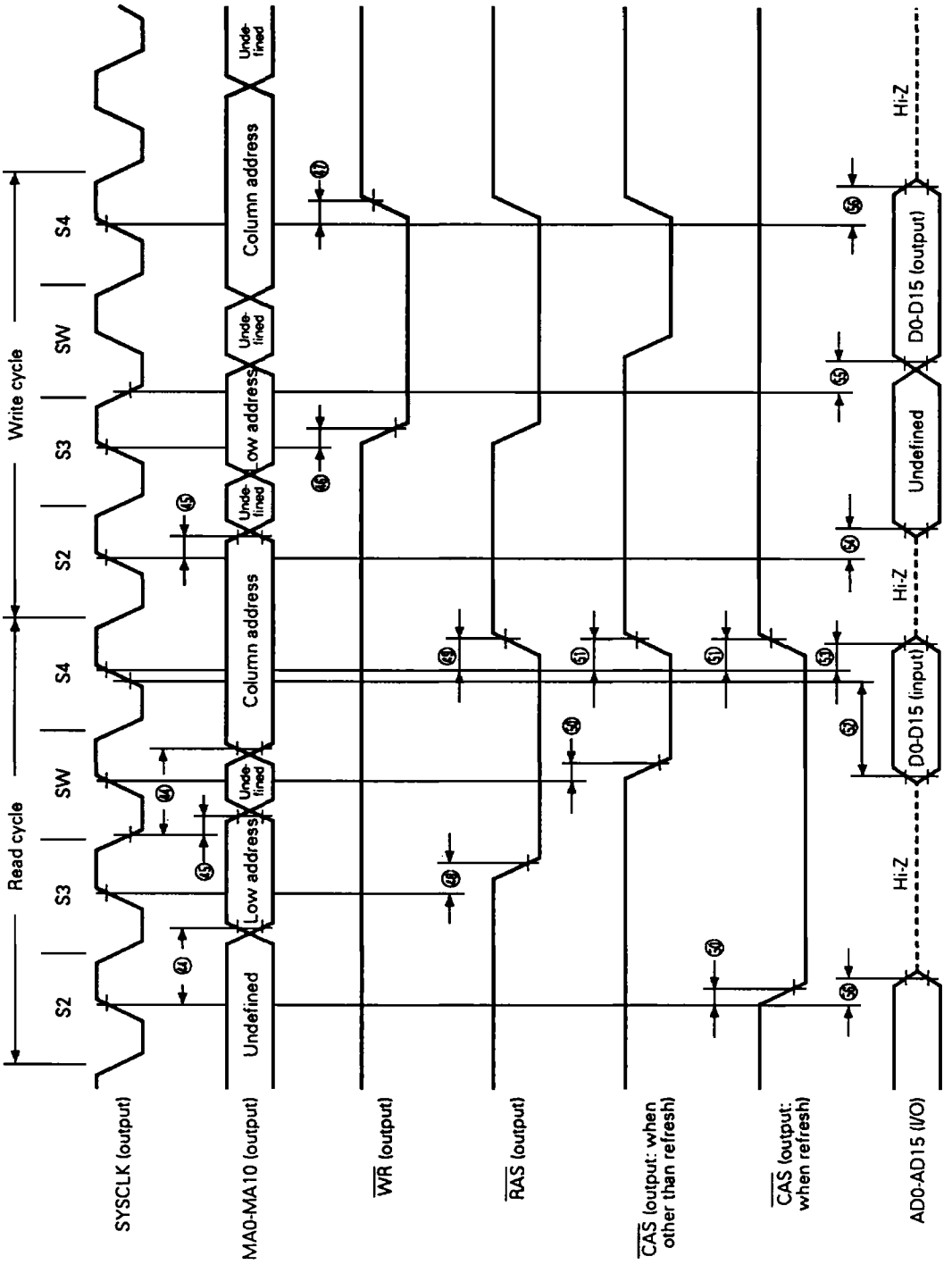
Reset Timing



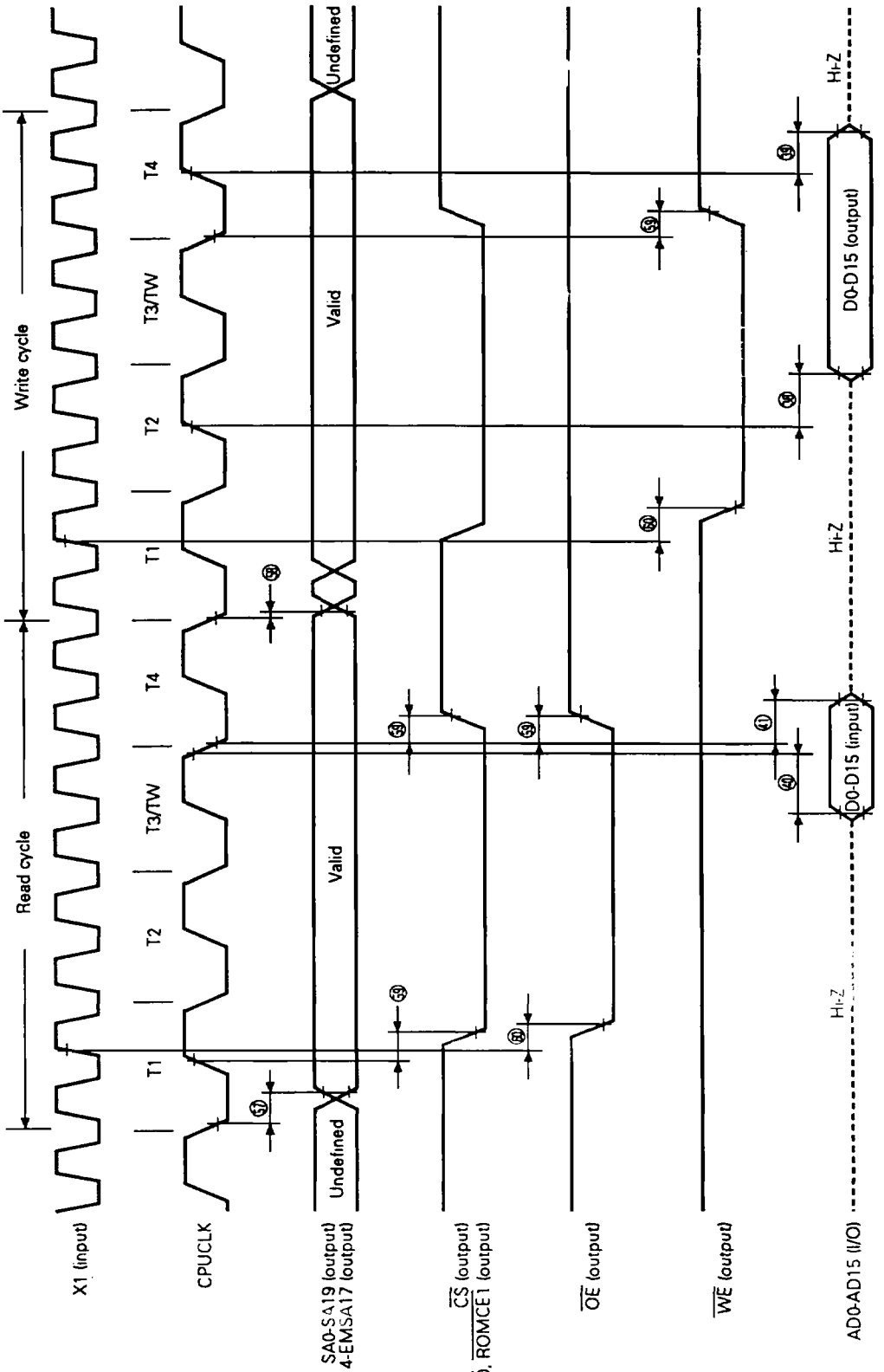
DRAM Access Timing (Other Than DMA Transfer)



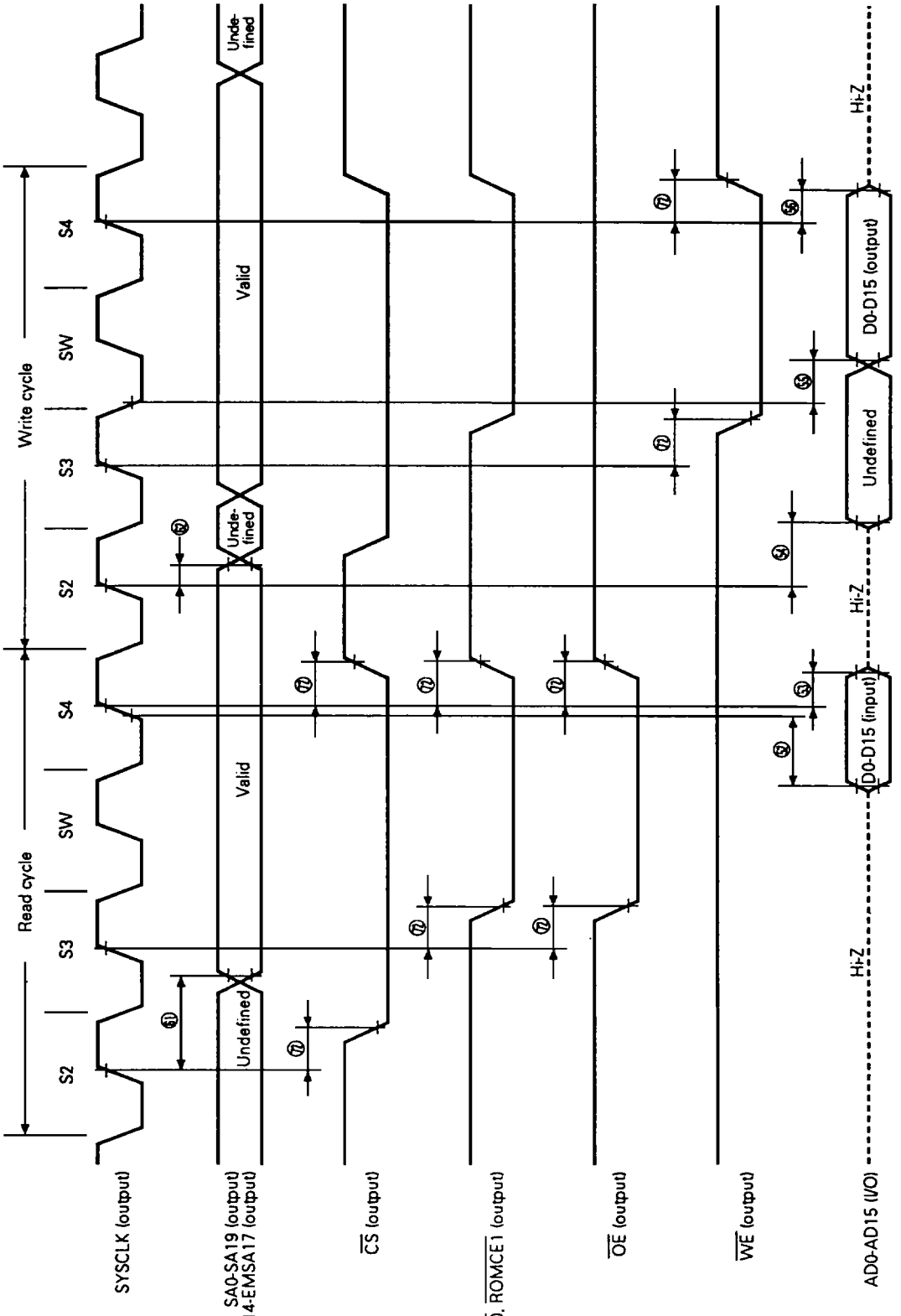
DRAM Access Timing (DMA Transfer)



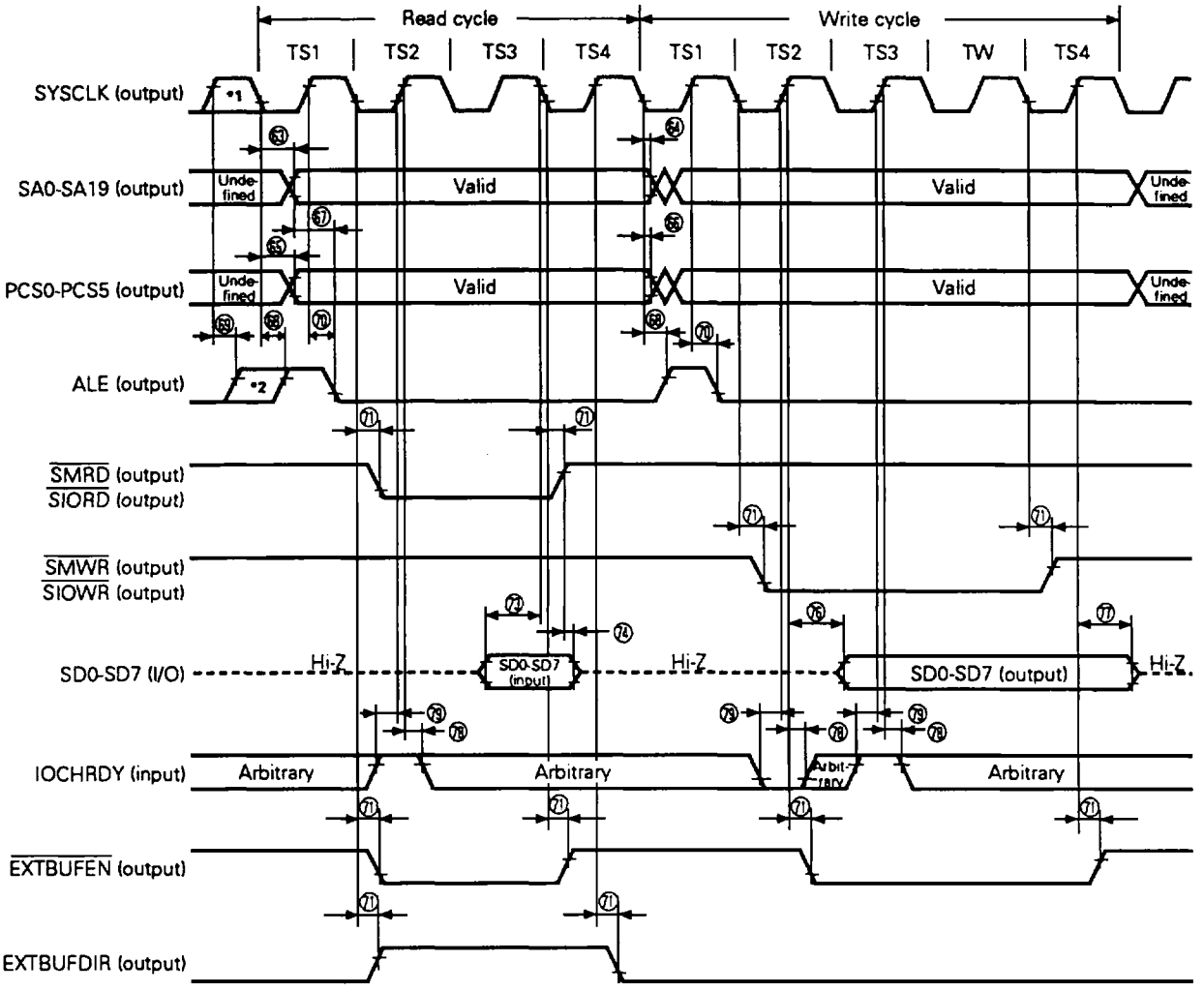
SRAM, Pseudo-SRAM and ROM Access Timing (Other Than DMA Transfer)



SRAM, Pseudo-SRAM and ROM Access Timing (DMA Transfer)



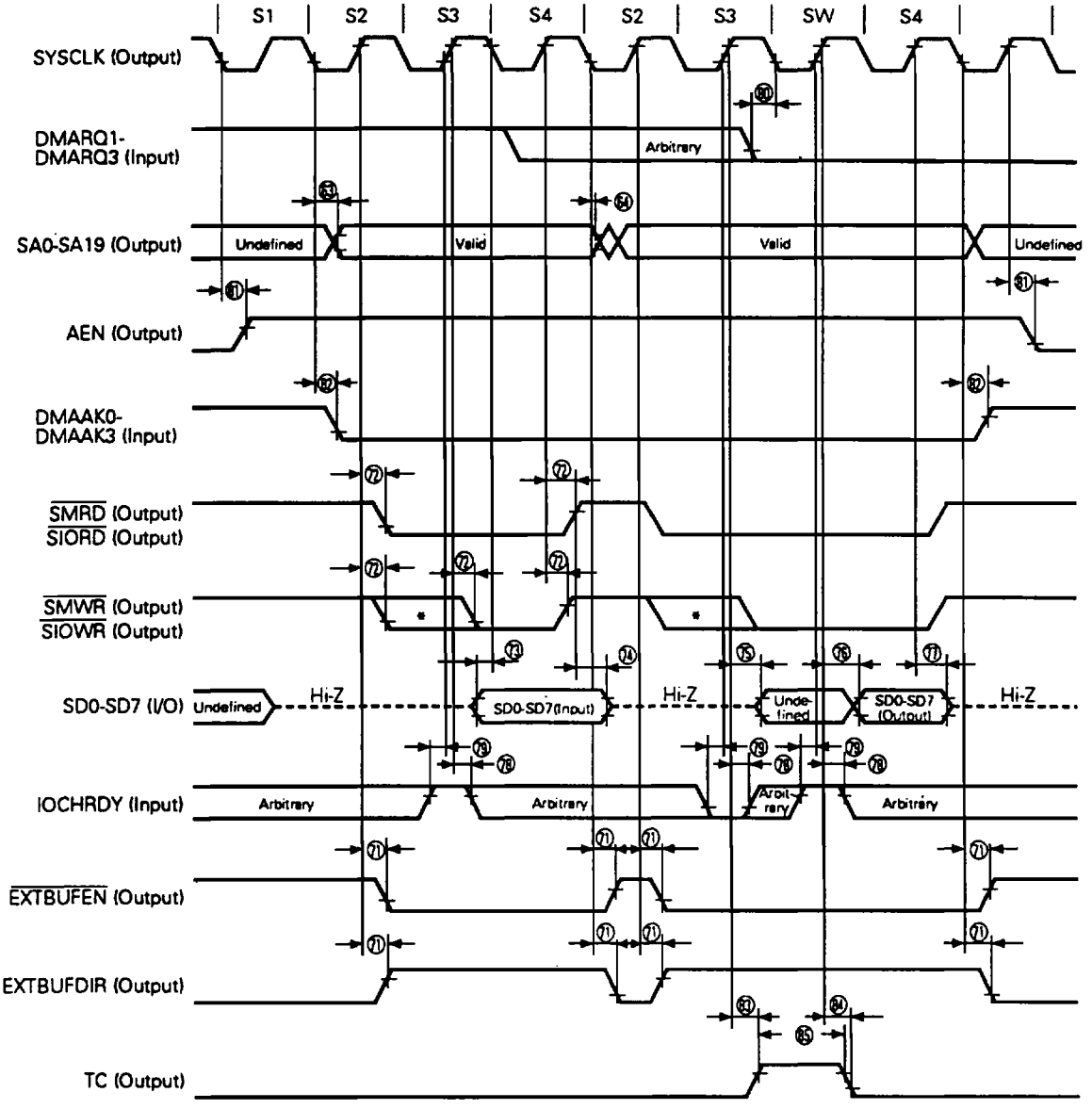
I/O Channel Interface Timing (Other Than DMA Transfer)



***1** : High-level only when cycles of SYSCLK are the same as those of CPUCLK.

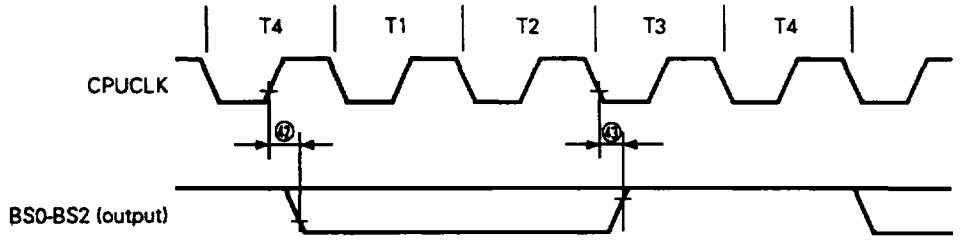
***2** : May become high-level half a clock before, unless bus cycles are continuous.

I/O Channel Interface Timing (DMA Transfer)

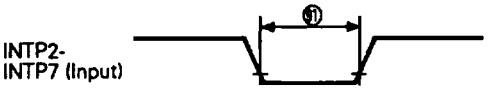


* : Outputs low level when extended write.

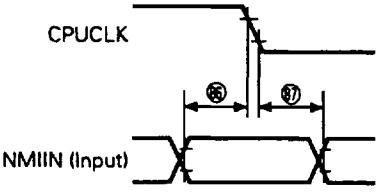
BS0-BS2 Output Timing



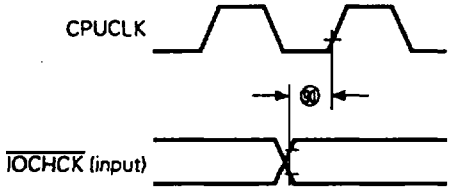
INTP2-INTP7 Input Timing



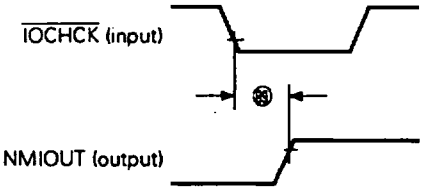
NMIIN Sumple Timing



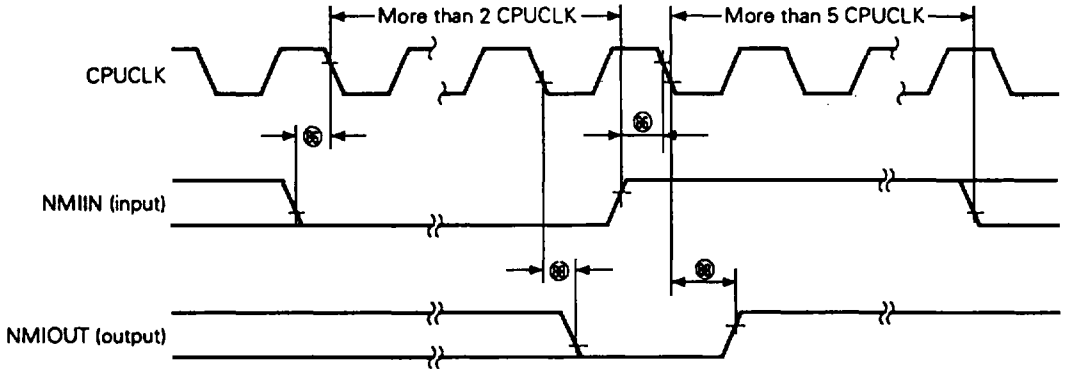
$\overline{\text{IOCHCK}}$ Input Timing



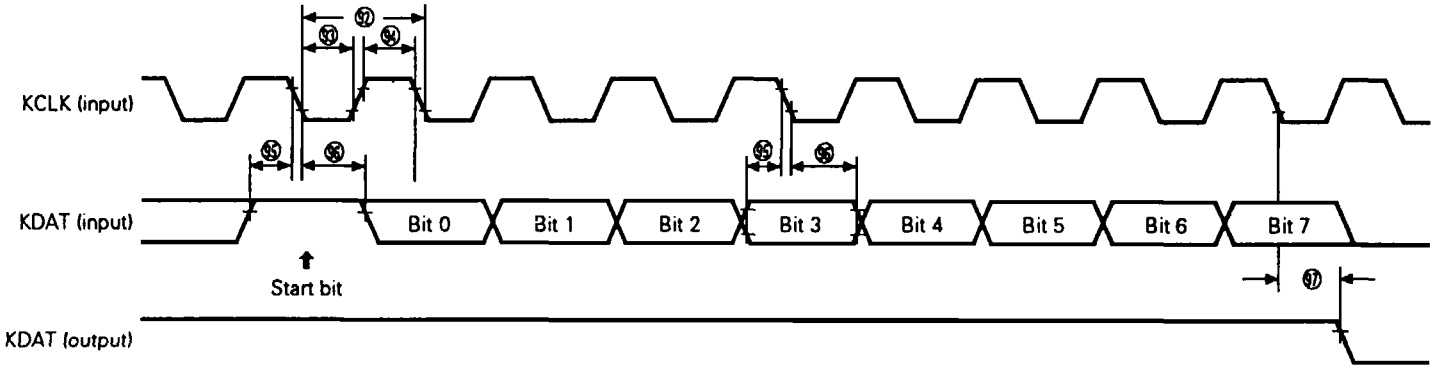
NMIOUT Output Timing (1)



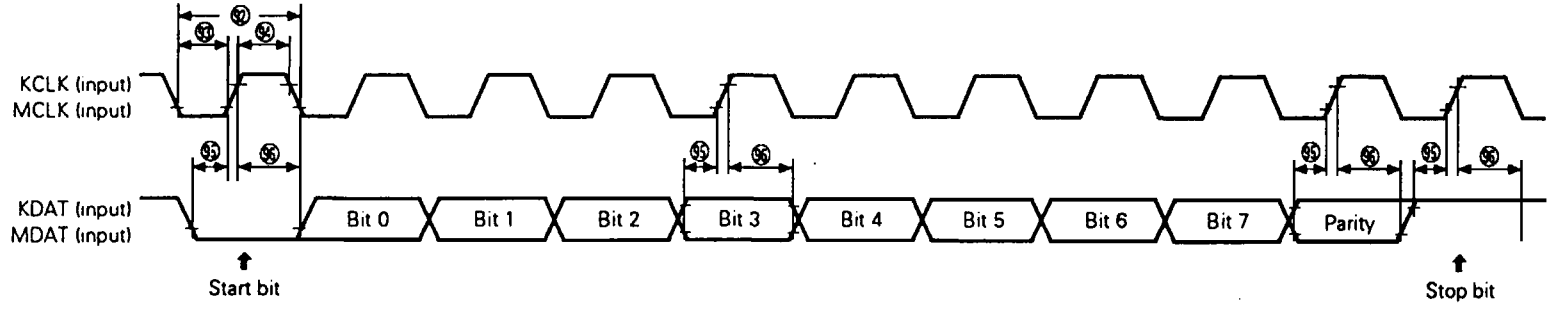
NMIOUT Output Timing (2)



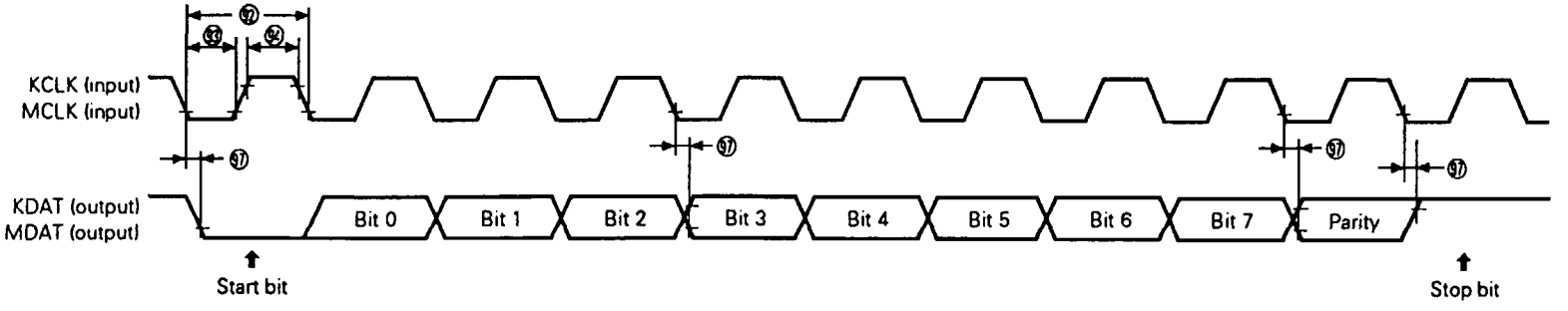
Keyboard Interface (XT Type: Reception)



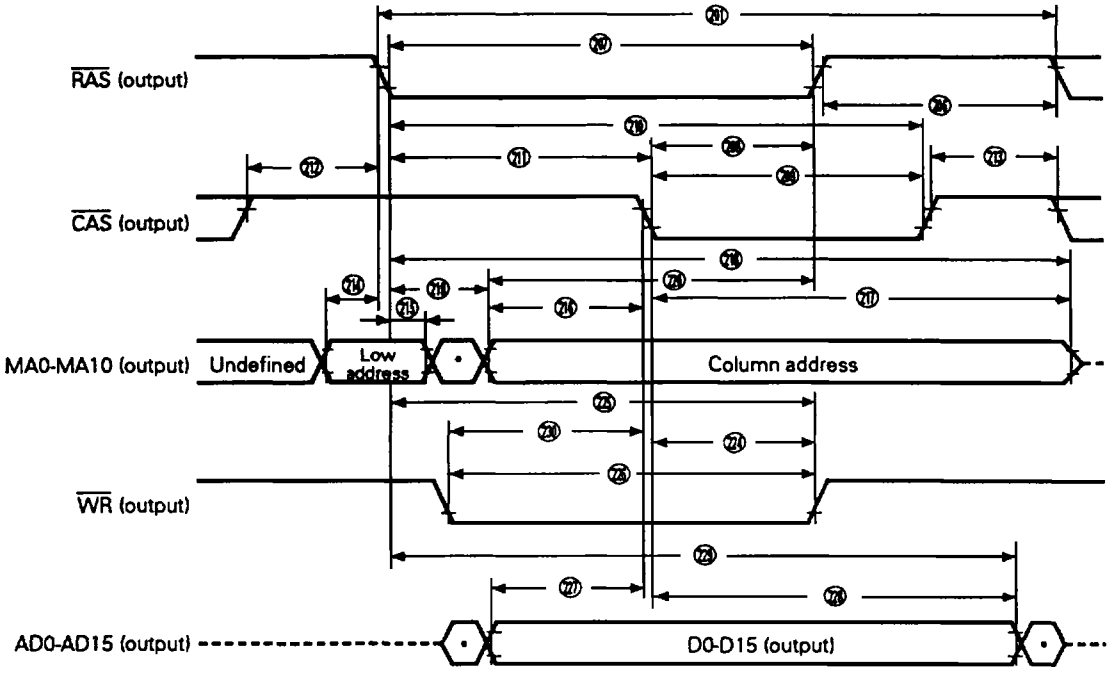
Keyboard Interface (PS/2 Model 30 Type: Reception)



Keyboard Interface (PS/2 Model 30 Type: Transfer)



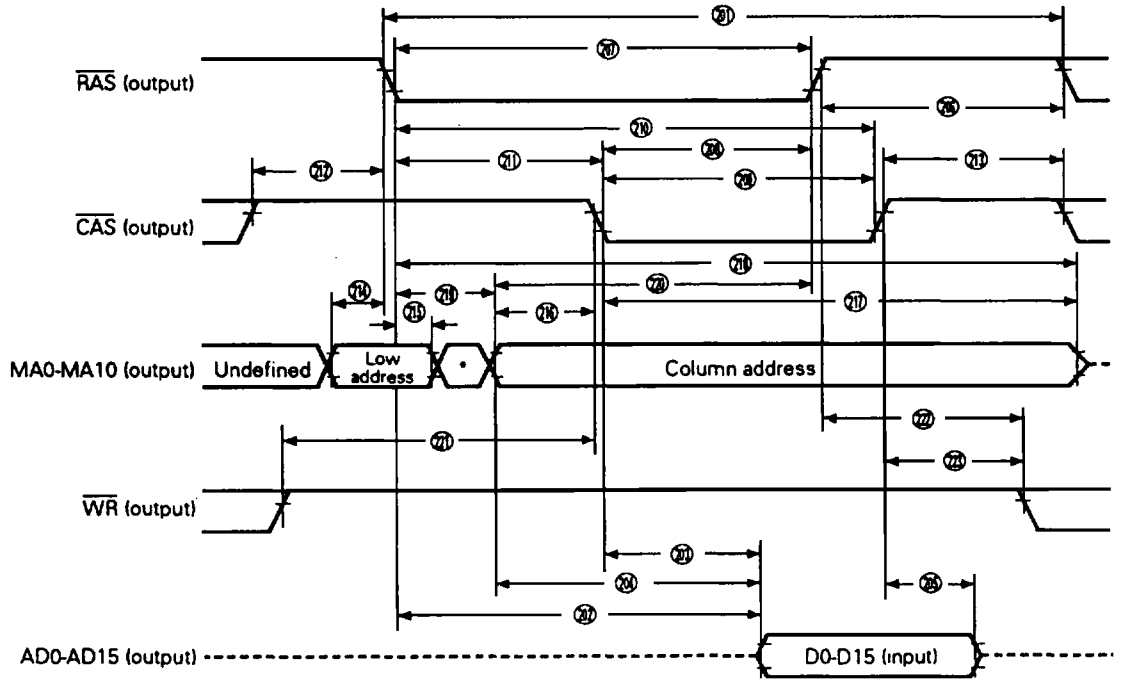
DRAM Write Timing



* : Undefined

Remarks : Broken lines indicate high impedance.

DRAM Read Timing



* : Undefined

Remarks : Broken lines indicate high impedance.

DRAM Refresh Cycle