ANALOG DEVICES

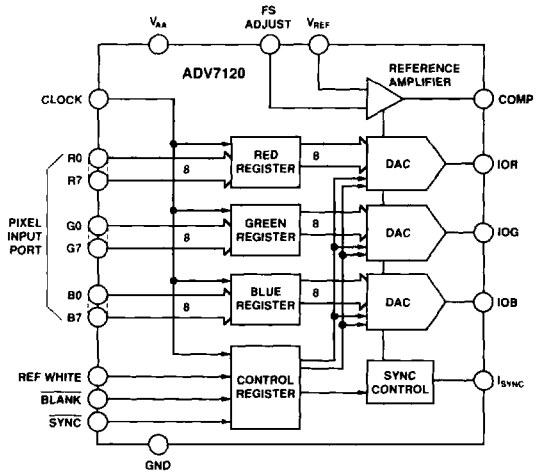
CMOS
80 MHz, Triple 8-Bit Video DAC
ADV7120

FEATURES
80 MHz Pipelined Operation
Triple 8-Bit D/A Converters
RS-343A/RS-170 Compatible Outputs
TTL Compatible Inputs
+5 V CMOS Monolithic Construction
40-Pin DIP or 44-Pin PLCC Package
Power Dissipation: 400 mW

APPLICATIONS
High Resolution Color Graphics
CAE/CAD/CAM Applications
Image Processing
Instrumentation
Video Signal Reconstruction
Desktop Publishing
Direct Digital Synthesis (DDS)

SPEED GRADES
80 MHz
50 MHz
30 MHz

FUNCTIONAL BLOCK DIAGRAM



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GENERAL DESCRIPTION

The ADV7120 (ADV®) is a digital to analog video converter on a single monolithic chip. The part is specifically designed for high resolution color graphics and video systems. It consists of three, high speed, 8-bit, video D/A converters (RGB); a standard TTL input interface and high impedance, analog output, current sources.

The ADV7120 has three separate, 8-bit, pixel input ports, one each for red, green and blue video data. Additional video input controls on the part include composite sync, blank and reference white. A single +5 V supply, an external 1.23 V reference and pixel clock input are all that are required to make the part operational.

The ADV7120 is capable of generating RGB video output signals, which are compatible with RS-343A and RS-170 video standards, without requiring external buffering.

The ADV7120 is fabricated in a +5 V CMOS process. Its monolithic CMOS construction ensures greater functionality with low power dissipation. The part is packaged in both a 0.6", 40-pin plastic DIP and a 44-pin plastic leaded (J-lead) chip carrier, PLCC.

PRODUCT HIGHLIGHTS

1. Fast video refresh rate, 80 MHz.
2. Compatible with a wide variety of high resolution color graphics video systems.
3. Guaranteed monotonic with a maximum differential nonlinearity of ±0.5 LSB. Integral nonlinearity is guaranteed to be a maximum of ±1 LSB.

ADV7120—SPECIFICATIONS

(V_{AA} = +5 V ±5%; V_{REF} = +1.235 V; R_L = 37.5 Ω, C_L = 10 pF; R_{SET} = 560 Ω. I_{SYNC} connected to IOG. All Specifications T_{MIN} to T_{MAX}[1] unless otherwise noted).

Parameter	All Versions	Units	Test Conditions/Comments
STATIC PERFORMANCE			
Resolution (Each DAC)	8	Bits	
Accuracy (Each DAC)			
Integral Nonlinearity, INL	±1	LSB max	
Differential Nonlinearity, DNL	±0.5	LSB max	Guaranteed Monotonic
Gray Scale Error	±5	% Gray Scale max	Max Gray Scale Current: IOG = (V_{REF}* 12,082/R_{SET}) mA
			IOR, IOB = (V_{REF}* 8,627/R_{SET}) mA
Coding	Binary		
DIGITAL INPUTS			
Input High Voltage, V_{INH}	2	V min	
Input Low Voltage, V_{INL}	0.8	V max	
Input Current, I_{IN}	±1	μA max	V_{IN} = 0.4 V or 2.4 V
Input Capacitance, C_{IN}[2]	10	pF max	
ANALOG OUTPUTS			
Gray Scale Current Range	15	mA min	
	22	mA max	
Output Current			
White Level Relative to Blank	17.69	mA min	Typically 19.05 mA
	20.40	mA max	
White Level Relative to Black	16.74	mA min	Typically 17.62 mA
	18.50	mA max	
Black Level Relative to Blank	0.95	mA min	Typically 1.44 mA
	1.90	mA max	
Blank Level on IOR, IOB	0	μA min	Typically 5 μA
	50	μA max	
Blank Level on IOG	6.29	mA min	Typically 7.62 mA
	9.5	mA max	
Sync Level on IOG	0	μA min	Typically 5 μA
	50	μA max	
LSB Size	69.1	μA typ	
DAC to DAC Matching	5	% max	Typically 2%
Output Compliance, V_{OC}	−1	V min	
	+1.4	V max	
Output Impedance, R_{OUT}[2]	100	kΩ typ	
Output Capacitance, C_{OUT}[2]	30	pF max	I_{OUT} = 0 mA
VOLTAGE REFERENCE			
Voltage Reference Range, V_{REF}	1.14/1.26	V min/V max	V_{REF} = 1.235 V for Specified Performance
Input Current, I_{VREF}	−5	mA typ	
POWER REQUIREMENTS			
V_{AA}	5	V nom	
I_{AA}	125	mA max	Typically 80 mA: 80 MHz Parts
	100	mA max	Typically 70 mA: 50 MHz & 35 MHz Parts
Power Supply Rejection Ratio	0.5	%/% max	Typically 0.12%/%: f = 1 kHz, COMP = 0.1 μF
Power Dissipation	625	mW max	Typically 400 mW: 80 MHz Parts
	500	mW max	Typically 350 mW: 50 MHz & 30 MHz Parts
DYNAMIC PERFORMANCE			
Glitch Impulse[2, 3]	50	pV secs typ	
DAC Noise[2, 3, 4]	200	pV secs typ	
Analog Output Skew	2	ns max	Typically 1 ns

NOTES

[1]Temperature Range (T_{min} to T_{max}); 0 to +70°C.

[2]Sample tested at +25°C to ensure compliance.

[3]TTL input values are 0 to 3 volts, with input rise/fall times <3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. See timing notes in Figure 1.

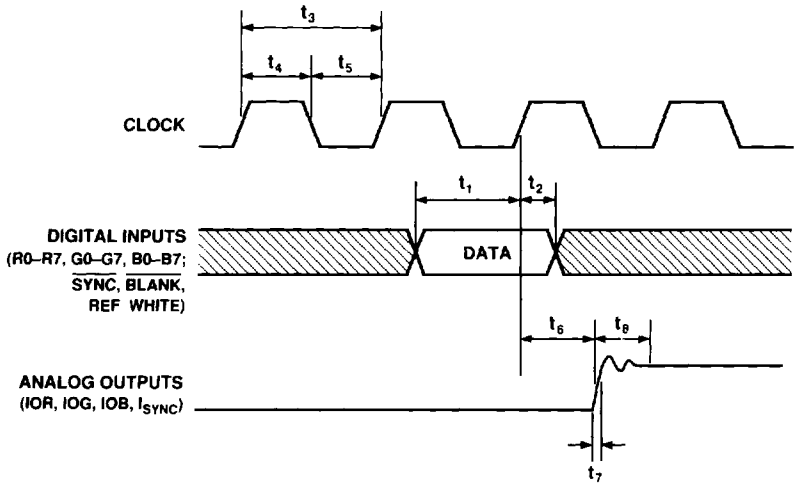
[4]This includes effects due to clock and data feedthrough as well as RGB analog crosstalk.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{AA} = +5 V ±5%; V_{REF} = +1.235 V; R_L = 37.5 Ω, C_L = 10 pF; R_{SET} = 560 Ω. I_{SYNC} connected to IOG. All Specifications T_{min} to T_{max}[2] unless otherwise noted.)

Parameter	80 MHz Version	50 MHz Version	30 MHz Version	Units	Conditions/Comments
f_{max}	80	50	30	MHz max	Clock Rate
t_1	3	6	8	ns min	Data & Control Setup Time
t_2	2	2	2	ns min	Data & Control Hold Time
t_3	12.5	20	33.3	ns min	Clock Cycle Time
t_4	4	7	9	ns min	Clock Pulse Width High Time
t_5	4	7	9	ns min	Clock Pulse Width Low Time
t_6	30	30	30	ns max	Analog Output Delay
	20	20	20	ns typ	
t_7	3	3	3	ns max	Analog Output Rise/Fall Time
t_8[3]	12	15	15	ns typ	Analog Output Transition Time

NOTES
[1]TTL input values are 0 to 3 volts, with input rise/fall times ≤3ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. See timing notes in Figure 1.
[2]Temperature range (T_{min} to T_{max}): 0 to +70°C
[3]Sample tested at +25°C to ensure compliance.
Specifications subject to change without notice.



NOTES
1. OUTPUT DELAY (t_6) MEASURED FROM THE 50% POINT OF THE RISING EDGE OF CLOCK TO THE 50% POINT OF FULL-SCALE TRANSITION.
2. TRANSITION TIME (t_8) MEASURED FROM THE 50% POINT OF FULL-SCALE TRANSITION TO WITHIN 2% OF THE FINAL OUTPUT VALUE.
3. OUTPUT RISE/FALL TIME (t_7) MEASURED BETWEEN THE 10% AND 90% POINTS OF FULL TRANSITION.

Figure 1. Video Input/Output Timing

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	V_{AA}	4.75	5.00	5.25	Volts
Ambient Operating Temperature	T_A	0		+70	°C
Output Load	R_L		37.5		Ω
Reference Voltage	V_{REF}	1.14	1.235	1.26	Volts

ABSOLUTE MAXIMUM RATINGS*

V_{AA} to GND . . . . . +7 V
Voltage on Any Digital Pin . . . . GND −0.5 V to V_{AA} +0.5 V
Ambient Operating Temperature (T_A) . . . . . 0 to +70°C
Storage Temperature (T_S) . . . . . −65°C to +150°C
Junction Temperature (T_J) . . . . . +175°C
Soldering Temperature (10 secs) . . . . . 300°C
Vapor Phase Soldering (1 minute) . . . . . 220°C
IOR, IOB, IOG, I_{SYNC} to GND[1] . . . . . 0 V to V_{AA}

NOTES

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[1]Analog Output Short Circuit to any Power Supply or Common can be of an indefinite duration.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

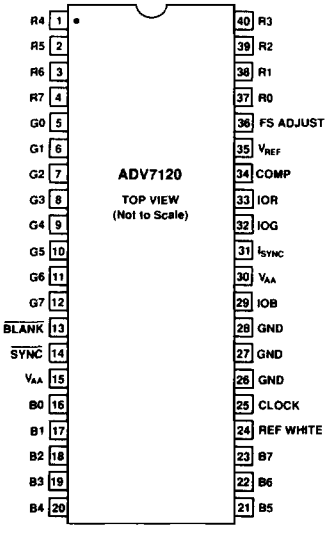
ORDERING GUIDE

Model	Speed	Temperature Range	Package Option*
ADV7120KN80	80 MHz	0°C to +70°C	N-40A
ADV7120KN50	50 MHz	0°C to +70°C	N-40A
ADV7120KN30	30 MHz	0°C to +70°C	N-40A
ADV7120KP80	80 MHz	0°C to +70°C	P-44A
ADV7120KP50	50 MHz	0°C to +70°C	P-44A
ADV7120KP30	30 MHz	0°C to +70°C	P-44A

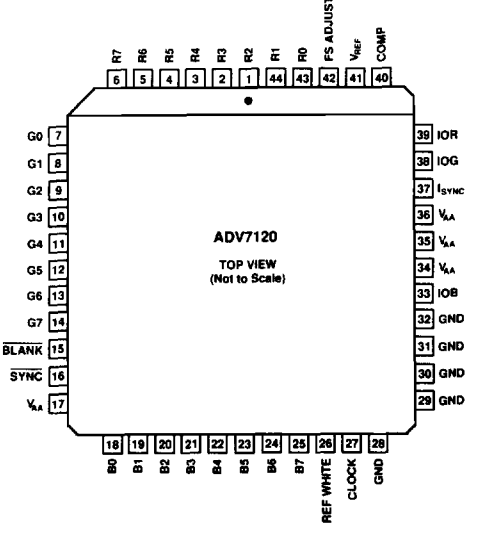
*N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

PIN CONFIGURATIONS

DIP



PLCC



PIN FUNCTION DESCRIPTION

Pin Mnemonic	Function
$\overline{\text{BLANK}}$	Composite blank control input (TTL compatible). A logic zero on this control input drives the analog outputs, IOR, IOB and IOG, to the blanking level. The $\overline{\text{BLANK}}$ signal is latched on the rising edge of CLOCK. While $\overline{\text{BLANK}}$ is a logical zero, the R0–R7, G0–G7, R0–R7 and REF WHITE pixel and control inputs are ignored.
$\overline{\text{SYNC}}$	Composite sync control input (TTL compatible). A logical zero on the $\overline{\text{SYNC}}$ input switches off a 40 IRE current source on the I_{SYNC} output. $\overline{\text{SYNC}}$ does not override any other control or data input; therefore, it should only be asserted during the blanking interval. $\overline{\text{SYNC}}$ is latched on the rising edge of CLOCK.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the R0–R7, G0–G7, B0–B7, $\overline{\text{SYNC}}$, $\overline{\text{BLANK}}$ and REF WHITE pixel and control inputs. It is typically the pixel clock rate of the video system. CLOCK should be driven by a dedicated TTL buffer.
REF WHITE	Reference white control input (TTL compatible). A logical one on this input forces the IOR, IOG and IOB outputs to the white level, regardless of the pixel input data (R0–R7, G0–G7 and B0–B7). REF WHITE is latched on the rising edge of clock.
R0–R7, G0–G7, B0–B7	Red, green and blue pixel data inputs (TTL compatible). Pixel data is latched on the rising edge of CLOCK. R0, G0 and B0 are the least significant data bits. Unused pixel data inputs should be connected to either the regular PCB power or ground plane.
IOR, IOG, IOB	Red, green, and blue current outputs. These high impedance current sources are capable of directly driving a doubly terminated 75 Ω coaxial cable. All three current outputs should have similar output loads whether or not they are all being used.
I_{SYNC}	Sync current output. This high impedance current source can be directly connected to the IOG output. This allows sync information to be encoded onto the green channel. I_{SYNC} does not output any current while $\overline{\text{SYNC}}$ is at logical zero. The amount of current output at I_{SYNC} while $\overline{\text{SYNC}}$ is at logical one is given by: $I_{SYNC}\ (mA) = 3{,}455 \times V_{REF}\ (V)/\ R_{SET}\ (\Omega)$ If sync information is not required on the green channel, I_{SYNC} should be connected to AGND.
FS ADJUST	Full-scale adjust control. A resistor (R_{SET}) connected between this pin and GND, controls the magnitude of the full-scale video signal. Note that the IRE relationships are maintained, regardless of the full-scale output current. The relationship between R_{SET} and the full-scale output current on IOG (assuming I_{SYNC} is connected to IOG) is given by: $R_{SET}\ (\Omega) = 12{,}082 \times V_{REF}\ (V)/IOG\ (mA)$ The relationship between R_{SET} and the full-scale output current on IOR and IOB is given by: $IOR,\ IOB\ (mA) = 8{,}628 \times V_{REF}\ (V)/\ R_{SET}\ (\Omega)$
COMP	Compensation pin. This is a compensation pin for the internal reference amplifier. A 0.1 μF ceramic capacitor must be connected between COMP and V_{AA}.
V_{REF}	Voltage reference input. An external 1.2 V voltage reference must be connected to this pin. The use of an external resistor divider network is not recommended. A 0.1 μF decoupling ceramic capacitor should be connected between V_{REF} and V_{AA}.
V_{AA}	Analog power supply (5 V ± 5%). All V_{AA} pins on the ADV7120 must be connected.
GND	Ground. All GND pins must be connected.

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TERMINOLOGY

Blanking Level
The level separating the $\overline{\text{SYNC}}$ portion from the video portion of the waveform. Usually referred to as the front porch or back porch. At 0 IRE units, it is the level which will shut off the picture tube, resulting in the blackest possible picture.

Color Video (RGB)
This usually refers to the technique of combining the three primary colors of red, green and blue to produce color pictures within the usual spectrum. In RGB monitors, three DACs are required, one for each color.

Sync Signal ($\overline{\text{SYNC}}$)
The position of the composite video signal which synchronizes the scanning process.

Gray Scale
The discrete levels of video signal between reference black and reference white levels. An 8-bit DAC contains 256 different levels while a 6-bit DAC contains 64.

Raster Scan
The most basic method of sweeping a CRT one line at a time to generate and display images.

Reference Black Level
The maximum negative polarity amplitude of the video signal.

Reference White Level
The maximum positive polarity amplitude of the video signal.

Sync Level
The peak level of the $\overline{\text{SYNC}}$ signal.

Video Signal
That portion of the composite video signal which varies in gray scale levels between reference white and reference black. Also referred to as the picture signal, this is the portion which may be visually observed.