Device Requirements and Characteristics

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Table 29. Absolute Maximum Ratings

Parameter	Min	Max	Unit
Voltage Range on Any Pin with Respect to Ground	–0.5	6.0	V
Power Dissipation	—	1.7	W
Storage Temperature	–65	150	°C
External Lead Bonding and Soldering Temperature	—	300	°C

Warning: All CMOS devices are prone to latch-up if excessive current is injected to/from the substrate. To prevent latch-up at powerup, no input pin should be subjected to input voltages greater than V_{IL}, or less than V_{SS} – 0.5 V before V_{DD} is applied. After powerup, input should not be greater than V_{DD} + 0.5 V or less than V_{SS} – 0.5 V.

Handling Precautions

All MOS devices must be handled with certain precautions to avoid damage due to the accumulation of static charge. **Although input protection circuitry has been incorporated into the devices to minimize the effect of this static buildup, proper precautions should be taken to avoid exposure to electrostatic discharge during handling and mounting.** AT&T employs a human-body model for ESD susceptibility testing. Since the failure voltage of electronic devices is dependent on the current and voltage and, hence, the resistance and capacitance, it is important that standard values be employed to establish a reference by which to compare test data. Values of 100 pF and 1500 Ω are the most common and are the values used in the AT&T human-body model test circuit. The breakdown voltage for the DSP32C is greater than 2000 V*, according to the human-body model. ESD data for the charged-device model is available on request.

* The value of 2000 V for the breakdown voltage is subject to change.

Device Requirements and Characteristics (continued)

Temperature Class Definitions

Table 30. Temperature Class Definitions

Temperature Class	Ambient Temperature T_A (°C)	
	Min	Max
Commercial	0	70
Industrial	–40	85

Recommended Operating Conditions

Table 31. Recommended Operating Conditions

Device Speed	Package	Temperature Class	Device Code	Supply Voltage V_{DD} (V)	
				Min	Max
50 ns	133-Pin CPGA	Commercial	DSP32C-R35---050	4.75	5.25
	164-Pin BQFP	Commercial	DSP32C-F35---050	4.75	5.25
	133-Pin CPGA	Industrial	DSP32C-R35---050-I	4.75	5.25
60 ns	133-Pin CPGA	Commercial	DSP32C-R35---060	4.75	5.25
	164-Pin BQFP	Commercial	DSP32C-F35---060	4.75	5.25
	133-Pin CPGA	Industrial	DSP32C-R35---060-I	4.75	5.25
80 ns	133-Pin CPGA	Commercial	DSP32C-R35---080	4.5	5.5
	164-Pin BQFP	Commercial	DSP32C-F35---080	4.5	5.5
	133-Pin CPGA	Industrial	DSP32C-R35---080-I	4.75	5.25
	164-Pin BQFP	Industrial	DSP32C-F35---080-I	4.75	5.25

Package Thermal Considerations

The recommended operating temperature specified above is based on the maximum power, package type, and maximum junction temperature. The following equation describes the relationship between these parameters. For certain applications, the maximum power may be less than the worst-case value and the following relationship can be used to determine the maximum ambient temperature allowed.

$$T_A = T_J - P \times \Theta_{JA}$$

Maximum Junction Temperature (T_J) in 133-Pin CPGA ..... +125 °C
133-Pin CPGA Maximum Thermal Resistance in Still-Air-Ambient (Θ_{JA}) ..... 25 °C/W

Maximum Junction Temperature (T_J) in 164-Pin BQFP ..... +125 °C
164-Pin BQFP Maximum Thermal Resistance in Still-Air-Ambient (Θ_{JA}) ..... 37 °C/W

Electrical Characteristics

The parameters below are valid for the following conditions:
Commercial temperature class device: T_A = 0 °C to 70 °C; V_{SS} = 0 V; C_{LOAD} = 50 pF.
Industrial temperature class device: T_A = –40 °C to +85 °C; V_{SS} = 0 V; C_{LOAD} = 50 pF.

Parameter	Sym	Min	Max	Unit
Input Voltage: All Pins Except PAB3—PAB0, PEN, PGN, PWN, OCK, ICK, SY*				
Low	V_{IL}	—	0.8	V
High (commercial temperature class device)	V_{IH}	2.0	—	V
High (industrial temperature class device)	V_{IH}	2.2	—	V
Input Voltage: Pins PAB3—PAB0, PEN, PGN, PWN, OCK, ICK, SY*				
Low	V_{IL}	—	0.8	V
High (commercial temperature class device)	V_{IH}	2.4	—	V
High (industrial temperature class device)	V_{IH}	2.7	—	V
Output Low Voltage				
Low (I_{OL} = 2 mA)	V_{OL}	—	0.4	V
Low (I_{OL} = 5 µA)	V_{OL}	—	0.2	V
Output High Voltage				
High (I_{OH} = –2 mA)	V_{OH}	V_{DD} – 0.7	—	V
High (I_{OH} = –5 µA)	V_{OH}	V_{DD} – 0.2	—	V
Input Leakage: All Inputs Except ZN				
Low (V_{IL} = 0 V) Low	I_{IL}	–5	—	µA
High (V_{IH} = 5.5 V) High	I_{IH}	—	5	µA
Input Leakage: ZN† Pin				
Low (V_{IL} = 0 V) Low	I_{IL}	–500	—	µA
High (V_{IH} = 5.5 V) High	I_{IH}	—	5	µA
Output Offset Current				
Low (V_{OL} = 0 V)	I_{OZL}	–10	—	µA
High (V_{OH} = 5.5 V)	I_{OZH}	—	10	µA
Input, Output, I/O Capacitance	CI	—	10	pF
Power Supply Current‡				
Instruction Cycle Time = 50 ns; tCKILCKIL = 12.5 ns	I_{DD}	—	306	mA
Instruction Cycle Time = 60 ns; tCKILCKIL = 15 ns	I_{DD}	—	255	mA
Instruction Cycle Time = 80 ns; tCKILCKIL = 20 ns	I_{DD}	—	225	mA
Power Dissipation§				
Instruction Cycle Time = 50 ns; tCKILCKIL = 12.5 ns	PD	—	1.7	W
Instruction Cycle Time = 60 ns; tCKILCKIL = 15 ns	PD	—	1.4	W
Instruction Cycle Time = 80 ns; tCKILCKIL = 20 ns	PD	—	1.25	W

* The ICK, OCK, and SY pins have Schmitt triggers with hysteresis in the range of 0.5 V to 0.8 V.
† This pin has a pull-up device.
‡ Current in the input buffers is highly dependent on the input voltage level. At full CMOS levels, essentially no dc current is drawn, but for levels near the threshold of 1.4 V, high and unstable levels of current may flow. There are 72 inputs to the chip (19 input-only and 53 input/output pins). If all inputs are connected to a dc voltage around 1.4 V, an additional current in the range of 150 mA can be drawn. This current can be almost totally eliminated by setting the input pins to CMOS voltage levels (V_{DD} or V_{SS}). Therefore, all unused inputs should be tied inactive to V_{DD} or V_{SS} and all unused I/O pins should be tied inactive through a 10 kΩ resistor to V_{DD} or V_{SS}.
§ The power dissipation listed is for output loads = 70 pF. Total power dissipation can be calculated on the basis of the application by adding $C \times V_{DD}^2 \times f$ for each output, where C is the load capacitance and f is the output frequency.