4.0 SDP3B FlashDisk Interface Description

4.1 Physical Description

The host is connected to the SDP3B FlashDisk using a standard 68 pin PCMCIA connector consisting of two rows of 34 female contacts each on 50 mil (1.27 mm) centers.

4.1.1 Pin Assignments and Pin Type

The signal/pin assignments are listed in Table 4-1. Low active signals have a "-" prefix. Pin types are Input, Output or Input/Output. Table 4-2 defines the DC characteristics for all input and output type structures.

4.2 Electrical Description

The SDP3B FlashDisk is optimized for operation with hosts which support the PCMCIA I/O interface standard conforming to the PC Card ATA specification. However, the SDP3B FlashDisk may also be configured to operate in systems that support only the memory interface standard. The configuration of the SDP3B FlashDisk will be controlled using the standard PCMCIA configuration registers starting at address 200h in the Attribute Memory space of the SDP3B FlashDisk.

Table 4-2 describes the I/O signals. Signals whose source is the host are designated as inputs while signals that the SDP3B FlashDisk sources are outputs. The SDP3B FlashDisk logic levels conform to those specified in the PCMCIA Release 2.1 specification.

Table 4-1 Pin Assignments and Pin Type

Pin Num	Signal Name	Pin Type	In / Out Type
1	GND		Ground
2	D03	I/O	I-1/O-3
3	D04	I/O	I-1/O-3
4	D05	I/O	I-1/O-3
5	D06	I/O	I-1/O-3
6	D07	I/O	I-1/O-3
7	-CE1	I	I-4
8	A10	I	I-1
9	-OE	I	I-4
10			
11	A09	I	I-1
12	A08	I	I-1
13			
14			
15	-WE	I	I-4
16	RDY/-BSY\-IREQ	O	O-2
17	VCC		Power
18	VPP		(Not Used)
19			
20			
21			
22	A07	I	I-1
23	A06	I	I-1
24	A05	I	I-1
25	A04	I	I-1
26	A03	I	I-1
27	A02	I	I-1
28	A01	I	I-1
29	A00	I	I-1
30	D00	I/O	I-1/O-3
31	D01	I/O	I-1/O-3
32	D02	I/O	I-1/O-3
33	WP\-IOIS16	O	O-3
34	GND		Ground

Pin Num	Signal Name	Pin Type	In / Out Type
35	GND		Ground
36	-CD1	O	Ground
37	D11*	I/O	I-1/O-3
38	D12*	I/O	I-1/O-3
39	D13*	I/O	I-1/O-3
40	D14*	I/O	I-1/O-3
41	D15*	I/O	I-1/O-3
42	-CE2*	I	I-4
43	-VS1	O	Ground
44	-IORD	I	I-4
45	-IOWR	I	I-4
46			
47			
48			
49			
50			
51	VCC		Power
52	VPP		(Not Used)
53			
54			
55			
56	-CSEL	I	I-2
57	-VS2	O	Open
58	RESET	I	I-4
59	-WAIT	O	O-3
60	-INPACK	O	O-2
61	-REG	I	I-4
62	BVD2\-SPKR	O	O-1
63	BVD1/-STSCHG	I/O	I-3/O-1
64	D08*	I/O	I-1/O-3
65	D09*	I/O	I-1/O-3
66	D10*	I/O	I-1/O-3
67	-CD2	O	Ground
68	GND		Ground

Note: Signals marked with an asterisk are required only for 16-bit access, but not required when installed in 8-bit systems. Signals which are defined differently in the Memory only interface and the I/O interface have the Memory only interface signal shown first, followed by a backslash (\) and then the I/O interface signal. The -IORD, -IOWR and -INPACK signals are not used in the memory only interface. Signals that have different functions in True IDE Mode are listed in Table 4-2.

Table 4-2 Signal Description

Signal Name	Dir.	Pin	Description
BVD2 (Memory) -SPKR (I/O) -DASP (True IDE Mode)	O I/O	62	This output line is always driven to a high state since a battery is not required for this product and no audio is produced. In the True IDE Mode, this input / output is the Disk Active / Slave Present signal in the Master / Slave handshake protocol.
-CD1, -CD2	O	36,67	These Card Detect pins are connected to ground on the SDP3B FlashDisk. They are used by the host to verify that the SDP3B FlashDisk is fully inserted into its socket.
D15 - D00	I/O	2, 3, 4, 5, 6, 30, 31, 32, 37, 38, 39, 40, 41, 64, 65, 66	These lines carry the Data, Commands and Status information between the host and the controller. D00 is the Least Significant Bit of the Even Byte of the Word. D08 is the Least Significant Bit of the Odd Byte of the Word. In True IDE Mode, all Task File operations occur in byte mode on the low order bus D00-D07 while all data transfers are 16-bit using D00-D15.
-IOWR (I/O)	I	45	The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the SDP3B FlashDisk controller registers when the SDP3B FlashDisk is configured to use the I/O interface. The clocking will occur on the negative to positive edge of the signal (trailing edge).
-IORD (I/O)	I	44	This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the SDP3B FlashDisk when the SDP3B FlashDisk is configured to use the I/O interface.
-WE	I	15	The Write Enable signal is driven by the host and used for strobing memory Write data to the registers of the SDP3B FlashDisk, when the SDP3B FlashDisk is configured in the Memory interface mode. It is also used for writing the configuration registers in all modes. In the True IDE Mode, this input signal is not used.
-OE	I	9	This is an Output Enable strobe generated by the host interface. It is used to read data from the SDP3B FlashDisk in memory mode and to read the Card Information Structure (CIS) and configuration registers in all modes. In True IDE Mode, this input should be grounded.

Table 4-2 Signal Description (continued)

Signal Name	Dir.	Pin	Description
RDY/-BSY (Memory) READY [RDY/-BSY] -IREQ (I/O) INTRQ (True IDE Mode)	O	16	In memory mode this signal is set high when the SDP3B FlashDisk is ready to accept a new data transfer operation and held low when the SDP3B FlashDisk is busy. The Host memory SDP3B FlashDisk socket must provide a pull-up resistor. See section 2.3 for power-on or reset to ready timing. At power up and at Reset, the RDY/-BSY signal is held low (busy) until the SDP3B FlashDisk has completed its power up or reset function. No access of any type should be made to the SDP3B FlashDisk during this time. The RDY/-BSY signal is held continuously ready whenever the following two conditions are True: 1) The SDP3B FlashDisk has been powered up with +RESET continuously disconnected or asserted, and; 2) the Set Feature 97H command with config value of 35H has been issued. I/O Operation - After the SDP3B FlashDisk has been configured for I/O operation, this signal is used as -Interrupt Request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt. In True IDE Mode, this signal is the active high -Interrupt Request to the host.
A10 - A0	I	8, 11, 12, 22, 23, 24, 25, 26, 27, 28, 29	These address lines along with the -REG signal are used to select the following: the I/O port registers within the SDP3B FlashDisk, the memory address mapped port registers within the SDP3B FlashDisk, a byte in the SDP3B FlashDisk's information structure and its configuration control and status registers. In True IDE Mode only, Host Address (HA) [2:0] is used to select one of eight registers in the Task File, the remaining address lines should be grounded.
-CE1, -CE2 Card Enable -CS0, -CS1 (True IDE Mode)	I	7,42	These signals are used both to select the SDP3B FlashDisk and to indicate to the SDP3B FlashDisk whether a byte or a word operation is being performed. -CE2 always accesses the odd byte of the word. -CE1 accesses the even byte or the Odd byte of the word depending on A0 and -CE2. A multi-plexing scheme based on A0, -CE1, -CE2 allows 8-bit hosts to access all data on D0-D7. See Tables 4-11, 4-13, 4-16 and 4-18. In True IDE Mode, -CS0 is the chip select for the task file registers while -CS1 is used to select the Alternate Status Register and the Device Control Register.
-CSEL	I	56	This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave.
-REG Attribute Memory Select	I	61	This signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory. The signal must also be active (low) during I/O Cycles when the I/O address is on the Bus. In True IDE Mode, this input signal is not used.

Table 4-2 Signal Description (continued)

Signal Name	Dir.	Pin	Description
WP (Memory) Write Protect -IOIS16 (I/O) I/O is 16-Bit	O	33	Memory Mode - The SDP3B FlashDisk does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence. I/O Operation - When the SDP3B FlashDisk is configured for I/O Operation, Pin 33 is used for the -I/O is 16-Bit Port (-IOIS16) function. A Low signal indicates that a 16-bit or odd byte only operation can be performed at the addressed port. In True IDE Mode, this output signal is asserted low when this device expects a word data transfer signal.
-INPACK (I/O) Input Acknowledge	O	60	The Input Acknowledge signal is asserted by the SDP3B FlashDisk when the SDP3B FlashDisk is selected and the SDP3B FlashDisk is responding to an I/O read cycle at the address which is on the address bus. This signal is used by the host to control the enable of any input data buffers between the SDP3B FlashDisk and the CPU. In True IDE Mode, this output signal is not used.
BVD1 (Memory) -STSCHG (I/O) Status Changed -PDIAG (True IDE Mode)	O I/O	63	Memory Mode - This signal is asserted high as the BVD1 signal since a battery is not used with this product. I/O Operation - This signal is asserted low to alert the host to changes in the RDY/-BSY and Write Protect states, while the I/O interface is configured. Its use is controlled by the Card Config and Status Register. In True IDE Mode, this input/output is the Pass Diagnostic signal in the Master/Slave handshake protocol.
-WAIT	O	59	The -WAIT signal is driven low by the SDP3B FlashDisk to signal the host to delay completion of the memory or I/O cycle which is in progress. In True IDE Mode, this output signal may be used as IORDY.
GND	--	1, 34, 35, 68	Ground.
VCC	--	17, 51	+5V or +3.3V power.
Reset -Reset (True IDE Mode)	I	58	When the pin is high, this signal Resets the SDP3B FlashDisk. The SDP3B FlashDisk is Reset only at power up if this pin is left high or open from power-up. The SDP3B FlashDisk is also Reset when the Soft Reset bit in the Card Configuration Option Register is set. In True IDE Mode, this input pin is the active low hardware reset from the host.
-VS1 -VS2	O	43 57	Voltage Sense Signals. -VS1 is grounded if the SDP3B FlashDisk CIS can be read at 3.3 volts and -VS2 is reserved by PCMCIA for a secondary voltage.
Vpp1, Vpp2	I	18, 52	Programming Voltage power supply is not connected on this SDP3B FlashDisk.

4.2.1 Electrical Specification

The following table defines all D.C. Characteristics for the SDP3B FlashDisk.

Unless otherwise stated, conditions are:

SDP3B	SDP3BI
Vcc = 5V ±10%	Vcc = 5V ± 5%
Vcc = 3.3V ± 5%	
Ta = 0°C to 60°C	Ta = -40°C to 85°C

Absolute Maximum Conditions:

Parameter	Symbol	Conditions
Input Power	Vcc	-0.3V min. to 7.0V max.
Voltage on any pin except Vcc with respect to GND.	V	-0.5V min. to Vcc + 0.5V max.

Input Leakage Current:

Type	Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
I-1	Input Leakage Current	IL	Vih = Vcc / Vil = Gnd	-1		1	µA
I-2	Pull Up Resistor	RPU1	Vcc = 5.0V	50k		500k	Ohm
I-3	Input Leakage Current	IL	Vih = Vcc / Vil = Gnd	-1		1	µA
I-4	Pull Up Resistor	RPU1	Vcc = 5.0V	50k		500k	Ohm

Input Characteristics:

Type	Parameter	Symbol	MIN	TYP	MAX	MIN	TYP	MAX	Units
			VCC = 3.3 V			VCC = 5.0 V			
I-1	Input Voltage CMOS	Vih Vil	2.4		0.6	4.0 [1]		0.8	Volts
I-2	Input Voltage CMOS	Vih Vil	1.5		0.6	2.0		0.8	Volts
I-3	Input Voltage CMOS Schmitt Trigger	Vth Vtl		1.8 1.0			2.8 2.0		Volts

Note 1: Per PCMCIA Electrical Specification Signal Interface Table 4-18 note 1, the host must provide a logic output high voltage for a CMOS load of .9 x VCC. For a 5 volt product, this translates to .9 x 4.5 = 4.05 volts minimum Voh.

Output Characteristics:

Type	Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
O-1	Output Voltage	Voh Vol	Ioh = -4 mA Iol = 4 mA	Vcc -0.8V		 Gnd +0.4V	Volts
O-2	Output Voltage	Voh Vol	Ioh = -8 mA Iol = 8 mA	Vcc -0.8V		 Gnd +0.4V	Volts
O-3	Output Voltage	Voh Vol	Ioh = -16 mA Iol = 16 mA	Vcc -0.8V		 Gnd +0.4V	Volts
O-X	Tri-State Leakage Current	Ioz	Vol = Gnd Voh = Vcc	-10		10	µA

4.2.2 *Interface/Bus Timing*

There are two types of bus cycles and timing sequences that occur in the PCMCIA type interface, a direct mapped I/O transfer and a memory access. The two timing sequences are explained in detail in the PCMCIA PC Card Standard Release 2.1. The SDP3B FlashDisk conforms to the timing in that reference document.

4.2.3 *Attribute Memory Read Timing Specification*

The Attribute Memory access time is defined as 300 ns. Detailed timing specifications are shown in Table 4-3.

Table 4-3 Attribute Memory Read Timing

Speed Version			300 ns	
Item	Symbol	IEEE Symbol	Min ns.	Max ns.
Read Cycle Time	tc(R)	tAVAV	300	
Address Access Time	ta(A)	tAVQV		300
Card Enable Access Time	ta(CE)	tELQV		300
Output Enable Access Time	ta(OE)	tGLQV		150
Output Disable Time from CE	tdis(CE)	tEHQZ		100
Output Disable Time from OE	tdis(OE)	tGHQZ		100
Address Setup Time	tsu (A)	tAVWL	30	
Output Enable Time from CE	ten(CE)	tELQNZ	5	
Output Enable Time from OE	ten(OE)	tGLQNZ	5	
Data Valid from Address Change	tv(A)	tAXQX	0	

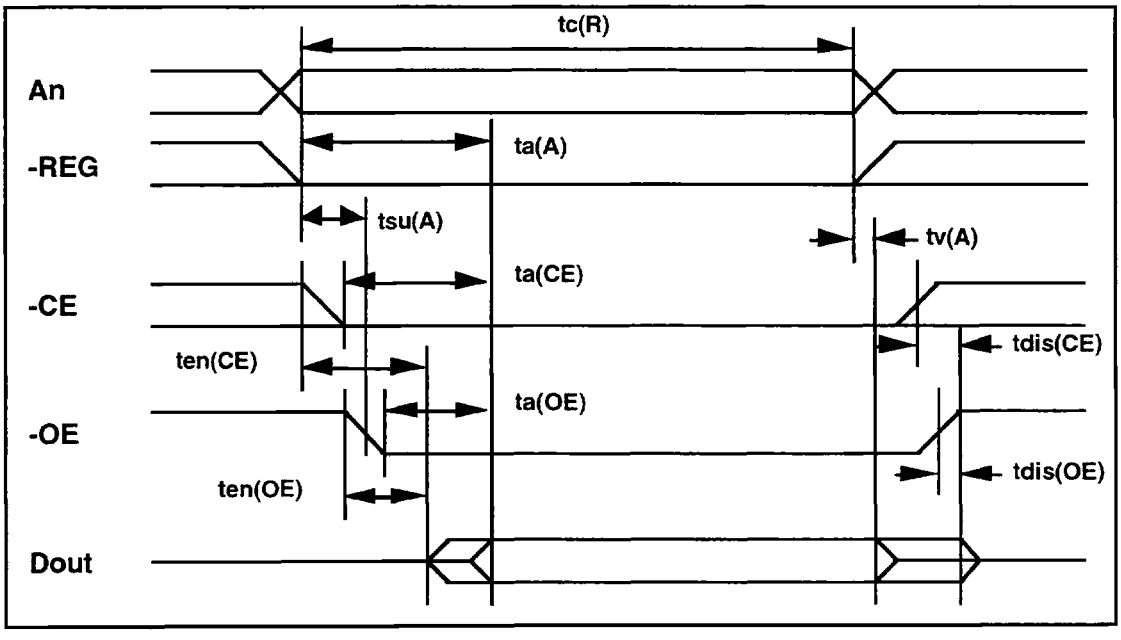

Figure 4-1 Attribute Memory Read Timing Diagram

Notes: All times are in nanoseconds. Dout signifies data provided by the SDP3B FlashDisk to the system. The -CE signal or both the -OE signal and the -WE signal must be de-asserted between consecutive cycle operations.

4.2.4 *Attribute Memory Write Timing Specification*

The Card Configuration write access time is defined as 250 ns. Detailed timing specifications are shown in Table 4-4.

Note: SanDisk does not allow writing from the Host to CIS Memory. Only writes to the Configuration register are allowed.

Table 4-4 Attribute Memory Write Timing

Speed Version			250 ns	
Item	Symbol	IEEE Symbol	Min ns	Max ns
Write Cycle Time	tc(W)	tAVAV	250	
Write Pulse Width	tw(WE)	tWLWH	150	
Address Setup Time	tsu(A)	tAVWL	30	
Write Recovery Time	trec(WE)	tWMAX	30	
Data Setup Time for WE	tsu(D-WEH)	tDVWH	80	
Data Hold Time	th(D)	tWMDX	30	

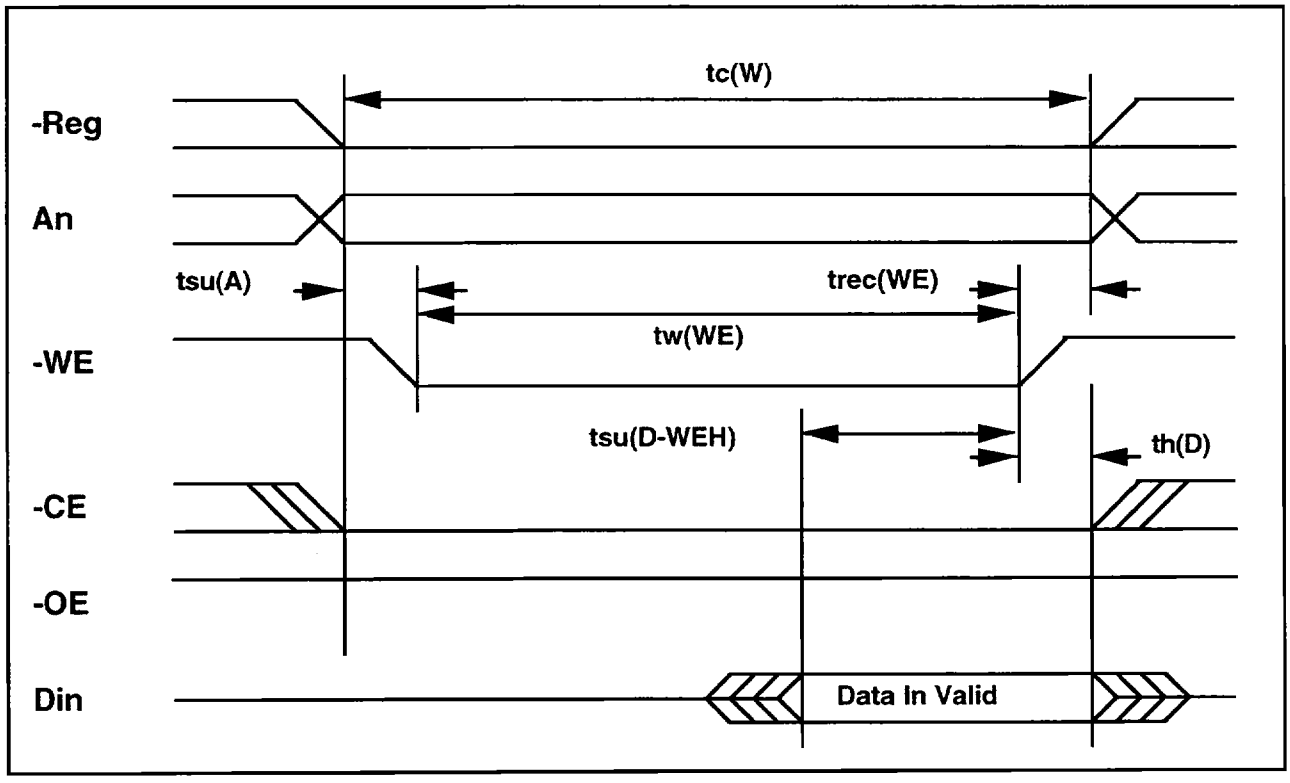

Figure 4-2 Attribute Memory Write Timing Diagram

Notes: All times are in nanoseconds. Din signifies data provided by the system to the SDP3B FlashDisk.

4.2.5 *Common Memory Read Timing Specification*

Table 4-5 Common Memory Read Timing

Item	Symbol	IEEE Symbol	Min ns.	Max ns.
Output Enable Access Time	ta(OE)	tGLQV		125
Output Disable Time from OE	tdis(OE)	tGHQZ		100
Address Setup Time	tsu(A)	tAVGL	30	
Address Hold Time	th(A)	tGHAX	20	
CE Setup before OE	tsu(CE)	tELGL	0	
CE Hold following OE	th(CE)	tGHEH	20	
Wait Delay Falling from OE	tv(WT-OE)	tGLWTV		35
Data Setup for Wait Release	tv(WT)	tQVWTH		0
Wait Width Time (Default Speed)	tw(WT)	tWTLWTH		350

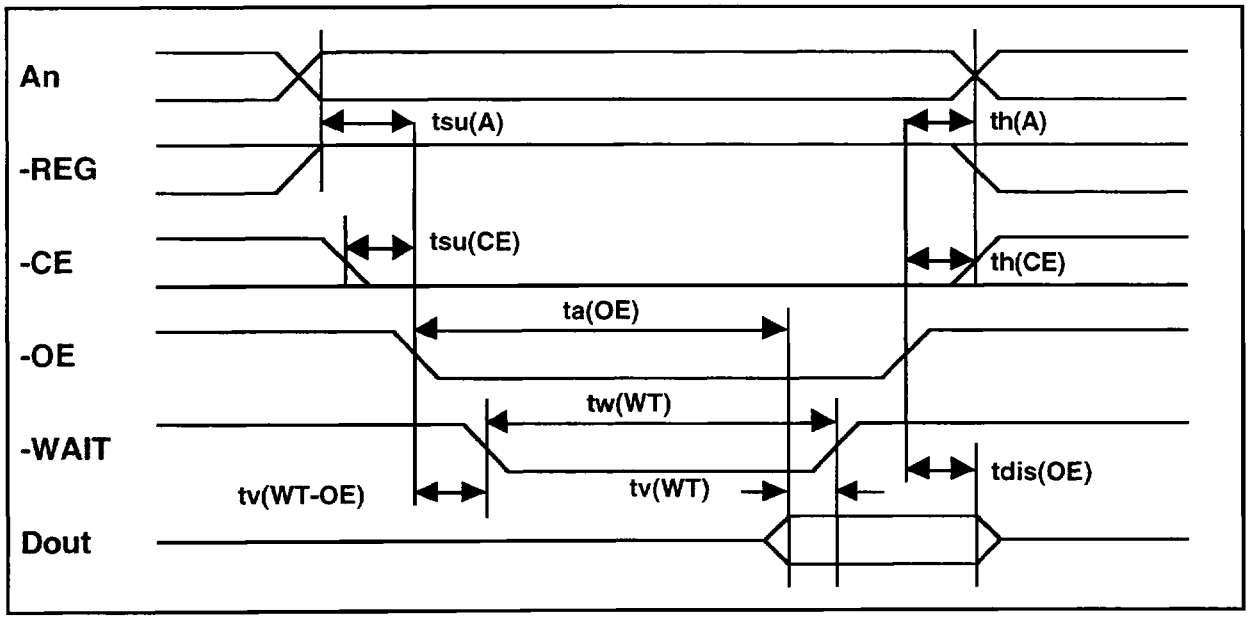

Figure 4-3 Common Memory Read Timing Diagram

Notes: The maximum load on -WAIT is 1 LSTTL with 50pF total load. All times are in nanoseconds.
Dout signifies data provided by the SDP3B FlashDisk to the system.
The -WAIT signal may be ignored if the -OE cycle to cycle time is greater than the Wait Width time.
The Max Wait Width time (in the slowest mode) can be determined from the Card Information Structure.

4.2.6 *Common Memory Write Timing Specification*

Table 4-6 Common Memory Write Timing

Item	Symbol	IEEE Symbol	Min ns.	Max ns.
Data Setup before WE	tsu(D-WEH)	tDVWH	80	
Data Hold following WE	th(D)	tlWMDX	30	
WE Pulse Width	tw(WE)	tWLWH	150	
Address Setup Time	tsu(A)	tAVWL	30	
CE Setup before WE	tsu(CE)	tELWL	0	
Write Recovery Time	trec(WE)	tWMAX	30	
Address Hold Time	th(A)	tGHAX	20	
CE Hold following WE	th(CE)	tGHEH	20	
Wait Delay Falling from WE	tv(WT-WE)	tWLWTV		35
WE High from Wait Release	tv(WT)	tWTHWH	0	
Wait Width Time (Default Speed)	tw (WT)	tWTLWTH		350

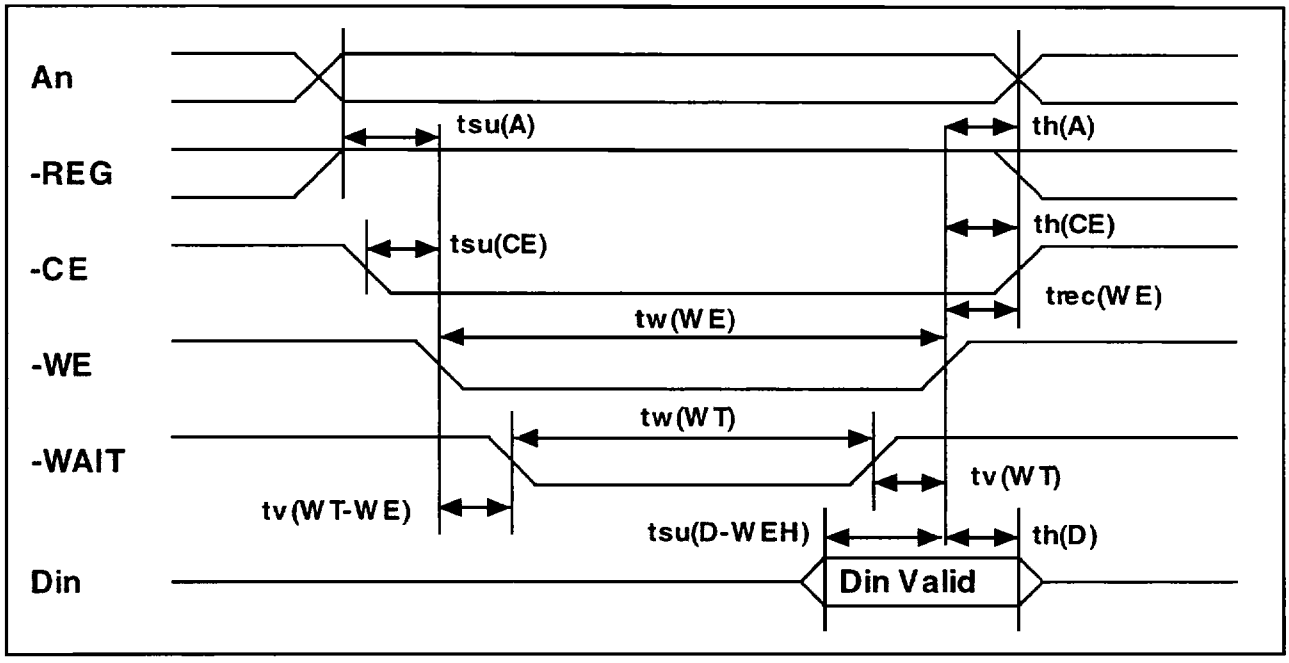

Figure 4-4 Common Memory Write Timing Diagram

Notes: The maximum load on -WAIT is 1 LSTTL with 50pF total load. All times are in nanoseconds.
Din signifies data provided by the system to the SDP3B FlashDisk.
The -WAIT signal may be ignored if the -WE cycle to cycle time is greater than the Wait Width time.
The Max Wait Width time (in the slowest mode) can be determined from the Card Information Structure.

4.2.7 I/O Input (Read) Timing Specification

Table 4-7 I/O Read Timing

Item	Symbol	IEEE Symbol	Min ns.	Max ns.
Data Delay after IORD	td(IORD)	tIGLQV		100
Data Hold following IORD	th(IORD)	tIGHQX	0	
IORD Width Time	tw(IORD)	tIGLIGH	165	
Address Setup before IORD	tsuA(IORD)	tAVIGL	70	
Address Hold following IORD	thA(IORD)	tIGHAX	20	
CE Setup before IORD	tsuCE(IORD)	tELIGL	5	
CE Hold following IORD	thCE(IORD)	tIGHEH	20	
REG Setup before IORD	tsuREG(IORD)	tRGLIGL	5	
REG Hold following IORD	thREG(IORD)	tIGHRGH	0	
INPACK Delay Falling from IORD	tdfINPACK(IORD)	tIGLIAL	0	45
INPACK Delay Rising from IORD	tdrINPACK(IORD)	tIGHIAH		45
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		35
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH		35
Wait Delay Falling from IORD	tdWT(IORD)	tIGLWTL		35
Data Delay from Wait Rising	td(WT)	tWTHQV		0
Wait Width Time (Default Speed)	tw(WT)	tWTLWTH		350

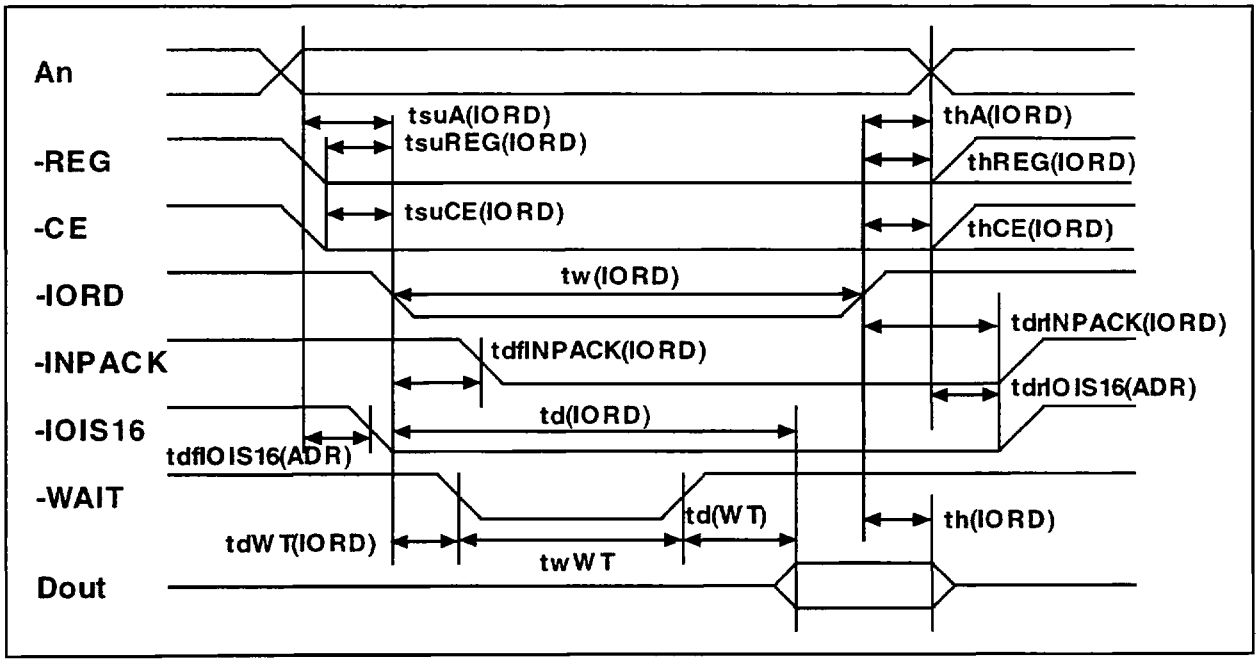

Figure 4-5 I/O Read Timing Diagram

Notes: The maximum load on -WAIT, -INPACK and -IOIS16 is 1 LSTTL with 50pF total load. All times are in nanoseconds.
Minimum time from -WAIT high to -IORD high is 0 nsec, but minimum -IORD width must still be met.
Dout signifies data provided by the SDP3B FlashDisk to the system.

4.2.8 I/O Output (Write) Timing Specification

Table 4-8 I/O Write Timing

Item	Symbol	IEEE Symbol	Min ns.	Max ns.
Data Setup before IOWR	tsu(IOWR)	tDVIWH	60	
Data Hold following IOWR	th(IOWR)	tIWHDX	30	
IOWR Width Time	twIOWR	tIWLIWH	165	
Address Setup before IOWR	tsuA(IOWR)	tAVIWL	70	
Address Hold following IOWR	thA(IOWR)	tIWHAX	20	
CE Setup before IOWR	tsuCE(IOWR)	tELIWL	5	
CE Hold following IOWR	thCE(IOWR)	tIWHEH	20	
REG Setup before IOWR	tsuREG(IOWR)	tRGLIWL	5	
REG Hold following IOWR	thREG(IOWR)	tIWHRGH	0	
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		35
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH		35
Wait Delay Falling from IOWR	tdWT(IOWR)	tIWLWTL		35
IOWR high from Wait high	tdrIOWR(WT)	tWTJIWH	0	
Wait Width Time (Default Speed) (Set Feature Speed <68 mA.)	tw(WT)	tWTLWTH		350 700

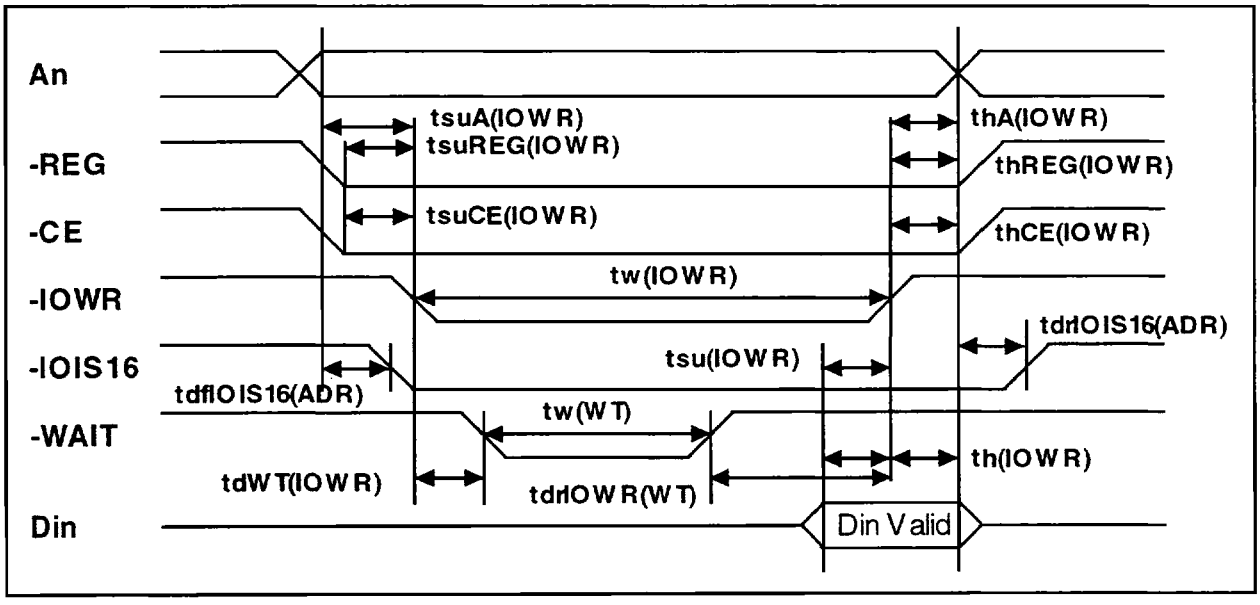

Figure 4-6 I/O Write Timing Diagram

Notes: The maximum load on -WAIT, -INPACK, and -IOIS16 is 1 LSTTL with 50pF total load. All times are in nanoseconds.
Minimum time from -WAIT high to -IOWR high is 0 nsec, but minimum -IOWR width must still be met.
Din signifies data provided by the system to the SDP3B FlashDisk.

4.2.9 *True IDE Mode I/O Input (Read) Timing Specification*

Table 4-9 True IDE Mode I/O Read Timing

Item	Symbol	IEEE Symbol	Min ns.	Max ns.
Data Delay after IORD	td(IORD)	tIGLQV		100
Data Hold following IORD	th(IORD)	tIGHQX	0	
IORD Width Time	tw(IORD)	tIGLIGH	165	
Address Setup before IORD	tsuA(IORD)	tAVIGL	70	
Address Hold following IORD	thA(IORD)	tIGHAX	20	
CE Setup before IORD	tsuCE(IORD)	tELIGL	5	
CE Hold following IORD	thCE(IORD)	tIGHEH	20	
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		35
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH		35

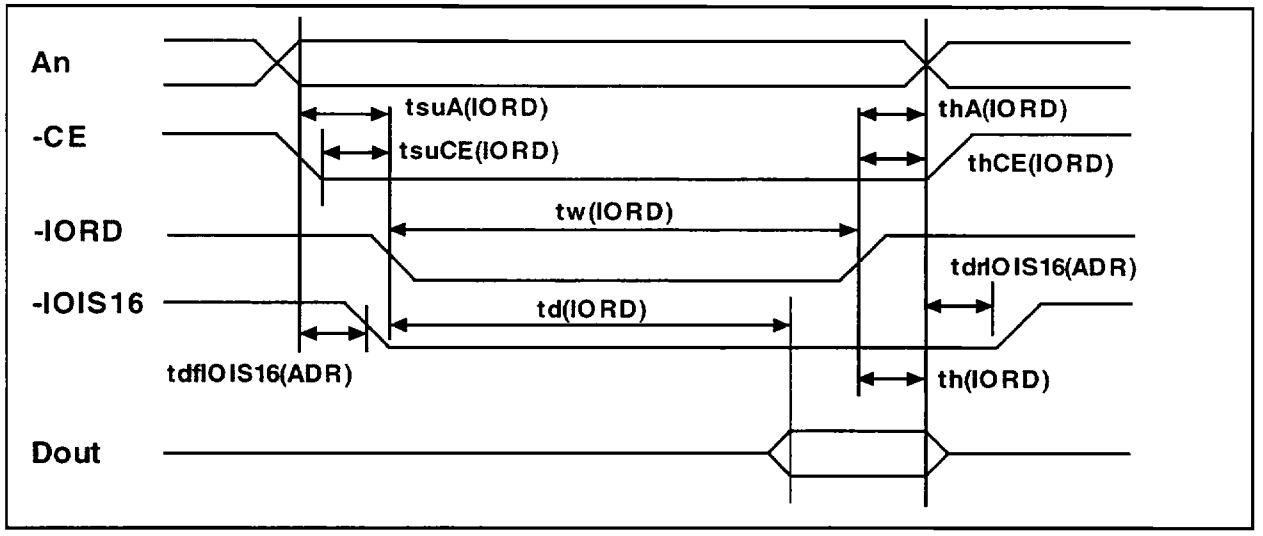

Figure 4-7 True IDE Mode I/O Read Timing Diagram

Notes: The maximum load on -IOIS16 is 1 LSTTL with 50pF total load. All times are in nanoseconds.
Minimum time from -WAIT high to -IORD high is 0 nsec, but minimum -IORD width must still be met.
Dout signifies data provided by the SDP3B FlashDisk to the system.

4.2.10 *True IDE Mode I/O Output (Write) Timing Specification*

Table 4-10 True IDE Mode I/O Write Timing

Item	Symbol	IEEE Symbol	Min ns.	Max ns.
Data Setup before IOWR	tsu(IOWR)	tDVIWH	60	
Data Hold following IOWR	th(IOWR)	tIWHDX	30	
IOWR Width Time	tw(IOWR)	tIWLIWH	165	
Address Setup before IOWR	tsuA(IOWR)	tAVIWL	70	
Address Hold following IOWR	thA(IOWR)	tIWHAX	20	
CE Setup before IOWR	tsuCE(IOWR)	tELIWL	5	
CE Hold following IOWR	thCE(IOWR)	tIWHEH	20	
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		35
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH		35

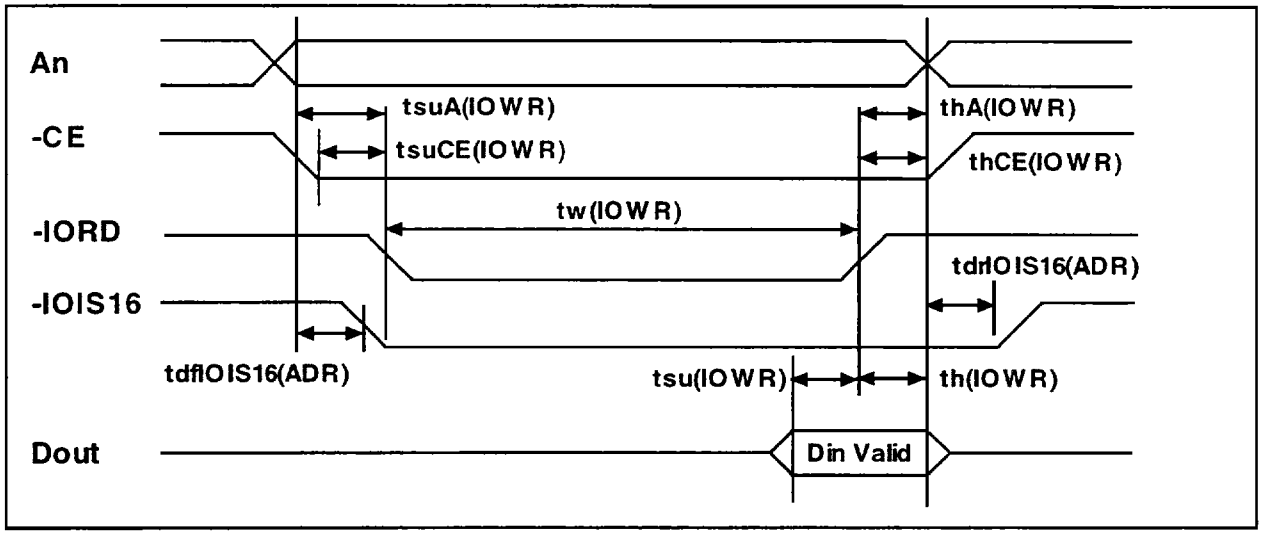

Figure 4-8 True IDE Mode I/O Write Timing Diagram

Notes: The maximum load on -IOIS16 is 1 LSTTL with 50pF total load. All times are in nanoseconds.
Minimum time from -WAIT high to -IOWR high is 0 nsec, but minimum -IOWR width must still be met.
Din signifies data provided by the system to the SDP3B FlashDisk.

4.3 *Card Configuration*

The SDP3B FlashDisks are identified by appropriate information in the Card Information Structure (CIS). The following configuration registers are used to coordinate the I/O spaces and the Interrupt level of cards that are located in the system. In addition, these registers provide a method for accessing status information about the SDP3B FlashDisk that may be used to arbitrate between multiple interrupt sources on the same interrupt level or to replace status information that appears on dedicated pins in memory cards that have alternate use in I/O cards.

Table 4-11 Registers and Memory Space Decoding

-CE2	-CE1	-REG	-OE	-WE	A10	A9	A8-A4	A3	A2	A1	A0	SELECTED SPACE
1	1	X	X	X	X	X	XX	X	X	X	X	Standby
X	0	0	0	1	X	1	XX	X	X	X	0	Configuration Registers Read
1	0	1	0	1	X	X	XX	X	X	X	X	Common Memory Read (8 Bit D7-D0)
0	1	1	0	1	X	X	XX	X	X	X	X	Common Memory Read (8 Bit D15-D8)
0	0	1	0	1	X	X	XX	X	X	X	0	Common Memory Read (16 Bit D15-D0)
X	0	0	1	0	X	1	XX	X	X	X	0	Configuration Registers Write
1	0	1	1	0	X	X	XX	X	X	X	X	Common Memory Write (8 Bit D7-D0)
0	1	1	1	0	X	X	XX	X	X	X	X	Common Memory Write (8 Bit D15-D8)
0	0	1	1	0	X	X	XX	X	X	X	0	Common Memory Write (16 Bit D15-D0)
X	0	0	0	1	0	0	XX	X	X	X	0	Card Information Structure Read
1	0	0	1	0	0	0	XX	X	X	X	0	Invalid Access (CIS Write)
1	0	0	0	1	X	X	XX	X	X	X	1	Invalid Access (Odd Attribute Read)
1	0	0	1	0	X	X	XX	X	X	X	1	Invalid Access (Odd Attribute Write)
0	1	0	0	1	X	X	XX	X	X	X	X	Invalid Access (Odd Attribute Read)
0	1	0	1	0	X	X	XX	X	X	X	X	Invalid Access (Odd Attribute Write)

Configuration Registers Decoding

-CE2	-CE1	-REG	-OE	-WE	A10	A9	A8-A4	A3	A2	A1	A0	SELECTED REGISTER
X	0	0	0	1	0	1	00	0	0	0	0	Configuration Option Reg Read
X	0	0	1	0	0	1	00	0	0	0	0	Configuration Option Reg Write
X	0	0	0	1	0	1	00	0	0	1	0	Card Status Register Read
X	0	0	1	0	0	1	00	0	0	1	0	Card Status Register Write
X	0	0	0	1	0	1	00	0	1	0	0	Pin Replacement Register Read
X	0	0	1	0	0	1	00	0	1	0	0	Pin Replacement Register Write
X	0	0	0	1	0	1	00	0	1	1	0	Socket and Copy Register Read
X	0	0	1	0	0	1	00	0	1	1	0	Socket and Copy Register Write

Note: The location of the card configuration registers should always be read from the CIS since these locations may vary in future products. No writes should be performed to the SDP3B FlashDisk attribute memory except to the card configuration register addresses. All other attribute memory locations are reserved.

4.3.1 Attribute Memory Function

Attribute memory is a space where SDP3B FlashDisk identification and configuration information is stored, and is limited to 8-bit wide accesses only at even addresses. The card configuration registers are also located here.

For the Attribute Memory Read function, signals -REG and -OE must be active and -WE inactive during the cycle. As in the Main Memory Read functions, the signals -CE1 and -CE2 control the even-byte and odd-byte address, but only the even-byte data is valid during the Attribute Memory access. Refer to Table 4-12 below for signal states and bus validity for the Attribute Memory function.

Table 4-12 Attribute Memory Function

Function Mode	-REG	-CE2	-CE1	A9	A0	-OE	-WE	D15-D8	D7-D0
Standby Mode	X	H	H	X	X	X	X	High Z	High Z
Read Byte Access CIS ROM (8 bits)	L	H	L	L	L	L	H	High Z	Even Byte
Write Byte Access CIS (8 bits) (Invalid)	L	H	L	L	L	H	L	Don't Care	Even Byte
Read Byte Access Configuration (8 bits)	L	H	L	H	L	L	H	High Z	Even Byte
Write Byte Access Configuration (8 bits)	L	H	L	H	L	H	L	Don't Care	Even Byte
Read Word Access CIS (16 bits)	L	L	L	L	X	L	H	Not Valid	Even Byte
Write Word Access CIS (16 bits) (Invalid)	L	L	L	L	X	H	L	Don't Care	Even Byte
Read Word Access Configuration (16 bits)	L	L	L	H	X	L	H	Not Valid	Even Byte
Write Word Access Configuration (16 bits)	L	L	L	H	X	H	L	Don't Care	Even Byte

Note: The -CE signal or both the -OE signal and the -WE signal must be de-asserted between consecutive cycle operations.

4.3.2 *Configuration Option Register (Address 200h in Attribute Memory)*

The Configuration Option Register is used to configure the cards interface, address decoding and interrupt and to issue a soft reset to the SDP3B FlashDisk.

Operation	D7	D6	D5	D4	D3	D2	D1	D0
R/W	SRESET	LevIREQ	Conf5	Conf4	Conf3	Conf2	Conf1	Conf0

SRESET Soft Reset - Setting this bit to one (1), waiting the minimum reset width time and returning to zero (0) places the SDP3B FlashDisk in the Reset state. Setting this bit to one (1) is equivalent to assertion of the +RESET signal except that the SRESET bit is not cleared. Returning this bit to zero (0) leaves the SDP3B FlashDisk in the same un-configured, Reset state as following power-up and hardware reset. This bit is set to zero (0) by power-up and hardware reset. Using the PCMCIA Soft Reset is considered a hard Reset by the ATA Commands. Contrast with Soft Reset in the Device Control Register.

LevIREQ This bit is set to one (1) when Level Mode Interrupt is selected, and zero (0) when Pulse Mode is selected. Set to zero (0) by Reset.

Conf5 - Conf0 Configuration Index. Set to zero (0) by reset. It's used to select operation mode of the SDP3B FlashDisk as shown below.

Note: Conf5 and Conf4 are reserved and must be written as zero (0).

Table 4-13 Card Configurations

Conf5	Conf4	Conf3	Conf2	Conf1	Conf0	Disk Card Mode
0	0	0	0	0	0	Memory Mapped
0	0	0	0	0	1	I/O Mapped, Any 16 byte system decoded boundary
0	0	0	0	1	0	I/O Mapped, 1F0-1F7/3F6-3F7
0	0	0	0	1	1	I/O Mapped, 170-177/376-377

4.3.3 *Card Configuration and Status Register (Address 202h in Attribute Memory)*

The Card Configuration and Status Register contains information about the Card's condition.

Card Configuration and Status Register Organization:

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	Changed	SigChg	IOis8	0	0	PwrDwn	Int	0
Write	0	SigChg	IOis8	0	0	PwrDwn	0	0

Changed Indicates that one or both of the Pin Replacement register CRdy, or CWProt bits are set to one (1). When the Changed bit is set, -STSCHG Pin 46 is held low if the SigChg bit is a One (1) and the SDP3B FlashDisk is configured for the I/O interface.

SigChg This bit is set and reset by the host to enable and disable a state-change "signal" from the Status Register, the Changed bit control pin 46 the Changed Status signal. If no state change signal is desired, this bit should be set to zero (0) and pin 46 (-STSCHG) signal will be held high while the SDP3B FlashDisk is configured for I/O.

IOis8 The host sets this bit to a one (1) if the SDP3B FlashDisk is to be configured in an 8 bit I/O mode. The SDP3B FlashDisk is always configured for both 8- and 16-bit I/O, so this bit is ignored.

PwrDwn This bit indicates whether the host requests the SDP3B FlashDisk to be in the power saving or active mode. When the bit is one (1), the SDP3B FlashDisk enters a power down mode. When zero (0), the host is requesting the SDP3B FlashDisk to enter the active mode. The PCMCIA Rdy/-Bsy value becomes BUSY when this bit is changed. Rdy/-Bsy will not become Ready until the power state requested has been entered. The SDP3B FlashDisk automatically powers down when it is idle and powers back up when it receives a command.

Int This bit represents the internal state of the interrupt request. This value is available whether or not I/O interface has been configured. This signal remains true until the condition which caused the interrupt request has been serviced. If interrupts are disabled by the -IEN bit in the Device Control Register, this bit is a zero (0).

4.3.4 Pin Replacement Register (Address 204h in Attribute Memory)

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	0	0	CRdy/-Bsy	CWProt	1	1	Rdy/-Bsy	WProt
Write	0	0	CRdy/-Bsy	CWProt	0	0	MRdy/-Bsy	MWProt

CRdy/-Bsy This bit is set to one (1) when the bit RRdy/-Bsy changes state. This bit can also be written by the host.

CWProt This bit is set to one (1) when the RWprot changes state. This bit may also be written by the host.

Rdy/-Bsy This bit is used to determine the internal state of the Rdy/-Bsy signal. This bit may be used to determine the state of the Ready/-Busy as this pin has been reallocated for use as Interrupt Request on an I/O card. When written, this bit acts as a mask for writing the corresponding bit CRdy/-Bsy.

WProt This bit is always zero (0) since the SDP3B FlashDisk does not have a Write Protect switch. When written, this bit acts as a mask for writing the corresponding bit CWProt.

MRdy/-Bsy This bit acts as a mask for writing the corresponding bit CRdy/-Bsy.

MWProt This bit when written acts as a mask for writing the corresponding bit CWProt.

Table 4-14 Pin Replacement Changed Bit/Mask Bit Values

Initial Value of (C) Status	Written by Host		Final	Comments
	"C" Bit	"M" Bit	"C" Bit	
0	X	0	0	Unchanged
1	X	0	1	Unchanged
X	0	1	0	Cleared by Host
X	1	1	1	Set by Host

4.3.5 Socket and Copy Register (Address 206h in Attribute Memory)

This register contains additional configuration information. This register is always written by the system before writing the card's Configuration Index Register.

Socket and Copy Register Organization:

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	Reserved	0	0	Drive #	0	0	0	0
Write	0	0	0	Drive # (0)	X	X	X	X

Reserved This bit is reserved for future standardization. This bit must be set to zero (0) by the software when the register is written.

Drive # This bit indicates the drive number of the card if twin card configuration is supported.

X The socket number is ignored by the SDP3B FlashDisk.

4.4 I/O Transfer Function

4.4.1 I/O Function

The I/O transfer to or from the SDP3B FlashDisk can be either 8 or 16 bits. When a 16-bit accessible port is addressed, the signal -IOIS16 is asserted by the SDP3B FlashDisk. Otherwise, the -IOIS16 signal is de-asserted. When a 16 bit transfer is attempted, and the -IOIS16 signal is not asserted by the SDP3B FlashDisk, the system must generate a pair of 8-bit references to access the word's even byte and odd byte. The SDP3B FlashDisk permits both 8- and 16-bit accesses to all of its I/O addresses, so -IOIS16 is asserted for all addresses to which the SDP3B FlashDisk responds.

The SDP3B FlashDisk may request the host to extend the length of an input cycle until data is ready by asserting the -WAIT signal at the start of the cycle.

Table 4-15 I/O Function

Function Code	-REG	-CE2	-CE1	A0	-IORD	-IOWR	D15-D8	D7-D0
Standby Mode	X	H	H	X	X	X	High Z	High Z
Byte Input Access (8 bits)	L L	H H	L L	L H	L L	H H	High Z High Z	Even-Byte Odd-Byte
Byte Output Access (8 bits)	L L	H H	L L	L H	H H	L L	Don't Care Don't Care	Even-Byte Odd-Byte
Word Input Access (16 bits)	L	L	L	L	L	H	Odd-Byte	Even-Byte
Word Output Access (16 bits)	L	L	L	L	H	L	Odd-Byte	Even-Byte
I/O Read Inhibit	H	X	X	X	L	H	Don't Care	Don't Care
I/O Write Inhibit	H	X	X	X	H	L	High Z	High Z
High Byte Input Only (8 bits)	L	L	H	X	L	H	Odd-Byte	High Z
High Byte Output Only (8 bits)	L	L	H	X	H	L	Odd-Byte	Don't Care

4.5 Common Memory Transfer Function

4.5.1 Common Memory Function

The Common Memory transfer to or from the SDP3B FlashDisk can be either 8 or 16 bits.

The SDP3B FlashDisk permits both 8 and 16 bit accesses to all of its Common Memory addresses.

The SDP3B FlashDisk may request the host to extend the length of a memory write cycle or extend the length of a memory read cycle until data is ready by asserting the -WAIT signal at the start of the cycle.

Table 4-16 Common Memory Function

Function Code	-REG	-CE2	-CE1	A0	-OE	-WE	D15-D8	D7-D0
Standby Mode	X	H	H	X	X	X	High Z	High Z
Byte ReadAccess (8 bits)	H H	H H	L L	L H	L L	H H	High Z High Z	Even-Byte Odd-Byte
Byte Write Access (8 bits)	H H	H H	L L	L H	H H	L L	Don't Care Don't Care	Even-Byte Odd-Byte
Word Read Access (16 bits)	H	L	L	X	L	H	Odd-Byte	Even-Byte
Word Write Access (16 bits)	H	L	L	X	H	L	Odd-Byte	Even-Byte
Odd Byte Read Only (8 bits)	H	L	H	X	L	H	Odd-Byte	High Z
Odd Byte Write Only (8 bits)	H	L	H	X	H	L	Odd-Byte	Don't Care

4.6 *True IDE Mode I/O Transfer Function*

4.6.1 True IDE Mode I/O Function

The SDP3B FlashDisk can be configured in a True IDE Mode of operation. This SDP3B FlashDisk is configured in this mode only when the -OE input signal is grounded by the host. In this True IDE Mode, the PCMCIA protocol and configuration are disabled and only I/O operations to the Task File and Data Register are allowed. In this mode, no Memory or Attribute Registers are accessible to the host. SDP3B FlashDisks permit 8 bit data accesses if the user issues a Set Feature Command to put the device in 8 bit Mode.

Note: Removing and reinserting the SDP3B FlashDisk while the host computer's power is on will reconfigure the SDP3B FlashDisk to PC Card ATA mode from the original True IDE Mode. To configure the SDP3B FlashDisk in True IDE Mode, the 68-pin socket must be power cycled with the SDP3B FlashDisk inserted and -OE (output enable) grounded by the host.

The following table defines the function of the operations for the True IDE Mode.

Table 4-17 IDE Mode I/O Function

Function Code	-CE2	-CE1	A0	-IORD	-IOWR	D15-D8	D7-D0
Invalid Mode	L	L	X	X	X	High Z	High Z
Standby Mode	H	H	X	X	X	High Z	High Z
Task File Write	H	L	1-7h	H	L	Don't Care	Data In
Task File Read	H	L	1-7h	L	H	High Z	Data Out
Data Register Write	H	L	0	H	L	Odd-Byte In	Even-Byte In
Data Register Read	H	L	0	L	H	Odd-Byte Out	Even-Byte Out
Control Register Write	L	H	6h	H	L	Don't Care	Control In
Alt Status Read	L	H	6h	L	H	High Z	Status Out