4.0 Double Density Flash Series Interface Description

4.1 Physical Description

The host is connected to the Double Density Flash Series FlashDisk using a standard 68 pin PCMCIA connector consisting of two rows of 34 female contacts each on 50 mil (1.27 mm) centers.

The host is connected to the Double Density Flash Series CompactFlash Storage Card using a standard 50 pin connector consisting of two rows of female contacts each on 50 mil (1.27 mm) centers.

4.1.1 Pin Assignments and Pin Type

The signal/pin assignments are listed in Tables 4-1 and 4-2. Low active signals have a "-" prefix. Pin types are Input, Output or Input/Output. Table 4-3 defines the DC characteristics for all input and output type structures.

4.2 Electrical Description

The Double Density Flash Series is optimized for operation with hosts which support the PCMCIA I/O interface standard conforming to the PC Card ATA specification. However, the Double Density Flash Series may also be configured to operate in systems that support only the memory interface standard. The configuration of the Double Density Flash Series product will be controlled using the standard PCMCIA configuration registers starting at address 200h in the Attribute Memory space of the Double Density product.

Table 4-3 describes the I/O signals. Signals whose source is the host are designated as inputs while signals that the Double Density Flash Series product sources are outputs. The Double Density Flash Series logic levels conform to those specified in the PCMCIA Release 2.1 specification. All outputs from the card are totempole except the data bus signals which are bi-directional tri-state. Refer to section 4.3 for definitions of Input and Output type.

Table 4-1 Double Density Flash Series FlashDisk Pin Assignments and Pin Type

PC Card Memory Mode				PC Card I/O Mode				True IDE Mode			
Pin Num	Signal Name	Pin Type	In, Out Type	Pin Num	Signal Name	Pin Type	In, Out Type	Pin Num	Signal Name	Pin Type	In, Out Type
1	GND		Ground	1	GND		Ground	1	GND		Ground
2	D03	I/O	I1Z,OZ3	2	D03	I/O	I1Z,OZ3	2	D03	I/O	I1Z,OZ3
3	D04	I/O	I1Z,OZ3	3	D04	I/O	I1Z,OZ3	3	D04	I/O	I1Z,OZ3
4	D05	I/O	I1Z,OZ3	4	D05	I/O	I1Z,OZ3	4	D05	I/O	I1Z,OZ3
5	D06	I/O	I1Z,OZ3	5	D06	I/O	I1Z,OZ3	5	D06	I/O	I1Z,OZ3
6	D07	I/O	I1Z,OZ3	6	D07	I/O	I1Z,OZ3	6	D07	I/O	I1Z,OZ3
7	-CE1	I	I3U	7	-CE1	I	I3U	7	-CS0	I	I3Z
8	A10	I	I1Z	8	A10	I	I1Z	8	A10[2]	I	I1Z
9	-OE	I	I3U	9	-OE	I	I3U	9	-ATA SEL	I	I3U
10				10				10			
11	A09	I	I1Z	11	A09	I	I1Z	11	A09[2]	I	I1Z
12	A08	I	I1Z	12	A08	I	I1Z	12	A08[2]	I	I1Z
13				13				13			
14				14				14			
15	-WE	I	I3U	15	-WE	I	I3U	15	-WE[3]	I	I3U
16	RDY/BSY	O	OT1	16	IREQ	O	OT1	16	INTRQ	O	OZ1
17	VCC		Power	17	VCC		Power	17	VCC		Power
18	VPP		(Not Used)	18	VPP		(Not Used)	18	VPP		(Not Used)
19				19				19			
20				20				20			
21				21				21			
22	A07	I	I1Z	22	A07	I	I1Z	22	A07[2]	I	I1Z
23	A06	I	I1Z	23	A06	I	I1Z	23	A06[2]	I	I1Z
24	A05	I	I1Z	24	A05	I	I1Z	24	A05[2]	I	I1Z
25	A04	I	I1Z	25	A04	I	I1Z	25	A04[2]	I	I1Z
26	A03	I	I1Z	26	A03	I	I1Z	26	A03[2]	I	I1Z
27	A02	I	I1Z	27	A02	I	I1Z	27	A02	I	I1Z
28	A01	I	I1Z	28	A01	I	I1Z	28	A01	I	I1Z
29	A00	I	I1Z	29	A00	I	I1Z	29	A00	I	I1Z
30	D00	I/O	I1Z,OZ3	30	D00	I/O	I1Z,OZ3	30	D00	I/O	I1Z,OZ3
31	D01	I/O	I1Z,OZ3	31	D01	I/O	I1Z,OZ3	31	D01	I/O	I1Z,OZ3
32	D02	I/O	I1Z,OZ3	32	D02	I/O	I1Z,OZ3	32	D02	I/O	I1Z,OZ3
33	WP	O	OT3	33	-IOIS16	O	OT3	33	-IOCS16	O	ON3
34	GND		Ground	34	GND		Ground	34	GND		Ground
35	GND		Ground	35	GND		Ground	35	GND		Ground
36	-CD1	O	Ground	36	-CD1	O	Ground	36	-CD1	O	Ground
37	D11[1]	I/O	I1Z,OZ3	37	D11[1]	I/O	I1Z,OZ3	37	D11[1]	I/O	I1Z,OZ3
38	D12[1]	I/O	I1Z,OZ3	38	D12[1]	I/O	I1Z,OZ3	38	D12[1]	I/O	I1Z,OZ3
39	D13[1]	I/O	I1Z,OZ3	39	D13[1]	I/O	I1Z,OZ3	39	D13[1]	I/O	I1Z,OZ3
40	D14[1]	I/O	I1Z,OZ3	40	D14[1]	I/O	I1Z,OZ3	40	D14[1]	I/O	I1Z,OZ3
41	D15[1]	I/O	I1Z,OZ3	41	D15[1]	I/O	I1Z,OZ3	41	D15[1]	I/O	I1Z,OZ3

Table 4-1 Double Density Flash Series FlashDisk Pin Assignments and Pin Type (continued)

PC Card Memory Mode				PC Card I/O Mode				True IDE Mode			
Pin Num	Signal Name	Pin Type	In, Out Type	Pin Num	Signal Name	Pin Type	In, Out Type	Pin Num	Signal Name	Pin Type	In, Out Type
42	-CE2[1]	I	I3U	42	-CE2[1]	I	I3U	42	-CS1[1]	I	I1Z
43	-VS1	O	Ground	43	-VS1	O	Ground	43	-VS1	O	Ground
44	-IORD	I	I3U	44	-IORD	I	I3U	44	-IORD	I	I3Z
45	-IOWR	I	I3U	45	-IOWR	I	I3U	45	-IOWR	I	I3Z
46				46				46			
47				47				47			
48				48				48			
49				49				49			
50				50				50			
51	VCC		Power	51	VCC		Power	51	VCC		Power
52	VPP		(Not Used)	52	VPP		(Not Used)	52	VPP		(Not Used)
53				53				53			
54				54				54			
55				55				55			
56	-CSEL	I	I2Z	56	-CSEL	I	I2Z	56	-CSEL	I	I2U
57	-VS2	O	OPEN	57	-VS2	O	OPEN	57	-VS2	O	OPEN
58	RESET	I	I2Z	58	RESET	I	I2Z	58	-RESET	I	I2Z
59	-WAIT	O	OT1	59	-WAIT	O	OT1	59	IORDY	O	ON1
60	-INPACK	O	OT1	60	-INPACK	O	OT1	60	-INPACK	O	OZ1
61	-REG	I	I3U	61	-REG	I	I3U	61	-REG[3]	I	I3U
62	BVD2	I/O	I1U,OT1	62	-SPKR	I/O	I1U,OT1	62	-DASP	I/O	I1U,ON1
63	BVD1	I/O	I1U,OT1	63	-STSCHG	I/O	I1U,OT1	63	-PDIAG	I/O	I1U,ON1
64	D08[1]	I/O	I1Z,OZ3	64	D08[1]	I/O	I1Z,OZ3	64	D08[1]	I/O	I1Z,OZ3
65	D09[1]	I/O	I1Z,OZ3	65	D09[1]	I/O	I1Z,OZ3	65	D09[1]	I/O	I1Z,OZ3
66	D10[1]	I/O	I1Z,OZ3	66	D10[1]	I/O	I1Z,OZ3	66	D10[1]	I/O	I1Z,OZ3
67	-CD2	O	Ground	67	-CD2	O	Ground	67	-CD2	O	Ground
68	GND		Ground	68	GND		Ground	68	GND		Ground

Note: 1. These signals are required only for 16 bit access and not required when installed in 8-bit systems. Devices should allow for 3-state signals not to consume current.
2. Should be grounded by the host.
3. Should be tied to VCC by the host.

Table 4-2 Double Density Flash Series CompactFlash Pin Assignments and Pin Type

PC Card Memory Mode				PC Card I/O Mode				True IDE Mode			
Pin Num	Signal Name	Pin Type	In, Out Type	Pin Num	Signal Name	Pin Type	In, Out Type	Pin Num	Signal Name	Pin Type	In, Out Type
1	GND		Ground	1	GND		Ground	1	GND		Ground
2	D03	I/O	I1Z,OZ3	2	D03	I/O	I1Z,OZ3	2	D03	I/O	I1Z,OZ3
3	D04	I/O	I1Z,OZ3	3	D04	I/O	I1Z,OZ3	3	D04	I/O	I1Z,OZ3
4	D05	I/O	I1Z,OZ3	4	D05	I/O	I1Z,OZ3	4	D05	I/O	I1Z,OZ3
5	D06	I/O	I1Z,OZ3	5	D06	I/O	I1Z,OZ3	5	D06	I/O	I1Z,OZ3
6	D07	I/O	I1Z,OZ3	6	D07	I/O	I1Z,OZ3	6	D07	I/O	I1Z,OZ3
7	-CE1	I	I3U	7	-CE1	I	I3U	7	-CS0	I	I3Z
8	A10	I	I1Z	8	A10	I	I1Z	8	A10[2]	I	I1Z
9	-OE	I	I3U	9	-OE	I	I3U	9	-ATA SEL	I	I3U
10	A09	I	I1Z	10	A09	I	I1Z	10	A09[2]	I	I1Z
11	A08	I	I1Z	11	A08	I	I1Z	11	A08[2]	I	I1Z
12	A07	I	I1Z	12	A07	I	I1Z	12	A07[2]	I	I1Z
13	VCC		Power	13	VCC		Power	13	VCC		Power
14	A06	I	I1Z	14	A06	I	I1Z	14	A06[2]	I	I1Z
15	A05	I	I1Z	15	A05	I	I1Z	15	A05[2]	I	I1Z
16	A04	I	I1Z	16	A04	I	I1Z	16	A04[2]	I	I1Z
17	A03	I	I1Z	17	A03	I	I1Z	17	A03[2]	I	I1Z
18	A02	I	I1Z	18	A02	I	I1Z	18	A02	I	I1Z
19	A01	I	I1Z	19	A01	I	I1Z	19	A01	I	I1Z
20	A00	I	I1Z	20	A00	I	I1Z	20	A00	I	I1Z
21	D00	I/O	I1Z,OZ3	21	D00	I/O	I1Z,OZ3	21	D00	I/O	I1Z,OZ3
22	D01	I/O	I1Z,OZ3	22	D01	I/O	I1Z,OZ3	22	D01	I/O	I1Z,OZ3
23	D02	I/O	I1Z,OZ3	23	D02	I/O	I1Z,OZ3	23	D02	I/O	I1Z,OZ3
24	WP	O	OT3	24	-IOIS16	O	OT3	24	-IOCS16	O	ON3
25	-CD2	O	Ground	25	-CD2	O	Ground	25	-CD2	O	Ground
26	-CD1	O	Ground	26	-CD1	O	Ground	26	-CD1	O	Ground
27	D11[1]	I/O	I1Z,OZ3	27	D11[1]	I/O	I1Z,OZ3	27	D11[1]	I/O	I1Z,OZ3
28	D12[1]	I/O	I1Z,OZ3	28	D12[1]	I/O	I1Z,OZ3	28	D12[1]	I/O	I1Z,OZ3
29	D13[1]	I/O	I1Z,OZ3	29	D13[1]	I/O	I1Z,OZ3	29	D13[1]	I/O	I1Z,OZ3
30	D14[1]	I/O	I1Z,OZ3	30	D14[1]	I/O	I1Z,OZ3	30	D14[1]	I/O	I1Z,OZ3
31	D15[1]	I/O	I1Z,OZ3	31	D15[1]	I/O	I1Z,OZ3	31	D15[1]	I/O	I1Z,OZ3
32	-CE2[1]	I	I3U	32	-CE2[1]	I	I3U	32	-CS1[1]	I	I1Z
33	-VS1	O	Ground	33	-VS1	O	Ground	33	-VS1	O	Ground
34	-IORD	I	I3U	34	-IORD	I	I3U	34	-IORD	I	I3Z

Table 4-2 Double Density Flash Series CompactFlash Pin Assignments and Pin Type (continued)

PC Card Memory Mode				PC Card I/O Mode				True IDE Mode			
Pin Num	Signal Name	Pin Type	In, Out Type	Pin Num	Signal Name	Pin Type	In, Out Type	Pin Num	Signal Name	Pin Type	In, Out Type
35	-IOWR	I	I3U	35	-IOWR	I	I3U	35	-IOWR	I	I3Z
36	-WE	I	I3U	36	-WE	I	I3U	36	-WE[3]	I	I3U
37	RDY/BSY	O	OT1	37	IREQ	O	OT1	37	INTRQ	O	OZ1
38	VCC		Power	38	VCC		Power	38	VCC		Power
39	-CSEL	I	I2Z	39	-CSEL	I	I2Z	39	-CSEL	I	I2U
40	-VS2	O	OPEN	40	-VS2	O	OPEN	40	-VS2	O	OPEN
41	RESET	I	I2Z	41	RESET	I	I2Z	41	-RESET	I	I2Z
42	-WAIT	O	OT1	42	-WAIT	O	OT1	42	IORDY	O	ON1
43	-INPACK	O	OT1	43	-INPACK	O	OT1	43	-INPACK	O	OZ1
44	-REG	I	I3U	44	-REG	I	I3U	44	-REG[3]	I	I3U
45	BVD2	I/O	I1U,OT1	45	-SPKR	I/O	I1U,OT1	45	-DASP	I/O	I1U,ON1
46	BVD1	I/O	I1U,OT1	46	-STSCHG	I/O	I1U,OT1	46	-PDIAG	I/O	I1U,ON1
47	D08[1]	I/O	I1Z,OZ3	47	D08[1]	I/O	I1Z,OZ3	47	D08[1]	I/O	I1Z,OZ3
48	D09[1]	I/O	I1Z,OZ3	48	D09[1]	I/O	I1Z,OZ3	48	D09[1]	I/O	I1Z,OZ3
49	D10[1]	I/O	I1Z,OZ3	49	D10[1]	I/O	I1Z,OZ3	49	D10[1]	I/O	I1Z,OZ3
50	GND		Ground	50	GND		Ground	50	GND		Ground

Note: 1. These signals are required only for 16 bit access and not required when installed in 8-bit systems. Devices should allow for 3-state signals not to consume current.
2. Should be grounded by the host.
3. Should be tied to VCC by the host.

Table 4-3 Signal Descriptions

Signal Name	Dir.	Pin	Description
A10 - A0 (PC Card Memory Mode)	I	8, 11, 12, 22, 23, 24, 25, 26, 27, 28, 29 (CF pins 8, 10, 11, 12, 14, 15, 16, 17, 18, 19, 20)	These address lines along with the -REG signal are used to select the following: The I/O port address registers within the Double Density Flash Series Card, the memory mapped port address registers within the card, a byte in the card's information structure and its configuration control and status registers.
A10 - A0 (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
A2 - A0 (True IDE Mode)	I	27, 28, 29 (CF pins 18, 19, 20)	In True IDE Mode only A[2:0] are used to select the one of eight registers in the Task File.
A10 - A3 (True IDE Mode)			In True IDE Mode, these remaining address lines should be grounded by the host.
BVD1 (PC Card Memory Mode)	I/O	63 (CF pin 46)	This signal is asserted high as the BVD1 signal since a battery is not used with this product.
-STSCHG (PC Card I/O Mode) Status Changed			This signal is asserted low to alert the host to changes in the RDY/-BSY and Write Protect states, while the I/O interface is configured. Its use is controlled by the Card Config and Status Register.
-PDIAG (True IDE Mode)			In the True IDE Mode, this input / output is the Pass Diagnostic signal in the Master / Slave handshake protocol.
BVD2 (PC Card Memory Mode)	I/O	62 (CF pin 45)	This output line is always driven to a high state in Memory Mode since a battery is not required for this product.
-SPKR (PC Card I/O Mode)			This output line is always driven to a high state in I/O Mode since this product does not support the audio function.
-DASP (True IDE Mode)			In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
-CD1, -CD2 (PC Card Memory Mode)	O	36, 67 (CF pins 26, 25)	These Card Detect pins are connected to ground on the Double Density Flash Series products. They are used by the host to determine if the product is fully inserted into its socket.
-CD1, -CD2 (PC Card I/O Mode)			This signal is the same for all modes.
-CD1, -CD2 (True IDE Mode)			This signal is the same for all modes.
-CE1, -CE2 (PC Card Memory Mode) Card Enable	I	7, 42 (CF pins 7, 32)	These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. -CE2 always accesses the odd byte of the word. -CE1 accesses the even byte or the Odd byte of the word depending on A0 and -CE2. A multi-plexing scheme based on A0, -CE1, -CE2 allows 8 bit hosts to access all data on D0-D7. See Tables 4-12, 4-13, 4-16, and 4-17.
-CE1, -CE2 (PC Card I/O Mode) Card Enable			This signal is the same as the PC Card Memory Mode signal.
-CS0, -CS1 (True IDE Mode)			In the True IDE Mode -CS0 is the chip select for the task file registers while -CS1 is used to select the Alternate Status Register and the Device Control Register.

Table 4-3 Signal Description (continued)

Signal Name	Dir.	Pin	Description
-CSEL (PC Card Memory Mode)	I	56	This signal is not used for this mode.
-CSEL (PC Card I/O Mode)		(CF pin 39)	This signal is not used for this mode.
-CSEL (True IDE Mode)			This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave.
D15 - D00 (PC Card Memory Mode)	I/O	41, 40, 39, 38, 37, 66, 65, 64, 6, 5, 4, 3, 2, 32, 31, 30	These lines carry the Data, Commands and Status information between the host and the controller. D00 is the LSB of the Even Byte of the Word. D08 is the LSB of the Odd Byte of the Word.
D15 - D00 (PC Card I/O Mode)		(CF pins 31, 30, 29, 28, 27, 49, 48, 47, 6, 5, 4, 3, 2, 23, 22, 21)	This signal is the same as the PC Card Memory Mode signal.
D15 - D00 (True IDE Mode)			In True IDE Mode, all Task File operations occur in byte mode on the low order bus D00-D07 while all data transfers are 16 bit using D00-D15.
GND (PC Card Memory Mode)	--	1, 34, 35, 68	Ground.
GND (PC Card I/O Mode)		(CF pins 1, 50)	This signal is the same for all modes.
GND (True IDE Mode)			This signal is the same for all modes.
-INPACK (PC Card Memory Mode)	O	60	This signal is not used in this mode.
-INPACK (PC Card I/O Mode) Input Acknowledge		(CF pin 43)	The Input Acknowledge signal is asserted by the Double Density Flash Series Card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the card and the CPU.
-INPACK (True IDE Mode)			In True IDE Mode this output signal is not used and should not be connected at the host.
-IORD (PC Card Memory Mode)	I	44	This signal is not used in this mode.
-IORD (PC Card I/O Mode)		(CF pin 34)	This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the Double Density Flash Series Card when the card is configured to use the I/O interface.
-IORD (True IDE Mode)			In True IDE Mode, this signal has the same function as in PC Card I/O Mode.

Table 4-3 Signal Description (continued)

Signal Name	Dir.	Pin	Description
-IOWR (PC Card Memory Mode)	I	45	This signal is not used in this mode.
-IOWR (PC Card I/O Mode)		(CF pin 35)	The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the Double Density Flash Series controller registers when the product is configured to use the I/O interface. The clocking will occur on the negative to positive edge of the signal (trailing edge).
-IOWR (True IDE Mode)			In True IDE Mode, this signal has the same function as in PC Card I/O Mode.
-OE (PC Card Memory Mode)	I	9 (CF pin 9)	This is an Output Enable strobe generated by the host interface. It is used to read data from the Double Density Flash Series products in Memory Mode and to read the CIS and configuration registers.
-OE (PC Card I/O Mode)			In PC Card I/O Mode, this signal is used to read the CIS and configuration registers.
-ATA SEL (True IDE Mode)			To enable True IDE Mode this input should be grounded by the host.
RDY/-BSY (PC Card Memory Mode)	O	16 (CF pin 37)	In Memory Mode this signal is set high when the Double Density Flash Series Card is ready to accept a new data transfer operation and held low when the card is busy. The Host memory card socket must provide a pull-up resistor. At power up and at Reset, the RDY/-BSY signal is held low (busy) until the Double Density Flash Series Card has completed its power up or reset function. No access of any type should be made to the Double Density Flash Series Card during this time. The RDY/-BSY signal is held high (disabled from being busy) whenever the following condition is true: The Double Density Flash Series Card has been powered up with +RESET continuously disconnected or asserted.
-IREQ (PC Card I/O Mode)			I/O Operation - After the Double Density Flash Series Card has been configured for I/O operation, this signal is used as -Interrupt Request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt.
INTRQ (True IDE Mode)			In True IDE Mode signal is the active high Interrupt Request to the host.
-REG (PC Card Memory Mode) Attribute Memory Select	I	61 (CF pin 44)	This signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory.
-REG (PC Card I/O Mode)			The signal must also be active (low) during I/O Cycles when the I/O address is on the Bus.
-REG (True IDE Mode)			In True IDE Mode this input signal is not used and should be connected to VCC by the host.

Table 4-3 Signal Description (continued)

Signal Name	Dir.	Pin	Description
RESET (PC Card Memory Mode)	I	58 (CF pin 41)	When the pin is high, this signal resets the Double Density Flash Card. The card is Reset only at power up if this pin is left high or open from power-up. The card is also reset when the Soft Reset bit in the Card Configuration Option Register is set.
RESET (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
-RESET (True IDE Mode)			In the True IDE Mode this input pin is the active low hardware reset from the host.
VCC (PC Card Memory Mode)	--	17, 51 (CF pins 13, 38)	+5 V, +3.3 V power.
VCC (PC Card I/O Mode)			This signal is the same for all modes.
VCC (True IDE Mode)			This signal is the same for all modes.
VPP (PC Card Memory Mode)		18, 52 (No CF pins)	Programming Voltage power supply is not connected on the Double Density Flash Series products.
VPP (PC Card I/O Mode)			This signal is the same for all modes.
VPP (True IDE Mode)			This signal is the same for all modes.
-VS1 -VS2 (PC Card Memory Mode)	O	43 57 (CF pins 33, 40)	Voltage Sense Signals. -VS1 is grounded so that the Double Density Flash Series product CIS can be read at 3.3 volts and -VS2 is open and reserved by PCMCIA for a secondary voltage.
-VS1 -VS2 (PC Card I/O Mode)			This signal is the same for all modes.
-VS1 -VS2 (True IDE Mode)			This signal is the same for all modes.
-WAIT (PC Card Memory Mode)	O	59 (CF pin 42)	The -WAIT signal is driven low by the Double Density Flash Card to signal the host to delay completion of a memory or I/O cycle that is in progress.
-WAIT (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
IORDY (True IDE Mode)			In True IDE Mode this output signal may be used as IORDY.
-WE (PC Card Memory Mode)	I	15 (CF pin 36)	This is a signal driven by the host and used for strobing memory write data to the registers of the Double Density Flash Series Card when the card is configured in the memory interface mode. It is also used for writing the configuration registers.
-WE (PC Card I/O Mode)			In PC Card I/O Mode, this signal is used for writing the configuration registers.
-WE (True IDE Mode)			In True IDE Mode this input signal is not used and should be connected to VCC by the host.

Table 4-3 Signal Description (continued)

Signal Name	Dir.	Pin	Description
WP (PC Card Memory Mode) Write Protect	O	33 (CF pin 24)	Memory Mode - The Double Density Flash Series Card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence.
-IOIS16 (PC Card I/O Mode)			I/O Operation - When the Double Density Flash Series Card is configured for I/O Operation, Pin 24 is used for the -I/O Selected is 16 Bit Port (-IOIS16) function. A Low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port.
-IOCS16 (True IDE Mode)			In True IDE Mode this output signal is asserted low when this device is expecting a word data transfer cycle.

4.3 *Electrical Specification*

The following table defines all D.C. Characteristics for the Double Density Flash Series.

Unless otherwise stated, conditions are:

SDP3C SDCFC	SDP3CI SDCFCI
Vcc = 5V ±10%	Vcc = 5V ± 5%
Vcc = 3.3V ± 5%	
Ta = 0°C to 60°C	Ta = -40°C to 85°C

4.3.1 Input Leakage Current

Note: In the table below, x refers to the characteristics described in section 4.3.2. For example, I1U indicates a pull up resistor with a type 1 input characteristic.

Type	Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
IxZ	Input Leakage Current	IL	Vih = Vcc / Vil = Gnd	-1		1	µA
IxU	Pull Up Resistor	RPU1	Vcc = 5.0V	50k		500k	Ohm
IxD	Pull Down Resistor	RPD1	Vcc = 5.0V	50k		500k	Ohm

Note: The minimum pullup resistor leakage current meets the PCMCIA specification of 10k ohms but is intentionally higher in the Double Density Flash Series product to reduce power use.

4.3.2 Input Characteristics

Type	Parameter	Symbol	MIN	TYP	MAX	MIN	TYP	MAX	Units
			VCC = 3.3 V			VCC = 5.0 V			
1	Input Voltage CMOS	Vih Vil	2.4		0.6	2.4		0.8	Volts
2	Input Voltage CMOS	Vih Vil	1.5		0.6	2.0		0.8	Volts
3	Input Voltage CMOS Schmitt Trigger	Vth Vtl		1.8 1.0			2.8 2.0		Volts

4.3.3 *Output Drive Type*

Note: In the table below, x refers to the characteristics described in section 4.3.4. For example, OT3 refers to Totempole output with a type 3 output drive characteristic.

Type	Output Type	Valid Conditions
OTx	Totempole	Ioh & Iol
OZx	Tri-State N-P Channel	Ioh & Iol
OPx	P-Channel Only	Ioh Only
ONx	N-Channel Only	Iol Only

4.3.4 *Output Drive Characteristics*

Type	Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
1	Output Voltage	Voh Vol	Ioh = -4 mA Iol = 4 mA	Vcc -0.8V		 Gnd +0.4V	Volts
2	Output Voltage	Voh Vol	Ioh = -8 mA Iol = 8 mA	Vcc -0.8V		 Gnd +0.4V	Volts
3	Output Voltage	Voh Vol	Ioh = -8 mA Iol = 8 mA	Vcc -0.8V		 Gnd +0.4V	Volts
X	Tri-State Leakage Current	Ioz	Vol = Gnd Voh = Vcc	-10		10	µA

4.3.5 *Interface/Bus Timing*

There are two types of bus cycles and timing sequences that occur in the PCMCIA type interface, a direct mapped I/O transfer and a memory access. The two timing sequences are explained in detail in the PCMCIA PC Card Standard Release 2.1. The Double Density Flash Series products conform to the timing in that reference document.

4.3.6 *Attribute Memory Read Timing Specification*

The Attribute Memory access time is defined as 300 ns. Detailed timing specifications are shown in Table 4-4.

Table 4-4 Attribute Memory Read Timing

Speed Version			300 ns	
Item	Symbol	IEEE Symbol	Min ns.	Max ns.
Read Cycle Time	tc(R)	tAVAV	300	
Address Access Time	ta(A)	tAVQV		300
Card Enable Access Time	ta(CE)	tELQV		300
Output Enable Access Time	ta(OE)	tGLQV		150
Output Disable Time from CE	tdis(CE)	tEHQZ		100
Output Disable Time from OE	tdis(OE)	tGHQZ		100
Address Setup Time	tsu (A)	tAVWL	30	
Output Enable Time from CE	ten(CE)	tELQNZ	5	
Output Enable Time from OE	ten(OE)	tGLQNZ	5	
Data Valid from Address Change	tv(A)	tAXQX	0	

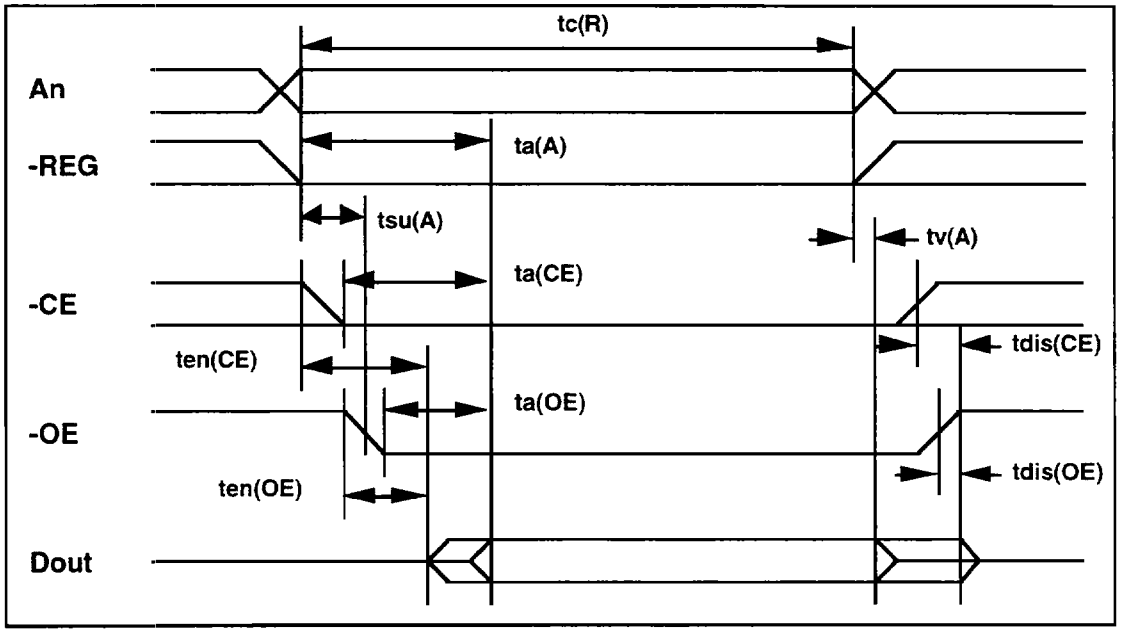

Figure 4-1 Attribute Memory Read Timing Diagram

Notes: All times are in nanoseconds. Dout signifies data provided by the Double Density Flash Series Card to the system. The -CE signal or both the -OE signal and the -WE signal must be de-asserted between consecutive cycle operations.

4.3.7 *Attribute Memory Write Timing Specification*

The Card Configuration write access time is defined as 250 ns. Detailed timing specifications are shown in Table 4-5.

Note: SanDisk does not allow writing from the Host to CIS Memory. Only writes to the Configuration register are allowed.

Table 4-5 Attribute Memory Write Timing

Speed Version			250 ns	
Item	Symbol	IEEE Symbol	Min ns	Max ns
Write Cycle Time	tc(W)	tAVAV	250	
Write Pulse Width	tw(WE)	tWLWH	150	
Address Setup Time	tsu(A)	tAVWL	30	
Write Recovery Time	trec(WE)	tWMAX	30	
Data Setup Time for WE	tsu(D-WEH)	tDVWH	80	
Data Hold Time	th(D)	tWMDX	30	

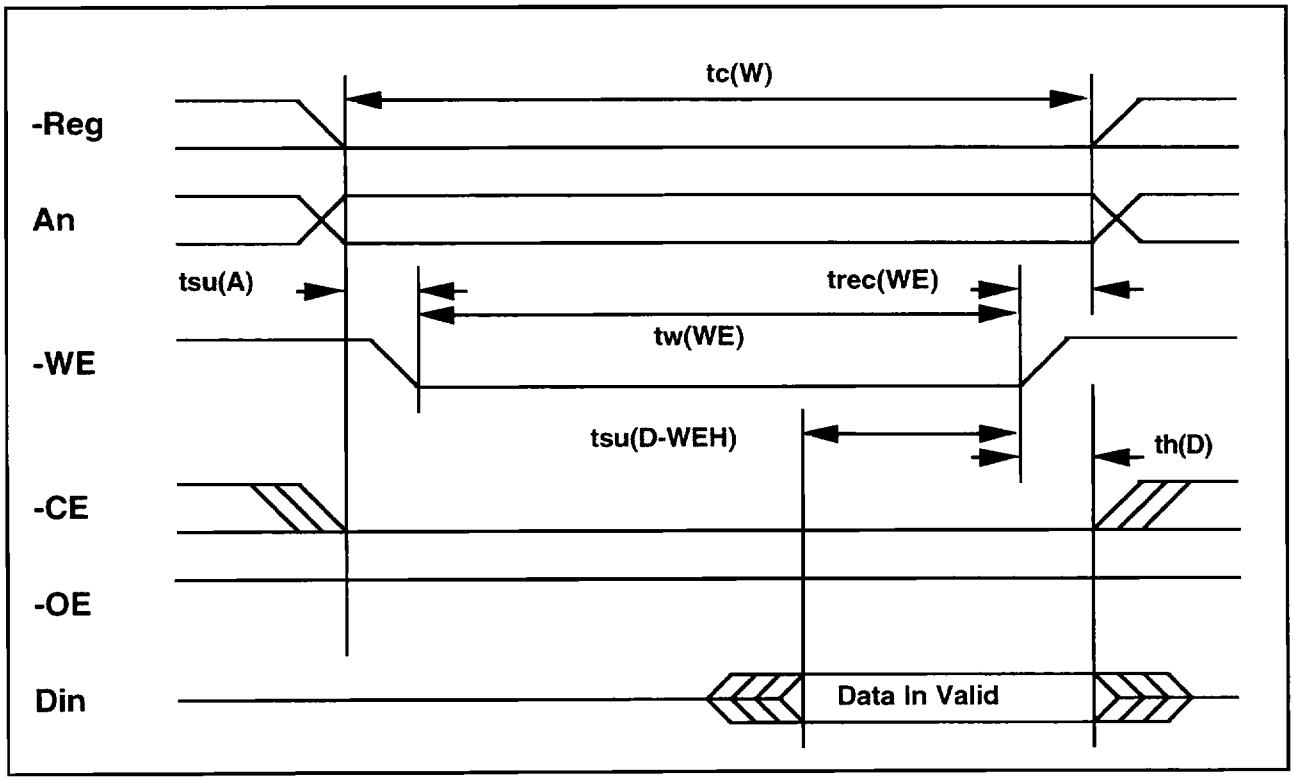

Figure 4-2 Attribute Memory Write Timing Diagram

Notes: All times are in nanoseconds. Din signifies data provided by the system to the Double Density Flash Series Card.

4.3.8 *Common Memory Read Timing Specification*

Table 4-6 Common Memory Read Timing

Item	Symbol	IEEE Symbol	Min ns.	Max ns.
Output Enable Access Time	ta(OE)	tGLQV		125
Output Disable Time from OE	tdis(OE)	tGHQZ		100
Address Setup Time	tsu(A)	tAVGL	30	
Address Hold Time	th(A)	tGHAX	20	
CE Setup before OE	tsu(CE)	tELGL	0	
CE Hold following OE	th(CE)	tGHEH	20	
Wait Delay Falling from OE	tv(WT-OE)	tGLWTV		35
Data Setup for Wait Release	tv(WT)	tQVWTH		0
Wait Width Time (Default Speed)	tw(WT)	tWTLWTH		350

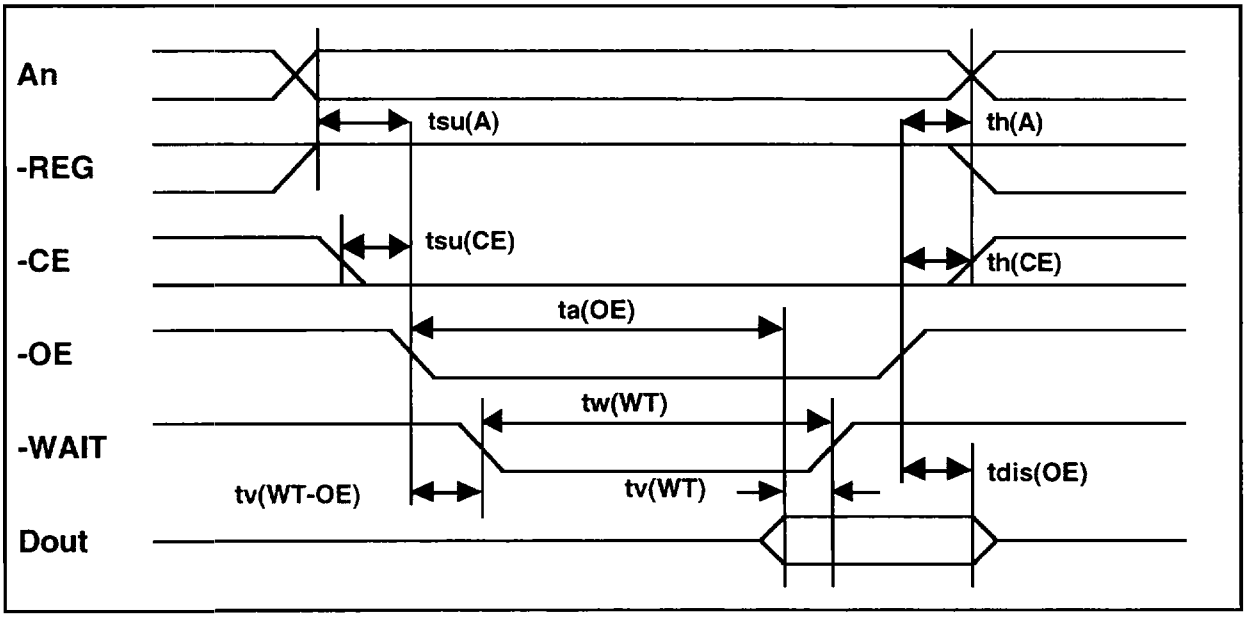

Figure 4-3 Common Memory Read Timing Diagram

Notes: The maximum load on -WAIT is 1 LSTTL with 50pF total load. All times are in nanoseconds.
Dout signifies data provided by the Double Density Flash Series Card to the system.
The -WAIT signal may be ignored if the -OE cycle to cycle time is greater than the Wait Width time.
The Max Wait Width time (in the slowest mode) can be determined from the Card Information Structure.

4.3.9 *Common Memory Write Timing Specification*

Table 4-7 Common Memory Write Timing

Item	Symbol	IEEE Symbol	Min ns.	Max ns.
Data Setup before WE	tsu(D-WEH)	tDVWH	80	
Data Hold following WE	th(D)	tlWMDX	30	
WE Pulse Width	tw(WE)	tWLWH	150	
Address Setup Time	tsu(A)	tAVWL	30	
CE Setup before WE	tsu(CE)	tELWL	0	
Write Recovery Time	trec(WE)	tWMAX	30	
Address Hold Time	th(A)	tGHAX	20	
CE Hold following WE	th(CE)	tGHEH	20	
Wait Delay Falling from WE	tv(WT-WE)	tWLWTV		35
WE High from Wait Release	tv(WT)	tWTHWH	0	
Wait Width Time (Default Speed)	tw (WT)	tWTLWTH		350

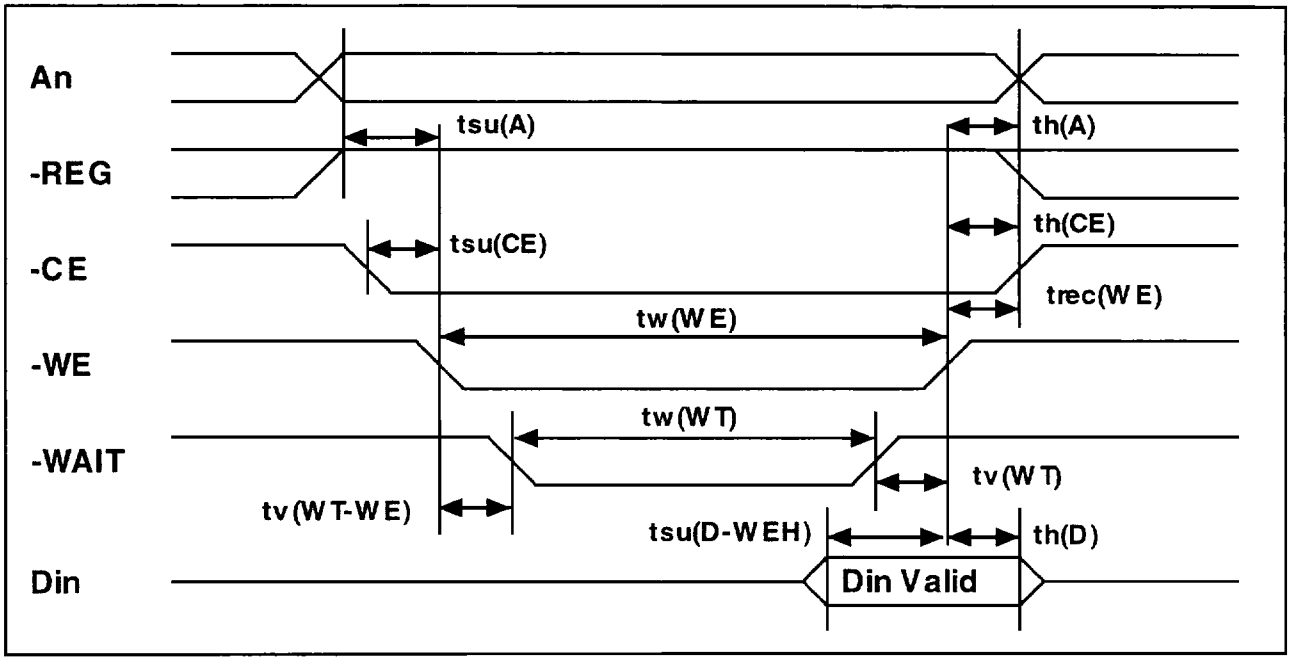

Figure 4-4 Common Memory Write Timing Diagram

Notes: The maximum load on -WAIT is 1 LSTTL with 50pF total load. All times are in nanoseconds.
Din signifies data provided by the system to the Double Density Flash Series Card.
The -WAIT signal may be ignored if the -WE cycle to cycle time is greater than the Wait Width time.
The Max Wait Width time (in the slowest mode) can be determined from the Card Information Structure.

4.3.10 I/O Input (Read) Timing Specification

Table 4-8 I/O Read Timing

Item	Symbol	IEEE Symbol	Min ns.	Max ns.
Data Delay after IORD	td(IORD)	tIGLQV		100
Data Hold following IORD	th(IORD)	tIGHQX	0	
IORD Width Time	tw(IORD)	tIGLIGH	165	
Address Setup before IORD	tsuA(IORD)	tAVIGL	70	
Address Hold following IORD	thA(IORD)	tIGHAX	20	
CE Setup before IORD	tsuCE(IORD)	tELIGL	5	
CE Hold following IORD	thCE(IORD)	tIGHEH	20	
REG Setup before IORD	tsuREG(IORD)	tRGLIGL	5	
REG Hold following IORD	thREG(IORD)	tIGHRGH	0	
INPACK Delay Falling from IORD	tdfINPACK(IORD)	tIGLIAL	0	45
INPACK Delay Rising from IORD	tdrINPACK(IORD)	tIGHIAH		45
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		35
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH		35
Wait Delay Falling from IORD	tdWT(IORD)	tIGLWTL		35
Data Delay from Wait Rising	td(WT)	tWTHQV		0
Wait Width Time (Default Speed)	tw(WT)	tWTLWTH		350

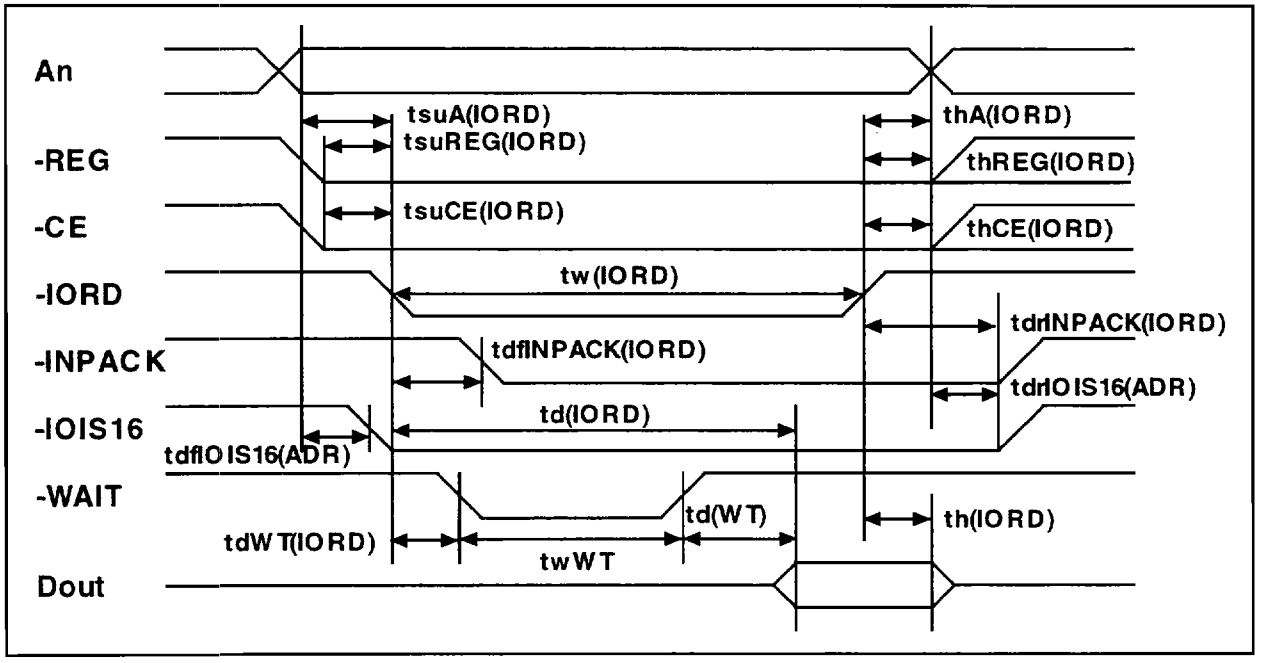

Figure 4-5 I/O Read Timing Diagram

Notes: The maximum load on -WAIT, -INPACK and -IOIS16 is 1 LSTTL with 50pF total load. All times are in nanoseconds.
Minimum time from -WAIT high to -IORD high is 0 nsec, but minimum -IORD width must still be met.
Dout signifies data provided by the Double Density Flash Series Card to the system.

4.3.11 I/O Output (Write) Timing Specification

Table 4-9 I/O Write Timing

Item	Symbol	IEEE Symbol	Min ns.	Max ns.
Data Setup before IOWR	tsu(IOWR)	tDVIWH	60	
Data Hold following IOWR	th(IOWR)	tIWHDX	30	
IOWR Width Time	twIOWR	tIWLIWH	165	
Address Setup before IOWR	tsuA(IOWR)	tAVIWL	70	
Address Hold following IOWR	thA(IOWR)	tIWHAX	20	
CE Setup before IOWR	tsuCE(IOWR)	tELIWL	5	
CE Hold following IOWR	thCE(IOWR)	tIWHEH	20	
REG Setup before IOWR	tsuREG(IOWR)	tRGLIWL	5	
REG Hold following IOWR	thREG(IOWR)	tIWHRGH	0	
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		35
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH		35
Wait Delay Falling from IOWR	tdWT(IOWR)	tIWLWTL		35
IOWR high from Wait high	tdrIOWR(WT)	tWTJIWH	0	
Wait Width Time (Default Speed) (Set Feature Speed <68 mA.)	tw(WT)	tWTLWTH		350 700

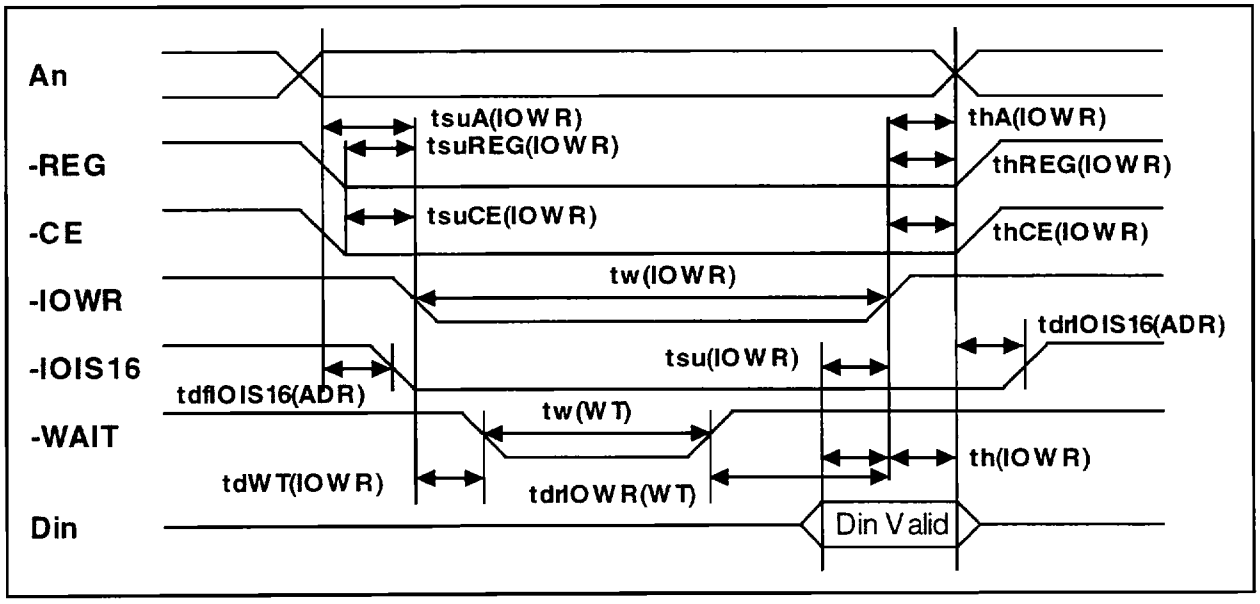

Figure 4-6 I/O Write Timing Diagram

Notes: The maximum load on -WAIT, -INPACK, and -IOIS16 is 1 LSTTL with 50pF total load. All times are in nanoseconds.
Minimum time from -WAIT high to -IOWR high is 0 nsec, but minimum -IOWR width must still be met.
Din signifies data provided by the system to the Double Density Flash Series Card.

4.3.12 *True IDE Mode I/O Input (Read) Timing Specification*

Table 4-10 True IDE Mode I/O Read Timing

Item	Symbol	IEEE Symbol	Min ns.	Max ns.
Data Delay after IORD	td(IORD)	tIGLQV		100
Data Hold following IORD	th(IORD)	tIGHQX	0	
IORD Width Time	tw(IORD)	tIGLIGH	165	
Address Setup before IORD	tsuA(IORD)	tAVIGL	70	
Address Hold following IORD	thA(IORD)	tIGHAX	20	
CE Setup before IORD	tsuCE(IORD)	tELIGL	5	
CE Hold following IORD	thCE(IORD)	tIGHEH	20	
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		35
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH		35

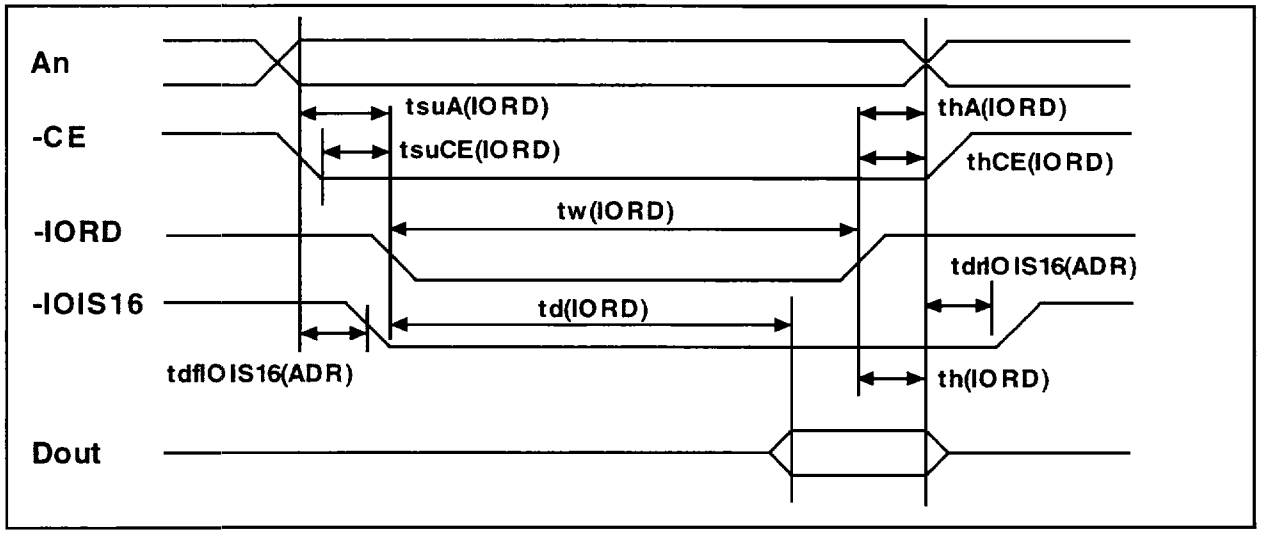

Figure 4-7 True IDE Mode I/O Read Timing Diagram

Notes: The maximum load on -IOIS16 is 1 LSTTL with 50pF total load. All times are in nanoseconds.
Minimum time from -WAIT high to -IORD high is 0 nsec, but minimum -IORD width must still be met.
Dout signifies data provided by the Double Density Flash Series Card to the system.

4.3.13 *True IDE Mode I/O Output (Write) Timing Specification*

Table 4-11 True IDE Mode I/O Write Timing

Item	Symbol	IEEE Symbol	Min ns.	Max ns.
Data Setup before IOWR	tsu(IOWR)	tDVIWH	60	
Data Hold following IOWR	th(IOWR)	tIWHDX	30	
IOWR Width Time	tw(IOWR)	tIWLIWH	165	
Address Setup before IOWR	tsuA(IOWR)	tAVIWL	70	
Address Hold following IOWR	thA(IOWR)	tIWHAX	20	
CE Setup before IOWR	tsuCE(IOWR)	tELIWL	5	
CE Hold following IOWR	thCE(IOWR)	tIWHEH	20	
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		35
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH		35

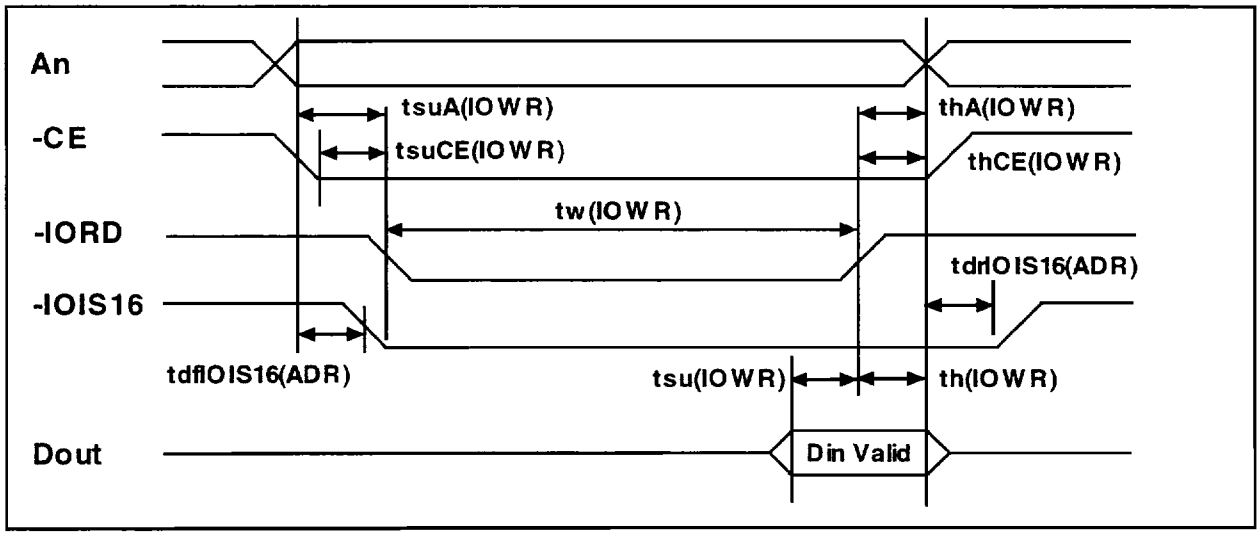

Figure 4-8 True IDE Mode I/O Write Timing Diagram

Notes: The maximum load on -IOIS16 is 1 LSTTL with 50pF total load. All times are in nanoseconds.
Minimum time from -WAIT high to -IOWR high is 0 nsec, but minimum -IOWR width must still be met.
Din signifies data provided by the system to the Double Density Flash Series Card.

4.4 *Card Configuration*

The Double Density Flash Series products are identified by appropriate information in the Card Information Structure (CIS). The following configuration registers are used to coordinate the I/O spaces and the Interrupt level of cards that are located in the system. In addition, these registers provide a method for accessing status information about the card that may be used to arbitrate between multiple interrupt sources on the same interrupt level or to replace status information that appears on dedicated pins in memory cards that have alternate use in I/O cards.

Table 4-12 Registers and Memory Space Decoding

-CE2	-CE1	-REG	-OE	-WE	A10	A9	A8-A4	A3	A2	A1	A0	SELECTED SPACE
1	1	X	X	X	X	X	XX	X	X	X	X	Standby
X	0	0	0	1	X	1	XX	X	X	X	0	Configuration Registers Read
1	0	1	0	1	X	X	XX	X	X	X	X	Common Memory Read (8 Bit D7-D0)
0	1	1	0	1	X	X	XX	X	X	X	X	Common Memory Read (8 Bit D15-D8)
0	0	1	0	1	X	X	XX	X	X	X	0	Common Memory Read (16 Bit D15-D0)
X	0	0	1	0	X	1	XX	X	X	X	0	Configuration Registers Write
1	0	1	1	0	X	X	XX	X	X	X	X	Common Memory Write (8 Bit D7-D0)
0	1	1	1	0	X	X	XX	X	X	X	X	Common Memory Write (8 Bit D15-D8)
0	0	1	1	0	X	X	XX	X	X	X	0	Common Memory Write (16 Bit D15-D0)
X	0	0	0	1	0	0	XX	X	X	X	0	Card Information Structure Read
1	0	0	1	0	0	0	XX	X	X	X	0	Invalid Access (CIS Write)
1	0	0	0	1	X	X	XX	X	X	X	1	Invalid Access (Odd Attribute Read)
1	0	0	1	0	X	X	XX	X	X	X	1	Invalid Access (Odd Attribute Write)
0	1	0	0	1	X	X	XX	X	X	X	X	Invalid Access (Odd Attribute Read)
0	1	0	1	0	X	X	XX	X	X	X	X	Invalid Access (Odd Attribute Write)

Configuration Registers Decoding

-CE2	-CE1	-REG	-OE	-WE	A10	A9	A8-A4	A3	A2	A1	A0	SELECTED REGISTER
X	0	0	0	1	0	1	00	0	0	0	0	Configuration Option Reg Read
X	0	0	1	0	0	1	00	0	0	0	0	Configuration Option Reg Write
X	0	0	0	1	0	1	00	0	0	1	0	Card Status Register Read
X	0	0	1	0	0	1	00	0	0	1	0	Card Status Register Write
X	0	0	0	1	0	1	00	0	1	0	0	Pin Replacement Register Read
X	0	0	1	0	0	1	00	0	1	0	0	Pin Replacement Register Write
X	0	0	0	1	0	1	00	0	1	1	0	Socket and Copy Register Read
X	0	0	1	0	0	1	00	0	1	1	0	Socket and Copy Register Write

Note: The location of the card configuration registers should always be read from the CIS since these locations may vary in future products. No writes should be performed to the Double Density Flash Series Card attribute memory except to the card configuration register addresses. All other attribute memory locations are reserved.

4.4.1 Attribute Memory Function

Attribute memory is a space where the Double Density Flash Series Card identification and configuration information is stored, and is limited to 8-bit wide accesses only at even addresses. The card configuration registers are also located here.

For the Attribute Memory Read function, signals -REG and -OE must be active and -WE inactive during the cycle. As in the Main Memory Read functions, the signals -CE1 and -CE2 control the even-byte and odd-byte address, but only the even-byte data is valid during the Attribute Memory access. Refer to Table 4-13 below for signal states and bus validity for the Attribute Memory function.

Table 4-13 Attribute Memory Function

Function Mode	-REG	-CE2	-CE1	A9	A0	-OE	-WE	D15-D8	D7-D0
Standby Mode	X	H	H	X	X	X	X	High Z	High Z
Read Byte Access CIS ROM (8 bits)	L	H	L	L	L	L	H	High Z	Even Byte
Write Byte Access CIS (8 bits) (Invalid)	L	H	L	L	L	H	L	Don't Care	Even Byte
Read Byte Access Configuration (8 bits)	L	H	L	H	L	L	H	High Z	Even Byte
Write Byte Access Configuration (8 bits)	L	H	L	H	L	H	L	Don't Care	Even Byte
Read Word Access CIS (16 bits)	L	L	L	L	X	L	H	Not Valid	Even Byte
Write Word Access CIS (16 bits) (Invalid)	L	L	L	L	X	H	L	Don't Care	Even Byte
Read Word Access Configuration (16 bits)	L	L	L	H	X	L	H	Not Valid	Even Byte
Write Word Access Configuration (16 bits)	L	L	L	H	X	H	L	Don't Care	Even Byte

Note: The -CE signal or both the -OE signal and the -WE signal must be de-asserted between consecutive cycle operations.

4.4.2 *Configuration Option Register (Address 200h in Attribute Memory)*

The Configuration Option Register is used to configure the cards interface, address decoding and interrupt and to issue a soft reset to the Double Density Flash Series Card.

Operation	D7	D6	D5	D4	D3	D2	D1	D0
R/W	SRESET	LevIREQ	Conf5	Conf4	Conf3	Conf2	Conf1	Conf0

SRESET Soft Reset - Setting this bit to one (1), waiting the minimum reset width time and returning to zero (0) places the card in the Reset state. Setting this bit to one (1) is equivalent to assertion of the +RESET signal except that the SRESET bit is not cleared. Returning this bit to zero (0) leaves the card in the same un-configured, Reset state as following power-up and hardware reset. This bit is set to zero (0) by power-up and hardware reset. Using the PCMCIA Soft Reset is considered a hard Reset by the ATA Commands. Contrast with Soft Reset in the Device Control Register.

LevIREQ This bit is set to one (1) when Level Mode Interrupt is selected, and zero (0) when Pulse Mode is selected. Set to zero (0) by Reset.

Conf5 - Conf0 Configuration Index. Set to zero (0) by reset. It's used to select operation mode of the card as shown below.

Note: Conf5 and Conf4 are reserved and must be written as zero (0).

Table 4-14 Card Configurations

Conf5	Conf4	Conf3	Conf2	Conf1	Conf0	Disk Card Mode
0	0	0	0	0	0	Memory Mapped
0	0	0	0	0	1	I/O Mapped, Any 16 byte system decoded boundary
0	0	0	0	1	0	I/O Mapped, 1F0-1F7/3F6-3F7
0	0	0	0	1	1	I/O Mapped, 170-177/376-377

4.4.3 *Card Configuration and Status Register (Address 202h in Attribute Memory)*

The Card Configuration and Status Register contains information about the Card's condition.

Card Configuration and Status Register Organization:

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	Changed	SigChg	IOis8	0	0	PwrDwn	Int	0
Write	0	SigChg	IOis8	0	0	PwrDwn	0	0

Changed Indicates that one or both of the Pin Replacement register CRdy, or CWProt bits are set to one (1). When the Changed bit is set, -STSCHG Pin 46 is held low if the SigChg bit is a One (1) and the card is configured for the I/O interface.

SigChg This bit is set and reset by the host to enable and disable a state-change "signal" from the Status Register, the Changed bit control pin 46 the Changed Status signal. If no state change signal is desired, this bit should be set to zero (0) and pin 46 (-STSCHG) signal will be held high while the card is configured for I/O.

IOis8 The host sets this bit to a one (1) if the card is to be configured in an 8 bit I/O mode. The Double Density Flash Series Card is always configured for both 8- and 16-bit I/O, so this bit is ignored.

PwrDwn This bit indicates whether the host requests the card to be in the power saving or active mode. When the bit is one (1), the card enters a power down mode. When zero (0), the host is requesting the card to enter the active mode. The PCMCIA Rdy/-Bsy value becomes BUSY when this bit is changed. Rdy/-Bsy will not become Ready until the power state requested has been entered. The card automatically powers down when it is idle and powers back up when it receives a command.

Int This bit represents the internal state of the interrupt request. This value is available whether or not I/O interface has been configured. This signal remains true until the condition which caused the interrupt request has been serviced. If interrupts are disabled by the -IEN bit in the Device Control Register, this bit is a zero (0).

4.4.4 Pin Replacement Register (Address 204h in Attribute Memory)

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	0	0	CRdy/-Bsy	CWProt	1	1	Rdy/-Bsy	WProt
Write	0	0	CRdy/-Bsy	CWProt	0	0	MRdy/-Bsy	MWProt

CRdy/-Bsy This bit is set to one (1) when the bit RRdy/-Bsy changes state. This bit can also be written by the host.

CWProt This bit is set to one (1) when the RWprot changes state. This bit may also be written by the host.

Rdy/-Bsy This bit is used to determine the internal state of the Rdy/-Bsy signal. This bit may be used to determine the state of the Ready/-Busy as this pin has been reallocated for use as Interrupt Request on an I/O card. When written, this bit acts as a mask for writing the corresponding bit CRdy/-Bsy.

WProt This bit is always zero (0) since the card does not have a Write Protect switch. When written, this bit acts as a mask for writing the corresponding bit CWProt.

MRdy/-Bsy This bit acts as a mask for writing the corresponding bit CRdy/-Bsy.

MWProt This bit when written acts as a mask for writing the corresponding bit CWProt.

Table 4-15 Pin Replacement Changed Bit/Mask Bit Values

Initial Value of (C) Status	Written by Host		Final	Comments
	"C" Bit	"M" Bit	"C" Bit	
0	X	0	0	Unchanged
1	X	0	1	Unchanged
X	0	1	0	Cleared by Host
X	1	1	1	Set by Host

4.4.5 Socket and Copy Register (Address 206h in Attribute Memory)

This register contains additional configuration information. This register is always written by the system before writing the card's Configuration Index Register.

Socket and Copy Register Organization:

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	Reserved	0	0	Drive #	0	0	0	0
Write	0	0	0	Drive # (0)	X	X	X	X

Reserved This bit is reserved for future standardization. This bit must be set to zero (0) by the software when the register is written.

Drive # This bit indicates the drive number of the card if twin card configuration is supported.

X The socket number is ignored by the Double Density Flash Series Card.

4.5 I/O Transfer Function

4.5.1 I/O Function

The I/O transfer to or from the Double Density Flash Series Card can be either 8 or 16 bits. When a 16-bit accessible port is addressed, the signal -IOIS16 is asserted by the card. Otherwise, the -IOIS16 signal is de-asserted. When a 16 bit transfer is attempted, and the -IOIS16 signal is not asserted by the card, the system must generate a pair of 8-bit references to access the word's even byte and odd byte. The Double Density Flash Series Card permits both 8- and 16-bit accesses to all of its I/O addresses, so -IOIS16 is asserted for all addresses to which the card responds.

The Double Density Flash Series Card may request the host to extend the length of an input cycle until data is ready by asserting the -WAIT signal at the start of the cycle.

Table 4-16 I/O Function

Function Code	-REG	-CE2	-CE1	A0	-IORD	-IOWR	D15-D8	D7-D0
Standby Mode	X	H	H	X	X	X	High Z	High Z
Byte Input Access (8 bits)	L L	H H	L L	L H	L L	H H	High Z High Z	Even-Byte Odd-Byte
Byte Output Access (8 bits)	L L	H H	L L	L H	H H	L L	Don't Care Don't Care	Even-Byte Odd-Byte
Word Input Access (16 bits)	L	L	L	L	L	H	Odd-Byte	Even-Byte
Word Output Access (16 bits)	L	L	L	L	H	L	Odd-Byte	Even-Byte
I/O Read Inhibit	H	X	X	X	L	H	Don't Care	Don't Care
I/O Write Inhibit	H	X	X	X	H	L	High Z	High Z
High Byte Input Only (8 bits)	L	L	H	X	L	H	Odd-Byte	High Z
High Byte Output Only (8 bits)	L	L	H	X	H	L	Odd-Byte	Don't Care

4.6 *Common Memory Transfer Function*

4.6.1 Common Memory Function

The Common Memory transfer to or from the Double Density Flash Series Card can be either 8 or 16 bits.

The Double Density Flash Series Card permits both 8 and 16 bit accesses to all of its Common Memory addresses.

The Double Density Flash Series Card may request the host to extend the length of a memory write cycle or extend the length of a memory read cycle until data is ready by asserting the -WAIT signal at the start of the cycle.

Table 4-17 Common Memory Function

Function Code	-REG	-CE2	-CE1	A0	-OE	-WE	D15-D8	D7-D0
Standby Mode	X	H	H	X	X	X	High Z	High Z
Byte Read Access (8 bits)	H H	H H	L L	L H	L L	H H	High Z High Z	Even-Byte Odd-Byte
Byte Write Access (8 bits)	H H	H H	L L	L H	H H	L L	Don't Care Don't Care	Even-Byte Odd-Byte
Word Read Access (16 bits)	H	L	L	X	L	H	Odd-Byte	Even-Byte
Word Write Access (16 bits)	H	L	L	X	H	L	Odd-Byte	Even-Byte
Odd Byte Read Only (8 bits)	H	L	H	X	L	H	Odd-Byte	High Z
Odd Byte Write Only (8 bits)	H	L	H	X	H	L	Odd-Byte	Don't Care

4.7 True IDE Mode I/O Transfer Function

4.7.1 True IDE Mode I/O Function

The Double Density Flash Series Card can be configured in a True IDE Mode of operation. This card is configured in this mode only when the -OE input signal is grounded by the host. In this True IDE Mode, the PCMCIA protocol and configuration are disabled and only I/O operations to the Task File and Data Register are allowed. In this mode, no Memory or Attribute Registers are accessible to the host. Double Density Flash Series Cards permit 8 bit data accesses if the user issues a Set Feature Command to put the device in 8 bit Mode.

Note: Removing and reinserting the Double Density Flash Series Cards while the host computer's power is on will reconfigure the card to PC Card ATA mode from the original True IDE Mode. To configure the card in True IDE Mode, the 68-pin socket must be power cycled with the card inserted and -OE (output enable) grounded by the host.

The following table defines the function of the operations for the True IDE Mode.

Table 4-18 IDE Mode I/O Function

Function Code	-CE2	-CE1	A0	-IORD	-IOWR	D15-D8	D7-D0
Invalid Mode	L	L	X	X	X	High Z	High Z
Standby Mode	H	H	X	X	X	High Z	High Z
Task File Write	H	L	1-7h	H	L	Don't Care	Data In
Task File Read	H	L	1-7h	L	H	High Z	Data Out
Data Register Write	H	L	0	H	L	Odd-Byte In	Even-Byte In
Data Register Read	H	L	0	L	H	Odd-Byte Out	Even-Byte Out
Control Register Write	L	H	6h	H	L	Don't Care	Control In
Alt Status Read	L	H	6h	L	H	High Z	Status Out