HIGH PERFORMANCE V53C105A	70/70L	80/80L	10/10L
Max. $\overline{RAS}$ Access Time, (t_{RAC})	70 ns	80 ns	100 ns
Max. Column Address Access Time, (t_{CAA})	35 ns	40 ns	50 ns
Min. Fast Page Mode Cycle Time, (t_{PC})	45 ns	50 ns	55 ns
Min. Read-Write Cycle Time, (t_{RC})	130 ns	150 ns	180 ns

LOW POWER V53C105AL	70L	80L	10L
Max. CMOS Standby Current, (I_{DD6})	1.0 mA	1.0 mA	1.0 mA

Features

- 256K x 4 organization
- $\overline{RAS}$ access time: 70, 80, 100 ns
- Low power dissipation for V53C105A-10
  - Operating Current—65 mA max.
  - TTL Standby Current—2.0 mA max.
- Low CMOS Standby Current
  - V53C105A—1.5 mA max.
  - V53C105AL—1.0 mA max.
- Read-Modify-Write, $\overline{RAS}$-Only Refresh, $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- Common I/O capability
- 512 Refresh cycles/8 ms
- On-chip substrate bias generator
- Fast Page Mode for a sustained data rate greater than 22 MHz
- Write-Per-Bit feature
- Standard packages are 20 pin Plastic DIP and 26/20 SOJ

Description

The V53C105A is a fast page mode, 262,144 word by four bit dynamic RAM. It is designed to operate from a single, 5 V ±10% tolerance power supply. Fabricated with Vitelic's VICMOS III technology, the device provides both high performance and high reliability over its operating range. Because it utilizes static circuitry, and its flow-through column address latches allow address pipelining, many critical system timing requirements are relaxed. These features make the V53C105A ideally suited for high resolution graphics, DSP, and high performance PC and workstation applications. The 70 ns version is capable of providing zero wait state memory in two memory clock cycle microprocessors running at 21 MHz clock rates.

Multiplexed address inputs and 1.0 micron design rules permit the V53C105A to be packaged in standard 300 mil plastic 20-pin DIPs and 300 mil plastic 26/20-pin SOJs.

Refreshing can be accomplished by using $\overline{CAS}$ before $\overline{RAS}$, $\overline{RAS}$-only or normal read or write cycles.

An internal address counter obviates the need for externally supplied addresses during the $\overline{CAS}$ before $\overline{RAS}$ refresh mode. Externally supplied addresses are required during $\overline{RAS}$-only, or normal read or write cycles.

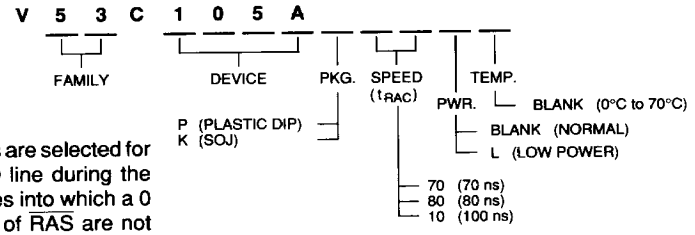
Write-Per-Bit Feature

The V53C105A has a write-per-bit function which permits selected bits of the I/O to be written into the memory, while the unselected (masked) I/O bits are not written into the memory. If $\overline{WB}/\overline{WE}$ is held High during the falling edge of $\overline{RAS}$, the write-per-bit feature is disabled, and the write operation is identical to that of a standard DRAM.

However, if $\overline{WB}/\overline{WE}$ is held Low during the falling edge of $\overline{RAS}$, the write-per-bit mode is enabled. In

Device Usage Chart

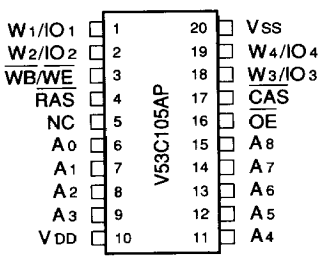
Operating Temperature Range	Package Outline		Access Time (ns)			Power		Temperature Mark
	P	K	70	80	100	Low	Std.	
0°C to 70°C	•	•	•	•	•	•	•	Blank



the enabled mode, individual I/O bits are selected for writing by asserting a 1 on the I/O line during the falling edge of $\overline{RAS}$. Those I/O lines into which a 0 is asserted during the falling edge of $\overline{RAS}$ are not written, i.e., they are masked, since their write circuitry is inhibited for that cycle. Immediately following this use of the I/O lines to select a masked or an unmasked write, data is placed on the I/O lines. The write (either masked or non-masked) is internally triggered by the falling edge of the latter of $\overline{CAS}$ or $\overline{WB/WE}$.

Description	Pkg.	Pin Count
Plastic DIP	P	20
SOJ	K	26/20

20-Pin Plastic DIP PIN CONFIGURATION
Top View



26/20-Pin Plastic SOJ PIN CONFIGURATION
Top View