1.2 Features

This section summarizes features of the 603e's implementation of the PowerPC architecture. Major features of the 603e are as follows:

- High-performance, superscalar microprocessor
  - As many as three instructions issued and retired per clock
  - As many as five instructions in execution per clock
  - Single-cycle execution for most instructions
  - Pipelined FPU for all single-precision and most double-precision operations
- Five independent execution units and two register files
  - BPU featuring static branch prediction
  - A 32-bit IU
  - Fully IEEE 754-compliant FPU for both single- and double-precision operations
  - LSU for data transfer between data cache and GPRs and FPRs
  - SRU that executes condition register (CR), special-purpose register (SPR) instructions, and integer add/compare instructions
  - Thirty-two GPRs for integer operands
  - Thirty-two FPRs for single- or double-precision operands
- High instruction and data throughput
  - Zero-cycle branch capability (branch folding)
  - Programmable static branch prediction on unresolved conditional branches
  - Instruction fetch unit capable of fetching two instructions per clock from the instruction cache
  - A six-entry instruction queue that provides lookahead capability
  - Independent pipelines with feed-forwarding that reduces data dependencies in hardware
  - 16-Kbyte data cache—four-way set-associative, physically addressed; LRU replacement algorithm
  - 16-Kbyte instruction cache—four-way set-associative, physically addressed; LRU replacement algorithm
  - Cache write-back or write-through operation programmable on a per page or per block basis
  - BPU that performs CR lookahead operations
  - Address translation facilities for 4-Kbyte page size, variable block size, and 256-Mbyte segment size
  - A 64-entry, two-way set-associative ITLB
  - A 64-entry, two-way set-associative DTLB
  - Four-entry data and instruction BAT arrays providing 128-Kbyte to 256-Mbyte blocks
  - Software table search operations and updates supported through fast-trap mechanism
  - 52-bit virtual address; 32-bit physical address
- Facilities for enhanced system performance
  - A 32- or 64-bit split-transaction external data bus with burst transfers
  - Support for one-level address pipelining and out-of-order bus transactions

- Integrated power management
  — Low-power 3.3-volt design
  — Internal processor/bus clock multiplier that provides 1/1, 1.5/1, 2/1, 2.5/1, 3/1, 3.5/1, and 4/1 ratios
  — Three power saving modes: doze, nap, and sleep
  — Automatic dynamic power reduction when internal functional units are idle
- In-system testability and debugging features through JTAG boundary-scan capability

1.3 General Parameters

The following list provides a summary of the general parameters of the 603e.

Technology	0.5 μ CMOS, four-layer metal
Die size	11.67 mm x 8.4 mm (98 mm^2)
Transistor count	2.6 million
Logic design	Fully-static
Package	Surface mount 240-pin ceramic quad flat pack (CQFP) or 255-pin ceramic ball grid array (CBGA)
Power supply	3.3 ± 5% V dc

1.4 Electrical and Thermal Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the 603e.

1.4.1 DC Electrical Characteristics

The tables in this section describe the 603e DC electrical characteristics. Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings

Characteristic	Symbol	Value	Unit
Core supply voltage	Vdd	−0.3 to 4.0	V
PLL supply voltage	AVdd	−0.3 to 4.0	V
I/O supply voltage	OVdd	−0.3 to 4.0	V
Input voltage	V_{in}	−0.3 to 5.5	V
Storage temperature range	T_{stg}	−55 to 150	°C

Notes:

1. Functional operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

2. **Caution**: V_{in} must not exceed OVdd by more than 2.5 V at any time including during power-on reset.

3. **Caution**: OVdd must not exceed Vdd/AVdd by more than 2.5 V at any time including during power-on reset.

4. **Caution**: Vdd/AVdd must not exceed OVdd by more than 0.4 V at any time including during power-on reset.

Table 2 provides the recommended operating conditions for the 603e.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Value	Unit
Core supply voltage	Vdd	3.135 to 3.465	V
PLL supply voltage	AVdd	3.135 to 3.465	V
I/O supply voltage	OVdd	3.135 to 3.465	V
Input voltage	V_{in}	-0.3 to 5.5	V
Die-junction temperature	T_j	0 to 105	°C

Notes: These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 3 provides the packages thermal characteristics for the 603e.

Table 3. Package Thermal Characteristics

Characteristic	Symbol	Value	Rating
Wire-bond CQFP package die junction-to-case thermal resistance (typical)	θ_{JC}	2.2	°C/W
Wire-bond CQFP package die junction-to-lead thermal resistance (typical)	θ_{JB}	18.0	°C/W
CBGA package die junction-to-case thermal resistance (typical)	θ_{JC}	0.08	°C/W
CBGA package die junction-to-ball thermal resistance (typical)	θ_{JB}	2.8	°C/W

Note: Refer to Section 1.8, "System Design Information," for more details about thermal management.

Table 4 provides the DC electrical characteristics for the 603e.

Table 4. DC Electrical Specifications

Vdd = AVdd = 3.3 ± 5% V dc, OVdd = 3.3 ± 5% V dc, GND = 0 V dc, $0 \le T_j \le 105$ °C

Characteristic	Symbol	Min	Max	Unit	Notes
Input high voltage (all inputs except SYSCLK)	V_{IH}	2.0	5.5	V	
Input low voltage (all inputs except SYSCLK)	V_{IL}	-0.3	0.8	V	
SYSCLK input high voltage	CV_{IH}	2.4	5.5	V	
SYSCLK input low voltage	CV_{IL}	-0.3	0.4	V	
Input leakage current, V_{in} = 3.465 V	I_{in}	—	10	μA	1
V_{in} = 5.5 V	I_{in}	—	245	μA	1
Hi-Z (off-state) leakage current, V_{in} = 3.465 V	I_{TSI}	—	10	μA	1
V_{in} = 5.5 V	I_{TSI}	—	245	μA	1

Table 4. DC Electrical Specifications (Continued)

Vdd = AVdd = 3.3 ± 5% V dc, OVdd = 3.3 ± 5% V dc, GND = 0 V dc, 0 ≤ T$_j$ ≤ 105 °C

Characteristic	Symbol	Min	Max	Unit	Notes
Output high voltage, I$_{OH}$ = –9 mA	V$_{OH}$	2.4	—	V	1
Output low voltage, I$_{OL}$ = 14 mA	V$_{OL}$	—	0.4	V	
Capacitance, V$_{in}$ = 0 V, f = 1 MHz (excludes $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, and $\overline{ARTRY}$)	C$_{in}$	—	10.0	pF	2
Capacitance, V$_{in}$ = 0 V, f = 1 MHz (for $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, and $\overline{ARTRY}$)	C$_{in}$	—	15.0	pF	2

Notes:

1. Excludes test signals (LSSD_MODE, L1_TSTCLK, L2_TSTCLK) and JTAG signals.

2. Capacitance is periodically sampled rather than 100% tested.

Table 5 provides the power consumption for the 603e.

Table 5. Power Consumption

Vdd = AVdd = 3.3 ± 5% V dc, OVdd = 3.3 ± 5% V dc, GND = 0 V dc, 0 ≤ T$_j$ ≤ 105 °C

CPU Clock: SYSCLK	Processor (CPU) Frequency			Unit	Notes
	100 MHz	120 MHz	133.33 MHz		
Full-On Mode (DPM Enabled)					
Typical	3.2	3.9	4.2	W	1, 3
Max.	4.0	4.8	5.3	W	1, 2
Doze Mode					
Typical	1.0	1.2	1.3	W	1, 2
Nap Mode					
Typical	70	80	85	mW	1, 2
Sleep Mode					
Typical	40	45	50	mW	1, 2
Sleep Mode—PLL Disabled					
Typical	5	6	6	mW	1, 2
Sleep Mode—PLL and SYSCLK Disabled					
Typical	3	3	3	mW	1, 2

Notes:

1. These values apply for all valid bus ratios (PLL_CFG[0–3] settings). The values do not include I/O supply power (OVdd) or PLL supply power (AVdd). OVdd power is system dependent, but is typically <10% of Vdd power. Worst-case power consumption for AVdd = 15 mw.

2. Maximum power is measured at Vdd = 3.465 V using a worst-case instruction mix.

3. Typical power is an average value measured at Vdd = AVdd = OVdd = 3.3 V in a system executing typical applications and benchmark sequences

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1.4.2 AC Electrical Characteristics

This section provides the AC electrical characteristics for the 603e. After fabrication, parts are sorted by maximum processor core frequency as shown in Section 1.4.2.1, "Clock AC Specifications" and tested for conformance to the AC specifications for that frequency. These specifications are for 100, 120, and 133.33 MHz processor core frequencies. The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG[0–3] signals. Parts are sold by maximum processor core frequency; see Section 1.9, "Ordering Information."

1.4.2.1 Clock AC Specifications

Table 6 provides the clock AC timing specifications as defined in Figure 1.

Table 6. Clock AC Timing Specifications

Vdd = AVdd = 3.3 ± 5% V dc, OVdd = 3.3 ± 5% V dc, GND = 0 V dc, 0 ≤ T_j ≤ 105 °C

Num	Characteristic	100 MHz		120 MHz		133.33 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max		
	Processor frequency	16.67	100	16.67	120	16.67	133.33	MHz	1
	VCO frequency	100	200	120	240	133.33	266.66	MHz	1
	SYSCLK (bus) frequency	16.67	66.67	16.67	66.67	16.67	66.67	MHz	
1	SYSCLK cycle time	15.0	60.0	15.0	60.0	15.0	60.0	ns	
2,3	SYSCLK rise and fall time	—	2.0	—	2.0	—	2.0	ns	2
4	SYSCLK duty cycle measured at 1.4 V	40.0	60.0	40.0	60.0	40.0	60.0	%	3
	SYSCLK jitter	—	±150	—	±150	—	±150	ps	4
	Internal PLL relock time	—	100	—	100	—	100	μs	3, 5

Notes:

1. **Caution:** The SYSCLK frequency and PLL_CFG[0–3] settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0–3] signal description in Section 1.8, "System Design Information," for valid PLL_CFG[0–3] settings.

2. Rise and fall times for the SYSCLK input are measured from 0.4 V to 2.4 V.

3. Timing is guaranteed by design and characterization, and is not tested.

4. Cycle-to-cycle jitter, and is guaranteed by design.

5. Relock timing is guaranteed by design and characterization, and is not tested. PLL-relock time is the maximum amount of time required for PLL lock after a stable Vdd and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that HRESET must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.

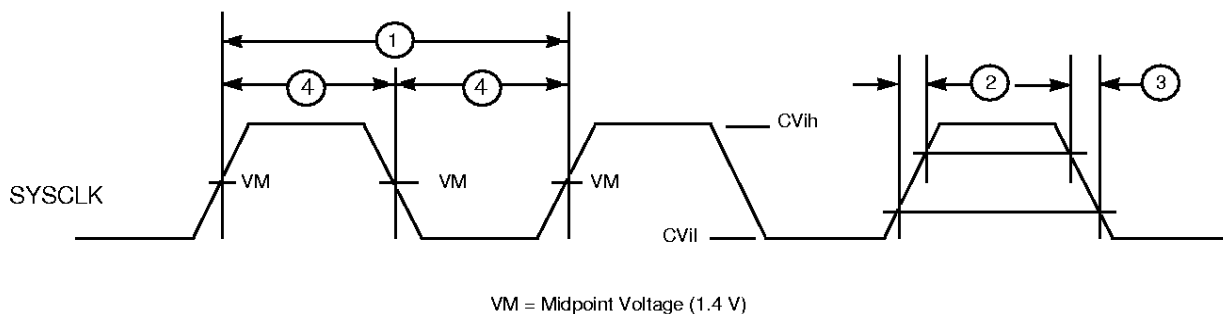Figure 1 provides the SYSCLK input timing diagram.

VM = Midpoint Voltage (1.4 V)

Figure 1. SYSCLK Input Timing Diagram

1.4.2.2 Input AC Specifications

Table 7 provides the input AC timing specifications for the 603e as defined in Figure 2 and Figure 3.

Table 7. Input AC Timing Specifications

Vdd = AVdd = 3.3 ± 5% V dc, OVdd = 3.3 ± 5% V dc, GND = 0 V dc, 0 ≤ T_j ≤ 105 °C

Num	Characteristic	100 MHz		120 MHz		133.33 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max		
10a	Address/data/transfer attribute inputs valid to SYSCLK (input setup)	3.0	—	3.0	—	3.0	—	ns	2
10b	All other inputs valid to SYSCLK (input setup)	5.0	—	5.0	—	5.0	—	ns	3
10c	Mode select inputs valid to $\overline{\text{HRESET}}$ (input setup) (for $\overline{\text{DRTRY}}$, $\overline{\text{QACK}}$ and $\overline{\text{TLBISYNC}}$)	$8*t_{sysclk}$	—	$8*t_{sysclk}$	—	$8*t_{sysclk}$	—	ns	4,5,6,7
11a	SYSCLK to address/data/transfer attribute inputs invalid (input hold)	1.0	—	1.0	—	1.0	—	ns	2
11b	SYSCLK to all other inputs invalid (input hold)	1.0	—	1.0	—	1.0	—	ns	3
11c	$\overline{\text{HRESET}}$ to mode select inputs invalid (input hold) (for $\overline{\text{DRTRY}}$, $\overline{\text{QACK}}$, and $\overline{\text{TLBISYNC}}$)	0	—	0	—	0	—	ns	4,6,7

Notes:

1. All input specifications are measured from the TTL level (0.8 or 2.0 V) of the signal in question to the 1.4 V of the rising edge of the input SYSCLK (see Figure 2). Both input and output timings are measured at the pin.

2. Address/data/transfer attribute input signals are composed of the following—A[0–31], AP[0–3], TT[0–4], TC[0–1], $\overline{\text{TBST}}$, TSIZ[0–2], $\overline{\text{GBL}}$, DH[0–31], DL[0–31], DP[0–7].

3. All other input signals are composed of the following— $\overline{\text{TS}}$, $\overline{\text{ABB}}$, $\overline{\text{DBB}}$, $\overline{\text{ARTRY}}$, $\overline{\text{BG}}$, $\overline{\text{AACK}}$, $\overline{\text{DBG}}$, $\overline{\text{DBWO}}$, $\overline{\text{TA}}$, $\overline{\text{DRTRY}}$, $\overline{\text{TEA}}$, $\overline{\text{DBDIS}}$, $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$, $\overline{\text{INT}}$, $\overline{\text{SMI}}$, $\overline{\text{MCP}}$, $\overline{\text{TBEN}}$, $\overline{\text{QACK}}$, $\overline{\text{TLBISYNC}}$.

4. The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$ (see Figure 3).

5. t_{sysclk} is the period of the external clock (SYSCLK) in nanoseconds.

6. These values are guaranteed by design, and are not tested.

7. This specification is for configuration mode select only. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.

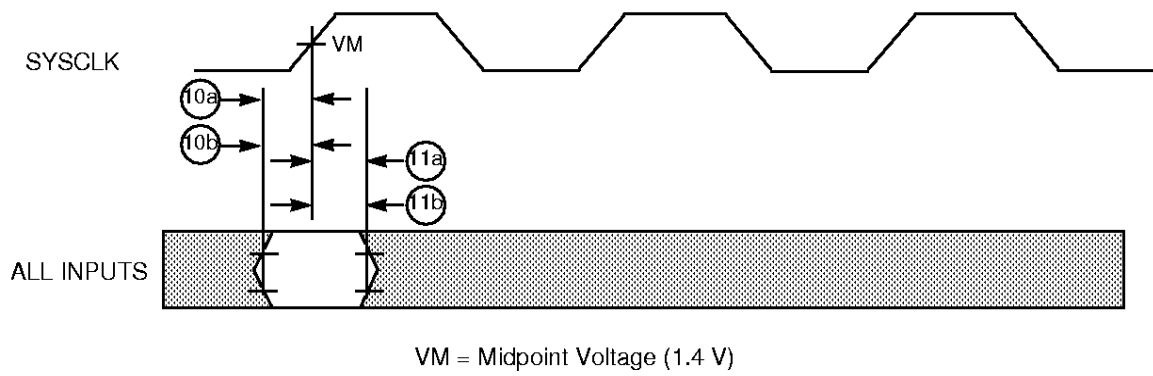Figure 2 provides the input timing diagram for the 603e.

VM = Midpoint Voltage (1.4 V)

Figure 2. Input Timing Diagram

Figure 3 provides the mode select input timing diagram for the 603e.

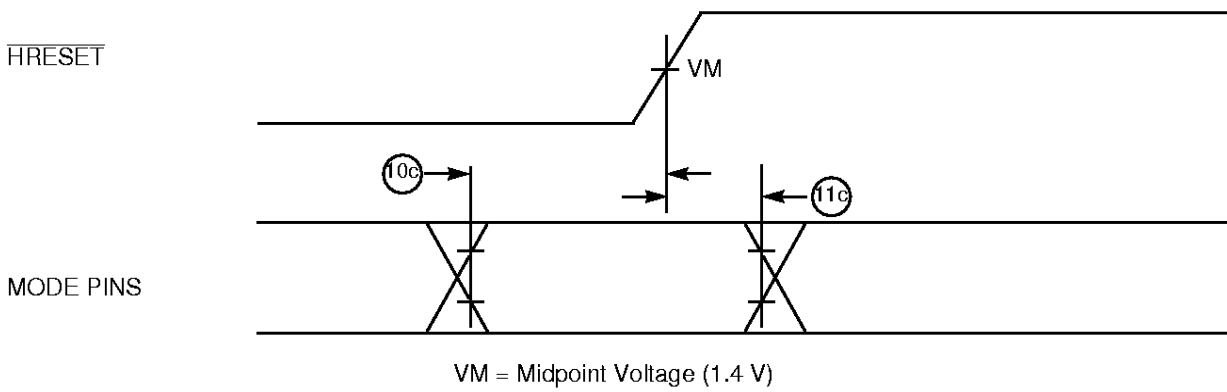VM = Midpoint Voltage (1.4 V)

Figure 3. Mode Select Input Timing Diagram

1.4.2.3 Output AC Specifications

Table 8 provides the output AC timing specifications for the 603e as defined in Figure 4.

Table 8. Output AC Timing Specifications[1]

Vdd = AVdd = 3.3 ± 5% V dc, OVdd = 3.3 ± 5% V dc, GND = 0 V dc, 0 ≤ T$_j$ ≤ 105 °C, C$_L$ = 50 pF[2]

Num	Characteristic	100 MHz		120 MHz		133.33 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max		
12	SYSCLK to output driven (output enable time)	1.0	—	1.0	—	1.0	—	ns	
13a	SYSCLK to output valid (5.5 V to 0.8 V—$\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$)	—	11.0	—	11.0	—	11.0	ns	4
13b	SYSCLK to output valid ($\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$)	—	10.0	—	10.0	—	10.0	ns	6
14a	SYSCLK to output valid (5.5 V to 0.8 V—all except $\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$)	—	13.0	—	13.0	—	13.0	ns	4
14b	SYSCLK to output valid (all except $\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$)	—	11.0	—	11.0	—	11.0	ns	6
15	SYSCLK to output invalid (output hold)	1.5	—	1.5	—	1.5	—	ns	3
16	SYSCLK to output high impedance (all except $\overline{ARTRY}$, $\overline{ABB}$, $\overline{DBB}$)	—	9.5	—	9.5	—	9.5	ns	
17	SYSCLK to $\overline{ABB}$, $\overline{DBB}$, high impedance after precharge	—	1.2	—	1.2	—	1.2	t$_{sysclk}$	5,7
18	SYSCLK to $\overline{ARTRY}$ high impedance before precharge	—	9.0	—	9.0	—	9.0	ns	
19	SYSCLK to $\overline{ARTRY}$ precharge enable	0.2 * t$_{sysclk}$ + 1.0	—	0.2 * t$_{sysclk}$ + 1.0	—	0.2 * t$_{sysclk}$ + 1.0	—	ns	3,5,8
20	Maximum delay to $\overline{ARTRY}$ precharge	—	1.2	—	1.2	—	1.2	t$_{sysclk}$	5,8
21	SYSCLK to $\overline{ARTRY}$ high impedance after precharge	—	2.25	—	2.25	—	2.25	t$_{sysclk}$	5,8

Notes:

1. All output specifications are measured from the 1.4 V of the rising edge of SYSCLK to the TTL level (0.8 V or 2.0 V) of the signal in question. Both input and output timings are measured at the pin (see Figure 4).

2. All maximum timing specifications assume C$_L$ = 50 pF.

3. This minimum parameter assumes C$_L$ = 0 pF.

4. SYSCLK to output valid (5.5 V to 0.8 V) includes the extra delay associated with discharging the external voltage from 5.5 V to 0.8 V instead of from Vdd to 0.8 V (5 V CMOS levels instead of 3.3 V CMOS levels).

5. t$_{sysclk}$ is the period of the external bus clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in nanoseconds) of the parameter in question.

6. Output signal transitions from GND to 2.0 V or Vdd to 0.8 V.

7. Nominal precharge width for $\overline{ABB}$ and $\overline{DBB}$ is 0.5 t$_{sysclk}$.

8. Nominal precharge width for $\overline{ARTRY}$ is 1.0 t$_{sysclk}$.

Figure 4 provides the output timing diagram for the 603e.

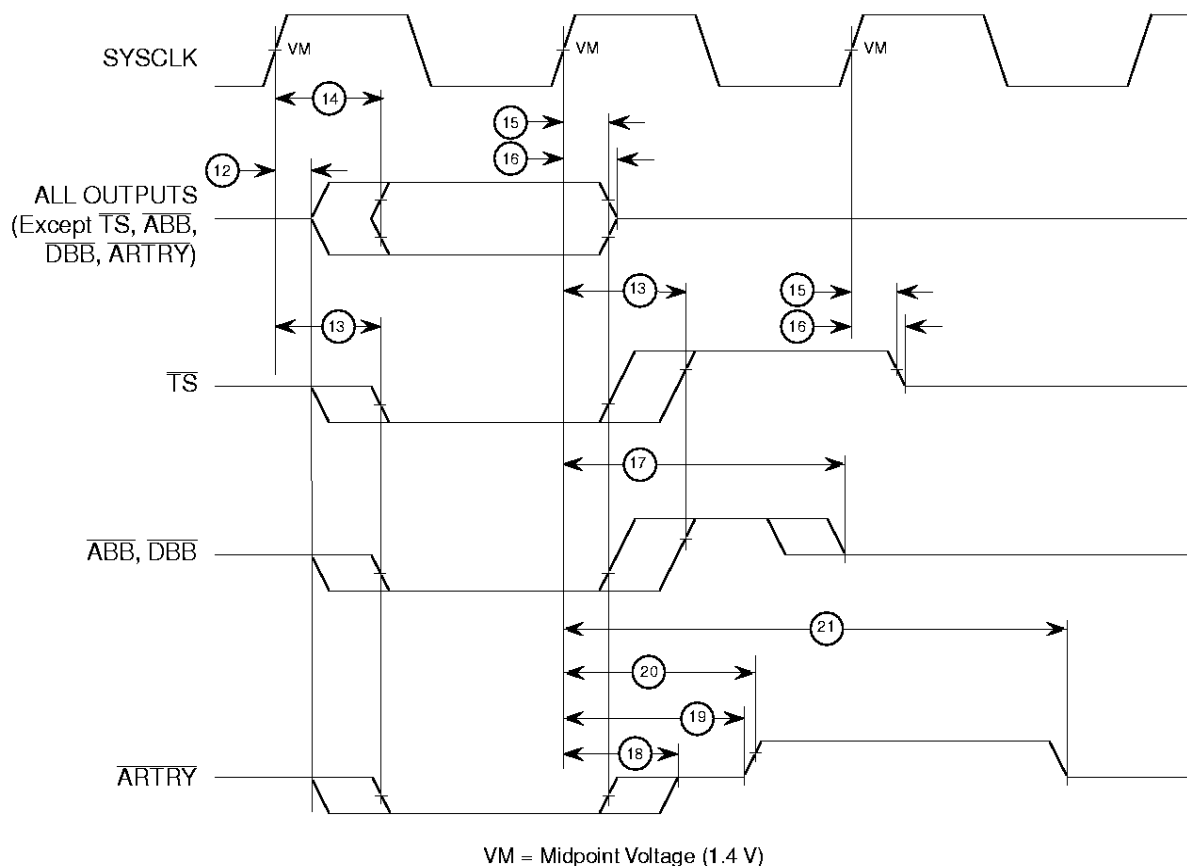VM = Midpoint Voltage (1.4 V)

Figure 4. Output Timing Diagram

1.4.3 JTAG AC Timing Specifications

Table 9 provides the JTAG AC timing specifications as defined in Figure 5 through Figure 8.

Table 9. JTAG AC Timing Specifications (Independent of SYSCLK)

Vdd = AVdd = 3.3 ± 5% V dc, OVdd = 3.3 ± 5% V dc, GND = 0 V dc, $0 \leq T_j \leq 105\ °C$, C_L = 50 pF

Num	Characteristic	Min	Max	Unit	Notes
	TCK frequency of operation	0	16	MHz	
1	TCK cycle time	62.5	—	ns	
2	TCK clock pulse width measured at 1.4 V	25	—	ns	
3	TCK rise and fall times	0	3	ns	
4	TRST setup time to TCK rising edge	13	—	ns	1
5	TRST assert time	40	—	ns	
6	Boundary-scan input data setup time	6	—	ns	2
7	Boundary-scan input data hold time	27	—	ns	2
8	TCK to output data valid	4	25	ns	3

Vdd = AVdd = 3.3 ± 5% V dc, OVdd = 3.3 ± 5% V dc, GND = 0 V dc, $0 \leq T_j \leq 105\,°C$, C_L = 50 pF

Num	Characteristic	Min	Max	Unit	Notes
9	TCK to output high impedance	3	24	ns	3
10	TMS, TDI data setup time	0	—	ns	
11	TMS, TDI data hold time	25	—	ns	
12	TCK to TDO data valid	4	24	ns	
13	TCK to TDO high impedance	3	15	ns	

Notes:

1. $\overline{\text{TRST}}$ is an asynchronous signal. The setup time is for test purposes only.

2. Non-test signal input timing with respect to TCK.

3. Non-test signal output timing with respect to TCK.
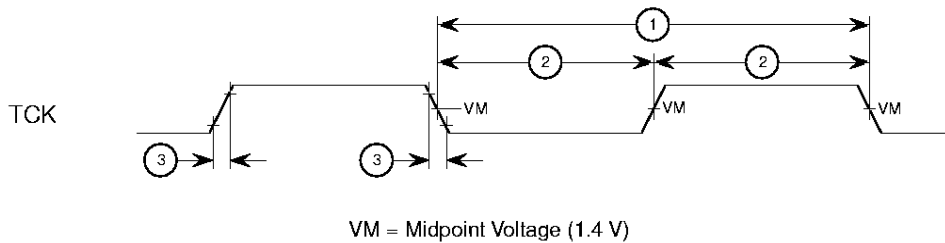
Figure 5 provides the JTAG clock input timing diagram.

VM = Midpoint Voltage (1.4 V)

Figure 5. JTAG Clock Input Timing Diagram

Figure 6 provides the $\overline{\text{TRST}}$ timing diagram.
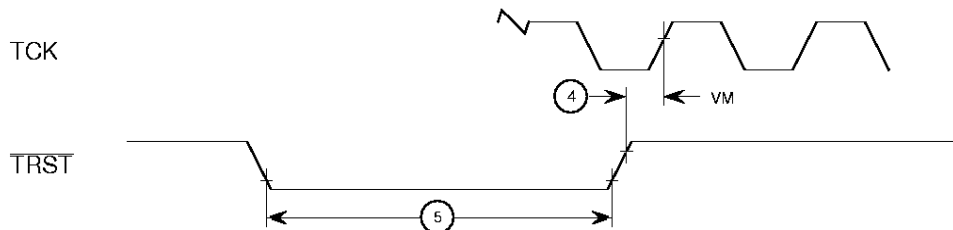

Figure 6. $\overline{\text{TRST}}$ Timing Diagram

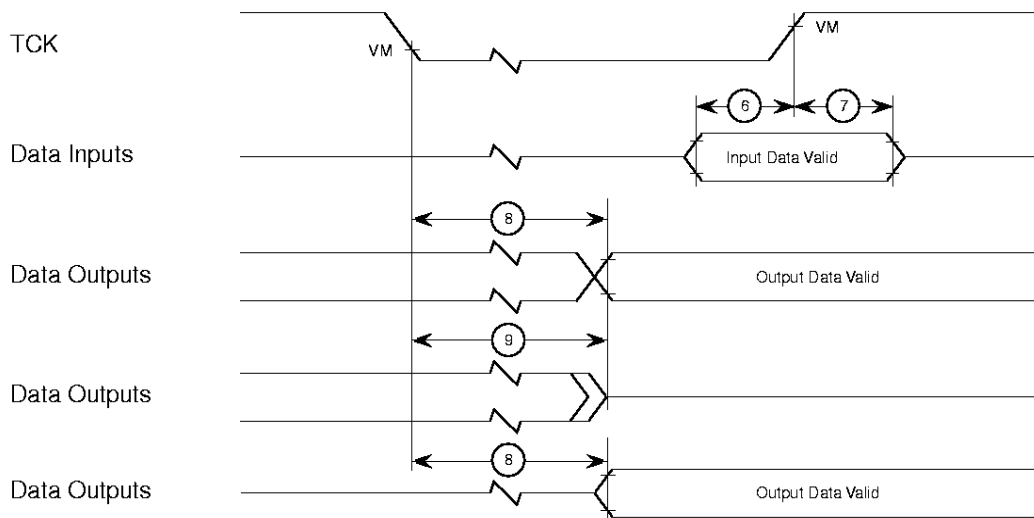Figure 7 provides the boundary-scan timing diagram.

Figure 7. Boundary-Scan Timing Diagram
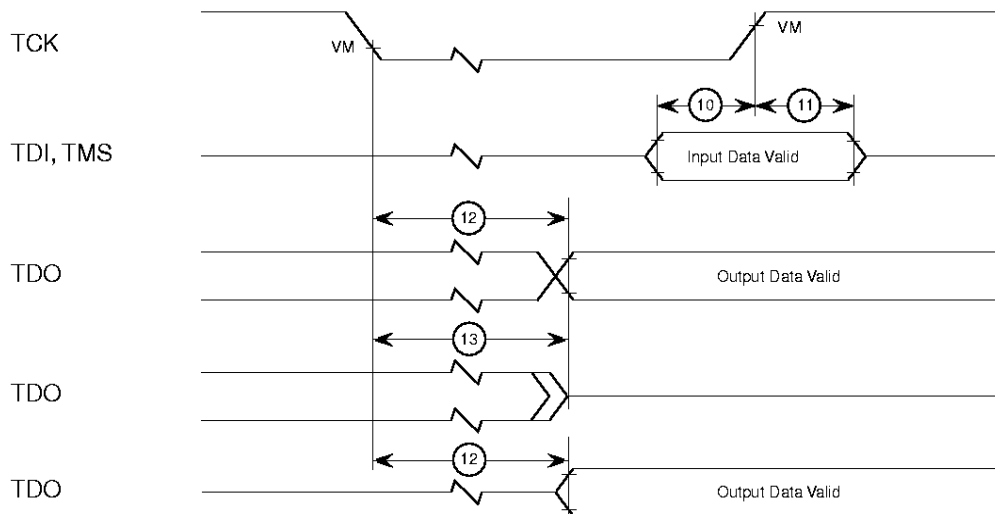
Figure 8 provides the test access port timing diagram.

Figure 8. Test Access Port Timing Diagram

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