**PowerPC**™

# PowerPC 603
# RISC Microprocessor

## Highlights

**Power Management Unit**
- Static low-power design
- Dynamic power management
- Hardware support for power saving modes
- Processor clock multiplier of 1x, 1.5x, 2x, 2.5x, 3x, 3.5x, and 4x from bus clock

**Instruction Fetching & Branch Unit**
- 6-instruction prefetch queue
- Static branch prediction

**Dispatch Unit**
- Dispatches 2 instuctions per cycle
- 4-stage pipeline: Fetch, Dispatch, Execute, and Complete

**Load/Store Unit**
- One cycle cache access

**Fixed-Point Execution Unit**
- One cycle add, subtract, shift, or rotate
- Hardware multiply and divide

- Thirty-two 32-bit General Purpose Registers

**Floating-Point Unit**
- Optimized for single-precision multiply/add
- IEEE-754 standard single- and double-precision floating point arithmetic
- Thirty-two 32-bit General Purpose Registers

**System Unit**
- Executes Condition Register logical, special register transfer, and other system instructions
- Execute integer add/compare instructions

**Memory Management Unit**
- 52-bit virtual and 32-bit real addressing
- 8 Block Address Translation registers
- 64-entry, 2-way data and instruction TLB
- Fast-trap mechanism for software reload TLB
- Support Big/Little-endian addressing

## Product Description

The PowerPC 603™ microprocessor is a 32-bit implementation of the PowerPC™ family of Reduced Instruction Set Computer (RISC) microprocessors. The PowerPC 603 microprocessor provides both industry leading RISC performance and power management to the notebook and energy sensitive desktop markets. High performance is achieved through concurrent execution of up to five instructions in five parallel execution units: the fixed-point unit, floating point unit, branch unit, system unit, and load/store unit. Low-power is delivered through a low power static design and dynamic power management with three power saving modes. It is this industry segment leading combination of high performance and low power that offers a competitive edge to the system developers using the PowerPC 603 microprocessor.

The 100 MHz version extends the performance leadership of the PowerPC 603 microprocessor in notebooks and energy sensitive desktops. The design, enhanced for higher speed and performance, contains twice the cache size of the original PowerPC 603 microprocessor and extends its speed from 80 MHz to 100 MHz.

The PowerPC Architecture™ is derived from IBM's Performance Optimized With Enhanced RISC (POWER™) architecture. The PowerPC Architecture shares all the benefits of POWER and is optimized for single-chip implementations.
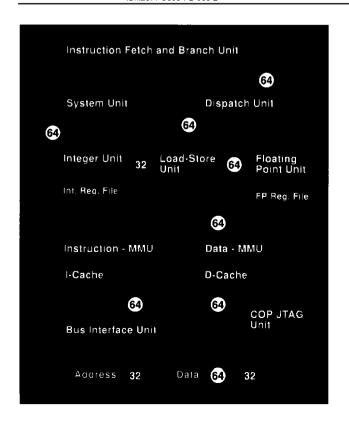
IBM

## Highlights (cont'd)

### Cache Unit
- 16k, 4 way or 8k, 2 way set associative instruction cache
- 16k, 4 way or 8k, 2 way set associative data cache
- 3-state coherency
- Physically tagged and addressed
- Copy-back data cache
- Data coherency in hardware

### Bus Interface Unit
- General purpose interface for a wide range of system configurations
- 32-bit address and 64- or 32-bit data bus
- Powerful diagnostic and test interface through the Common On-Chip Processor (COP) and IEEE 1149.1 (JTAG) interface.

## Specifications

| | 66 & 80 MHz | 100 MHz |
|---|---|---|
| Technology | 0.5μm CMOS, four levels of metal | 0.5μm CMOS, four levels of metal |
| Die Size | 7.4mm x 11.5mm (85 mm²) | 8.4mm x 11.67mm (98 mm²) |
| Number of Transistors | ~ 1.6 million | ~ 2.6 million |
| Temperature Range (Tj) | 0° C to 105° C | 0° C to 105° C |
| Performance | 75 SPECint92, 65 SPECfp92 @ 80 MHz<br>62 SPECint92, 54 SPECfp92 @ 66 MHz | 120 SPECint92, 105 SPECfp92 @ 100 MHz (est.) |
| Signal I/O | 165 | 165 |
| Power Supply | 3.3 V ± 5% | 3.3 V ± 5% |
| Power Dissipation (typ.) | 2.5 W @ 80 MHz,<br>2.2 W @ 66.67 MHz | 3 @ 100 MHz |
| Packaging | C4 Ceramic quad flat pack (240 pins) | C4 Ceramic quad flat pack (240 pins) Ball Grid Array (16 x 16) |
| Part Numbers | IBM25PPC603-FE-080-2<br>IBM25PPC603-FE-066-2 | IBM25PPC603E-FA-100-2 |



**IBM**

### For more information, contact: