FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-13745-1E

16-bit Microcontroller

CMOS

F²MC-16LX MB90925 Series

MB90F927/F927S/V925-101/V925-102

■ DESCRIPTION

MB90925 series is a 16-bit general-purpose high-capacity microcontroller designed for vehicle meter control applications etc.

The instruction set retains the same AT architecture as F²MC-8L and F²MC-16L series, with further refinements including high-level language instructions, expanded addressing mode, enhanced signed multiplication and division computation and bit processing.

In addition, a 32-bit accumulator is built in to enable long word processing.

Note : F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

■ FEATURES

- Clock
  Built-in PLL clock frequency multiplication circuit.
  Selection of machine clocks (PLL clocks) is allowed among frequency division by 2 on oscillation clock and multiplication of 1 to 4 times of oscillation clock(for 4 MHz oscillation clock, 4 MHz to 16 MHz).
  Operation by sub clock(up to 50 kHz : 100 kHz oscillation clock divided by 2).

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Be sure to refer to the “Check Sheet” for the latest cautions on development.

“Check Sheet” is seen at the following support page
URL : http://www.fujitsu.com/global/services/microelectronics/product/micom/support/index.html

“Check Sheet” lists the minimal requirement items to be checked to prevent problems beforehand in system development.

FUJITSU

- 16-bit input capture (4 channels)
  Detects rising, falling, or both edges.
  16-bit capture register × 4
  Pin input edge detection latches the 16-bit free-run timer counter value, and generates an interrupt request.
- 16-bit reload timer (2 channels)
  16-bit reload timer operation (select toggle output or one-shot output)
  Event count function selection provided
- Real Time watch timer (main clock)
  Operates directly from oscillator clock.
  Interrupt can be generated by second/minute/hour/date counter overflow.
- 16-bit PPG (3 channels)
  Output pins (3 channels) , external trigger input pin (1 channel)
  Output clock frequencies : f_{CP}, $f_{CP}/2^2$, $f_{CP}/2^4$, $f_{CP}/2^6$
- Delay interrupt
  Generates interrupt for task switching.
  Interrupts to CPU can be generated/deleted by software setting.
- External interrupts (8 channels)
  8-channel independent operation
  Interrupt source setting available : “L” to “H” edge/ “H” to “L” edge/ “L” level/ “H” level.
- A/D converter
  10-bit or 8-bit resolution × 8 channels (input multiplexed)
  Conversion time : 2.6µs (at f_{CP} = 16 MHz)
  External trigger startup available (P50/INT0/ADTG)
  Internal timer startup available (16-bit reload timer 1)
- UART(LIN/SCI) (2 channels)
  Equipped with full duplex double buffer
  Clock-asynchronous or clock-synchronous serial transfer is available
- SIO (1 channel)
  Clock synchronized data transmission.
  LSB-first or MSB-first data transfer selection is available.
- CAN interface
  Conforms to CAN specifications version 2.0 Part A and B.
  Automatic resend in case of error.
  Automatic transfer in response to remote frame.
  16 prioritized message buffers for data and ID
  Multiple message support
  Receiving filter has flexible configuration : Full bit compare/full bit mask/two partial bit masks
  Supports up to 1 Mbps
  CAN WAKEUP function (connects RX internally to INT0)
- LCD controller/driver (32 segment x 4 common)
  Segment driver and command driver with direct LCD panel (display) drive capability
- Low voltage/Program looping detect reset
  Automatic reset when low voltage is detected
  Program looping detection function

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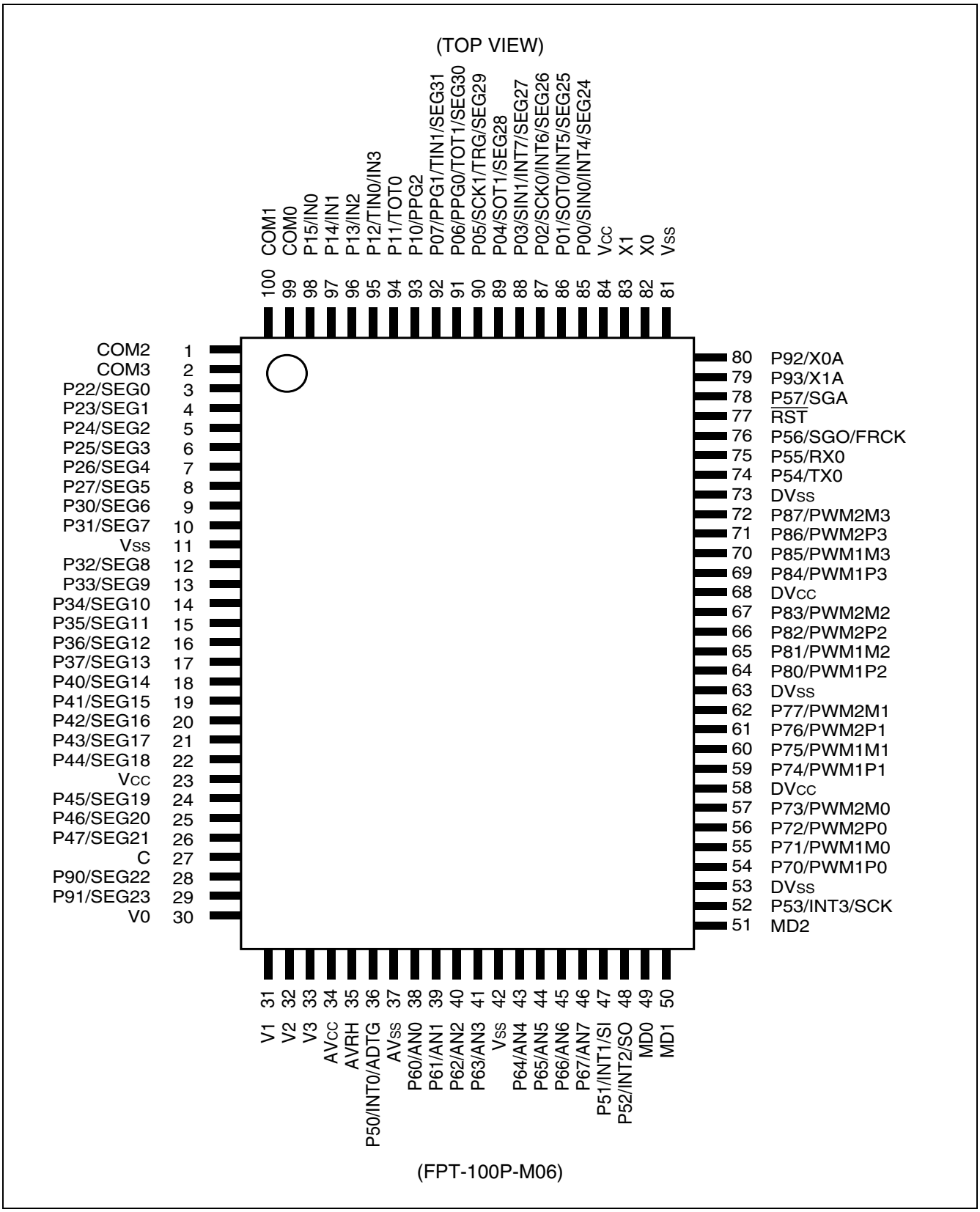
- Stepping motor controller (4 channels)
  High current output for each channel × 4
  Synchronized 8/10-bit PWM for each channel × 2
- Sound generator
  8-bit PWM signal mixed with tone frequency from 8-bit reload counter.
  PWM frequencies : 62.5 kHz, 31.2 kHz, 15.6 kHz, 7.8 kHz (at f_{CP} = 16 MHz)
  Tone frequencies : 1/2 PWM frequency, divided by (reload frequency +1)
- Input/output ports
  General-purpose input/output port (CMOS output)
  - 70 ports (dual clock system)
  - 72 ports (single clock system)
- Input level select function for port
  Automotive/CMOS-Schmitt (initial level is Automotive in single chip mode)
- Flash memory security function
  Protect the content of Flash memory (Flash memory product only)

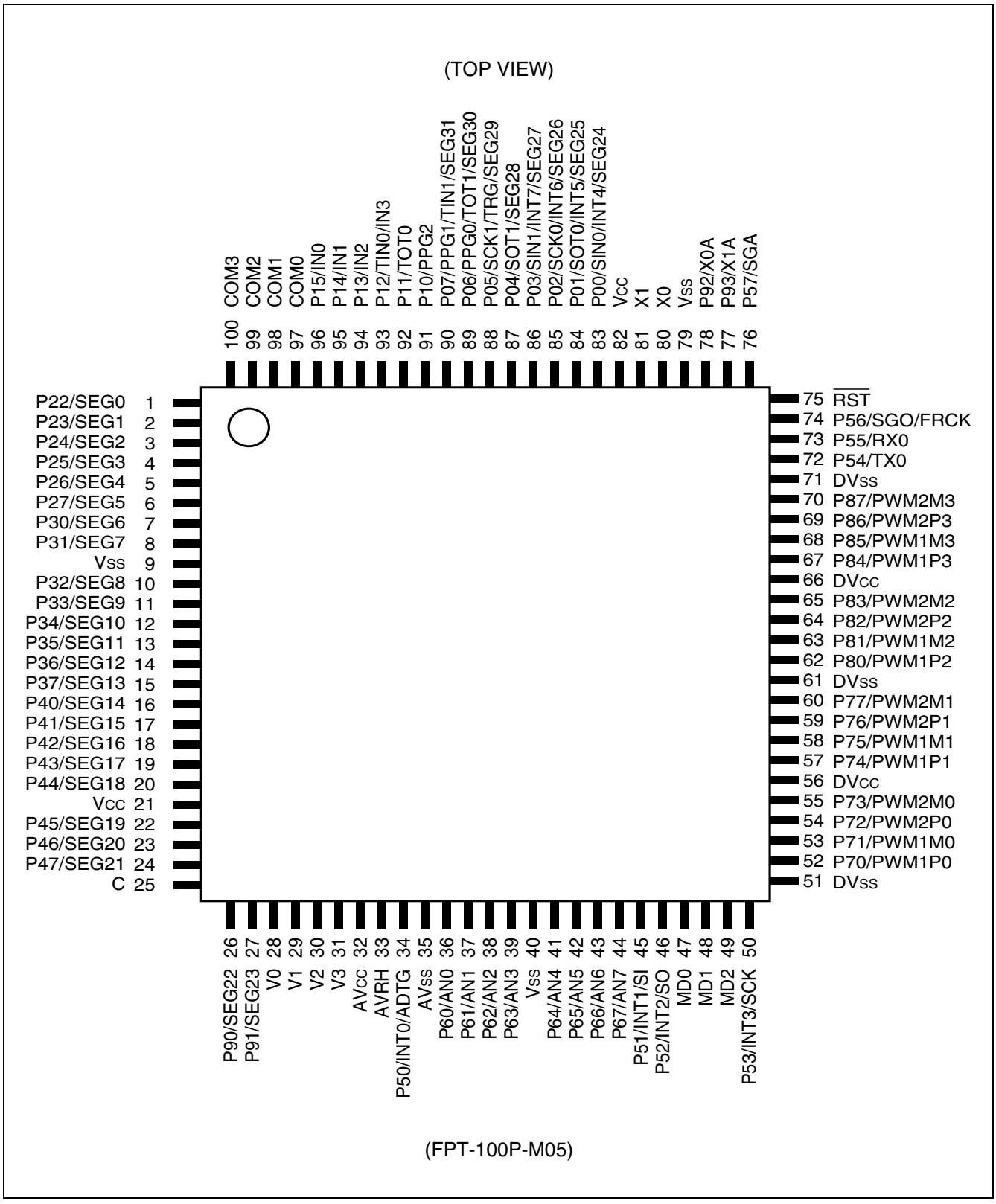
■ PRODUCT LINEUP

Part number / Parameter	MB90F927	MB90F927S	MB90V925-101	MB90V925-102
Type	Flash memory product		Evaluation product	
CPU	F²MC-16LX CPU			
System clock	PLL clock multiplier circuit (× 1, × 2, × 3, × 4, 1/2 when PLL stopped) Minimum instruction execution time 62.5 ns (with 4 MHz oscillation clock × 4)			
Sub clock pin (X0A, X1A)	Yes	No		Yes
ROM	Flash memory 64 Kbytes		External	
RAM	4 Kbytes		13.5 Kbytes	
I/O port	70 ports	72 ports		70 ports
SIO	1 channel			
LCD segment	32			
UART	UART(LIN/SCI) 2 channels			
CAN interface	1 channel			
16-bit input capture	4 channels			
16-bit reload timer	2 channels			
16-bit free-run timer	1 channel			
Real time watch timer	1 channel			
16-bit PPG	3 channels			
External interrupt	8 channels			
8/10-bit A/D converter	8 channels			
LVD/CPU loop reset	Yes		No	
Stepping motor controller	4 channels			
Sound generator	1 channel			
Flash memory security	Yes		No	
Operation voltage	3.7 V to 5.5 V		4.5 V to 5.5 V	
Packages	QFP-100, LQFP-100		PGA-299	

■ PIN ASSIGNMENTS



(FPT-100P-M06)


(TOP VIEW)
100 COM3
99 COM2
98 COM1
97 COM0
96 P15/IN0
95 P14/IN1
94 P13/IN2
93 P12/TIN0/IN3
92 P11/TOT0
91 P10/PPG2
90 P07/PPG1/TIN1/SEG31
89 P06/PPG0/TOT1/SEG30
88 P05/SCK1/TRG/SEG29
87 P04/SOT1/SEG28
86 P03/SIN1/INT7/SEG27
85 P02/SCK0/INT6/SEG26
84 P01/SOT0/INT5/SEG25
83 P00/SIN0/INT4/SEG24
82 VCC
81 X1
80 X0
79 VSS
78 P92/X0A
77 P93/X1A
76 P57/SGA
1 P22/SEG0
2 P23/SEG1
3 P24/SEG2
4 P25/SEG3
5 P26/SEG4
6 P27/SEG5
7 P30/SEG6
8 P31/SEG7
9 VSS
10 P32/SEG8
11 P33/SEG9
12 P34/SEG10
13 P35/SEG11
14 P36/SEG12
15 P37/SEG13
16 P40/SEG14
17 P41/SEG15
18 P42/SEG16
19 P43/SEG17
20 P44/SEG18
21 VCC
22 P45/SEG19
23 P46/SEG20
24 P47/SEG21
25 C
75 RST
74 P56/SGO/FRCK
73 P55/RX0
72 P54/TX0
71 DVSS
70 P87/PWM2M3
69 P86/PWM2P3
68 P85/PWM1M3
67 P84/PWM1P3
66 DVCC
65 P83/PWM2M2
64 P82/PWM2P2
63 P81/PWM1M2
62 P80/PWM1P2
61 DVSS
60 P77/PWM2M1
59 P76/PWM2P1
58 P75/PWM1M1
57 P74/PWM1P1
56 DVCC
55 P73/PWM2M0
54 P72/PWM2P0
53 P71/PWM1M0
52 P70/PWM1P0
51 DVSS
26 P90/SEG22
27 P91/SEG23
28 V0
29 V1
30 V2
31 V3
32 AVCC
33 AVRH
34 P50/INT0/ADTG
35 AVSS
36 P60/AN0
37 P61/AN1
38 P62/AN2
39 P63/AN3
40 VSS
41 P64/AN4
42 P65/AN5
43 P66/AN6
44 P67/AN7
45 P51/INT1/SI
46 P52/INT2/SO
47 MD0
48 MD1
49 MD2
50 P53/INT3/SCK

(FPT-100P-M05)

■ PIN DESCRIPTIONS

Pin no.		Pin name	I/O circuit type*3	Function
LQFP*1	QFP*2			
80	82	X0	A	High speed oscillator input pin
81	83	X1		High speed oscillator output pin
78	80	P92	G	General-purpose I/O port
		X0A	A	Low speed oscillator input pin. If no oscillator is connected, apply pull-down processing.
77	79	P93	G	General-purpose I/O port
		X1A	A	Low speed oscillator output pin. If no oscillator is connected, leave open.
75	77	$\overline{\text{RST}}$	B	Reset input pin
83	85	P00	J	General-purpose input/output port
		SIN0		UART ch.0 serial data input pin
		INT4		INT4 external interrupt input pin
		SEG24		LCD controller/driver segment output
84	86	P01	E	General-purpose input/output port
		SOT0		UART ch.0 serial data output pin
		INT5		INT5 external interrupt input pin
		SEG25		LCD controller/driver segment output
85	87	P02	E	General-purpose input/output port
		SCK0		UART ch.0 serial clock input/output pin
		INT6		INT6 external interrupt input pin
		SEG26		LCD controller/driver segment output
86	88	P03	J	General-purpose input/output port
		SIN1		UART ch.1 serial data input pin
		INT7		INT7 external interrupt input pin
		SEG27		LCD controller/driver segment output
87	89	P04	E	General-purpose input/output port
		SOT1		UART ch.1 serial data output pin
		SEG28		LCD controller/driver segment output
88	90	P05	E	General-purpose input/output port
		SCK1		UART ch.1 serial clock input/output pin
		TRG		16-bit PPG ch.0 to ch.2 external trigger input pin
		SEG29		LCD controller/driver segment output

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Pin no.		Pin name	I/O circuit type*3	Function
LQFP*1	QFP*2			
89	91	P06	E	General-purpose input/output port
		PPG0		16-bit PPG ch.0 output pin
		TOT1		16-bit reload timer ch.1 TOT output pin
		SEG30		LCD controller/driver segment output
90	92	P07	E	General-purpose input/output port
		PPG1		16-bit PPG ch.1 output pin
		TIN1		16-bit reload timer ch.1 TIN output pin
		SEG31		LCD controller/driver segment output
91	93	P10	G	General-purpose input/output port
		PPG2		16-bit PPG ch.2 output pin
92	94	P11	G	General-purpose input/output port
		TOT0		16-bit reload timer ch.0 TOT output pin
93	95	P12	G	General-purpose input/output port
		TIN0		16-bit reload timer ch.0 TIN output pin
		IN3		Input capture ch.3 trigger input pin
94 to 96	96 to 98	P13 to P15	G	General-purpose input/output port
		IN2 to IN0		Input capture ch.2 to ch.0 trigger input pins
97 to 100	99, 100, 1, 2	COM0 to COM3	I	LCD controller/driver common output pins
1 to 6	3 to 8	P22 to P27	E	General-purpose input/output ports
		SEG0 to SEG5		LCD controller/driver segment output pins
7, 8, 10 to 15	9, 10, 12 to 17	P30 to P37	E	General-purpose input/output port
		SEG6 to SEG13		LCD controller/driver segment output pins
16 to 20, 22 to 24	18 to 22, 24 to 26	P40 to P47	E	General-purpose input/output port
		SEG14 to SEG21		LCD controller/driver segment output pins
26, 27	28, 29	P90, P91	E	General-purpose input/output port
		SEG22, SEG23		LCD controller/driver segment output pins
34	36	P50	G	General-purpose input/output port
		INT0		INT0 external interrupt input pin
		ADTG		A/D converter external trigger input pin

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Pin no.		Pin name	I/O circuit type*3	Function
LQFP*1	QFP*2			
36 to 39, 41 to 44	38 to 41, 43 to 46	P60 to P67	F	General-purpose input/output port
		AN0 to AN7		A/D converter input pins
45	47	P51	K	General-purpose input/output port
		INT1		INT1 external interrupt input pin
		SI		SIO data input pin
46	48	P52	G	General-purpose input/output port
		INT2		INT2 external interrupt input pin
		SO		SIO data output pin
50	52	P53	G	General-purpose input/output port
		INT3		INT3 external interrupt input pin
		SCK		SIO clock input/output pin
52 to 55	54 to 57	P70 to P73	H	General-purpose input/output port
		PWM1P0, PWM1M0, PWM2P0, PWM2M0		Stepping motor controller ch.0 output pins
57 to 60	59 to 62	P74 to P77	H	General-purpose input/output port
		PWM1P1, PWM1M1, PWM2P1, PWM2M1		Stepping motor controller ch.1 output pins
62 to 65	64 to 67	P80 to P83	H	General-purpose input/output port
		PWM1P2, PWM1M2, PWM2P2, PWM2M2		Stepping motor controller ch.2 output pins
67 to 70	69 to 72	P84 to P87	H	General-purpose input/output port
		PWM1P3, PWM1M3, PWM2P3, PWM2M3		Stepping motor controller ch.3 output pins
72	74	P54	G	General-purpose input/output port
		TX0		CAN interface 0 TX output pin
73	75	P55	G	General-purpose output port
		RX0		CAN interface 0 RX input pin

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Pin no.		Pin name	I/O circuit type*3	Function
LQFP*1	QFP*2			
74	76	P56	G	General-purpose input/output port
		SGO		Sound generator SGO output pin
		FRCK		Free-run timer clock input pin
76	78	P57	G	General-purpose input/output port
		SGA		Sound generator SGA output pin
28 to 31	30 to 33	V0 to V3	—	LCD controller /driver reference power supply pins
56, 66	58, 68	DV_{CC}	—	Power supply input pins dedicated for high current output buffer (pin numbers 54 to 57, 59 to 62, 64 to 67, 69 to 72) .
51, 61, 71	53, 63, 73	DV_{SS}	—	Power supply GND pins dedicated for high current output buffer (pin numbers 54 to 57, 59 to 62, 64 to 67, 69 to 72) .
32	34	AV_{CC}	—	A/D converter dedicated power supply input pin
35	37	AV_{SS}	—	A/D converter dedicated power supply GND pin
33	35	AVRH	—	A/D converter Vref + input pin
47, 48	49, 50	MD0, MD1	C	Test mode input pins. Connect to V_{CC}.
49	51	MD2	C/D*4	Test mode input pin. Connect to V_{SS}.
25	27	C	—	External capacitor pin. Connect an 0.1 μF capacitor between this pin and V_{SS}.
21, 82	23, 84	V_{CC}	—	Power supply input pins
9, 40, 79	11, 42, 81	V_{SS}	—	Power supply GND pins

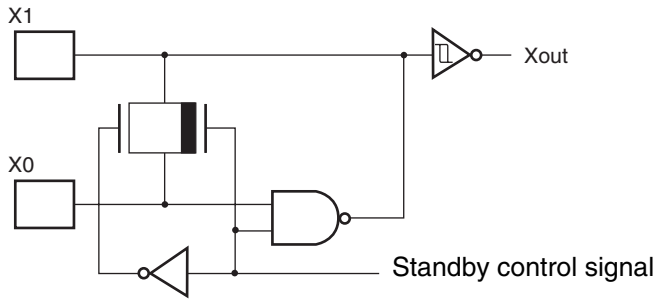
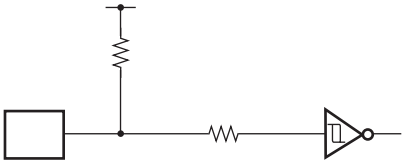
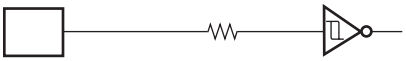
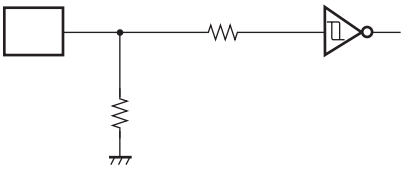
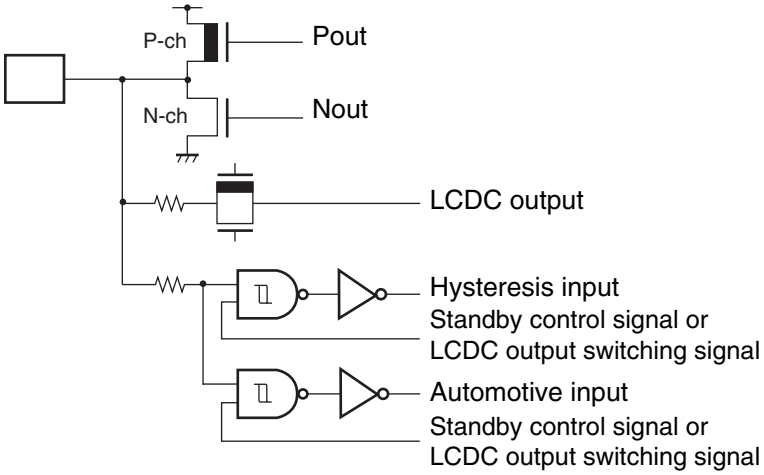
*1: FPT-100P-M05

*2: FPT-100P-M06

*3: For the I/O circuit type, refer to “■ I/O CIRCUIT TYPE”

*4: Type C in MB90F927 and MB90F927S, type D in MB90V925-101 and MB90V925-102.

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• High-speed oscillation pin Oscillation feedback resistance : approx. 1 MΩ (X0, X1 : MAIN) • Low-speed oscillation pin Oscillation feedback resistance : approx. 10 MΩ (X0A, X1A : SUB)
B		Input dedicated pin (with pull-up resistance) • Pull-up resistance attached : approx. 50 kΩ • Hysteresis input (V_{IH}/V_{IL} = 0.8V_{CC}/0.2V_{CC})
C		Input dedicated pin Hysteresis input (V_{IH}/V_{IL} = 0.8V_{CC}/0.2V_{CC})
D		Input dedicated pin (with pull-down resistance) • Pull-down resistance attached : approx. 50 kΩ • Hysteresis input (V_{IH}/V_{IL} = 0.8V_{CC}/0.2V_{CC})
E		LCDC output common general-purpose port • CMOS output (I_{OH}/I_{OL} = ± 4 mA) • Hysteresis input (V_{IH}/V_{IL} = 0.8V_{CC}/0.2V_{CC}) • Automotive input (V_{IH}/V_{IL} = 0.8V_{CC}/0.5V_{CC})

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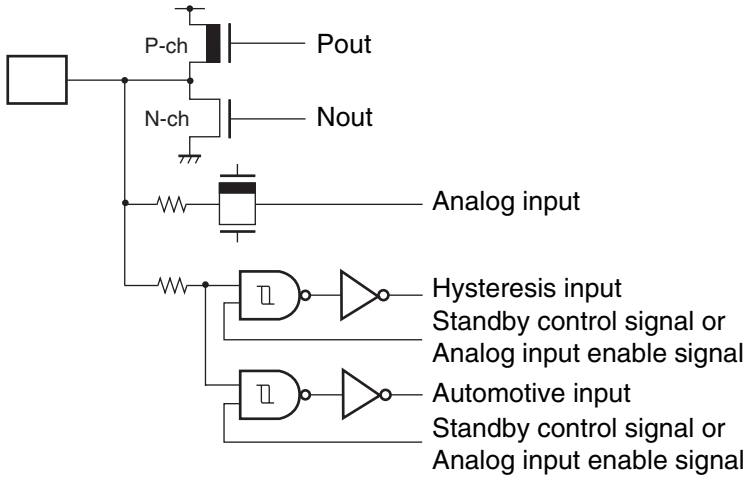
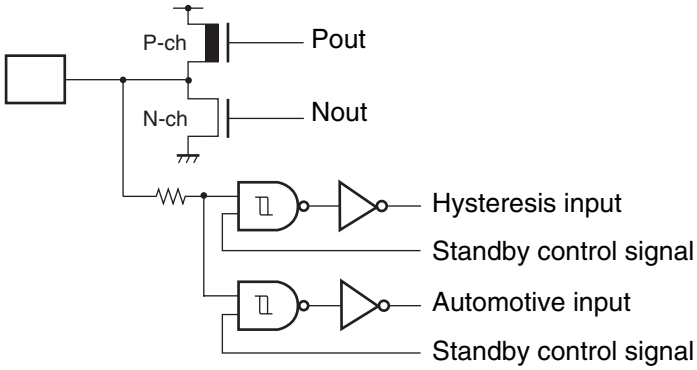
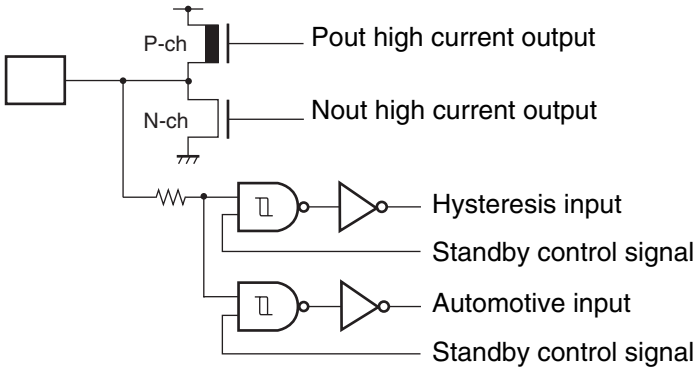
Type	Circuit	Remarks
F		A/D converter input common general-purpose port • CMOS output (I_{OH}/I_{OL} = ± 4 mA) • Hysteresis input (V_{IH}/V_{IL} = 0.8V_{CC}/0.2V_{CC}) • Automotive input (V_{IH}/V_{IL} = 0.8V_{CC}/0.5V_{CC})
G		General-purpose port • CMOS output (I_{OH}/I_{OL} = ± 4 mA) • Hysteresis input (V_{IH}/V_{IL} = 0.8V_{CC}/0.2V_{CC}) • Automotive input (V_{IH}/V_{IL} = 0.8V_{CC}/0.5V_{CC})
H		High current output common general-purpose port • CMOS output (I_{OH}/I_{OL} = ± 30 mA) • Hysteresis input (V_{IH}/V_{IL} = 0.8V_{CC}/0.2V_{CC}) • Automotive input (V_{IH}/V_{IL} = 0.8V_{CC}/0.5V_{CC})

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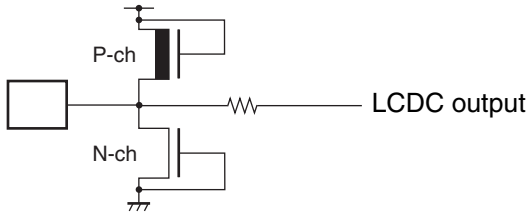
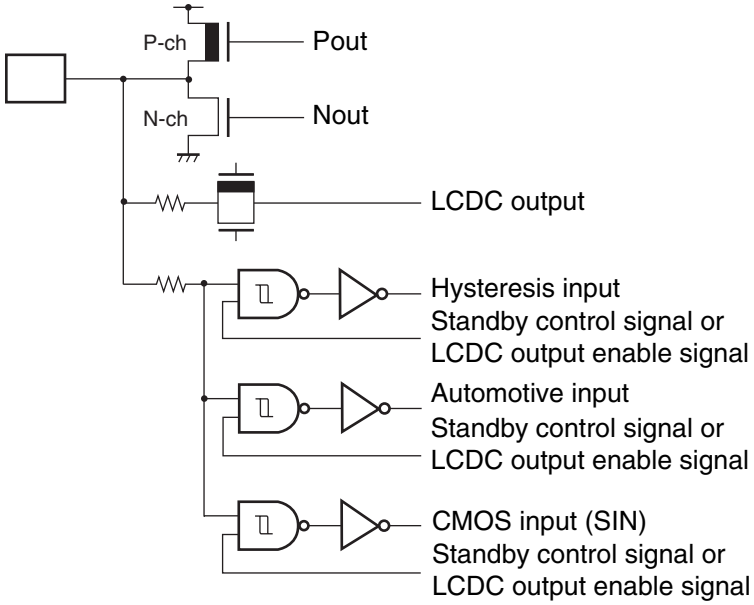
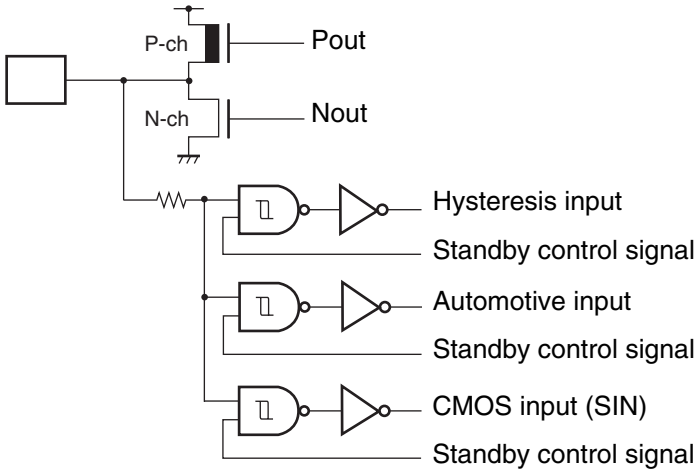
Type	Circuit	Remarks
I		LCDC output pin (COM pin)
J		LCDC output common general-purpose port (serial input) • CMOS output (I_{OH}/I_{OL} = ± 4 mA) • Hysteresis input (V_{IH}/V_{IL} = 0.8V_{CC}/0.2V_{CC}) • CMOS input (SIN) (V_{IH}/V_{IL} = 0.7V_{CC}/0.3V_{CC}) • Automotive input (V_{IH}/V_{IL} = 0.8V_{CC}/0.5V_{CC})
K		General-purpose port (serial input) • CMOS output (I_{OH}/I_{OL} = ± 4 mA) • Hysteresis input (V_{IH}/V_{IL} = 0.8V_{CC}/0.2V_{CC}) • CMOS input (SIN) (V_{IH}/V_{IL} = 0.7V_{CC}/0.3V_{CC}) • Automotive input (V_{IH}/V_{IL} = 0.8V_{CC}/0.5V_{CC})

■ HANDLING DEVICES

- **Strictly observe maximum rated voltages (preventing latch-up)**

In CMOS IC devices, a condition known as latch-up may occur if voltages higher than V_{CC} or lower than V_{SS} are applied to input or output pins other than medium-or high-voltage pins, or if the voltage applied between V_{CC} and V_{SS} exceeds the rated voltage level. In a latch-up condition, the power supply current can increase dramatically and may destroy semiconductor elements. In using semiconductor devices, always take sufficient care to avoid exceeding maximum ratings.

Also care must be taken when the analog system power supply is switched on or off to ensure that the analog power supply (AV_{CC}, AVRH) , the analog input voltages and the power supply voltage for the high current output buffer pins (DV_{CC}) do not exceed the digital power supply voltage (V_{CC}) .

Once the digital power supply voltage (V_{CC}) has been disconnected, the analog power supply (AV_{CC}, AVRH) and the power supply voltage for the high current output buffer pins (DV_{CC}) may be turned on in any sequence.

- **Stable supply voltage**

Even within the warranted operating range of V_{CC} power supply voltage, rapid fluctuations in the power supply voltage can cause malfunctions. The recommended stability for ripple fluctuations (P-P value) at commercial frequencies (50 Hz/60 Hz) should be within 10% of the standard V_{CC} value, and voltage fluctuations that occur during switching of power supplies etc. should be limited to transient fluctuation rates of 0.1 V/ms or less.

- **Notes on energization Power-on procedures**

In order to prevent the built-in step-down circuits from malfunctioning, the voltage rising time (0.2 V to 2.7 V) during power-on should be attained within 50 µs.

- **Treatment of unused pins**

If unused input pins are left open, they may cause malfunctions or latch-up which may lead to permanent damage to the semiconductor. Unused input pins should therefore be pulled up or pulled down through a resistor of at least 2 kΩ.

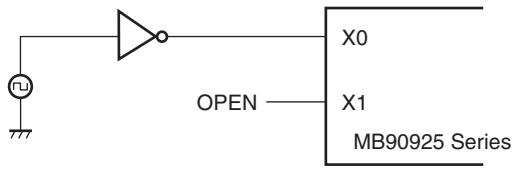
Any unused input/output pins should be left open in output status, or if found set to input status, they should be treated in the same way as input pins.

- **Treatment of A/D converter power supply pins**

Even if the A/D converter is not used, pins should be connected so that $AV_{CC} = V_{CC}$, and $AV_{SS} = AVRH = V_{SS}$.

- **Notes on Using an external clock**

Even when an external clock is used, an oscillation stabilization wait time is required following power-on reset or release from sub clock mode or stop mode. Also, when an external clock is used, it should drive only the X0 pin and the X1 pin should be left open, as shown below.

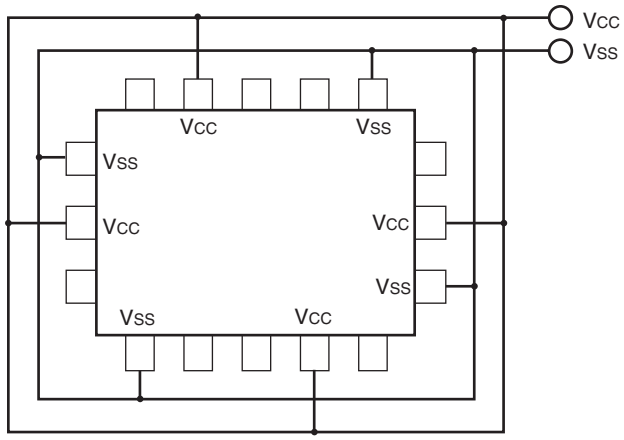


Sample external clock connection

- **Power supply pins**

Devices are designed to prevent problems such as latch-up when multiple V_{CC} and V_{SS} pins are used, by providing internal connections between pins having the same potential. However, in order to reduce unwanted radiation, to prevent abnormal operation of strobe signals due to rise in ground level, and to maintain total output current ratings, all V_{CC} and V_{SS} pins should always be connected externally to power supplies and ground respectively.

As shown in the figure below, all V_{CC} pins must have the same potential and all V_{SS} pins must be at the same potential. If there are multiple V_{CC} or V_{SS} systems, the device will not operate properly even within the warranted operating range.



Power supply input pins (V_{CC}/V_{SS})

In addition, care must be given to connecting the V_{CC} and V_{SS} pins of this device to the current supply source with as low impedance as possible. It is recommended that a 1.0 µF bypass capacitor be connected between the V_{CC} and V_{SS} pins as close to the pins as possible.

- **Turning-on sequence of power supply to A/D converter and analog inputs**

The A/D converter power supply (AV_{CC}, AVRH) and analog inputs (AN0 to AN7) must be applied after the digital power supply (V_{CC}) is switched on. When power is shut off, the A/D converter power supply and analog inputs must be cut off before the digital power supply is switched off (V_{CC}) . In both power-on and power-off, care should be taken that AVRH does not exceed AV_{CC}. Even when pins which double as analog input pins are used as input ports, be sure that the input voltage does not exceed AV_{CC}.

- **Handling the power supply for high-current output buffer pins (DV_{CC}, DV_{SS})**

Always apply power supply to high-current output buffer pins (DV_{CC}, DV_{SS}) after the digital power supply (V_{CC}) is turned on. Also when switching the power off, always shut off the power supply to the high-current output buffer pins (DV_{CC}, DV_{SS}) before switching off the digital power supply (V_{CC}) . There is no problem if the high-current output buffer pins and digital power supplies are turned off and on at the same time.

Even when the high-current output buffer pins are used as general-purpose ports, the power supply for high current output buffer pins (DV_{CC}, DV_{SS}) should be applied to these pins.

- **Pull-up/pull-down resistor**

MB90925 series does not support internal pull-up/pull-down resistor. If necessary, use external components.

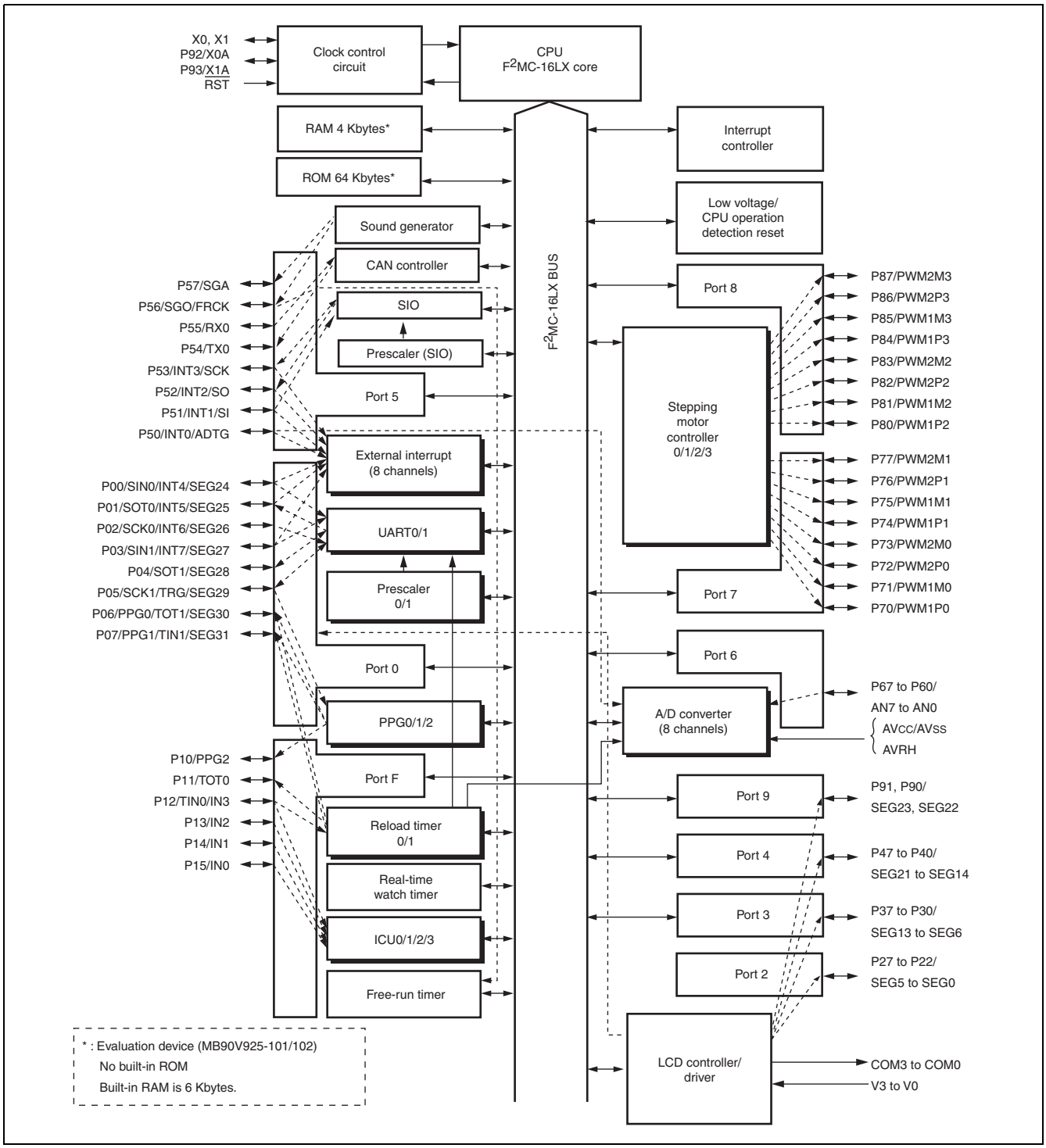
- **Precautions for when not using a sub clock signal**

If the X0A and X1A pins are not connected to an oscillator, apply pull-down treatment to the X0A pin and leave the X1A pin open.

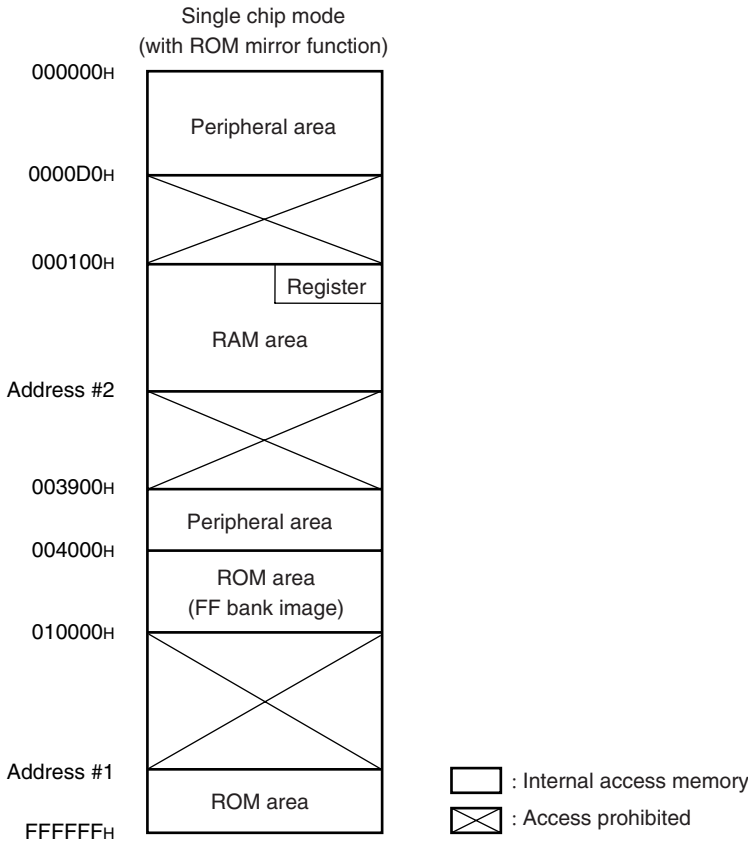
- **Notes on operation when external clock is stopped**

When there is no external oscillator or external clock input is stopped, performance of the operation by MB90925 series the internal oscillation circuit cannot be guaranteed.

■ BLOCK DIAGRAM



■ MEMORY MAP



Part number	Address #1	Address #2
MB90F927/MB90F927S	FF0000H	001100H
MB90V925-101/MB90V925-102	F80000H	003700H

Note : To select models without the ROM mirror function, refer to the “ROM Mirror Function Selection Module” in Hardware Manual. The image of the ROM data in the FF bank appears at the top of the 00 bank, in order to enable efficient use of small C compiler models. The lower 16-bit address for the FF bank will be assigned to the same address, so that tables in ROM can be referenced without declaring a “far” indication with the pointer. For example when accessing the address 00C000H, the actual access is to address FFC000H in ROM. Here the FF bank ROM area exceeds 48 Kbytes, so that it is not possible to see the entire area in the 00 bank image. Therefore because the ROM data from FF4000H to FFFFFFH will appear in the image from 004000H to 00FFFFH, it is recommended that the ROM data table be stored in the area from FF4000H to FFFFFFH.

■ I/O MAP

• Other than CAN Interface

Address	Register name	Symbol	Read/write	Resource name	Initial value
000000H	Port 0 data register	PDR0	R/W	Port 0	XXXXXXXXB
000001H	Port 1 data register	PDR1	R/W	Port 1	- - XXXXXXB
000002H	Port 2 data register	PDR2	R/W	Port 2	XXXXXX - -B
000003H	Port 3 data register	PDR3	R/W	Port 3	XXXXXXXXB
000004H	Port 4 data register	PDR4	R/W	Port 4	XXXXXXXXB
000005H	Port 5 data register	PDR5	R/W	Port 5	XXXXXXXXB
000006H	Port 6 data register	PDR6	R/W	Port 6	XXXXXXXXB
000007H	Port 7 data register	PDR7	R/W	Port 7	XXXXXXXXB
000008H	Port 8 data register	PDR8	R/W	Port 8	XXXXXXXXB
000009H	Port 9 data register	PDR9	R/W	Port 9	- - - -XXXXB
00000AH to 00000FH	(Disabled)				
000010H	Port 0 direction register	DDR0	R/W	Port 0	0 0 0 0 0 0 0 0B
000011H	Port 1 direction register	DDR1	R/W	Port 1	- - 0 0 0 0 0 0B
000012H	Port 2 direction register	DDR2	R/W	Port 2	0 0 0 0 0 0 - -B*
000013H	Port 3 direction register	DDR3	R/W	Port 3	0 0 0 0 0 0 0 0B*
000014H	Port 4 direction register	DDR4	R/W	Port 4	0 0 0 0 0 0 0 0B
000015H	Port 5 direction register	DDR5	R/W	Port 5	0 0 0 0 0 0 0 0B
000016H	Port 6 direction register	DDR6	R/W	Port 6	0 0 0 0 0 0 0 0B
000017H	Port 7 direction register	DDR7	R/W	Port 7	0 0 0 0 0 0 0 0B
000018H	Port 8 direction register	DDR8	R/W	Port 8	0 0 0 0 0 0 0 0B
000019H	Port 9 direction register	DDR9	R/W	Port 9	- - - - 0 0 0 0B
00001AH	Analog input enable	ADER	R/W	Port 6, A/D	1 1 1 1 1 1 1 1B
00001BH to 00001FH	(Disabled)				
000020H	A/D control status register lower	ADCS0	R/W	8/10-bit A/D converter	0 0 0 - - - - 0B
000021H	A/D control status register higher	ADCS1	R/W		0 0 0 0 0 0 0 -B
000022H	A/D data register lower	ADCR0	R		0 0 0 0 0 0 0 0B
000023H	A/D data register higher	ADCR1	R		- - - - - - 0 0B
000024H	Compare clear register	CPCLR	R/W	16-bit free-run timer	XXXXXXXXB
000025H			R/W		XXXXXXXXB
000026H	Timer data register	TCDT	R/W		0 0 0 0 0 0 0 0B
000027H			R/W		0 0 0 0 0 0 0 0B
000028H	Timer control status register lower	TCCSL	R/W		0 0 0 0 0 0 0 0B
000029H	Timer control status register higher	TCCSH	R/W		0 1 - 0 0 0 0 0B

(Continued)

Address	Register name	Symbol	Read/write	Resource name	Initial value
00002AH	PPG0 control status register lower	PCNTL0	R/W	16-bit PPG0	0 0 0 0 0 0 0 0B
00002BH	PPG0 control status register higher	PCNTH0	R/W		0 0 0 0 0 0 0 1B
00002CH	PPG1 control status register lower	PCNTL1	R/W	16-bit PPG1	0 0 0 0 0 0 0 0B
00002DH	PPG1 control status register higher	PCNTH1	R/W		0 0 0 0 0 0 0 1B
00002EH	PPG2 control status register lower	PCNTL2	R/W	16-bit PPG2	0 0 0 0 0 0 0 0B
00002FH	PPG2 control status register higher	PCNTH2	R/W		0 0 0 0 0 0 0 1B
000030H	External interrupt enable	ENIR	R/W	External interrupt	0 0 0 0 0 0 0 0B
000031H	External interrupt request	EIRR	R/W		0 0 0 0 0 0 0 0B
000032H	External interrupt level lower	ELVRL	R/W		0 0 0 0 0 0 0 0B
000033H	External interrupt level higher	ELVRH	R/W		0 0 0 0 0 0 0 0B
000034H	Serial mode register 0	SMR0	R/W	UART(LIN/SCI) 0	0 0 0 0 0 0 0 0B
000035H	Serial control register 0	SCR0	R/W		0 0 0 0 0 0 0 0B
000036H	Reception/transmission data register 0	RDR0/ TDR0	R/W		0 0 0 0 0 0 0 0B
000037H	Serial status register 0	SSR0	R/W		0 0 0 0 1 0 0 0B
000038H	Extended communication control register 0	ECCR0	R/W		0 0 0 0 0 0 XXB
000039H	Extended status control register	ESCR0	R/W		0 0 0 0 0 1 0 0B
00003AH	Baud rate generator register 00	BGR00	R/W		0 0 0 0 0 0 0 0B
00003BH	Baud rate generator register 01	BGR01	R/W		0 0 0 0 0 0 0 0B
00003CH, 00003DH	(Disabled)				
00003EH	CAN wake-up control register	CWUCR	R/W	CAN	- - - - - - - 0B
00003FH	(Disabled)				
000040H to 00004FH	Area reserved for CAN interface 0				
000050H	Timer control status register 0 lower	TMCSR0L	R/W	16-bit reload timer 0	0 0 0 0 0 0 0 0B
000051H	Timer control status register 0 higher	TMCSR0H	R/W		- - 1 0 0 0 0 0B
000052H	Timer register 0/reload register 0	TMR0/ TMRLR0	R/W		XXXXXXXXB
000053H					XXXXXXXXB
000054H	Timer control status register 1 lower	TMCSR1L	R/W	16-bit reload timer 1	0 0 0 0 0 0 0 0B
000055H	Timer control status register 1 higher	TMCSR1H	R/W		- - 1 0 0 0 0 0B
000056H	Timer register 1/reload register 1	TMR1/ TMRLR1	R/W		XXXXXXXXB
000057H					XXXXXXXXB

(Continued)

Address	Register name	Symbol	Read/write	Resource name	Initial value
000058H	LCD output control register 1	LOCR1	R/W	LCD	1 1 1 1 1 1 1 1B
000059H	LCD output control register 2	LOCR2	R/W		0 0 0 0 0 0 0 0B
00005AH	Sound control register lower	SGCRL	R/W	Sound generator	0 0 0 0 0 0 0 0B
00005BH	Sound control register higher	SGCRH	R/W		0 - - - - 1 0 0B
00005CH	Frequency data register	SGFR	R/W		XXXXXXXXB
00005DH	Amplitude data register	SGAR	R/W		0 0 0 0 0 0 0 0B
00005EH	Decrement grade register	SGDR	R/W		XXXXXXXXB
00005FH	Tone count register	SGTR	R/W		XXXXXXXXB
000060H	Input capture register 0	IPCP0	R	Input capture 0/1	XXXXXXXXB
000061H					XXXXXXXXB
000062H	Input capture register 1	IPCP1	R		XXXXXXXXB
000063H					XXXXXXXXB
000064H	Input capture register 2	IPCP2	R	Input capture 2/3	XXXXXXXXB
000065H					XXXXXXXXB
000066H	Input capture register 3	IPCP3	R		XXXXXXXXB
000067H					XXXXXXXXB
000068H	Input capture control status 0/1	ICS01	R/W	Input capture 0/1	0 0 0 0 0 0 0 0B
000069H	Input capture edge register 0/1	ICE01	R/W	Input capture 0/1	XXX0X0XXB
00006AH	Input capture control status 2/3	ICS23	R/W	Input capture 2/3	0 0 0 0 0 0 0 0B
00006BH	Input capture edge register 2/3	ICE23	R/W	Input capture 2/3	XXXXXXXXB
00006CH	LCD control register lower	LCRL	R/W	LCD controller/ driver	0 0 0 1 0 0 0 0B
00006DH	LCD control register higher	LCRH	R/W		0 0 0 0 0 0 0 0B
00006EH	Low voltage/CPU operation detection reset control register	LVRC	R/W	Low voltage/CPU operation detection reset	0 0 1 1 1 0 0 0B
00006FH	ROM mirror	ROMM	W	ROM mirror	XXXXXXX1B
000070H to 00007FH	(Disabled)				
000080H	PWM control register 0	PWC0	R/W	Stepping motor controller 0	0 0 0 0 0 - - 0B
000081H	(Disabled)				
000082H	PWM control register 1	PWC1	R/W	Stepping motor controller 1	0 0 0 0 0 - - 0B
000083H	(Disabled)				
000084H	PWM control register 2	PWC2	R/W	Stepping motor controller 2	0 0 0 0 0 - - 0B
000085H	(Disabled)				
000086H	PWM control register 3	PWC3	R/W	Stepping motor controller 3	0 0 0 0 0 - - 0B

(Continued)

Address	Register name	Symbol	Read/write	Resource name	Initial value
000087H to 000089H	(Disabled)				
00008AH	A/D setting register 0	ADSR0	R/W	A/D	0 0 0 0 0 0 0 0B
00008BH	A/D setting register 1	ADSR1	R/W		0 0 0 0 0 0 0 0B
00008CH	Port input level select 0	PIL0	R/W	Port Input Level Select	0 0 0 0 0 0 0 0B
00008DH	Port input level select 1	PIL1	R/W		- - - 0 0 0 0 0B
00008EH to 00009DH	(Disabled)				
00009EH	ROM correction control register	PACSR	R/W	Address match detection function	- - - - - 0 - 0B
00009FH	Delay interrupt/release	DIRR	R/W	Delay interrupt	- - - - - - - 0B
0000A0H	Power saving mode	LPMCR	R/W	Power saving control circuit	0 0 0 1 1 0 0 0B
0000A1H	Clock select	CKSCR	R/W		1 1 1 1 1 1 0 0B
0000A2H to 0000A7H	(Disabled)				
0000A8H	Watchdog control	WDTC	R/W	Watchdog timer	XXXXX 1 1 1B
0000A9H	Time-base timer control register	TBTC	R/W	Time-base timer	1 - - 0 0 1 0 0B
0000AAH	Watch timer control register	WTC	R/W	Watch timer (sub clock)	1 X 0 0 0 0 0 0B
0000ABH to 0000ADH	(Disabled)				
0000AEH	Flash control register	FMCS	R/W	Flash memory interface	0 0 0 X 0 XX 0B
0000AFH	(Disabled)				
0000B0H	Interrupt control register 00	ICR00	R/W	Interrupt controller	0 0 0 0 0 1 1 1B
0000B1H	Interrupt control register 01	ICR01	R/W		0 0 0 0 0 1 1 1B
0000B2H	Interrupt control register 02	ICR02	R/W		0 0 0 0 0 1 1 1B
0000B3H	Interrupt control register 03	ICR03	R/W		0 0 0 0 0 1 1 1B
0000B4H	Interrupt control register 04	ICR04	R/W		0 0 0 0 0 1 1 1B
0000B5H	Interrupt control register 05	ICR05	R/W	Interrupt controller	0 0 0 0 0 1 1 1B
0000B6H	Interrupt control register 06	ICR06	R/W		0 0 0 0 0 1 1 1B
0000B7H	Interrupt control register 07	ICR07	R/W		0 0 0 0 0 1 1 1B
0000B8H	Interrupt control register 08	ICR08	R/W		0 0 0 0 0 1 1 1B
0000B9H	Interrupt control register 09	ICR09	R/W		0 0 0 0 0 1 1 1B
0000BAH	Interrupt control register 10	ICR10	R/W		0 0 0 0 0 1 1 1B
0000BBH	Interrupt control register 11	ICR11	R/W		0 0 0 0 0 1 1 1B
0000BCH	Interrupt control register 12	ICR12	R/W		0 0 0 0 0 1 1 1B

(Continued)

Address	Register name	Symbol	Read/write	Resource name	Initial value
0000BDH	Interrupt control register 13	ICR13	R/W	Interrupt controller	0 0 0 0 0 1 1 1B
0000BEH	Interrupt control register 14	ICR14	R/W		0 0 0 0 0 1 1 1B
0000BFH	Interrupt control register 15	ICR15	R/W		0 0 0 0 0 1 1 1B
0000C0H	Serial mode control register (lower)	SMCSL	R/W	SIO	- - - - 0 0 0 0B
0000C1H	Serial mode control register (higher)	SMCSH	R/W		0 0 0 0 0 0 1 0B
0000C2H	Serial data register	SDR	R/W		XXXXXXXXB
0000C3H	Communication prescaler control register	SDCR	R/W	Communication prescaler (SIO)	0 - - - 0 0 0 0B
0000C4H	Serial mode register 1	SMR1	R/W	UART(LIN/SCI) 1	0 0 0 0 0 0 0 0B
0000C5H	Serial control register 1	SCR1	R/W		0 0 0 0 0 0 0 0B
0000C6H	Reception/transmission data register 1	RDR1/ TDR1	R/W		0 0 0 0 0 0 0 0B
0000C7H	Serial status register 1	SSR1	R/W		0 0 0 0 1 0 0 0B
0000C8H	Extended communication control register 1	ECCR1	R/W		0 0 0 0 0 0 XXB
0000C9H	Extended status control register 1	ESCR1	R/W		0 0 0 0 0 1 0 0B
0000CAH	Baud rate generator register 10	BGR10	R/W		0 0 0 0 0 0 0 0B
0000CBH	Baud rate generator register 11	BGR11	R/W		0 0 0 0 0 0 0 0B
0000CCH	Watch timer control register lower	WTCRL	R/W	Real-time watch timer	0 0 0 - - 0 0 0B
0000CDH	Watch timer control register middle	WTCRM	R/W		0 0 0 0 0 0 0 0B
0000CEH	Watch timer control register higher	WTCRH	R/W		- - - - 0 0 0 0B
0000CFH	Sub clock control register	SCCR	W	Sub clock	- - - - 0 0 0 0B
0000D0H to 0000FFH	(Disabled)				
001FF0H	ROM correction address 0	PADR0	R/W	Address match detection function	XXXXXXXXB
001FF1H	ROM correction address 1	PADR0	R/W		XXXXXXXXB
001FF2H	ROM correction address 2	PADR0	R/W		XXXXXXXXB
001FF3H	ROM correction address 3	PADR1	R/W	Address match detection function	XXXXXXXXB
001FF4H	ROM correction address 4	PADR1	R/W		XXXXXXXXB
001FF5H	ROM correction address 5	PADR1	R/W		XXXXXXXXB
003900H to 00391FH	(Disabled)				
003920H	PPG0 down counter register	PDCR0	R	16-bit PPG 0	1 1 1 1 1 1 1 1B
003921H					1 1 1 1 1 1 1 1B
003922H	PPG0 cycle setting register	PCSR0	W		XXXXXXXXB
003923H					XXXXXXXXB
003924H	PPG0 duty setting register	PDUT0	W		XXXXXXXXB
003925H					XXXXXXXXB

(Continued)

Address	Register name	Symbol	Read/write	Resource name	Initial value
003926H, 003927H	(Disabled)				
003928H	PPG1 down counter register	PDCR1	R	16-bit PPG 1	1 1 1 1 1 1 1 1B
003929H					1 1 1 1 1 1 1 1B
00392AH	PPG1 cycle setting register	PCSR1	W		XXXXXXXXB
00392BH					XXXXXXXXB
00392CH	PPG1 duty setting register	PDUT1	W		XXXXXXXXB
00392DH					XXXXXXXXB
00392EH, 00392FH	(Disabled)				
003930H	PPG2 down counter register	PDCR2	R	16-bit PPG 2	1 1 1 1 1 1 1 1B
003931H					1 1 1 1 1 1 1 1B
003932H	PPG2 cycle setting register	PCSR2	W		XXXXXXXXB
003933H					XXXXXXXXB
003934H	PPG2 duty setting register	PDUT2	W		XXXXXXXXB
003935H					XXXXXXXXB
003936H to 003957H	(Disabled)				
003958H	Sub second data register	WTBR	R/W	Real time watch timer	XXXXXXXXB
003959H					XXXXXXXXB
00395AH					- - - XXXXXB
00395BH	Second data register	WTSR	R/W		- - 0 0 0 0 0 0B
00395CH	Minute data register	WTMR	R/W		- - 0 0 0 0 0 0B
00395DH	Hour data register	WTHR	R/W		- - - 0 0 0 0 0B
00395EH	Day data register	WTDR	R/W		0 0 - 0 0 0 0 1B
00395FH	(Disabled)				
003960H to 00396FH	LCD display RAM	VRAM	R/W	LCD controller/ driver	XXXXXXXXB
003970H to 00397FH	(Disabled)				
003980H	PWM1 compare register 0	PWC10	R/W	Stepping motor controller 0	XXXXXXXXB
003981H					- - - - - - XXB
003982H	PWM2 compare register 0	PWC20	R/W		XXXXXXXXB
003983H					- - - - - - XXB
003984H	PWM1 select register 0	PWS10	R/W		- - 0 0 0 0 0 0B
003985H	PWM2 select register 0	PWS20	R/W		- 0 0 0 0 0 0 0B

(Continued)

Address	Register name	Symbol	Read/write	Resource name	Initial value
003986H, 003987H	(Disabled)				
003988H	PWM1 compare register 1	PWC11	R/W	Stepping motor controller 1	XXXXXXXXB
003989H					-------XXB
00398AH	PWM2 compare register 1	PWC21	R/W		XXXXXXXXB
00398BH					-------XXB
00398CH	PWM1 select register 1	PWS11	R/W		--000000B
00398DH	PWM2 select register 1	PWS21	R/W		-0000000B
00398EH, 00398FH	(Disabled)				
003990H	PWM1 compare register 2	PWC12	R/W	Stepping motor controller 2	XXXXXXXXB
003991H					-------XXB
003992H	PWM2 compare register 2	PWC22	R/W		XXXXXXXXB
003993H					-------XXB
003994H	PWM1 select register 2	PWS12	R/W		--000000B
003995H	PWM2 select register 2	PWS22	R/W		-0000000B
003996H, 003997H	(Disabled)				
003998H	PWM1 compare register 3	PWC13	R/W	Stepping motor controller 3	XXXXXXXXB
003999H					-------XXB
00399AH	PWM2 compare register 3	PWC23	R/W		XXXXXXXXB
00399BH					-------XXB
00399CH	PWM1 select register 3	PWS13	R/W		--000000B
00399DH	PWM2 select register 3	PWS23	R/W		-0000000B
00399EH to 0039FFH	(Disabled)				
003A00H to 003AFFH	Area reserved for CAN interface 0				
003B00H to 003BFFH	(Disabled)				
003C00H to 003CFFH	Area reserved for CAN interface 0				
003D00H to 003EFFH	(Disabled)				

(Continued)

(Continued)

- Initial value symbols :
  "0" : initial value 0
  "1" : initial value 1
  "X" : initial value undetermined
  "-" : initial value undetermined (none)
- Write/read symbols :
  "R/W" : read/write enabled
  "R" : read only
  "W" : write only
- Addresses in the area 0000_H to $00FF_H$ are reserved for the principal functions of the MCU. Read access attempts to reserved areas will result in an "X" value. Also, write access to reserved areas is prohibited.

* : P22/SEG0 to P27/SEG5 and P30/SEG6 to P35/SEG11 initially will be LCD segment output as LCD output control register LOCR1 (58_H) is "11111111_B" initially. To use port 2 and port 3 as the general-purpose input/output ports, set LOCR1 to "00000000_B" to disable the LCD segment output first.

• CAN Interface

Address	Register name	Symbol	Read/ write	Initial value
000040H	Message buffer valid area	BVALR	R/W	0 0 0 0 0 0 0 0B
000041H				0 0 0 0 0 0 0 0B
000042H	Transmission request register	TREQR	R/W	0 0 0 0 0 0 0 0B
000043H				0 0 0 0 0 0 0 0B
000044H	Transmission cancel register	TCANR	W	0 0 0 0 0 0 0 0B
000045H				0 0 0 0 0 0 0 0B
000046H	Transmission completed register	TCR	R/W	0 0 0 0 0 0 0 0B
000047H				0 0 0 0 0 0 0 0B
000048H	Receiving completed register	RCR	R/W	0 0 0 0 0 0 0 0B
000049H				0 0 0 0 0 0 0 0B
00004AH	Remote request receiving register	RRTRR	R/W	0 0 0 0 0 0 0 0B
00004BH				0 0 0 0 0 0 0 0B
00004CH	Receiving overrun register	ROVRR	R/W	0 0 0 0 0 0 0 0B
00004DH				0 0 0 0 0 0 0 0B
00004EH	Receiving interrupt enable register	RIER	R/W	0 0 0 0 0 0 0 0B
00004FH				0 0 0 0 0 0 0 0B
003C00H	Control status register	CSR	R/W, R	0 0 - - - 0 0 0B
003C01H				0 - - - - 0 - 1B
003C02H	Last event indicator register	LEIR	R/W	- - - - - - - -B
003C03H				0 0 0 - 0 0 0 0B
003C04H	RX/TX error counter	RTEC	R	0 0 0 0 0 0 0 0B
003C05H				0 0 0 0 0 0 0 0B
003C06H	Bit timing register	BTR	R/W	- 1 1 1 1 1 1 1B
003C07H				1 1 1 1 1 1 1 1B
003C08H	IDE register	IDER	R/W	XXXXXXXXB
003C09H				XXXXXXXXB
003C0AH	Transmission RTR register	TRTRR	R/W	0 0 0 0 0 0 0 0B
003C0BH				0 0 0 0 0 0 0 0B
003C0CH	Remote frame receiving wait register	RFWTR	R/W	XXXXXXXXB
003C0DH				XXXXXXXXB
003C0EH	Transmission interrupt enable register	TIER	R/W	0 0 0 0 0 0 0 0B
003C0FH				0 0 0 0 0 0 0 0B

(Continued)

Address	Register name	Symbol	Read/ write	Initial value
003C10H	Acceptance mask select register	AMSR	R/W	XXXXXXXXB
003C11H				XXXXXXXXB
003C12H				XXXXXXXXB
003C13H				XXXXXXXXB
003C14H	Acceptance mask register 0	AMR0	R/W	XXXXXXXXB
003C15H				XXXXXXXXB
003C16H				XXXXX- - -B
003C17H				XXXXXXXXB
003C18H	Acceptance mask register 1	AMR1	R/W	XXXXXXXXB
003C19H				XXXXXXXXB
003C1AH				XXXXX- - -B
003C1BH				XXXXXXXXB
003A00H to 003A1FH	General-purpose RAM	—	R/W	XXXXXXXXB to XXXXXXXXB
003A20H	ID register 0	IDR0	R/W	XXXXXXXXB
003A21H				XXXXXXXXB
003A22H				XXXXX- - -B
003A23H				XXXXXXXXB
003A24H	ID register 1	IDR1	R/W	XXXXXXXXB
003A25H				XXXXXXXXB
003A26H				XXXXX- - -B
003A27H				XXXXXXXXB
003A28H	ID register 2	IDR2	R/W	XXXXXXXXB
003A29H				XXXXXXXXB
003A2AH				XXXXX- - -B
003A2BH				XXXXXXXXB
003A2CH	ID register 3	IDR3	R/W	XXXXXXXXB
003A2DH				XXXXXXXXB
003A2EH				XXXXX- - -B
003A2FH				XXXXXXXXB
003A30H	ID register 4	IDR4	R/W	XXXXXXXXB
003A31H				XXXXXXXXB
003A32H				XXXXX- - -B
003A33H				XXXXXXXXB

(Continued)

Address	Register name	Symbol	Read/ write	Initial value
003A34H	ID register 5	IDR5	R/W	XXXXXXXXB
003A35H				XXXXXXXXB
003A36H				XXXXX- - -B
003A37H				XXXXXXXXB
003A38H	ID register 6	IDR6	R/W	XXXXXXXXB
003A39H				XXXXXXXXB
003A3AH				XXXXX- - -B
003A3BH				XXXXXXXXB
003A3CH	ID register 7	IDR7	R/W	XXXXXXXXB
003A3DH				XXXXXXXXB
003A3EH				XXXXX- - -B
003A3FH				XXXXXXXXB
003A40H	ID register 8	IDR8	R/W	XXXXXXXXB
003A41H				XXXXXXXXB
003A42H				XXXXX- - -B
003A43H				XXXXXXXXB
003A44H	ID register 9	IDR9	R/W	XXXXXXXXB
003A45H				XXXXXXXXB
003A46H				XXXXX- - -B
003A47H				XXXXXXXXB
003A48H	ID register 10	IDR10	R/W	XXXXXXXXB
003A49H				XXXXXXXXB
003A4AH				XXXXX- - -B
003A4BH				XXXXXXXXB
003A4CH	ID register 11	IDR11	R/W	XXXXXXXXB
003A4DH				XXXXXXXXB
003A4EH				XXXXX- - -B
003A4FH				XXXXXXXXB
003A50H	ID register 12	IDR12	R/W	XXXXXXXXB
003A51H				XXXXXXXXB
003A52H				XXXXX- - -B
003A53H				XXXXXXXXB

(Continued)

Address	Register name	Symbol	Read/ write	Initial value
003A54H	ID register 13	IDR13	R/W	XXXXXXXXB
003A55H				XXXXXXXXB
003A56H				XXXXX- - -B
003A57H				XXXXXXXXB
003A58H	ID register 14	IDR14	R/W	XXXXXXXXB
003A59H				XXXXXXXXB
003A5AH				XXXXX- - -B
003A5BH				XXXXXXXXB
003A5CH	ID register 15	IDR15	R/W	XXXXXXXXB
003A5DH				XXXXXXXXB
003A5EH				XXXXX- - -B
003A5FH				XXXXXXXXB
003A60H	DLC register 0	DLCR0	R/W	- - - -XXXXB
003A61H				- - - -XXXXB
003A62H	DLC register 1	DLCR1	R/W	- - - -XXXXB
003A63H				- - - -XXXXB
003A64H	DLC register 2	DLCR2	R/W	- - - -XXXXB
003A65H				- - - -XXXXB
003A66H	DLC register 3	DLCR3	R/W	- - - -XXXXB
003A67H				- - - -XXXXB
003A68H	DLC register 4	DLCR4	R/W	- - - -XXXXB
003A69H				- - - -XXXXB
003A6AH	DLC register 5	DLCR5	R/W	- - - -XXXXB
003A6BH				- - - -XXXXB
003A6CH	DLC register 6	DLCR6	R/W	- - - -XXXXB
003A6DH				- - - -XXXXB
003A6EH	DLC register 7	DLCR7	R/W	- - - -XXXXB
003A6FH				- - - -XXXXB
003A70H	DLC register 8	DLCR8	R/W	- - - -XXXXB
003A71H				- - - -XXXXB
003A72H	DLC register 9	DLCR9	R/W	- - - -XXXXB
003A73H				- - - -XXXXB
003A74H	DLC register 10	DLCR10	R/W	- - - -XXXXB
003A75H				- - - -XXXXB

(Continued)

Address	Register name	Symbol	Read/ write	Initial value
003A76H	DLC register 11	DLCR11	R/W	----XXXXB
003A77H				----XXXXB
003A78H	DLC register 12	DLCR12	R/W	----XXXXB
003A79H				----XXXXB
003A7AH	DLC register 13	DLCR13	R/W	----XXXXB
003A7BH				----XXXXB
003A7CH	DLC register 14	DLCR14	R/W	----XXXXB
003A7DH				----XXXXB
003A7EH	DLC register 15	DLCR15	R/W	----XXXXB
003A7FH				----XXXXB
003A80H to 003A87H	Data register 0 (8 bytes)	DTR0	R/W	XXXXXXXXB to XXXXXXXXB
003A88H to 003A8FH	Data register 1 (8 bytes)	DTR1	R/W	XXXXXXXXB to XXXXXXXXB
003A90H to 003A97H	Data register 2 (8 bytes)	DTR2	R/W	XXXXXXXXB to XXXXXXXXB
003A98H to 003A9FH	Data register 3 (8 bytes)	DTR3	R/W	XXXXXXXXB to XXXXXXXXB
003AA0H to 003AA7H	Data register 4 (8 bytes)	DTR4	R/W	XXXXXXXXB to XXXXXXXXB
003AA8H to 003AAFH	Data register 5 (8 bytes)	DTR5	R/W	XXXXXXXXB to XXXXXXXXB
003AB0H to 003AB7H	Data register 6 (8 bytes)	DTR6	R/W	XXXXXXXXB to XXXXXXXXB
003AB8H to 003ABFH	Data register 7 (8 bytes)	DTR7	R/W	XXXXXXXXB to XXXXXXXXB
003AC0H to 003AC7H	Data register 8 (8 bytes)	DTR8	R/W	XXXXXXXXB to XXXXXXXXB
003AC8H to 003ACFH	Data register 9 (8 bytes)	DTR9	R/W	XXXXXXXXB to XXXXXXXXB

(Continued)

(Continued)

Address	Register name	Symbol	Read/ write	Initial value
003AD0H to 003AD7H	Data register 10 (8 bytes)	DTR10	R/W	XXXXXXXXB to XXXXXXXXB
003AD8H to 003ADFH	Data register 11 (8 bytes)	DTR11	R/W	XXXXXXXXB to XXXXXXXXB
003AE0H to 003AE7H	Data register 12 (8 bytes)	DTR12	R/W	XXXXXXXXB to XXXXXXXXB
003AE8H to 003AEFH	Data register 13 (8 bytes)	DTR13	R/W	XXXXXXXXB to XXXXXXXXB
003AF0H to 003AF7H	Data register 14 (8 bytes)	DTR14	R/W	XXXXXXXXB to XXXXXXXXB
003AF8H to 003AFFH	Data register 15 (8 bytes)	DTR15	R/W	XXXXXXXXB to XXXXXXXXB

■ INTERRUPT SOURCES, INTERRUPT VECTORS, AND INTERRUPT CONTROL REGISTERS

Interrupt source	EI²OS corre-sponding	Interrupt vector			Interrupt control register		Priority *2
		Number		Address	ICR	Address	
Reset	×	#08	08H	FFFFDCH	—	—	High
INT9 instruction	×	#09	09H	FFFFD8H	—	—	
Exception processing	×	#10	0AH	FFFFD4H	—	—	
CAN0 RX	×	#11	0BH	FFFFD0H	ICR00	0000B0H *1	
CAN0 TX/NS	×	#12	0CH	FFFFCCH			
(Reserved) *3	×	#13	0DH	FFFFC8H	ICR01	0000B1H *1	
SIO *3	△	#14	0EH	FFFFC4H			
Input capture 0	△	#15	0FH	FFFFC0H	ICR02	0000B2H *1	
DTP/external interrupt - ch.0 detected	△	#16	10H	FFFFBCH			
Reload timer 0	△	#17	11H	FFFFB8H	ICR03	0000B3H *1	
DTP/external interrupt - ch.1 detected	△	#18	12H	FFFFB4H			
Input capture 1	△	#19	13H	FFFFB0H	ICR04	0000B4H *1	
DTP/external interrupt - ch.2 detected	△	#20	14H	FFFFACH			
Input capture 2	△	#21	15H	FFFFA8H	ICR05	0000B5H *1	
DTP/external interrupt - ch.3 detected	△	#22	16H	FFFFA4H			
Input capture 3	△	#23	17H	FFFFA0H	ICR06	0000B6H *1	
DTP/external interrupt - ch.4/ch.5 detected	△	#24	18H	FFFF9CH			
PPG timer 0	△	#25	19H	FFFF98H	ICR07	0000B7H *1	
DTP/external interrupt - ch.6/ch.7 detected	△	#26	1AH	FFFF94H			
PPG timer 1	△	#27	1BH	FFFF90H	ICR08	0000B8H *1	
Reload timer 1	△	#28	1CH	FFFF8CH			
PPG timer 2	○	#29	1DH	FFFF88H	ICR09	0000B9H *1	
Real time watch timer	×	#30	1EH	FFFF84H			
Free-run timer overflow	×	#31	1FH	FFFF80H	ICR10	0000BAH *1	
A/D converter conversion end	○	#32	20H	FFFF7CH			
Free-run timer clear	×	#33	21H	FFFF78H	ICR11	0000BBH *1	
Sound generator	×	#34	22H	FFFF74H			
Time-base timer	×	#35	23H	FFFF70H	ICR12	0000BCH *1	
Watchdog (sub clock)	×	#36	24H	FFFF6CH			
UART 1 RX	◎	#37	25H	FFFF68H	ICR13	0000BDH *1	
UART 1 TX	△	#38	26H	FFFF64H			
UART 0 RX	◎	#39	27H	FFFF60H	ICR14	0000BEH *1	
UART 0 TX	△	#40	28H	FFFF5CH			
Flash memory status	×	#41	29H	FFFF58H	ICR15	0000BFH *1	
Delay interrupt generator module	×	#42	2AH	FFFF54H			Low

(Continued)

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◎ : Usable, with EI²OS stop function
○ : Usable
△ : Usable when interrupt sources sharing ICR are not in use
× : Unusable

*1 : • Peripheral functions sharing the ICR register have the same interrupt level.
• If peripheral functions sharing the ICR register are using expanded intelligent I/O services, one or the other cannot be used.
• When peripheral functions are sharing the ICR register and one specifies expanded intelligent I/O services, the interrupt from the other function cannot be used.

*2 : Priority applies when interrupts of the same level are generated.

*3 : SIO and CAN1 TX/NX will share IRQ3 in evaluation chip (MB90V925-101/102) .

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	$AV_{CC} = V_{CC}$*2
	AVRH	V_{SS} – 0.3	V_{SS} + 6.0	V	$AV_{CC} \geq$ AVRH*2
	DV_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	$DV_{CC} = V_{CC}$*2
Input voltage*1	V_I	V_{SS} – 0.3	V_{CC} + 0.3	V	*3
Output voltage*1	V_O	V_{SS} – 0.3	V_{CC} + 0.3	V	
Maximum clamp current	I_{CLAMP}	– 400	+ 400	µA	*7
Total maximum clamp current	$\Sigma\|I_{CLAMP}\|$	—	4	mA	*7
"L" level maximum output current*4	I_{OL1}	—	15	mA	Other than P70 to P77 and P80 to P87
	I_{OL2}	—	40	mA	P70 to 77 and P80 to87
"L" level average output current*5	I_{OLAV1}	—	4	mA	Other than P70 to P77 and P80 to P87
	I_{OLAV2}	—	30	mA	P70 to 77 and P80 to 87
"L" level maximum total output current	ΣI_{OL1}	—	100	mA	Other than P70 to P77 and P80 to P87
	ΣI_{OL2}	—	330	mA	P70 to 77 and P80 to 87
"L" level average total output current	ΣI_{OLAV1}	—	50	mA	Other than P70 to P77 and P80 to P87
	ΣI_{OLAV2}	—	250	mA	P70 to 77 and P80 to 87
"H" level maximum output current	I_{OH1}*4	—	–15	mA	Other than P70 to P77 and P80 to P87
	I_{OH2}*4	—	–40	mA	P70 to 77 and P80 to 87
"H" level average output current	I_{OHAV1}*5	—	–4	mA	Other than P70 to P77 and P80 to P87
	I_{OHAV2}*5	—	–30	mA	P70 to 77 and P80 to 87
"H" level maximum total output current	ΣI_{OH1}	—	–100	mA	Other than P70 to P77 and P80 to P87
	ΣI_{OH2}	—	–330	mA	P70 to 77 and P80 to 87
"H" level average total output current	ΣI_{OHAV1}*6	—	–50	mA	Other than P70 to P77 and P80 to P87
	ΣI_{OHAV2}*6	—	–250	mA	P70 to 77 and P80 to 87
Power consumption	P_D	—	500	mW	
Operating temperature	T_A	–40	+105	°C	
Storage temperature	T_{STG}	–55	+150	°C	

*1 : The parameter is based on $V_{SS} = AV_{SS} = DV_{SS} = 0.0$ V.

*2 : AV_{CC}, AVRH and DV_{CC} shall never exceed V_{CC}.
Also, AVRH shall never exceed AV_{CC}.

*3 : The maximum current to/from and input are limited by some means with external components, the I_{CLAMP} rating supersedes the VI rating.

*4 : Maximum output current is defined as the peak value of the current of any one of the corresponding pins.

*5 : Average output current is defined as the value of the average current flowing over 100 ms at any one of the corresponding pins. The "average value" can be calculated from the formula of "operating current" times "operating factor".

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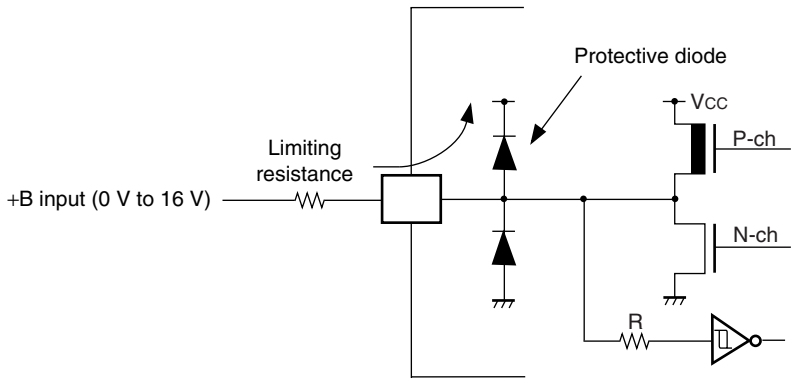
*6 : Average total output current is defined as the value of the average current flowing over 100 ms at all of the corresponding pins. The “average value” can be calculated from the formula of “operating current” times “ operating factor”.

*7 :
- Applicable to pins : P10 to P15, P50 to P57, P70 to P77, P80 to P87
- Use within recommended operating conditions.
- Use at DC voltage (current) .
- The +B signal should always be applied with a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied, the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting power supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Note that analog system input/output pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal input.
- Sample recommended circuits :

• Input/Output equivalent circuits



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

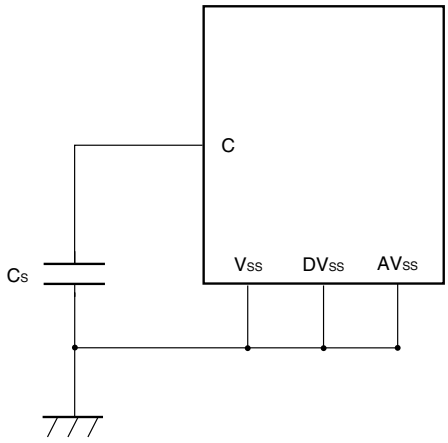
2. Recommended Operating Conditions

(V_{SS} = DV_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC} AV_{CC} DV_{CC}	3.7	5.5	V	(MB90F927/MB90F927S) Low voltage detection reset starts to work when power supply voltage is 4.0 V ± 0.3 V.
		4.3	5.5	V	Holding stop operation status (MB90F927/MB90F927S)
Smoothing capacitor*	C_S	0.1	1.0	µF	Use a ceramic capacitor or other capacitor of equivalent frequency characteristics. A bypass capacitor on the V_{CC} pin should have a capacitance greater than Cs.
Operating temperature	T_A	− 40	+ 105	°C	

* : For smoothing capacitor Cs connections, refer to the illustration below.

• C pin connection diagram



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

(V_{CC} = 5.0 V±10%, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IHA}	—	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Pin inputs if Automotive input levels are selected*1
	V_{IHS2}	—	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Pin inputs if CMOS hysteresis input levels are selected*1 (0.8Vcc/0.2Vcc CMOS hysteresis is selected for P00, P03 and P51)
	V_{IHS1}	—	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	Pin inputs if 0.7Vcc/ 0.3Vcc CMOS hysteresis input levels is selected for P00, P03 and P51.
	V_{IHR}	—	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	$\overline{RST}$ input pin (CMOS hysteresis)
	V_{IHM}	—	—	V_{CC} – 0.3	—	V_{CC} + 0.3	V	MD pin*2
"L" level input voltage	V_{ILA}	—	—	V_{SS} – 0.3	—	0.5 V_{CC}	V	Pin inputs if Automotive input levels are selected*1
	V_{ILS2}	—	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	Pin inputs if CMOS hysteresis input levels are selected*1 (0.8Vcc/0.2Vcc CMOS hysteresis is selected for P00, P03 and P51)
	V_{ILS1}	—	—	V_{SS} – 0.3	—	0.3 V_{CC}	V	Pin inputs if 0.7Vcc/ 0.3Vcc CMOS hysteresis input levels is selected for P00, P03 and P51.
	V_{ILR}	—	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	$\overline{RST}$ input pin (CMOS hysteresis)
	V_{ILM}	—	—	V_{SS} – 0.3	—	V_{SS} + 0.3	V	MD pin*2

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(V_{CC} = 5.0 V±10%, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*3	I_{CC}	V_{CC}	Operating frequency F_{CP} = 16 MHz, normal operation	—	35	45	mA	
			Operating frequency F_{CP} = 16 MHz, writing Flash memory	—	50	60	mA	Flash memory product
			Operating frequency F_{CP} = 16 MHz, erasing Flash memory	—	50	60	mA	
	I_{CCS}		Operating frequency F_{CP} = 16 MHz, sleep mode	—	12	20	mA	
	I_{CTS}		Operating frequency F_{CP} = 2 MHz, time-base timer mode	—	0.4	1.0	mA	
	I_{CTSPLL}		Operating frequency F_{CP} = 16 MHz, PLL timer mode, External frequency = 4MHz	—	4	7	mA	
	I_{CCL}		Operating frequency F_{CP} = 8 kHz, T_A = + 25 °C, sub clock operation	—	90	200	µA	
	I_{CCLS}		Operating frequency F_{CP} = 8 kHz, T_A = + 25 °C, sub sleep operation	—	60	150	µA	
	I_{CCT}		Operating frequency F_{CP} = 8 kHz, T_A = + 25 °C, watch mode	—	60	130	µA	
	I_{CCH}		T_A = + 25 °C, stop mode	—	50	130	µA	
Input leakage current	I_{IL}	All input pins	V_{CC} = DV_{CC} = AV_{CC} = 5.5 V V_{SS} < V_I < V_{CC}	–5	—	+5	µA	
Input capacitance 1	C_{IN1}	Other than V_{CC}, V_{SS}, DV_{CC}, DV_{SS}, AV_{CC}, AV_{SS}, C, P70 to P77, P80 to P87	—	—	5	15	pF	

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(V_{CC} = 5.0 V±10%, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input capacitance 2	C_{IN2}	P70 to P77, P80 to P87	—	—	15	45	pF	
Pull-up resistance	R_{UP}	$\overline{RST}$	—	25	50	100	kΩ	
Pull-down resistance	R_{DOWN}	MD2	—	25	50	100	kΩ	Except Flash memory product
Output “H” voltage 1	V_{OH1}	Other than P70 to P77, P80 to P87	V_{CC} = 4.5 V I_{OH} = –4.0 mA	V_{CC} – 0.5	—	—	V	
Output “H” voltage 2	V_{OH2}	P70 to P77, P80 to P87	V_{CC} = 4.5 V I_{OH} = –30.0 mA	V_{CC} – 0.5	—	—	V	
Output “L” voltage 1	V_{OL1}	Other than P70 to P77, P80 to P87	V_{CC} = 4.5 V I_{OL} = 4.0 mA	—	—	0.4	V	
Output “L” voltage 2	V_{OL2}	P70 to P77, P80 to P87	V_{CC} = 4.5 V I_{OL} = 30.0 mA	—	—	0.55	V	
Large current output drive capacity variation 1	ΔV_{OH2}	PWM1Pn, PWM1Mn, PWM2Pn, PWM2Mn, (n = 0 to 3)	V_{CC} = 4.5 V I_{OH} = 30.0 mA V_{OH2} maximum variation	0	—	90	mV	*4
Large current output drive capacity variation 2	ΔV_{OL2}	PWM1Pn, PWM1Mn, PWM2Pn, PWM2Mn, (n = 0 to 3)	V_{CC} = 4.5 V I_{OH} = 30.0 mA V_{OL2} maximum variation	0	—	90	mV	*4
LCD internal divider resistance	R_{LCD}	V0 to V3	—	50	100	200	kΩ	
COM0 to COM3 output impedance	R_{VCOM}	COMn (n = 0 to 3)	—	—	—	2.5	kΩ	
SEG0 to SEG31 output impedance	R_{VSEG}	SEGn (n = 0 to 31)	—	—	—	15	kΩ	
LCD leakage current	I_{LCDC}	V0 to V3 COMm (m = 0 to 3) SEGn (n = 0 to 31)	—	–5.0	—	+5.0	µA	

*1 : All input pins except X0, X0A, MD0, MD1, and MD2.

*2 : MD0, MD1, and MD2 pins.

*3 : Power supply current values assume external clock feed from the X1 pin and X1A pin. Users must be aware that power supply current levels differ depending on whether an external clock or oscillator is used.

*4 : Defined as maximum variation in V_{OH2}/V_{OL2} with all ch.0 PWM1P0/PWM1M0/PWM2P0/PWM2M0 simultaneously ON. Similarly for other channels.

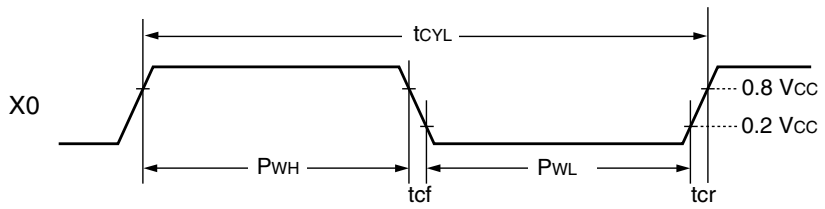
4. AC Characteristics

(1) Clock timing

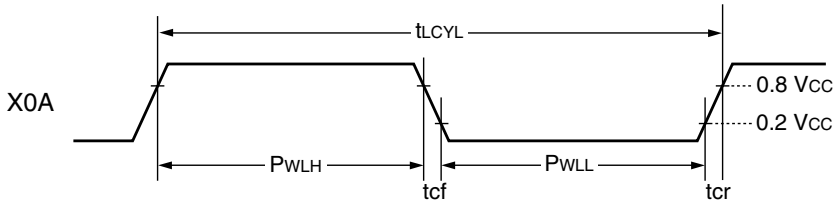
(V_{CC} = 5.0 V±10%, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin name	Condi-tions	Value			Unit	Remarks
				Min	Typ	Max		
Base oscillation clock frequency	F_C	X0, X1	—	4	—	12	MHz	1/2 (when PLL stops)
				4	—	12	MHz	PLL x 1
				4	—	8	MHz	PLL x 2
				4	—	5.33	MHz	PLL x 3
				4	—	4	MHz	PLL x 4
	F_{LC}	X0A, X1A		—	32.768	—	kHz	
Base oscillation clock cycle time	t_{CYL}	X0, X1		—	250	—	ns	
	t_{LCYL}	X0A, X1A		—	30.5	—	µs	
Input clock pulse width	P_{WH}, P_{WL}	X0		10	—	—	ns	Use duty ratio of 40 to 60% as a guideline
	P_{WLH}, P_{WLL}	X0A		—	15.2	—	µs	
Input clock rise and fall time	tcr, tcf	X0, X0A		—	—	5	ns	external clock signal
Internal operating clock frequency	F_{CP}	—		2	—	16	MHz	Using main clock (PLL clock)
	F_{LCP}	—		—	8.192	—	kHz	Using sub clock
Internal operating clock cycle time	t_{CP}	—		62.5	—	500	ns	Using main clock (PLL clock)
	t_{LCP}	—		—	122.1	—	µs	Using sub clock

• X0 clock timing

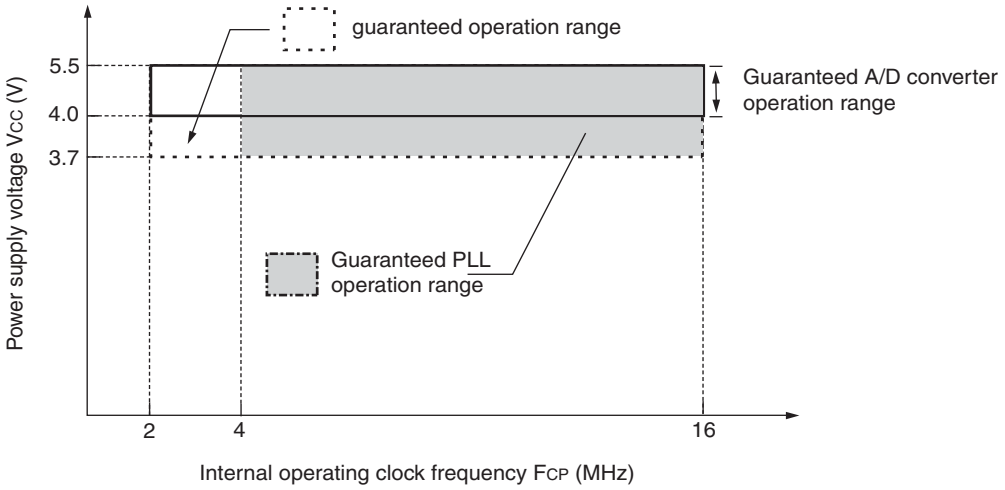


• X0A clock timing

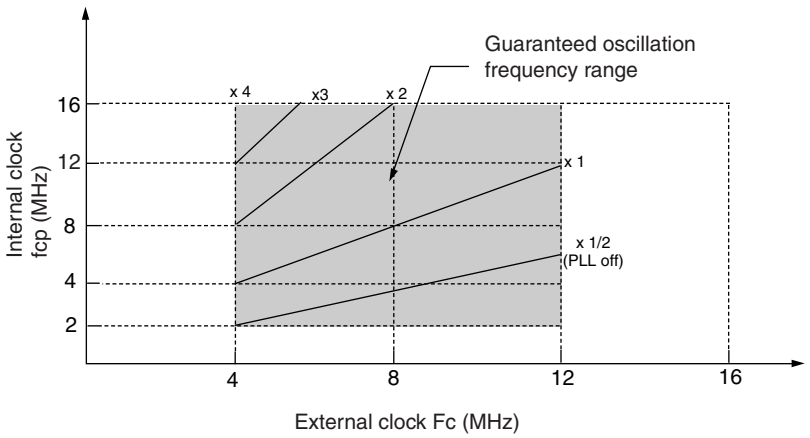


- Range of guaranteed operation

Relation between internal operating clock frequency and power supply voltage



Note : The MB90F927/ MB90F927S enters reset mode at power supply voltage below 4 V ± 0.3 V.



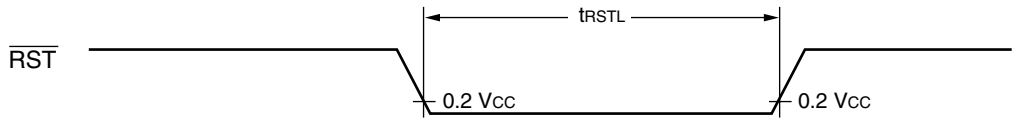
(2) Reset input

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

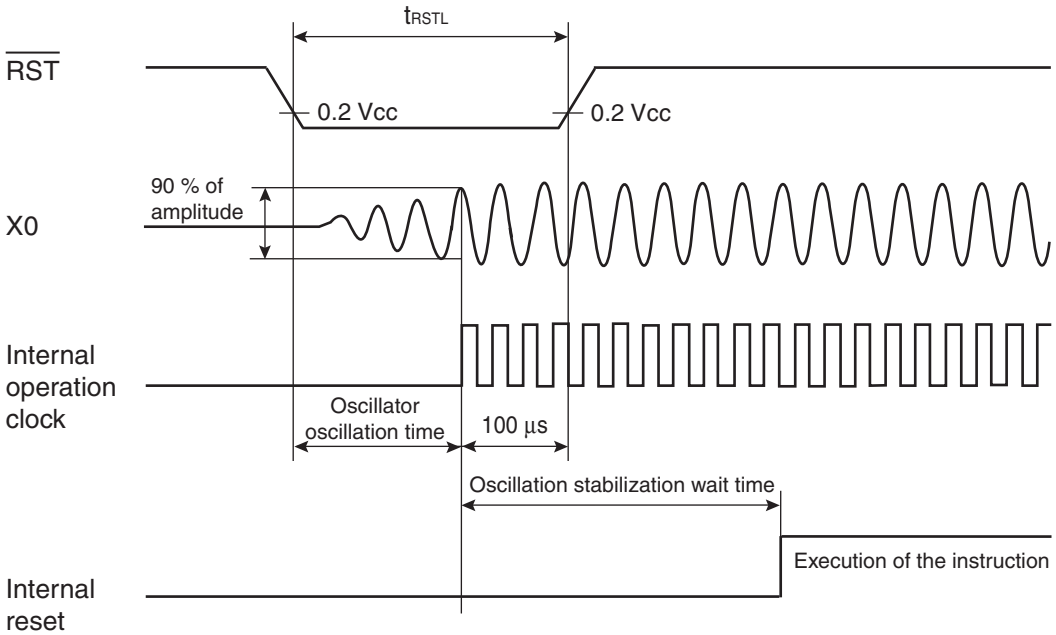
Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	500	—	ns	At normal operation
			Oscillator oscillation time* + 100 µs	—	ms	At stop mode, sub clock mode, sub sleep mode, and watch mode
			100	—	µs	At time-base timer mode

*: Oscillator's oscillation time is the time that the amplitude reaches 90%. The oscillation time of a crystal oscillator is between several ms and tens of ms. The oscillation time of a ceramic oscillator is between hundreds of µs and several ms. The oscillation time of an external clock is 0 ms.

- At normal operation



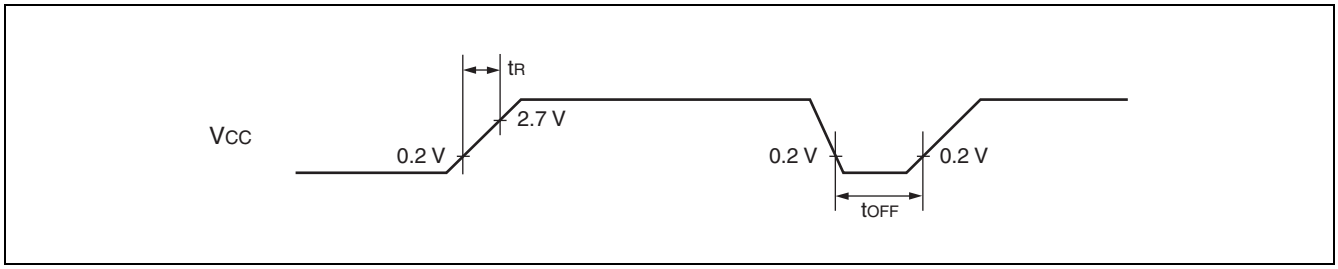
- At stop mode, sub clock mode, sub sleep mode, watch mode, and power-on



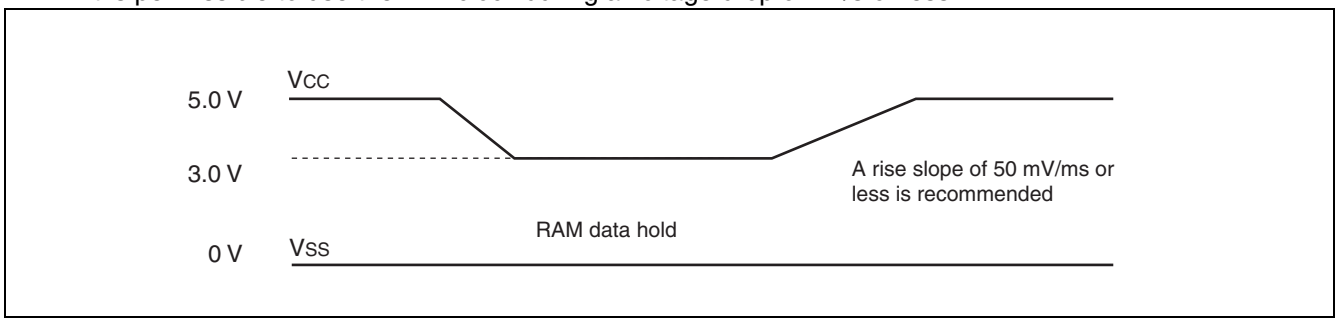
(3) Power-on reset

(V_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Power supply rise time	t_R	V_{CC}	—	0.05	30	ms	
Power supply start voltage	V_{OFF}			—	0.2	V	
Power supply attained voltage	V_{ON}			2.7	—	V	
Power supply cutoff time	t_{OFF}			50	—	ms	Waiting time until power-on



Note : Extreme variations in power supply voltage may activate a power-on reset. As the illustration below shows, when varying power supply voltage during operation, the use of a smooth voltage rise with suppressed fluctuation is recommended. Also in this situation, the PLL clock on the device should not be used, however it is permissible to use the PLL clock during a voltage drop of 1V/s or less.



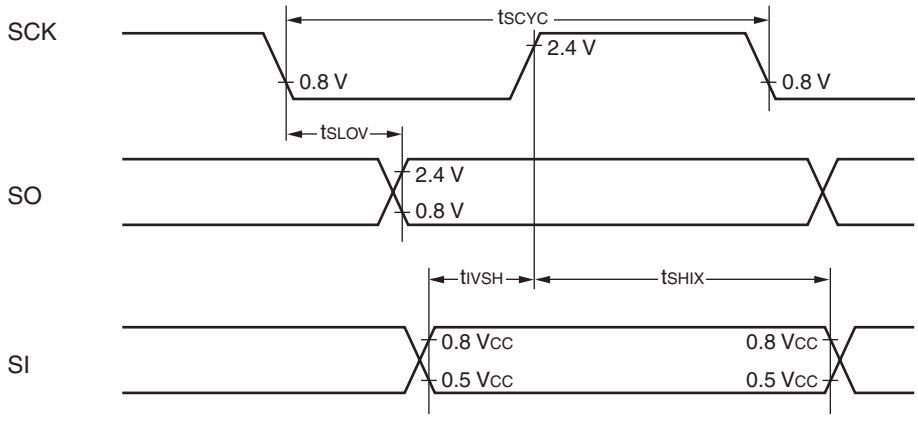
(4) SIO timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

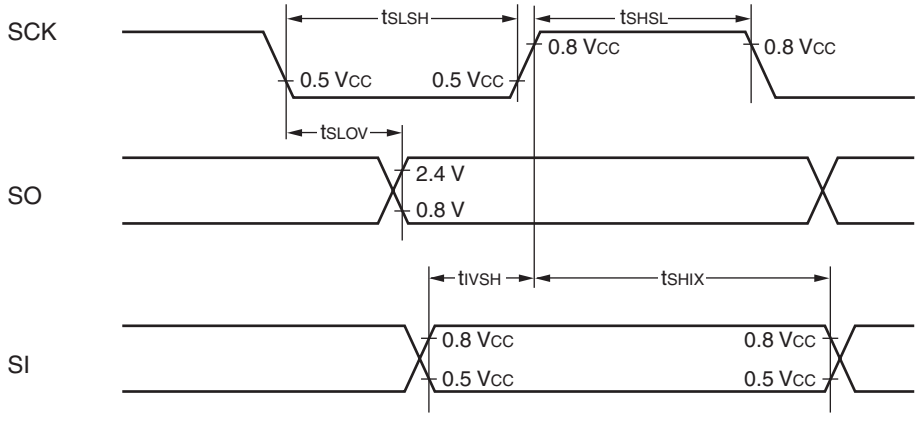
Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal shift clock mode output pin C_L = 80 pF + 1TTL	8 t_{CP}	—	ns
SCK ↓ → SO delay time	t_{SLOV}	SCK, SO		–80	+ 80	ns
Valid SI → SCK ↑	t_{IVSH}	SCK, SI		100	—	ns
SCK ↑ → valid SI hold time	t_{SHIX}			60	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK	External shift clock mode output pin C_L = 80 pF + 1TTL	4 t_{CP}	—	ns
Serial clock “L” pulse width	t_{SLSH}			4 t_{CP}	—	ns
SCK ↓ → SO delay time	t_{SLOV}	SCK, SO		—	150	ns
Valid SI → SCK ↑	t_{IVSH}	SCK, SI		60	—	ns
SCK ↑ → valid SI hold time	t_{SHIX}			60	—	ns

Notes : • AC ratings are for CLK synchronous mode.
• C_L is load capacitance connected to pin during testing.
• t_{CP} is internal operating clock cycle time. Refer to “ (1) Clock timing”.

• Internal shift clock mode



• External shift clock mode



(5) UART0/1 (LIN/SCI)

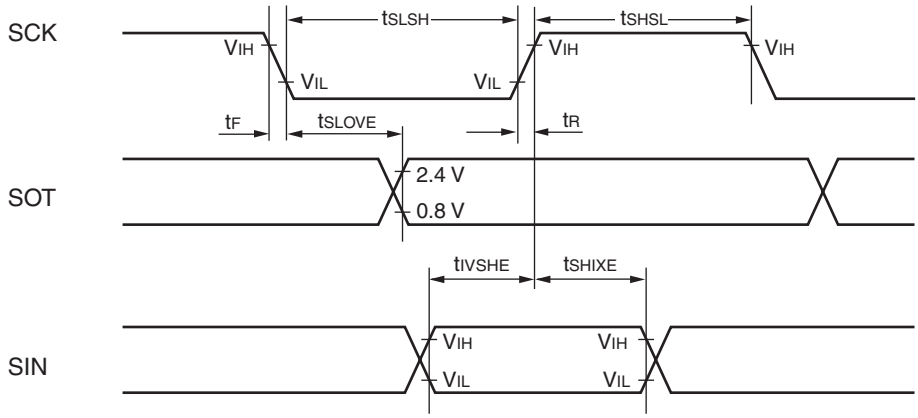
- **Bit setting: ESCR0/1:SCES=0, ECCR0/1:SCDE=0**

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

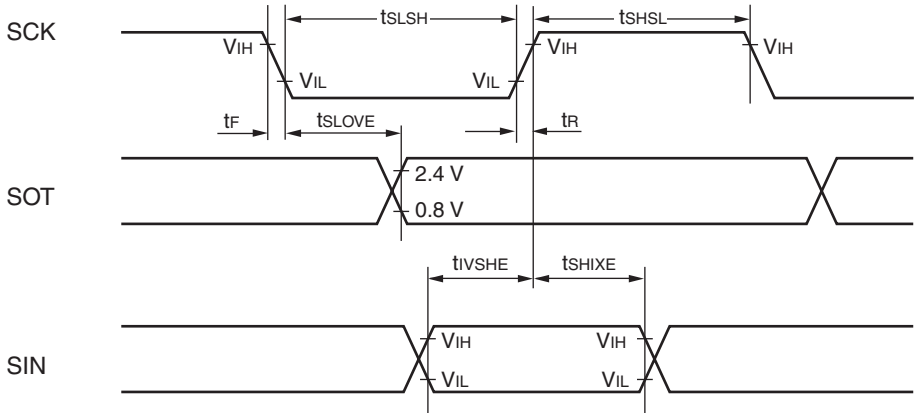
Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0, SCK1	Internal shift clock mode output pins are C_L = 80 pF + 1TTL	5 t_{CP}	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCK0, SCK1, SOT0, SOT1		– 50	+ 50	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK0, SCK1, SIN0, SIN1		t_{CP} + 80	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXI}			0	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK0, SCK1	External shift clock mode output pins are C_L = 80 pF + 1TTL	t_{CP} + 10	—	ns
Serial clock “H” pulse width	t_{SHSL}			3 t_{CP} – t_R	—	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCK0, SCK1, SOT0, SOT1		—	2 t_{CP} + 60	ns
Valid SIN → SCK ↑	t_{IVSHE}	SCK0, SCK1, SIN0, SIN1		30	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXE}			t_{CP} + 30	—	ns
SCK fall time	t_F	SCK0, SCK1		—	10	ns
SCK rise time	t_R			—	10	ns

Notes :
- AC characteristic in CLK synchronized mode.
- C_L is load capacity value of pins when testing.
- t_{CP} is internal operating clock cycle time (machine clock). Refer to “ (1) Clock timing”.

- Internal shift clock mode



- External shift clock mode

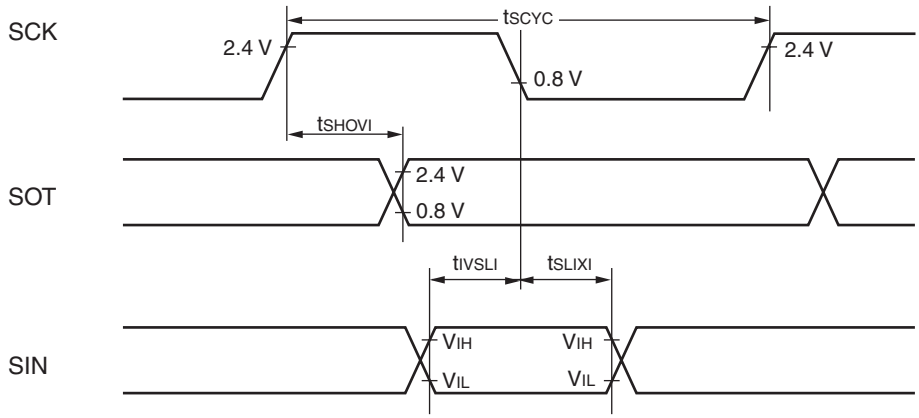


• **Bit setting: ESCR0/1:SCES=1, ECCR0/1:SCDE=0**

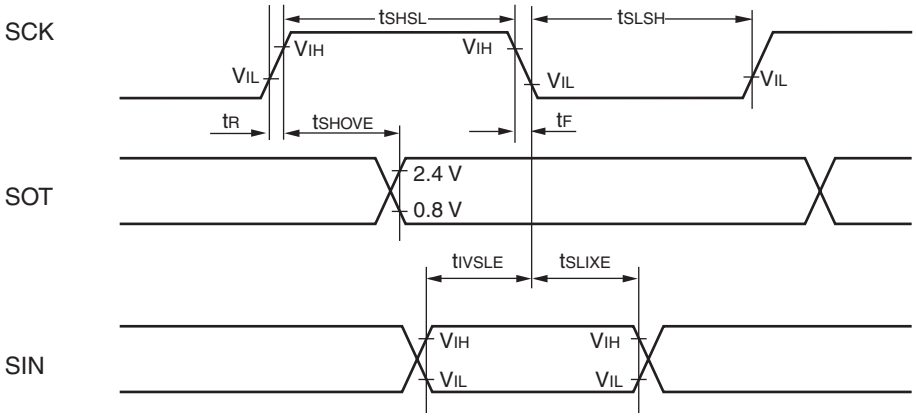
(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0, SCK1	Internal shift clock mode output pins are C_L = 80 pF + 1TTL	5 t_{CP}	—	ns
SCK ↑ → SOT delay time	t_{SLOVI}	SCK0, SCK1, SOT0, SOT1		– 50	+ 50	ns
Valid SIN → SCK ↓	t_{IVSHI}	SCK0, SCK1, SIN0, SIN1		t_{CP} + 80	—	ns
SCK ↓ → valid SIN hold time	t_{SHIXI}			0	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK0, SCK1	External shift clock mode output pins are C_L = 80 pF + 1TTL	3 t_{CP} – t_R	—	ns
Serial clock “L” pulse width	t_{SLSH}			t_{CP} + 10	—	ns
SCK ↑ → SOT delay time	t_{SLOVE}	SCK0, SCK1, SOT0, SOT1		—	2 t_{CP} + 60	ns
Valid SIN → SCK ↓	t_{IVSHE}	SCK0, SCK1, SIN0, SIN1		30	—	ns
SCK ↓ → valid SIN hold time	t_{SHIX}			t_{CP} + 30	—	ns
SCK fall time	t_F	SCK0, SCK1		—	10	ns
SCK rise time	t_R			—	10	ns

- Internal shift clock mode



- External shift clock mode

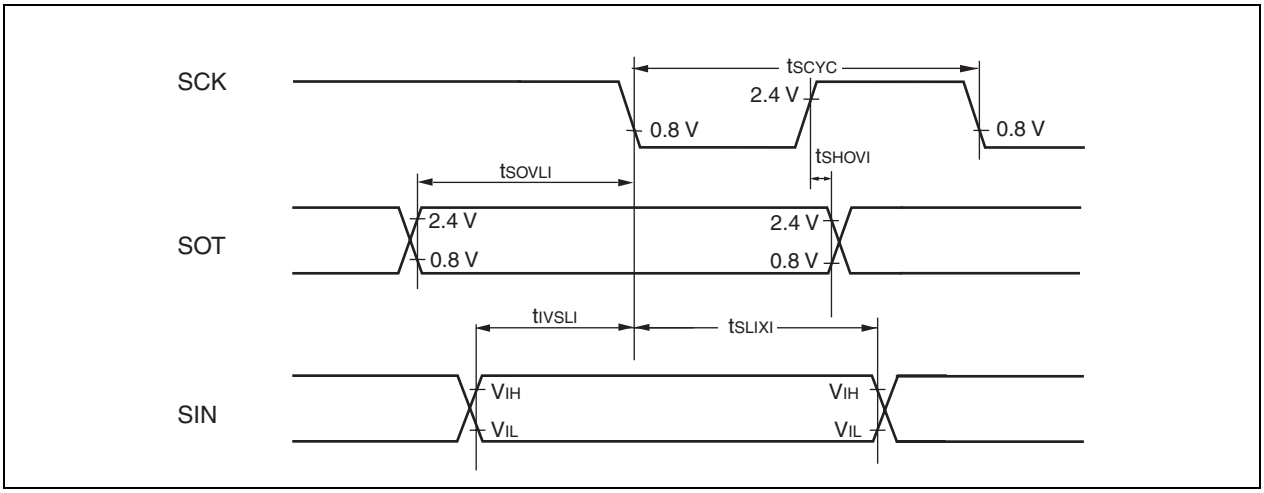


• **Bit setting: ESCR0/1:SCES=0, ECCR0/1:SCDE=1**

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0, SCK1	Internal clock operation output pins are C_L = 80 pF + 1TTL	5 t_{CP}	—	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCK0, SCK1, SOT0, SOT1		– 50	+ 50	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK0, SCK1, SIN0, SIN1		t_{CP} + 80	—	ns
SCK ↓ → valid SIN hold time	t_{SLIXI}			0	—	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCK0, SCK1, SOT0, SOT1		3 t_{CP} – 70	—	ns

Notes : t_{CP} is the machine clock cycle time (Unit : ns) . Refer to “ (1) Clock timing”rating for t_{CP}.

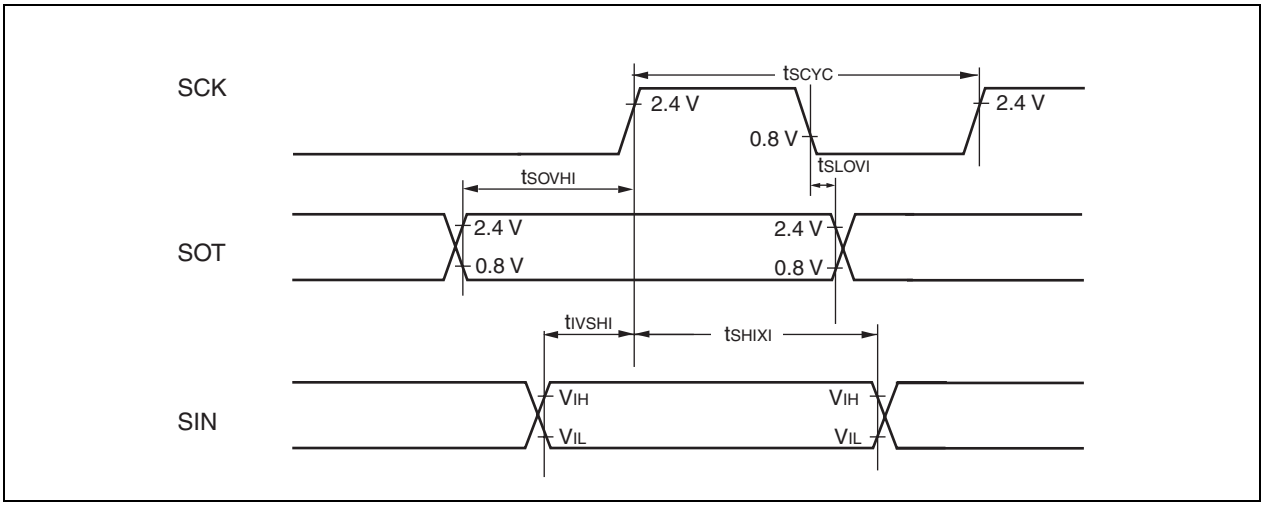


• **Bit setting: ESCR0/1:SCES=1, ECCR0/1:SCDE=1**

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0, SCK1	Internal clock operation output pins are C_L = 80 pF + 1TTL	5 t_{CP}	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCK0, SCK1, SOT0, SOT1		– 50	+ 50	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK0, SCK1, SIN0, SIN1		t_{CP} + 80	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXI}			0	—	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCK0, SCK1, SOT0, SOT1		3 t_{CP} – 70	—	ns

Notes : t_{CP} is the machine clock cycle time (Unit : ns) . Refer to “ (1) Clock timing”rating for t_{CP}.



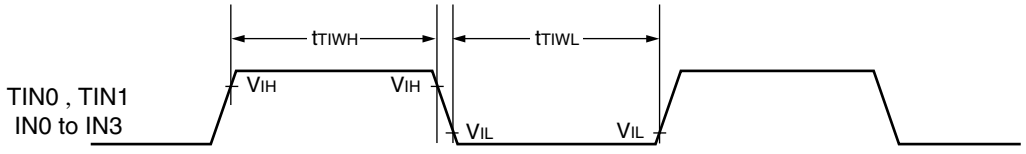
(6) Timer input timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH} t_{TIWL}	TIN0, TIN1, IN0 to IN3	—	4 t_{CP}	—	ns

Note : t_{CP} is internal operating clock cycle time. Refer to “ (1) Clock timing”.

- Timer input timing



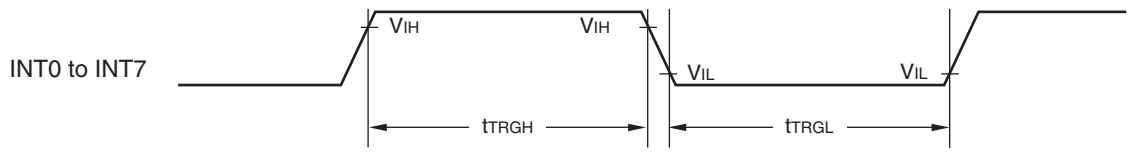
(7) Trigger input timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Input pulse width	t_{TRGH}, t_{TRGL}	INT0 to INT7	—	200	—	ns
		ADTG	—	t_{CP} + 200	—	ns

Note : t_{CP} is internal operating clock cycle time (machine clock) . Refer to “ (1) Clock timing”.

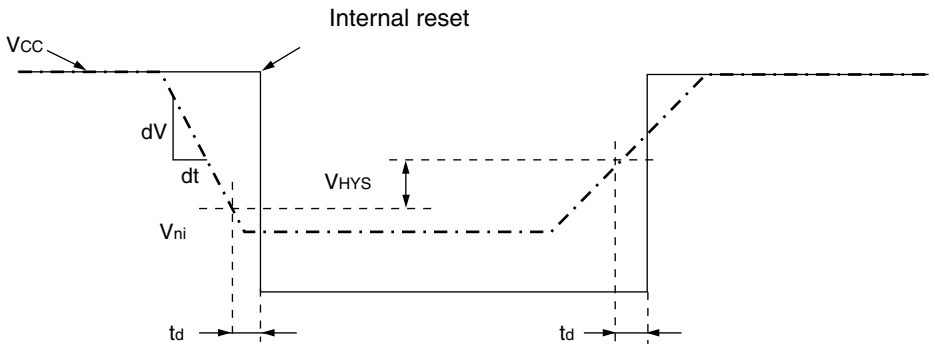
- Trigger input timing



(8) Low voltage detection

(V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Detection voltage	V_{DL}	V_{CC}	—	3.7	4.0	4.3	V	During voltage drop
Hysteresis width	V_{HYS}	V_{CC}	—	0.1	—	—	V	During voltage rise
Power supply voltage fluctuation ratio	dV/dt	V_{CC}	—	–0.1	—	+0.02	V/µs	
Detection delay time	td	—	—	—	—	35	µs	



5. A/D Converter

(1) Electrical Characteristics

(V_{CC} = AV_{CC} = 5.0 V±10%, 3.0V ≤ AVRH-AVss, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +105 °C)

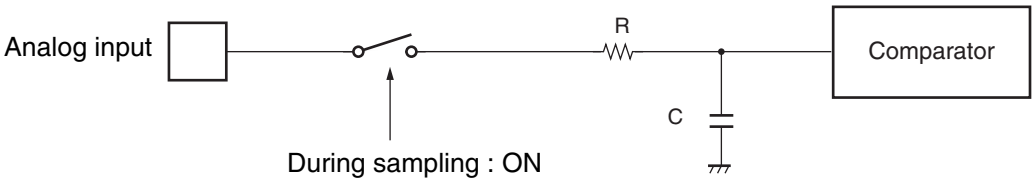
Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	—	—	±3.0	LSB	
Non-linear error	—	—	—	—	±2.5	LSB	
Differential linear error	—	—	—	—	±1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN7	AV_{SS} – 1.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.5 LSB	V	1 LSB = (AVRH – AV_{SS}) / 1024
Full scale transition voltage	V_{FST}	AN0 to AN7	AVRH – 3.5 LSB	AVRH – 1.5 LSB	AVRH + 0.5 LSB	V	
Sampling time	t_{SMP}	—	1.4	—	16500	µs	4.5 V ≤ AVcc ≤ 5.5 V
			2.0				4.0 V ≤ AVcc ≤ 4.5 V
Compare time	t_{CMP}	—	0.5	—	—	µs	4.5 V ≤ AVcc ≤ 5.5 V
			1.2				4.0 V ≤ AVcc ≤ 4.5 V
Analog port input current	I_{AIN}	AN0 to AN7	– 0.3	—	+0.3	µA	
Analog input voltage	V_{AIN}	AN0 to AN7	AVss	—	AVRH	V	
Reference voltage	AVRH	AVRH	AVss+2.7	—	AV_{CC}	V	
Power supply current	I_A	AV_{CC}	—	3.5	7.5	mA	
	I_{AH}		—	—	5	µA	*
Reference voltage supply current	I_R	AVRH	—	600	900	µA	V_{AVRH} = 5.0 V
	I_{RH}	AVRH	—	—	5	µA	*
Inter-channel variation	—	AN0 to AN7	—	—	4	LSB	

* : Defined as supply current (when V_{CC} = AV_{CC} = AVRH = 5.0 V) with A/D converter not operating, and CPU in stop mode.

• **Notes of the external impedance of the analog input and its sampling time**

A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. Also, if the sampling time cannot be sufficient, connect a capacitor of about 0.1 μF to the analog input pin.

• Analog input equivalent circuit



MB90F927/MB90F927S

	R	C
4.5 V ≤ AVcc ≤ 5.5 V :	2.0 kΩ (Max)	16.0 pF (Max)
4.0 V ≤ AVcc ≤ 4.5 V :	8.2 kΩ (Max)	16.0 pF (Max)

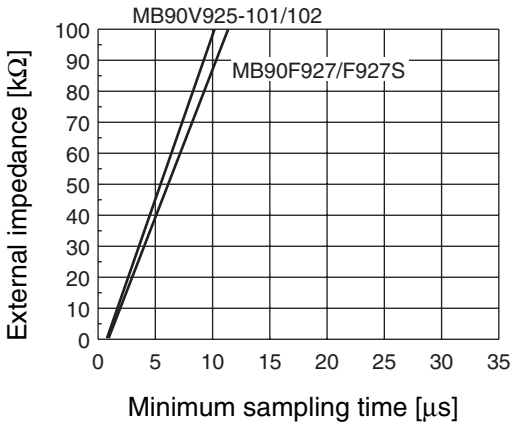
MB90V925-101/102

4.5 V ≤ AVcc ≤ 5.5 V :	2.0 kΩ (Max)	14.4 pF (Max)
4.0 V ≤ AVcc ≤ 4.5 V :	8.2 kΩ (Max)	14.4 pF (Max)

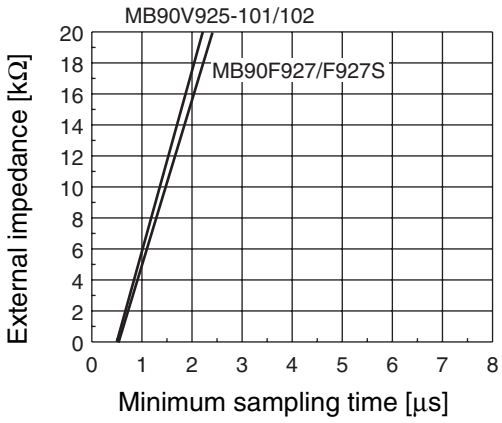
Note : The values are reference values.

- The relationship between the external impedance and minimum sampling time
- At 4.5 V ≤ AVcc ≤ 5.5 V

(External impedance = 0 kΩ to 100 kΩ)

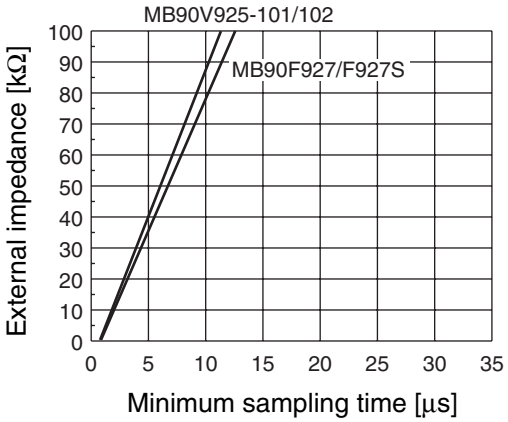


(External impedance = 0 kΩ to 20 kΩ)

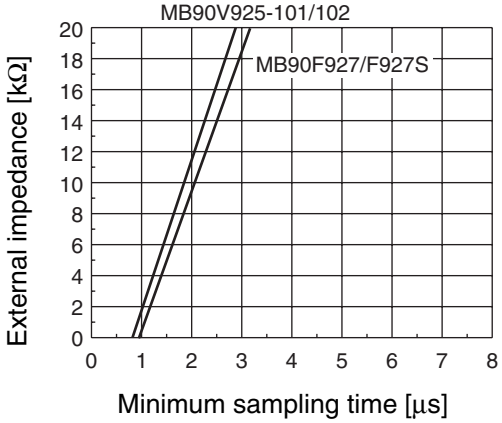


- At 4.0 V ≤ AVcc ≤ 4.5 V

(External impedance = 0 kΩ to 100 kΩ)



(External impedance = 0 kΩ to 20 kΩ)



- About errors
  As |AVRH - AV_{SS}| becomes smaller, values of relative errors grow larger.

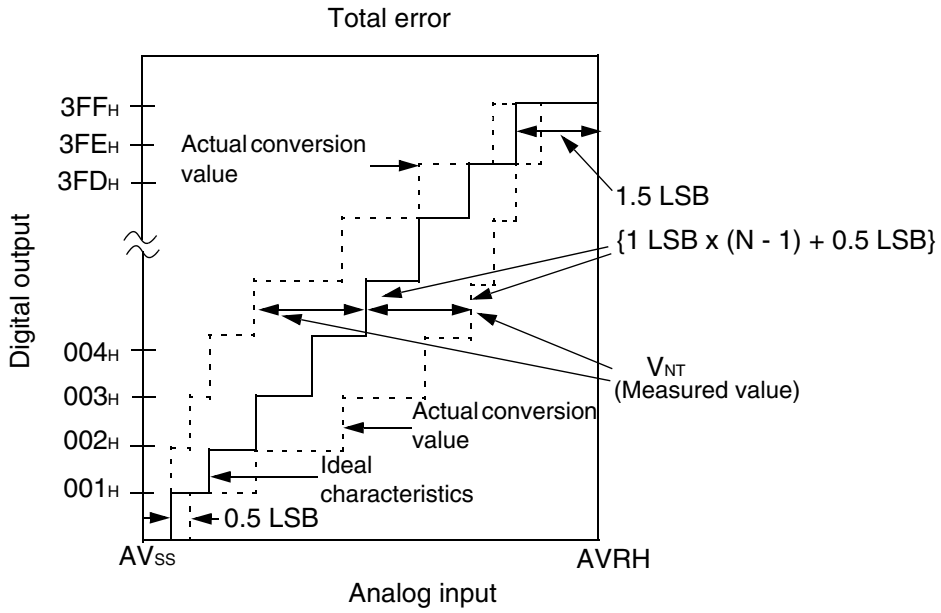
(2) Definition of terms

Resolution : Analog changes that are identifiable with the A/D converter.

Non-Linear error : The deviation of the straight line connecting the zero transition point ("00 0000 0000" ↔ "00 0000 0001") with the full-scale transition point ("11 1111 1110" ↔ "11 1111 1111") from actual conversion characteristics.

Differential linear error : The deviation of input voltage needed to change the output code by 1 LSB from the ideal value.

Total error : The total error is defined as a difference between the actual value and the theoretical value, which includes zero-transition error/full-scale transition error and linear error.



$$\text{Total error for digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$1\ \text{LSB(Ideal)} = \frac{AVRH - AV_{SS}}{1024}\ [\text{V}]$$

N : A/D converter digital output value

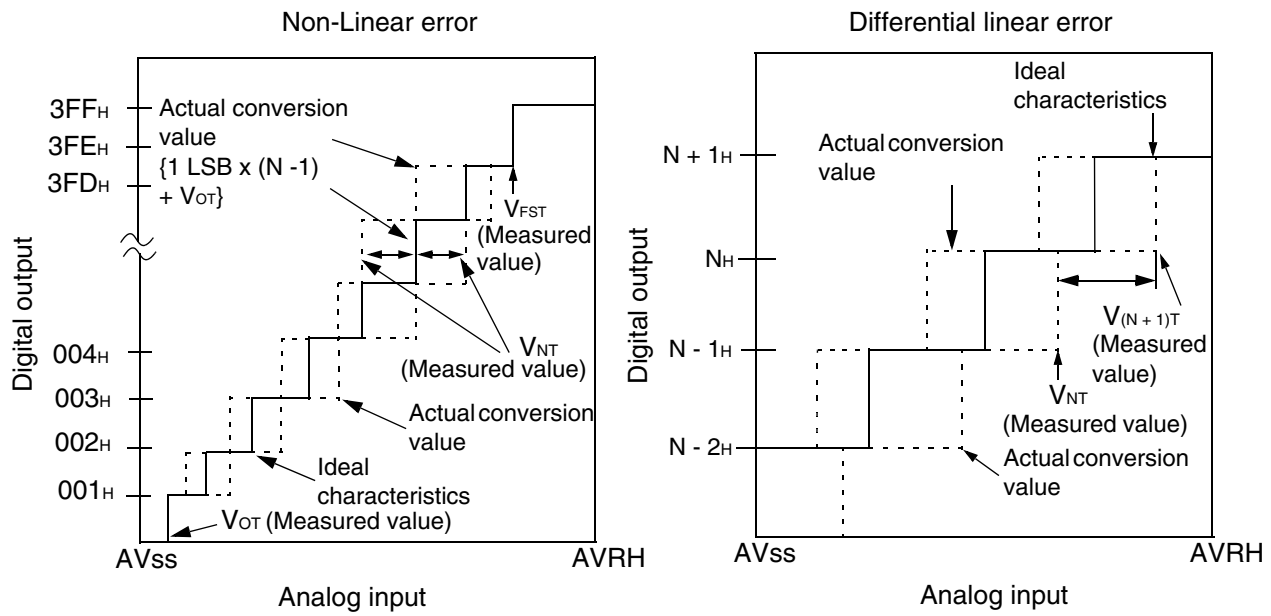
V_{OT} (Ideal) = AVss + 0.5 LSB [V]

V_{FST} (Ideal) = AVRH − 1.5 LSB [V]

V_{NT} : Voltage at a transition of digital output from $(N - 1)_H$ to N_H

(Continued)

(Continued)



$$\text{Non-Linear error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linear error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

N : A/D converter digital output value
V_{OT} : Voltage at transition of digital output from “000_H” to “001_H”
V_{FST} : Voltage at transition of digital output from “$3FE_H$” to “$3FF_H$”

6. Flash Memory Program/Erase Characteristics

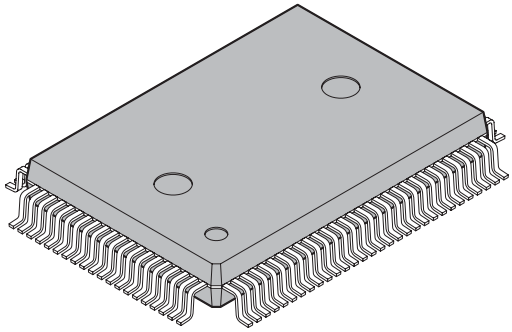
Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Chip erase time	T_A = + 25 °C V_{CC} = 5.0 V	—	1	15	s	Excludes pre-programming before erase
Byte (8-bit width) programming time		—	32	3600	µs	Excludes system-level overhead
Erase/program cycle	—	10000	—	—	cycle	
Flash memory data retention time	Average T_A = + 85 °C	20	—	—	year	*

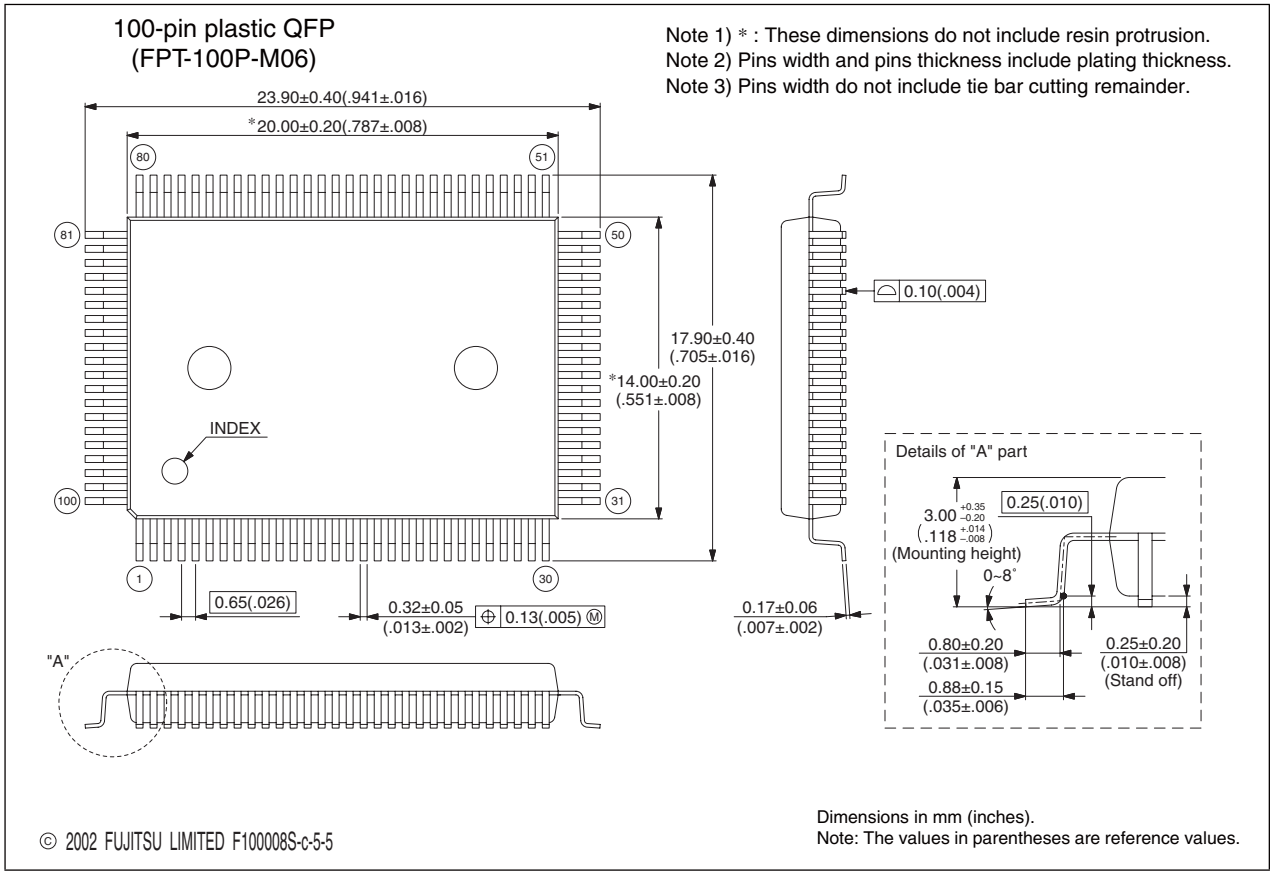
* : This value comes from the technology qualification. (using Arrhenius equation to translate high temperature measurements into normalized value at + 85 °C)

■ ORDERING INFORMATION

Part number	Package	Remarks
MB90F927PF-GE1 MB90F927SPF-GE1	100-pin plastic QFP (FPT-100P-M06)	
MB90F927PFV-GE1 MB90F927SPFV-GE1	100-pin plastic LQFP (FPT-100P-M05)	
MB90V925-101 MB90V925-102	299-pin ceramic PGA (PGA-299C-A01)	For evaluation

■ PACKAGE DIMENSIONS

100-pin plastic QFP		
 (FPT-100P-M06)	Lead pitch	0.65 mm
	Package width × package length	14.00 × 20.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	3.35 mm MAX
	Code (Reference)	P-QFP100-14×20-0.65



Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/fj/DATASHEET/ef-ovpklv.html

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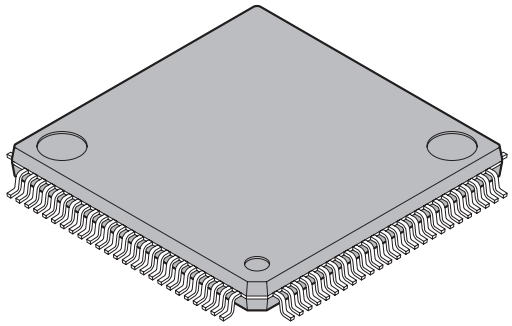
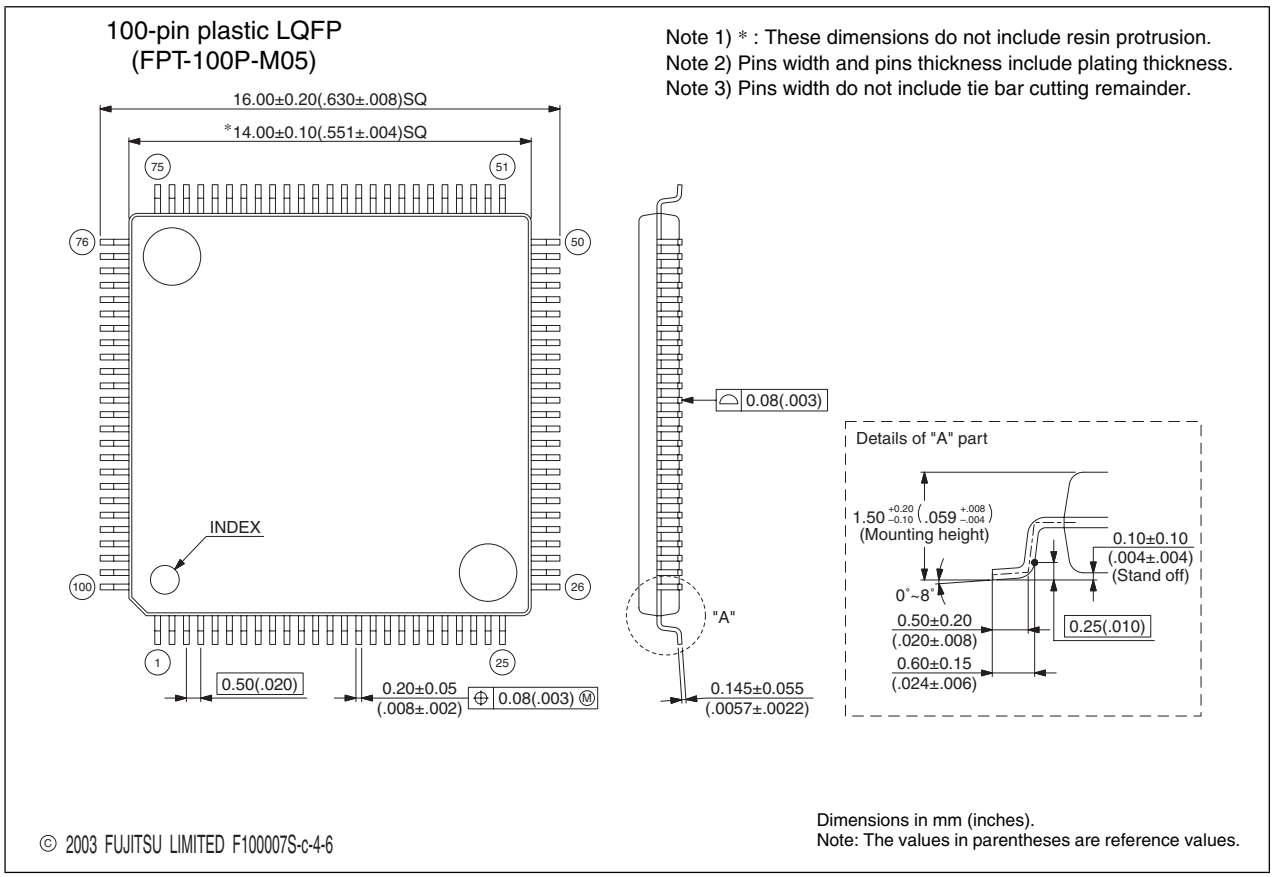
100-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	14.0 × 14.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.65g
(FPT-100P-M05)	Code (Reference)	P-LFQFP100-14×14-0.50



Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/fj/DATASHEET/ef-ovpklv.html

The information for microcontroller supports is shown in the following homepage.
http://www.fujitsu.com/global/services/microelectronics/product/micom/support/index.html

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