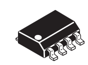
3.3 V Zero Delay Buffer

The MPC962304 is a 3.3 V Zero Delay Buffer designed to distribute high-speed clocks in PC, workstation, datacom, telecom and other high-performance applications. The MPC962304 uses an internal PLL and an external feedback path to lock its low-skew clock output phase to the reference clock phase, providing virtually zero propagation delay. The input-to-output skew is guaranteed to be less than 250 ps and output-to-output skew is guaranteed to be less than 200 ps.

MPC962304



D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-06

Features

- 1:4 outputs LVCMOS zero-delay buffer
- Zero input-output propagation delay, adjustable by the capacitive load on FBK input
- Multiple Configurations, See **Table 1. Available MPC962304 Configurations**
- Multiple low-skew outputs
  – 200 ps max output-output skew
  – 500 ps max device-device skew
- Supports a clock I/O frequency range of 10 MHz to 133 MHz
- Low jitter, 200 ps max cycle-cycle
- 8-pin SOIC package
- Single 3.3 V supply
- Ambient temperature range: –40°C to +85°C
- Compatible with the CY2304

Functional Description

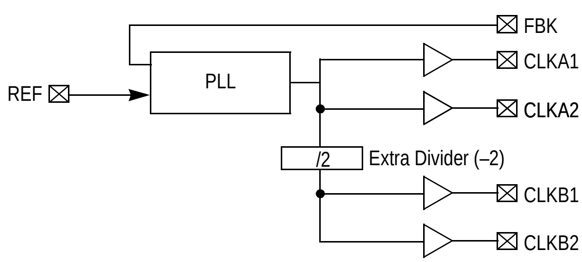
The MPC962304 has two banks of two outputs each. The MPC962304 PLL enters a power down state when there are no rising edges on the REF input. During this state, all of the outputs are in tristate. When the PLL is turned off, there is less than 25 µA of current draw.

Multiple MPC962304 devices can accept and distribute the same input clock throughout the system. In this situation, the difference between the output skews of two devices will be less than 500 ps.

The MPC962304 is offered in two configurations. In the -1 version, the reference frequency is reproduced by the PLL and provided to the outputs.

The MPC962304-2 provides 1/2X and 2X the reference frequency at the output banks.

Block Diagram



Pin Configuration

8-pin SOIC
Top View

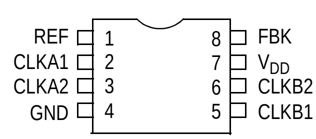


Table 1. Available MPC962304 Configurations

Device	Feedback From	Bank A Frequency	Bank B Frequency
MPC962304-1	Bank A or Bank B	Reference	Reference
MPC962304-2	Bank A	Reference	Reference/2
MPC962304-2	Bank B	2 X Reference	Reference

Table 2. Pin Description

Pin	Signal	Description
1	REF[1]	Input reference frequency, 5 V tolerant input
2	CLKA1[2]	Clock output, Bank A
3	CLKA2[2]	Clock output, Bank A
4	GND	Ground
5	CLKB1[2]	Clock output, Bank B
6	CLKB2[2]	Clock output, Bank B
7	V_{DD}	3.3 V supply
8	FBK	PLL feedback input

1. Weak pull-down.
2. Weak pull-down on all outputs.

Table 3. Maximum Ratings

Characteristics	Value	Unit
Supply Voltage to Ground Potential	–0.5 to +3.9	V
DC Input Voltage (Except REF)	–0.5 to V_{DD}+0.5	V
DC Input Voltage REF	–0.5 to 5.5	V
Storage Temperature	–65 to +150	°C
Junction	150	°C
Static Discharge Voltage (per MIL-STD-883, Method 3015)	>2000	V

Table 4. Operating Conditions for MPC962304-X Industrial Temperature Devices

Parameter	Description	Min	Max	Unit
V_{DD}	Supply Voltage	3.0	3.6	V
T_A	Operating Temperature (Ambient Temperature)	–40	85	°C
C_L	Load Capacitance, below 100 MHz		30	pF
	Load Capacitance, from 100 MHz to 133 MHz		15	pF
C_{IN}	Input Capacitance[1]		7	pF

1. Applies to both REF clock and FBK.

Table 5. Electrical Characteristics for MPC962304-X Industrial Temperature Devices[1]

Parameter	Description	Test Conditions	Min	Max.	Unit
V_{IL}	Input LOW Voltage			0.8	V
V_{IH}	Input HIGH Voltage		2.0		V
I_{IL}	Input LOW Current	V_{IN} = 0 V		50.0	μA
I_{IH}	Input HIGH Current	$V_{IN} = V_{DD}$		100.0	μA
V_{OL}	Output LOW Voltage[2]	I_{OL} = 8 mA (-1, -2)		0.4	V
V_{OH}	Output HIGH Voltage[2]	I_{OH} = -8 mA (-1, -2)	2.4		V
I_{DD} (PD mode)	Power Down Supply Current	REF = 0 MHz		25.0	μA
I_{DD}	Supply Current	Unloaded outputs, 100 MHz, Select inputs at V_{DD} or GND		45.0	mA
		Unloaded outputs, 66-MHz REF (-1, -2)		35.0	mA
		Unloaded outputs, 35-MHz REF (-1, -2)		20.0	mA

1. All parameters are specified with loaded outputs.
2. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Table 6. Switching Characteristics for MPC962304-X Industrial Temperature Devices[1]

Parameter	Name	Test Conditions	Min	Typ	Max	Unit
t_1	Output Frequency	30-pF load, all devices	10		100	MHz
	Output Frequency	15-pF load, all devices	10		133.3	MHz
	Duty Cycle[2] = $t_2 \div t_1$ (-1, -2)	Measured at 1.4 V, FOUT = 66.66 MHz 30-pF load	40.0		60.0	%
	Duty Cycle[2] = $t_2 \div t_1$ (-1, -2)	Measured at 1.4 V, FOUT < 50.0 MHz 15-pF load	45.0		55.0	%
t_3	Rise Time[2] (-1, -2)	Measured between 0.8 V and 2.0 V, 30-pF load			2.50	ns
	Rise Time[2] (-1, -2)	Measured between 0.8 V and 2.0 V, 15-pF load			1.50	ns
t_4	Fall Time[2] (-1, -2)	Measured between 0.8 V and 2.0 V, 30-pF load			2.50	ns
	Fall Time[2] (-1, -2)	Measured between 0.8 V and 2.0 V, 15-pF load			1.50	ns
t_5	Output to Output Skew on same Bank (-1, -2)[2]	All outputs equally loaded			200	ps
	Output Bank A to Output Bank B Skew (-1)	All outputs equally loaded			200	ps
	Output Bank A to Output Bank B Skew (-2)	All outputs equally loaded			400	ps
t_6	Delay, REF Rising Edge to FBK Rising Edge[2]	Measured at $V_{DD}/2$		0	±250	ps
t_7	Device to Device Skew[2]	Measured at $V_{DD}/2$ on the FBK pins of devices		0	500	ps
t_J	Cycle to Cycle Jitter[2] (-1)	Measured at 66.67 MHz, loaded outputs, 15-pF load			180	ps
		Measured at 66.67 MHz, loaded outputs, 30-pF load			200	ps
		Measured at 133.3 MHz, loaded outputs, 15 pF load			100	ps
t_J	Cycle to Cycle Jitter[2] (-2)	Measured at 66.67 MHz, loaded outputs 30-pF load			400	ps
		Measured at 66.67 MHz, loaded outputs 15-pF load			380	ps
t_{LOCK}	PLL Lock Time[2]	Stable power supply, valid clocks presented on REF and FBK pins			1.0	ms

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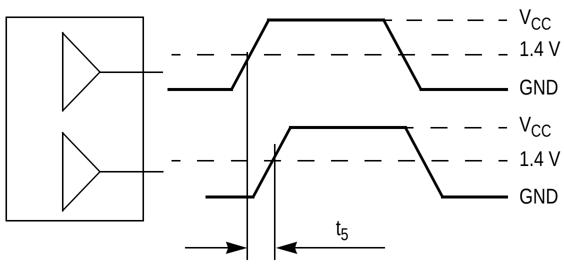
APPLICATIONS INFORMATION



The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 1. Output-to-Output Skew $t_{SK(O)}$

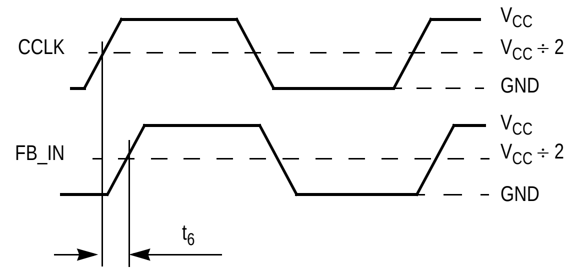
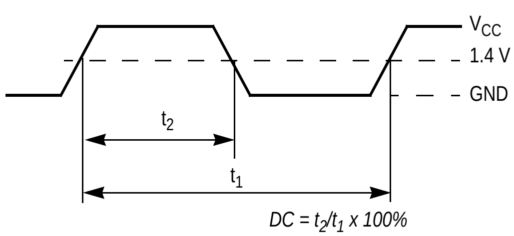


Figure 2. Static Phase Offset Test Reference



The time from the PLL controlled edge to the non-controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 3. Output Duty Cycle (DC)

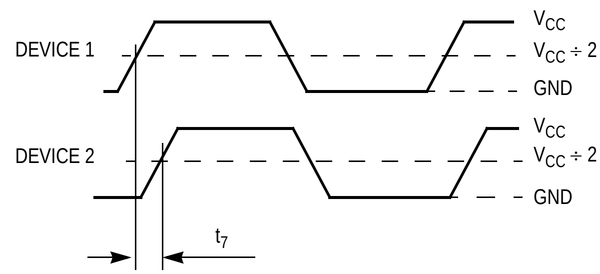
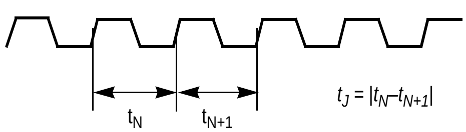


Figure 4. Device-to-Device Skew



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 5. Cycle-to-Cycle Jitter

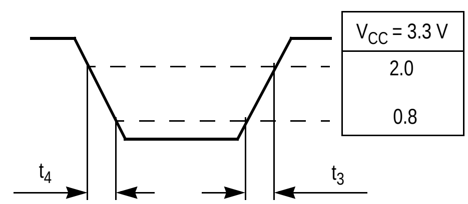
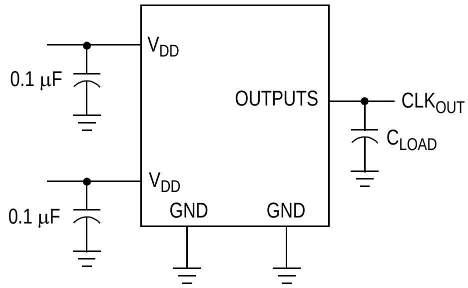


Figure 6. Output Transition Time Test Reference

Test Circuit #1



Test Circuit for all parameters

Ordering Information (Available)

Ordering Code	Package Name	Package Type
MPC962304D-1	D8	8-pin 150-mil SOIC
MPC962304D-1R2	D8	8-pin 150-mil SOIC — Tape and Reel
MPC962304D-2	D8	8-pin 150-mil SOIC
MPC962304D-2R2	D8	8-pin 150-mil SOIC — Tape and Reel