Combinatorial ECL PAL Device

PAL10H20P8

Features/Benefits

- 20 logic inputs: 12 external, 8 feedback
- 8 outputs with programmable polarity
- ECL technology for ultra-high speed—max t_{PD} = 6 ns
- 32 product terms with term sharing
- 10 KH ECL compatible
- Fully AC tested
- Input pull-down resistors
- Voltage compensated
- Space-saving 24-pin SKINNYDIP® and 28-pin PLCC packages
- Programmable using standard TTL programmers with adapter
- Greater than 99% programming yield
- Security fuse prevents unauthorized copying

Ordering Information

PAL10H20P8 NS STD

PROGRAMMABLE ARRAY LOGIC

ECL 10KH TECHNOLOGY

NUMBER OF ARRAY INPUTS

OUTPUT TYPE
P = Combinatorial with Programmable Polarity

PROCESSING
STD = Standard
XXXX = Other

PACKAGE
NS = Plastic SKINNYDIP
JS = Ceramic SKINNYDIP
FN = Plastic Leaded Chip Carrier
SG = Small-Outline Gull-wing

NUMBER OF OUTPUTS

Description

The PAL10H20P8 is a 10KH family compatible ECL PAL device having twelve dedicated inputs and eight outputs with feedback. A programmable AND array and a fixed OR array make possible the implementation of a wide variety of logic functions with far fewer packages than with SSI devices. The logic is implemented by opening metal fuse connections within the AND array. Designs can be specified by using any of a variety of software packages which accept the design and assemble a file that can be downloaded into a device programmer. The device can be programmed using any of the qualified PAL device programmers (refer to the Programmer Reference Guide).

The outputs are equipped with programmable polarity. They can drive a 50-Ω termination (to V_{CC}−2.0 V). Product term sharing is provided to allow greater flexibility in assigning product terms to outputs.

The input pins have 50-kΩ internal pull-down resistors, which allow unused inputs to be left open. Open inputs will assume a logic low state.
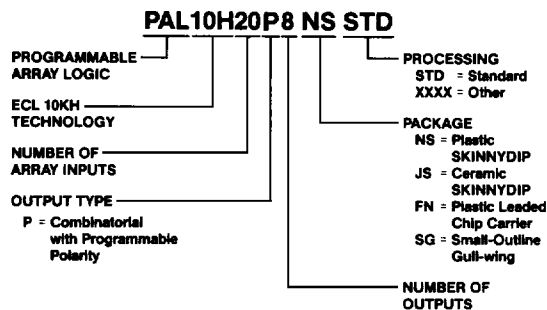
Features

Each output has a programmable polarity fuse, allowing for more efficient representation of many logic functions. Each output is active high with polarity fuse intact, and active low with the polarity fuse blown.

The programmable AND array contains a total of thirty-two product terms. Product terms are arranged in groups of eight. The terms in each group can be shared mutually exclusively between two adjacent output cells. If a particular product term is needed for two outputs, then two identical product terms are generated: one for each output.

A security fuse is provided to help protect the fuse pattern from unauthorized copying. Once the security fuse has been programmed, it is no longer possible to verify the contents of the fuse array electrically. The security fuse has no effect on functionality.

Packages

The PAL10H20P8 is available in the plastic SKINNYDIP (NS), ceramic SKINNYDIP (JS), and plastic leaded chip carrier (FN) packages. For drawings, refer to PAL Device Package Outlines.

Monolithic MMI Memories

Absolute Maximum Ratings

These ratings specify the conditions above which the device may be permanently damaged. AC and DC specifications are not necessarily guaranteed over this range.

Supply voltage V_{EE} ($V_{CC1} = V_{CC2} = V_{CC3} = 0$ V) .... -8.0 V to 0 V

Input voltage V_I ($V_{CC1} = V_{CC2} = V_{CC3} = 0$ V) .... 0 V to V_{EE}

Output current, I_{OUT}:

    Continuous .... 35 mA

    Surge .... 100 mA

Storage temperature range, T_{stg} .... $-65°$C to $150°$C

Operating Conditions

SYMBOL	PARAMETER	COMMERCIAL MIN TYP MAX			UNIT
V_{EE}	Supply voltage ($V_{CC} = 0$ V)	-5.46	-5.2	-4.94	V
T_A	Operating free-air temperature	0		75	$°$C

Electrical Characteristics V_{EE} = -5.2 V ±5% (See note 1)

SYMBOL	PARAMETER	TEST CONDITIONS	0°C MIN	0°C MAX	25°C MIN	25°C MAX	75°C MIN	75°C MAX	UNIT
I_{EE}	Power supply current	Inputs $V_{IN} = V_{IH}$ MAX	—	210	—	210	—	210	mA
I_{inH}	Input current high	V_{IH} MIN < V_{in} < V_{IH} MAX	—	425	—	265	—	265	μA
I_{inL}	Input current low	V_{IL} MIN < V_{in} < V_{IL} MAX	0.5	—	0.5	—	0.3	—	μA
V_{OH}	High output voltage	(See note 2)	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	V_{dc}
V_{OL}	Low output voltage	(See note 2)	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	V_{dc}
V_{IH}	High input voltage	(See note 2)	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	V_{dc}
V_{IL}	Low input voltage	(See note 2)	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	V_{dc}

Switching Characteristics V_{EE} = -5.2 V ±5% (See note 2)

SYMBOL	PARAMETER	0°C MIN	0°C MAX	25°C MIN	25°C MAX	75°C MIN	75°C MAX	UNIT
t_{PD}	Propagation delay	2.0	6.0	2.0	6.0	2.0	6.0	ns
t_R	Rise time (20%–80%)	0.7	2.2	0.7	2.0	0.7	2.2	ns
t_F	Fall time (80%-20%)	0.7	2.2	0.7	2.0	0.7	2.2	ns

Notes:

1. Each ECL 10KH series circuit has been designed to meet the specifications shown in test table after thermal equilibrium has been established. The circuit is in test socket or mounted on a printed board and transverse air flow greater than 500 linear fpm is maintained.

2. Outputs are terminated through a 50 Ω resistor to V_{CC} -2.0 V. Discrete carbon resistors should be used for terminations. Multiple-resistor packs and metal film discrete resistors are inductive and should be avoided. The single-ended nature of the outputs demands strict adherence to ground and termination plane design techniques

3. If pin 13 (PLCC pin 16) is not used, it should be left open or terminated to V_{TT} (= V_{CC} -2.0 V). It should not be terminated to V_{EE}.

Logic Diagram
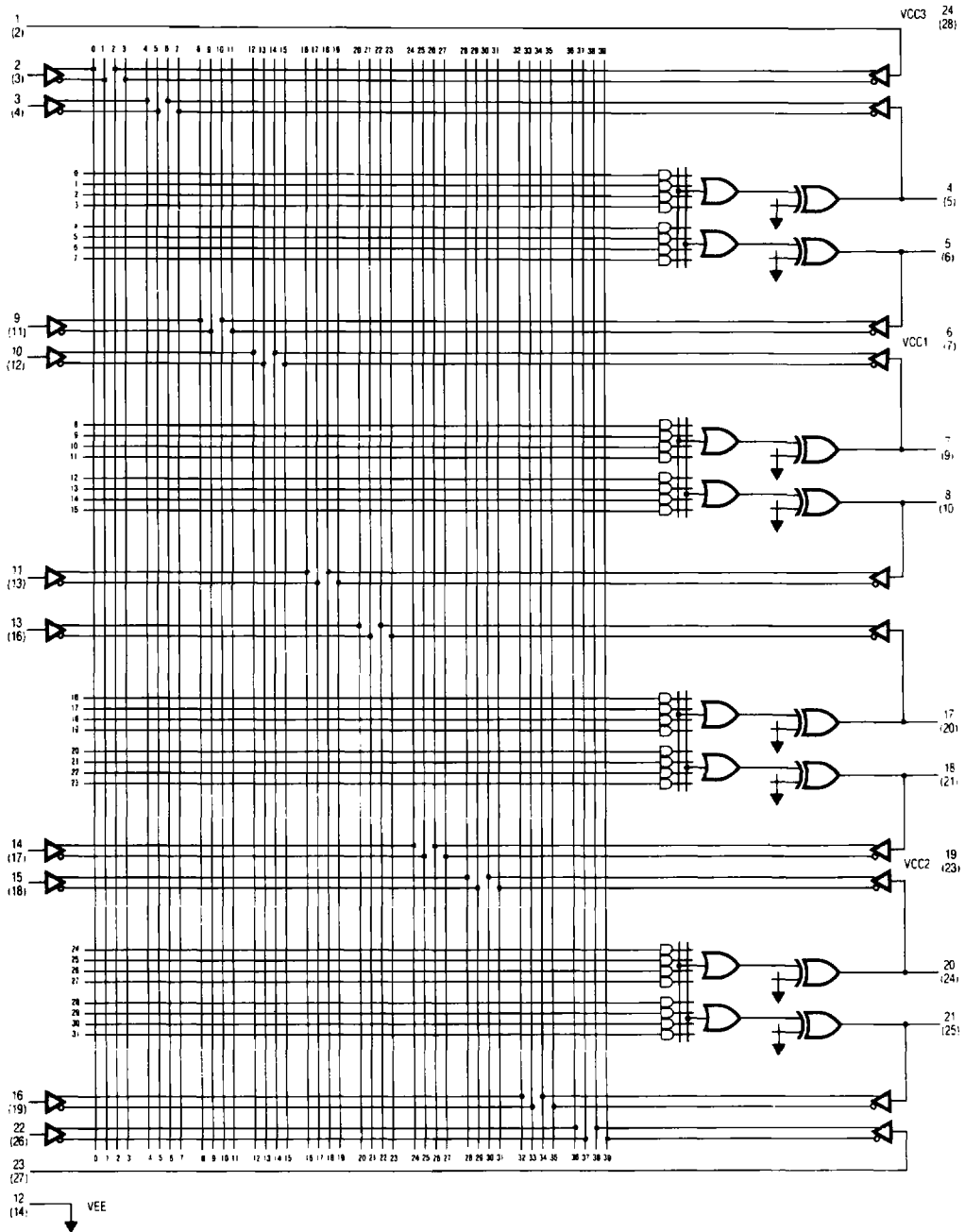
Note. Numbers in parentheses refer to the PLCC pin number.
PLCC pins 1, 8, 15, and 22 are not connected.