NEC

MOS INTEGRATED CIRCUIT

μPD78042F, 78043F, 78044F, 78045F

8-BIT SINGLE-CHIP MICROCONTROLLER

The μPD78042F, μPD78043F, μPD78044F, and μPD78045F are 8-bit single-chip microcontrollers that incorporate many hardware peripherals such as an FIP® controller/driver, 8-bit resolution A/D converter, timer, serial interface, and interrupt controller.

The one-time PROM and EPROM models that can operate in the same voltage range as that of masked ROM models, and various development tools are provided.

The functions of these microcontrollers are described in detail in the following User's Manual. Be sure to read this manual when you design a system using any of these microcontrollers.

μPD78044F Sub-Series User's Manual : U10906E

78K/0 Series User's Manual, Instruction: IEU-1372

FEATURES

- High-capacity ROM and RAM

Item / Product name	Program memory (ROM)	Data memory		
		Internal high-speed RAM	Buffer RAM	FIP display RAM
μPD78042F	16K bytes	512 bytes	64 bytes	48 bytes
μPD78043F	24K bytes			
μPD78044F	32K bytes	1024 bytes		
μPD78045F	40K bytes			

- Wide range of instruction execution time - from high-speed (0.4 μs) to ultra low-speed (122 μs)
- I/O ports: 68
- FIP controller/driver: total display outputs: 34
- 8-bit resolution A/D converter: 8 channels
- Serial interface: 2 channels
- Timer: 6 channels
- Power supply voltage: V_{DD} = 2.7 to 5.5 V ★

APPLICATIONS

CD players, cassete tape recorders, tuners, minicomponent stereos, VCRs, microwave ovens, ECRs, etc.

ORDERING INFORMATION

Part number	Package
μPD78042FGF-xxx-3B9	80-pin plastic QFP (14 × 20 mm)
μPD78043FGF-xxx-3B9	80-pin plastic QFP (14 × 20 mm)
μPD78044FGF-xxx-3B9	80-pin plastic QFP (14 × 20 mm)
μPD78045FGF-xxx-3B9	80-pin plastic QFP (14 × 20 mm)

Remark xxx indicates ROM code number.

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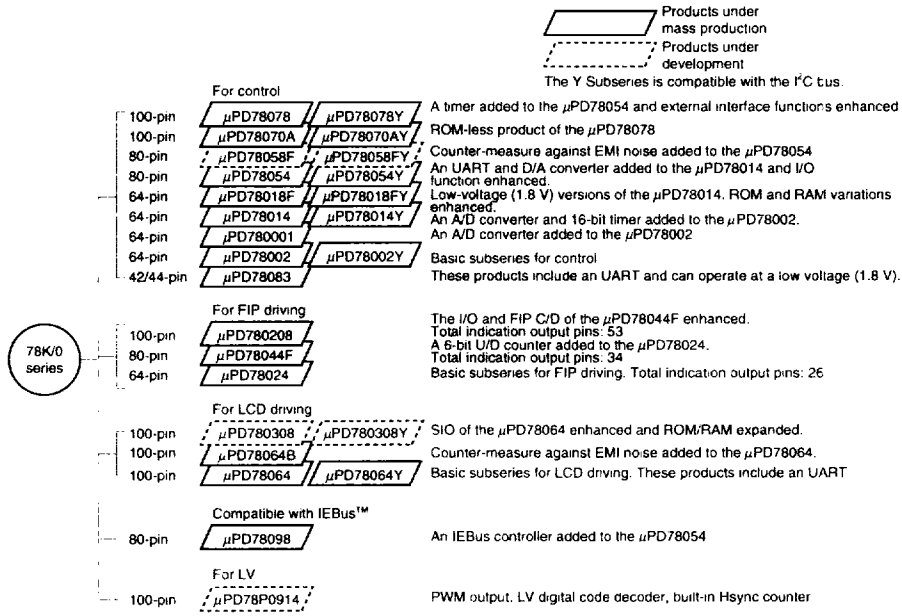
The mark ★ shows major revised points.

★ 78K/0 SERIES PRODUCT DEVELOPMENT

The 78K/0 series products were developed as shown below. The sub-series names are indicated in frames.



The table below shows the main differences between subseries.

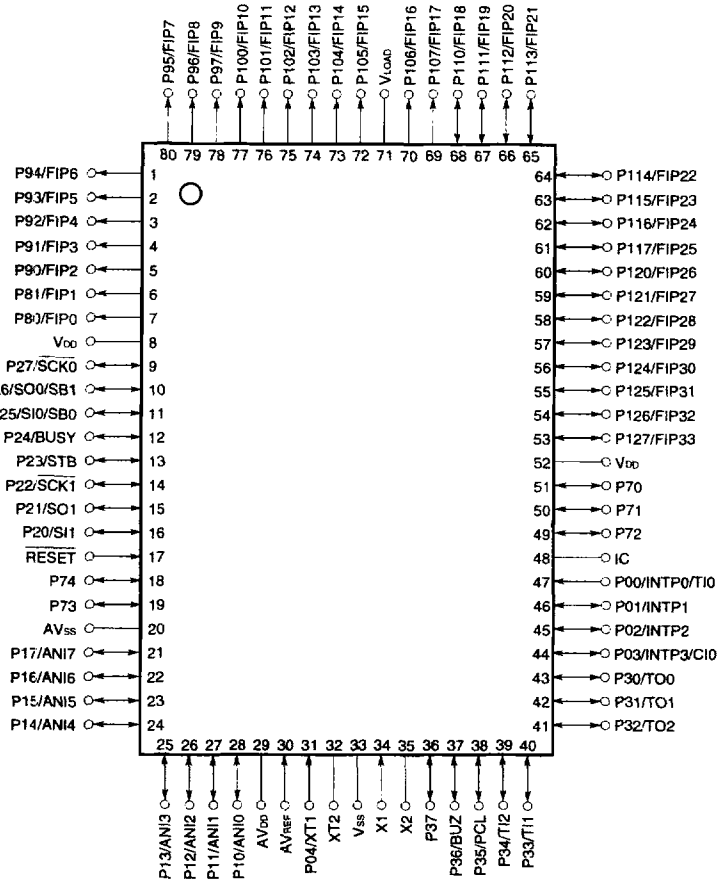
Subseries name \ Function		ROM capacity	Timer				8-bit A/D	8-bit D/A	Serial interface	I/O	V_{DD} Min. value	External expansion	
			8-bit	16-bit	Watch	WDT							
For control	μPD78078	32K-60K	4ch	1ch	1ch	1ch	8ch	2ch	3ch (UART : 1ch)	88 pins	1.8 V	○	
	μPD78070A	–								61 pins	2.7 V		
	μPD78058F	48K-60K	2ch							69 pins			★
	μPD78054	16K-60K									2.0 V		
	μPD78018F	8K-60K						–	2ch	53 pins	1.8 V		
	μPD78014	8K-32K									2.7 V		
	μPD780001	8K		–	–				1ch	39 pins		–	
	μPD78002	8K-16K			1ch		–			53 pins		○	
	μPD78083	8K-16K			–		8ch		1ch (UART : 1ch)	33 pins	1.8 V	–	
For FIP driving	μPD780208	32K-60K	2ch	1ch	1ch	1ch	8ch	–	2ch	74 pins	2.7 V	–	
	μPD78044F	16K-40K								68 pins			
	μPD78024	24K-32K								54 pins			
For LCD driving	μPD780308	48K-60K	2ch	1ch	1ch	1ch	8ch	–	3ch (UART : 1ch)	57 pins	1.8 V	–	★
	μPD78064B	32K							2ch (UART : 1ch)		2.0 V		
	μPD78064	16K-32K											
Compatible with IEBus	μPD78098	32K-60K	2ch	1ch	1ch	1ch	8ch	2ch	3ch (UART : 1ch)	69 pins	2.7 V	○	
For LV	μPD78P0914	32K	6ch	–	–	1ch	8ch	–	2ch	54 pins	4.5 V	○	★

FUNCTIONAL OUTLINE

Item \ Product name		μPD78042F	μPD78043F	μPD78044F	μPD78045F
Internal memory	ROM	16K bytes	24K bytes	32K bytes	40K bytes
	Internal high-speed RAM	512 bytes		1024 bytes	
	Buffer RAM	64 bytes			
	FIP display RAM	48 bytes			
General registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)			
Instruction cycle		Variable instruction execution time			
	For main system clock	0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs (at 5.0 MHz)			
	For subsystem clock	122 μs (at 32.768 kHz)			
Instruction set		• Multiplication/division (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit (set. reset, test, Boolean algebra)			
I/O ports (including those multiplexed with FIP pins)		Total : 68 lines • CMOS input : 2 lines • CMOS I/O : 27 lines • N-ch open-drain : 5 lines • P-ch open-drain I/O : 16 lines • P-ch open-drain output : 18 lines			
FIP controller/driver		Total : 34 lines • Segments : 9 to 24 lines • Digits : 2 to 16 lines			
★ A/D converter		• 8-bit resolution × 8 channels • Power supply voltage: AV_{DD} = 4.0 to 5.5 V			
Serial interface		• 3-wire serial I/O/SBI/2-wire serial I/O selectable modes: 1 channel • 3-wire serial I/O mode (with automatic transmission/reception function of up to 64 bytes) : 1 channel			
Timer		• 16-bit timer/event counter : 1 channel • 8-bit timer/event counter : 2 channels • Watch timer : 1 channel • Watchdog timer : 1 channel • 6 bit up/down counter : 1 channel			
Timer output		3 lines (one for 14-bit PWM output)			
Clock output		19.5 kHz, 39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz (Main system clock: at 5.0 MHz) 32.768 kHz (Subsystem clock: at 32.768 kHz)			
Buzzer output		1.2 kHz, 2.4 kHz, 4.9 kHz (Main system clock: at 5.0 MHz)			
Vectored interrupt	Maskable interrupt	Internal 10 lines, external 4 lines			
	Non-maskable interrupt	Internal 1 line			
	Software interrupt	1 line			
Text input		Internal 1 line			
★ Power supply voltage		V_{DD} = 2.7 to 5.5 V			
Package		80-pin plastic QFP (14 × 20 mm)			

1. PIN CONFIGURATION (TOP VIEW)

- 80-pin plastic QFP (14 x 20 mm)
  μPD78042FGF-xxx-3B9, μPD78043FGF-xxx-3B9
  μPD78044FGF-xxx-3B9, μPD78045FGF-xxx-3B9



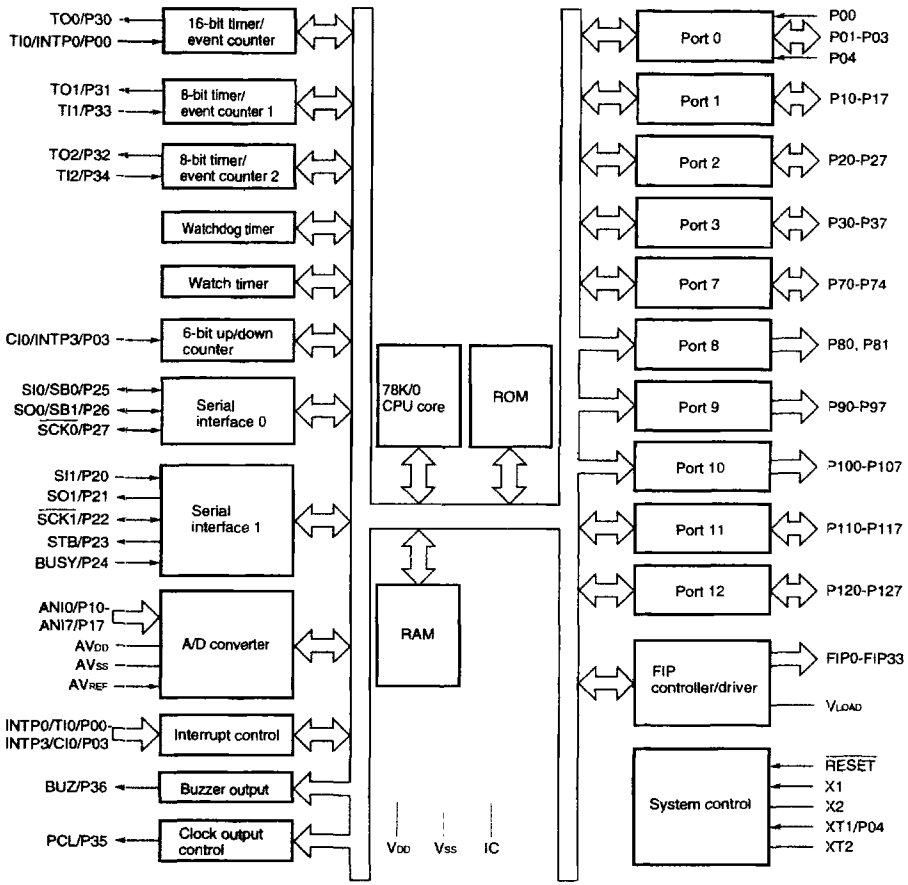
Cautions 1. Connect the IC (Internally Connected) pins directly to the V_{SS}.

2. Connect the AV_{DD} pin to the V_{DD} pin.

3. Connect the AVss pin to the Vss pin.

P00-P04	:	Port 0
P10-P17	:	Port 1
P20-P27	:	Port 2
P30-P37	:	Port 3
P70-P74	:	Port 7
P80, P81	:	Port 8
P90-P97	:	Port 9
P100-P107	:	Port 10
P110-P117	:	Port 11
P120-P127	:	Port 12
INTP0-INTP3	:	Interrupt from peripherals
TI0-TI2	:	Timer input
TO0-TO2	:	Timer output
CIC	:	Counter input
SB0, SB1	:	Serial bus
SI0, SI1	:	Serial input
SO0, SO1	:	Serial output
$\overline{SCK0}$, $\overline{SCK1}$	:	Serial clock
PCL	:	Programmable clock
BUZ	:	Buzzer clock
STB	:	Strobe
BUSY	:	Busy
FIP0-FIP33	:	Fluorescent indicator panel
V_{LOAD}	:	Negative power supply
X1, X2	:	Crystal (main system clock)
XT1, XT2	:	Crystal (subsystem clock)
$\overline{RESET}$	:	Reset
ANI0-ANI7	:	Analog input
AV_{DD}	:	Analog power supply
AV_{SS}	:	Analog ground
AV_{REF}	:	Analog reference voltage
V_{DD}	:	Power supply
V_{SS}	:	Ground
IC	:	Internally connected

2. BLOCK DIAGRAM



Remark The capacities of the internal ROM and RAM differ depending on the product.

3. PINS FUNCTIONS

3.1 PORT PINS (1/2)

Pin name	I/O	Function		On reset	Shared by:
P00	Input	Port 0	Input only	Input	INTP0/TI0
P01	I/O	5-bit I/O port	Can be specified for input or output in 1-bit units. When used as an input port pin, a built-in pull-up resistor can be used by software.	Input	INTP1
P02					INTP2
P03					INTP3/CI0
P04[Note 1]	Input		Input only	Input	XT1
P10-P17	I/O	Port 1 8-bit I/O port Can be specified for input or output in 1-bit units. When used as an input port pin, a built-in pull-up resistor can be used by software.[Note 2]		Input	ANI0-ANI7
P20	I/O	Port 2 8-bit I/O port Can be specified for input or output in 1-bit units. When used as an input port pin, a built-in pull-up resistor can be used by software.		Input	SI1
P21					SO1
P22					$\overline{SCK1}$
P23					STB
P24					BUSY
P25					SI0/SB0
P26					SO0/SB1
P27					$\overline{SCK0}$
P30	I/O	Port 3 8-bit I/O port Can be specified for input or output in 1-bit units. Can directly drive LEDs. When used as an input port pin, a built-in pull-up resistor can be used by software. A pull-down resistor can be connected in 1-bit units by the mask option.		Input	TO0
P31					TO1
P32					TO2
P33					TI1
P34					TI2
P35					PCL
P36					BUZ
P37					—

Notes 1. When the P04/XT1 pins is used as an input port pin, bit 6 (FRC) of the processor clock control register (PCC) must be set to 1. At this time, do not use the feedback resistor of the subsystem clock oscillator circuit.

2. When the P10/ANI0 through P17/ANI7 pins are used as the analog input lines of the A/D converter, be sure to place the port 1 in the input mode. In this case, the built-in pull-up resistors are automatically unused.

3.1 PORT PINS (2/2)

Pin name	I/O	Function	On reset	Shared by:
P70-P74	I/O	Port 7 5-bit N-ch open-drain I/O port Can be specified for input or output in 1-bit units. Can directly drive LEDs. A pull-up resistor can be connected in 1-bit units by the mask option.	Input	—
P80, P81	Output	Port 8 2-bit P-ch open-drain high-voltage output port. Can directly drive LEDs. A pull-down resistor can be connected in 1-bit units by the mask option (whether V_{LOAD} or V_{SS} is connected can be specified in bit units).	Output	FIP0, FIP1
P90-P97	Output	Port 9 8-bit P-ch open-drain high-voltage output port. Can directly drive LEDs. A pull-down resistor can be connected in 1-bit units by the mask option (whether V_{LOAD} or V_{SS} is connected can be specified in 4-bit units).	Output	FIP2-FIP9
P100-P107	Output	Port 10 8-bit P-ch open-drain high-voltage output port. Can directly drive LEDs. A pull-down resistor can be connected in 1-bit units by the mask option (whether V_{LOAD} or V_{SS} is connected can be specified in 4-bit units).	Output	FIP10-FIP17
P110-P117	I/O	Port 11 8-bit P-ch open-drain high-voltage I/O port. Can be specified for input or output in 1-bit units. Can directly drive LEDs. A pull-down resistor can be connected in 1-bit units by the mask option (whether V_{LOAD} or V_{SS} is connected can be specified in 4-bit units).	Input	FIP18-FIP25
P120-P127	I/O	Port 12 8-bit P-ch open-drain high-voltage I/O port Can be specified for input or output in 1-bit units. Can directly drive LEDs. A pull-down resistor can be connected in 1-bit units by the mask option (whether V_{LOAD} or V_{SS} is connected can be specified in 4-bit units).	Input	FIP26-FIP33

3.2 PINS OTHER THAN PORT PINS (1/2)

Pin name	I/O	Function	On reset	Shared by:
INTP0	Input	Valid edge (rising, falling, or both rising and falling edges) can	Input	P00/TI0
INTP1		be specified.		P01
INTP2		External interrupt input		P02
INTP3		Falling edge-active external interrupt input	Input	P03/CI0
SI0	Input	Serial data input lines of serial interface	Input	P25/SB0
SI1				P20
SO0	Output	Serial data output lines of serial interface	Input	P26/SB1
SO1				P21
SB0	I/O	Serial data I/O lines of serial interface	Input	P25/SI0
SB1				P26/SO0
$\overline{SCK0}$	I/O	Serial clock I/O lines of serial interface	Input	P27
$\overline{SCK1}$				P22
STB	Output	Automatic transmission/reception strobe output line of serial interface	Input	P23
BUSY	Input	Automatic transmission/reception busy input line of serial interface	Input	P24
TI0	Input	External count clock input to 16-bit timer (TM0)	Input	P00/INTP0
TI1		External count clock input to 8-bit timer (TM1)		P33
TI2		External count clock input to 8-bit timer (TM2)		P34
TO0	Output	16-bit timer output (multiplexed with 14-bit PWM output)	Input	P30
TO1		8-bit timer output		P31
TO2				P32
CI0	Input	Clock input to 6-bit up/down counter	Input	P03/INTP3
PCL	Output	Clock output (for trimming main system clock and subsystem clock)	Input	P35
BUZ	Output	Buzzer output	Input	P36
FIP0, FIP1	Output	High-voltage, high-current digit/segment output of FIP	Output	P80, P81
FIP2-FIP9		controller/driver		P90-P97
FIP10-FIP15	Output	High-voltage, high-current digit/segment output of FIP controller/driver	Output	P100-P105
FIP16, FIP17	Output	High-voltage segment output of FIP controller/driver	Output	P106, P107
FIP18-FIP25			Input	P110-P117
FIP26-FIP33				P120-P127
V_{LOAD}	—	Connects pull-down resistor to FIP controller/driver	—	—

3.2 PINS OTHER THAN PORT PINS (2/2)

Pin name	I/O	Function	On reset	Shared by:
ANI0-ANI7	Input	A/D converter analog input lines	Input	P10-P17
AV_{REF}	Input	A/D converter reference voltage input line	—	—
AV_{DD}	—	Analog power supply to A/D converter. Connected to the V_{DD} pin.	—	—
AV_{SS}	—	A/D converter ground line. Connected to the V_{SS} pin.	—	—
$\overline{RESET}$	Input	System reset input	—	—
X1	Input	Connect crystal for main system clock oscillation	—	—
X2	—		—	—
XT1	Input	Connect crystal for subsystem clock oscillation	Input	P04
XT2	—		—	—
V_{DD}	—	Positive power supply	—	—
V_{SS}	—	Ground potential	—	—
IC	—	Internal connection. Connected directly to the V_{SS} pin.	—	—

3.3 PIN I/O CIRCUITS AND PROCESSING OF UNUSED PINS

Table 3-1 shows the I/O circuit type of each pin and the processing of unused pins.

For the configuration of the I/O circuit of each type, refer to Fig. 3-1.

Table 3-1 I/O Circuit Type

Pin name	I/O Circuit type	I/O	Recommended connections when unused
P00/INTP0/TI0	2	Input	Connected to V_{SS}.
P01/INTP1	8-A	I/O	Individually connected to V_{SS} with a resistor.
P02/INTP2			
P03/INTP3/CI0			
P04/XT1	16	Input	Connected to V_{DD} or V_{SS}.
P10/ANI0-P17/ANI7	11	I/O	Individually connected to V_{DD} or V_{SS} with a resistor.
P20/SI1	8-A		
P21/SO1	5-A		
P22/$\overline{SCK1}$	8-A		
P23/STB	5-A		
P24/BUSY	8-A		
P25/SI0/SB0	10-A		
P26/SO0/SB1			
P27/$\overline{SCK0}$			
P30/TO0	5-C		
P31/TO1			
P32/TO2			
P33/TI1	8-B		
P34/TI2			
P35/PCL	5-C		
P36/BUZ			
P37			
P70-P74	13-B		
P80/FIP0, P81/FIP1	14-A	Output	Open
P90/FIP2-P97/FIP9			
P100/FIP10-P107/FIP17			
P110/FIP18-P117/FIP25	15-C	I/O	Individually connected to V_{DD} or V_{SS} with a resistor.
P120/FIP26-P127/FIP33			
$\overline{RESET}$	2	Input	—
XT2	16	—	Open
AV_{REF}	—		Connected to V_{SS}.
AV_{DD}			Connected to V_{DD}.
AV_{SS}			Connected to V_{SS}.
V_{LOAD}			
IC			Connected directly to V_{SS}.

Fig. 3-1 Pin I/O Circuits (1/2)

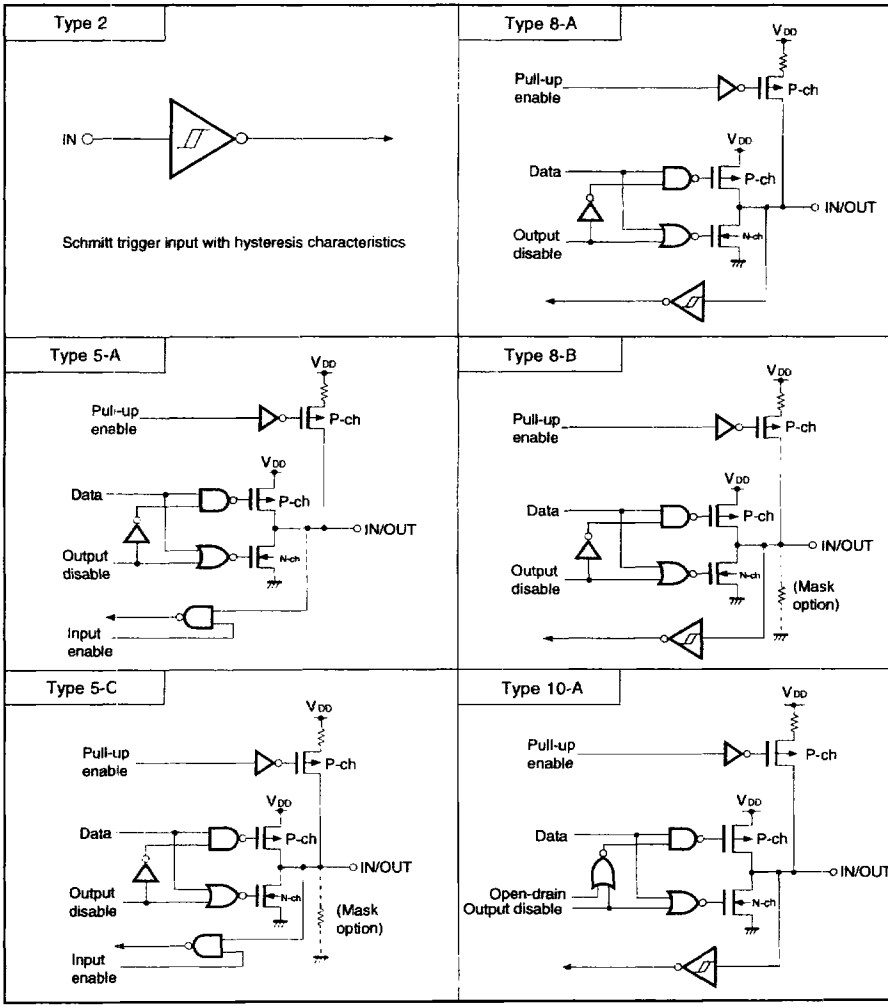
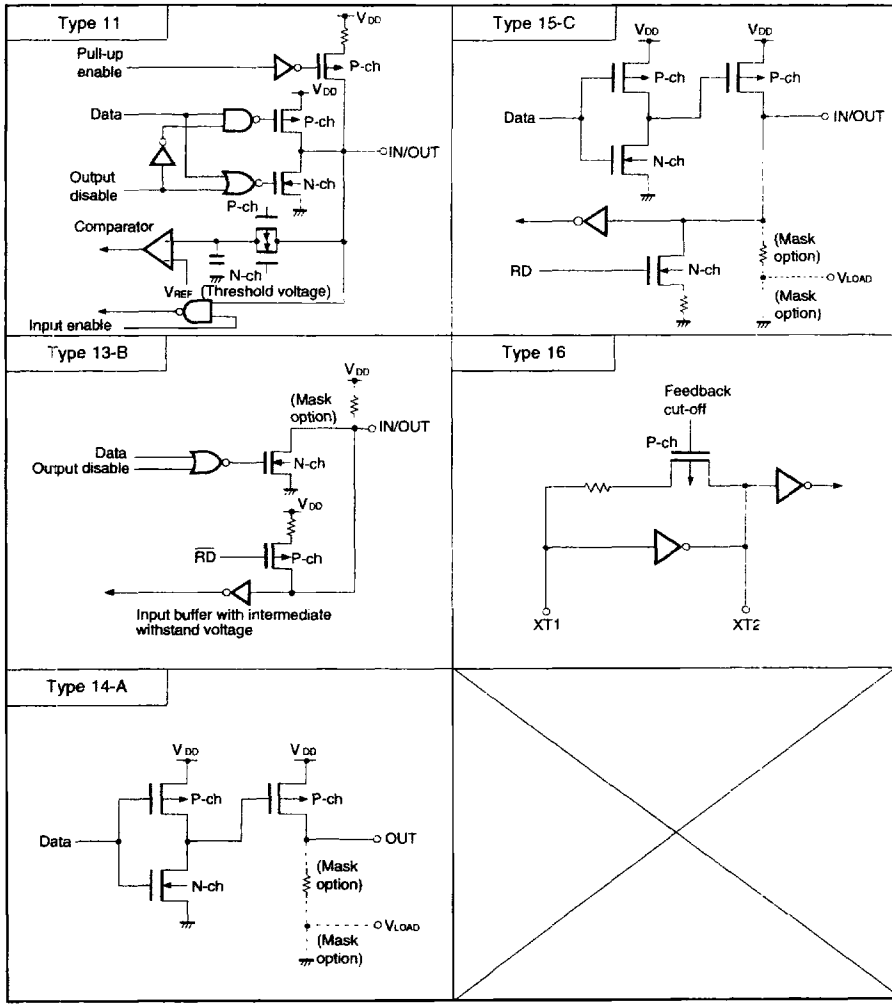


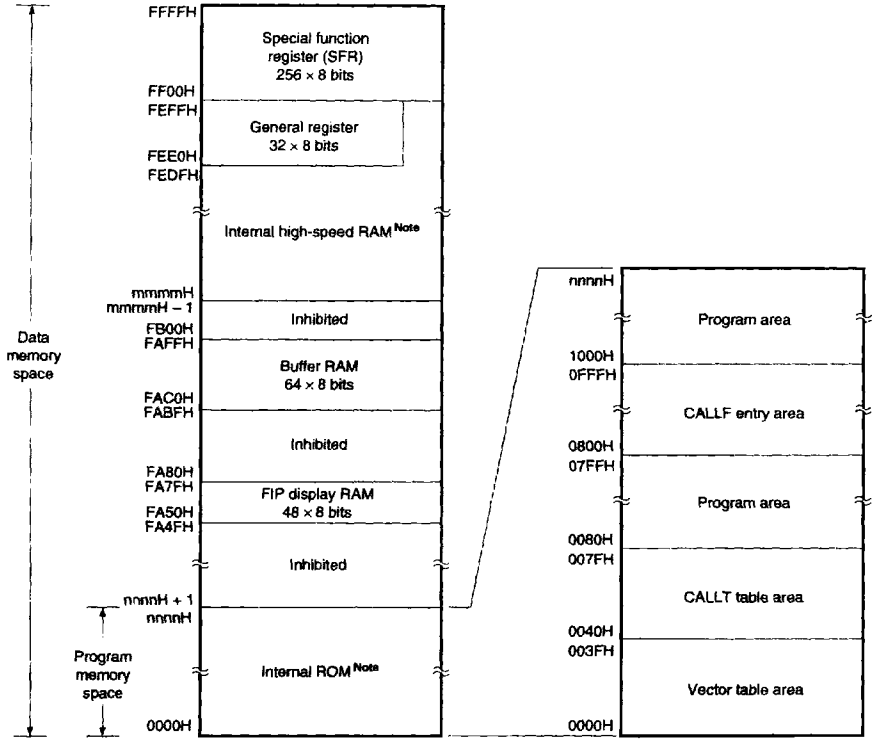
Fig. 3-1 Pin I/O Circuits (2/2)



4. MEMORY SPACE

Fig. 4-1 shows the memory map for μPD78042F, μPD78043F, μPD78044F, and μPD78045F.

Fig. 4-1 Memory Map



Note The internal ROM and internal high-speed RAM capacities vary depending on the product. (See the table below.)

Product name	Last Address of Internal ROM nnnnH	First address of internal high-speed RAM mmmmH
μPD78042F	3FFFH	FD00H
μPD78043F	5FFFH	
μPD78044F	7FFFH	FB00H
μPD78045F	9FFFH	

5. PERIPHERAL HARDWARE FUNCTIONS

5.1 PORTS

I/O ports are classified into the following five types:

- CMOS input (P00, P04) : 2
- CMOS input/output (P01 - P03, ports 1 - 3) : 27
- N-ch open-drain input/output (port 7) : 5
- P-ch open-drain output (ports 8 - 10) : 18
- P-ch open-drain input/output (ports 11 and 12) : 16

Total : 68

Table 5-1 Port Function

Product	Pin	Function
Port 0	P00, P04	Input-only port
	P01-P03	I/O port. Can be specified for input or output in 1-bit units. When used as input port, internal pull-up resistor can be connected through software.
Port 1	P10-P17	I/O port. Can be specified for input or output in 1-bit units. When used as input port, internal pull-up resistor can be connected through software.
Port 2	P20-P27	I/O port. Can be specified for input or output in 1-bit units. When used as input port, internal pull-up resistor can be connected through software.
Port 3	P30-P37	I/O port. Can be specified for input or output in 1-bit units. When used as input port, internal pull-up resistor can be connected through software. Pull-down resistor can be connected in 1-bit units by the mask option. Can directly drive LED.
Port 7	P70-P74	N-ch open-drain I/O port. Can be specified for input or output in 1-bit units. Pull-up resistor can be connected in 1-bit units by the mask option. Can directly drive LED.
Port 8	P80, P81	P-ch open-drain output port with high withstand voltage. Pull-down resistor can be connected in 2-bit units by the mask option (connection to V_{LOAD} or V_{SS} can be specified in 2-bit units). Can directly drive LED.
Port 9	P90-P97	P-ch open-drain output port with high withstand voltage. Pull-down resistor can be connected in 1-bit units by the mask option (connection to V_{LOAD} or V_{SS} can be specified in 4-bit units). Can directly drive LED.
Port 10	P100-P107	P-ch open-drain output port with high withstand voltage. Pull-down resistor can be connected in 1-bit units by the mask option (connection to V_{LOAD} or V_{SS} can be specified in 4-bit units). Can directly drive LED.
Port 11	P110-P117	P-ch open-drain I/O port with high withstand voltage. Can be specified for input or output in 1-bit units. Pull-down resistor can be connected in 1-bit units by the mask option (connection to V_{LOAD} or V_{SS} can be specified in 4-bit units). Can directly drive LED.
Port 12	P120-P127	P-ch open-drain I/O port with high withstand voltage. Can be specified for input or output in 1-bit units. Pull-down resistor can be connected in 1-bit units by the mask option (connection to V_{LOAD} or V_{SS} can be specified in 4-bit units). Can directly drive LED.

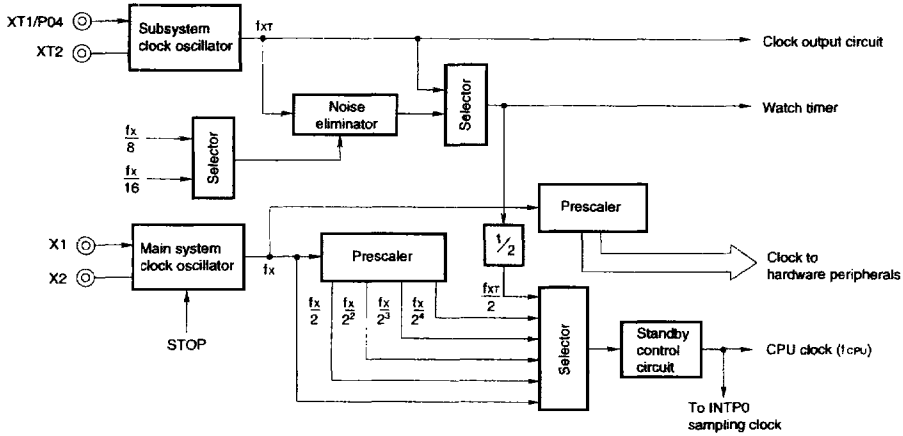
5.2 CLOCK GENERATOR CIRCUIT

The clock generator circuit has two kinds of generator circuits: the main system clock and subsystem clock.

The instruction time can be changed.

- 0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs (with main system clock: 5.0 MHz)
- 122 μs (with subsystem clock: 32.768 kHz)

Fig. 5-1 Clock Generator Circuit Block Diagram



5.3 TIMER/EVENT COUNTER

Six channels of timer/event counters are provided.

- 16-bit timer/event counter : 1 channel
- 8-bit timer/event counter : 2 channels
- Watch timer : 1 channel
- Watchdog timer : 1 channel
- 6-bit up/down counter : 1 channel

Table 5-2 Timer/Event Counter Groups and Configurations

		16-bit timer/ event counter	8-bit timer/ event counter	Watch timer	Watchdog timer	6-bit up/ down counter
Group	Interval timer	1 channel	2 channels	1 channel	1 channel	—
	External event counter	1 channel	2 channels	—	—	1 channel
Function	Timer output	1 output	2 outputs	—	—	—
	PWM output	1 output	—	—	—	—
	Pulse width measurement	1 input	—	—	—	—
	Square wave output	1 output	2 outputs	—	—	—
	Interrupt Request	1	2	1	1	1
	Test input	—	—	1 input	—	—

Fig. 5-2 16-Bit Timer/Event Counter Block Diagram

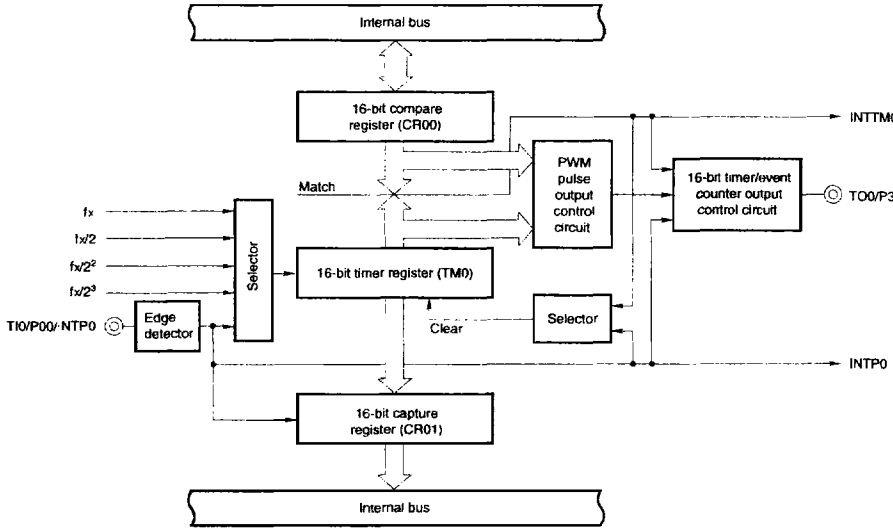


Fig. 5-3 8-Bit Timer/Event Counter Block Diagram

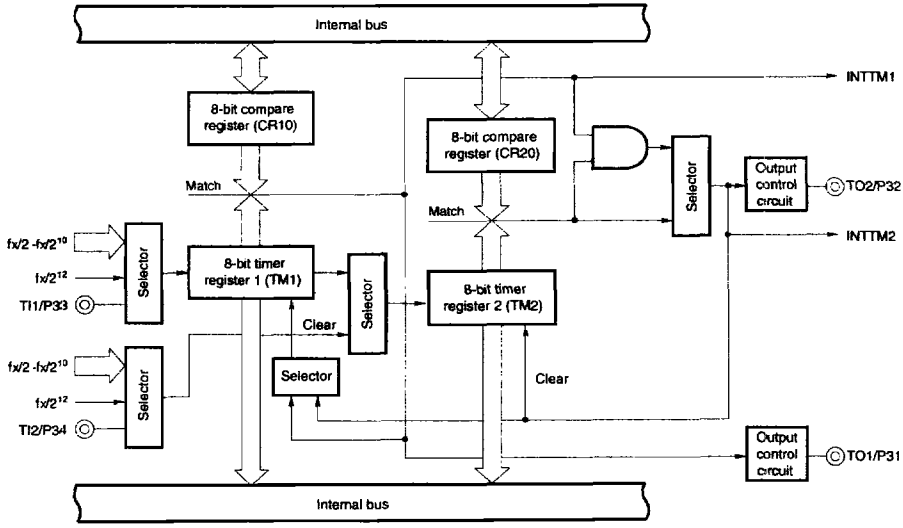


Fig. 5-4 Watch Timer Block Diagram

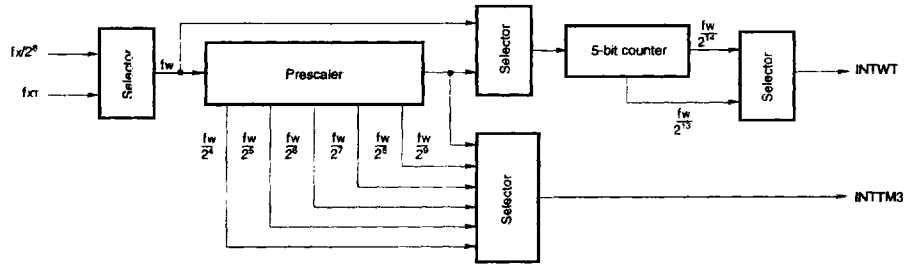


Fig. 5-5 Watchdog Timer Block Diagram

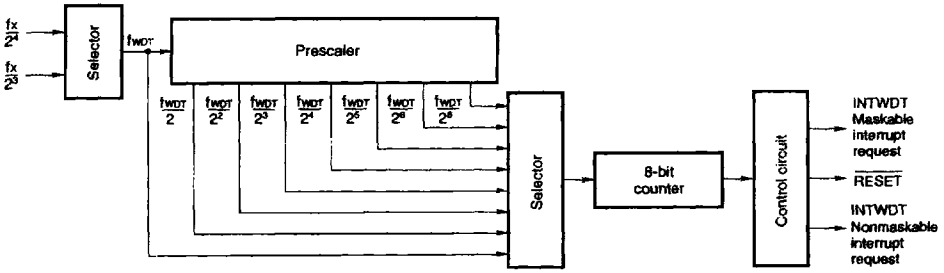
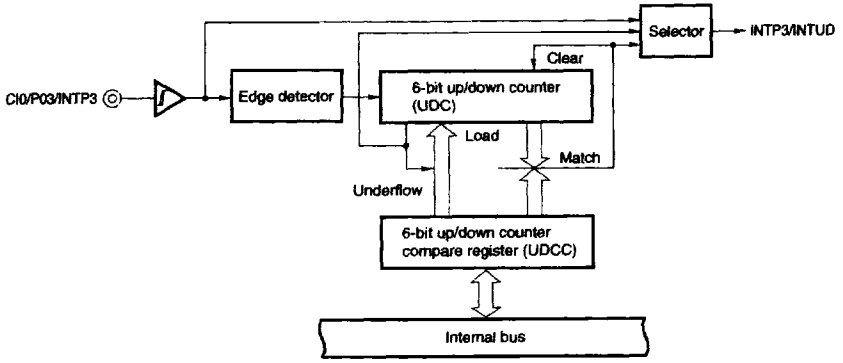


Fig. 5-6 6-Bit Up/Down Counter Block Diagram



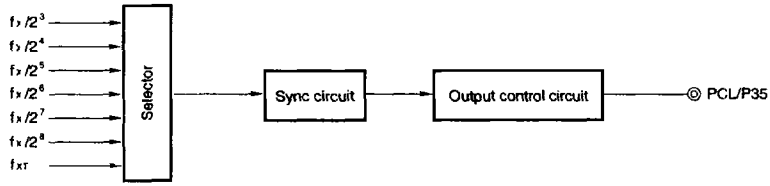
Caution When using the 6-bit up/down counter, set the CI0/P03/INTP3 pin in the input mode (set bit 3 of port mode register 0 (PM03) to 1).

5.4 CLOCK OUTPUT CONTROL CIRCUIT

Clocks of the following frequencies can be output to the clock:

- 19.5 kHz/39.1 kHz/78.1 kHz/156 kHz/313 kHz/625 kHz (with main system clock: 5.0 MHz)
- 32.768 kHz (with subsystem clock: 32.768 kHz)

Fig. 5-7 Clock Output Control Circuit Block Diagram

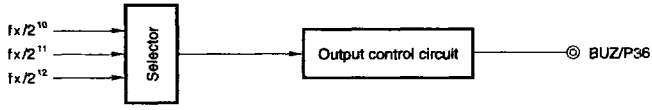


5.5 BUZZER OUTPUT CONTROL CIRCUIT

Clocks of the following frequencies can be output to the buzzer:

- 1.2 kHz/2.4 kHz/4.9 kHz (with main system clock: 5.0 MHz)

Fig. 5-8 Buzzer Output Control Circuit Block Diagram



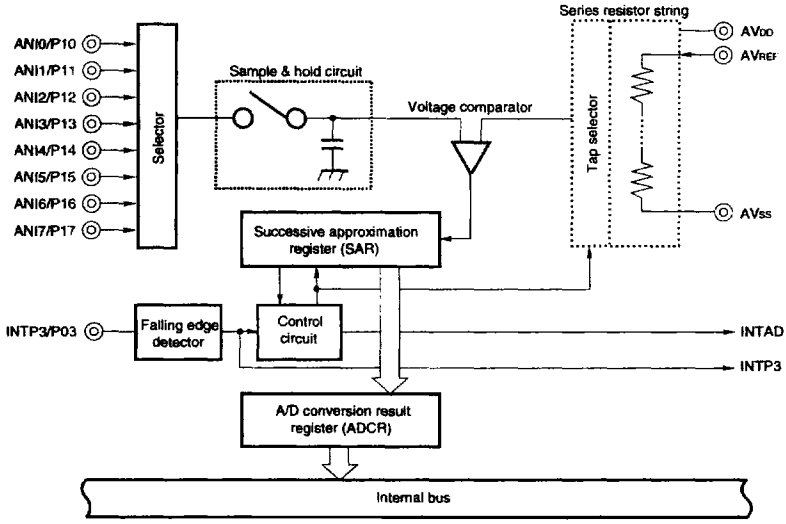
5.6 A/D CONVERTER

An 8-bit resolution 8-channel A/D converter is provided.

This A/D converter can be started in the following two modes:

- Hardware start
- Software start

Fig. 5-9 A/D Converter Block Diagram



5.7 SERIAL INTERFACE

Two channels of clocked serial interfaces are provided.

- Serial interface channel 0
- Serial interface channel 1

Table 5-3 Serial Interface Groups and Functions

Function	Serial interface channel 0	Serial interface channel 1
3-wire serial I/O mode	• (MSB/LSB first selectable)	• (MSB/LSB first selectable)
SBI (serial bus interface) mode	• (MSB first)	—
2-wire serial I/O mode	• (MSB first)	—
3-wire serial I/O mode with automatic transmission/ reception function	—	• (MSB/LSB first selectable)

Fig. 5-10 Serial Interface Channel 0 Block Diagram

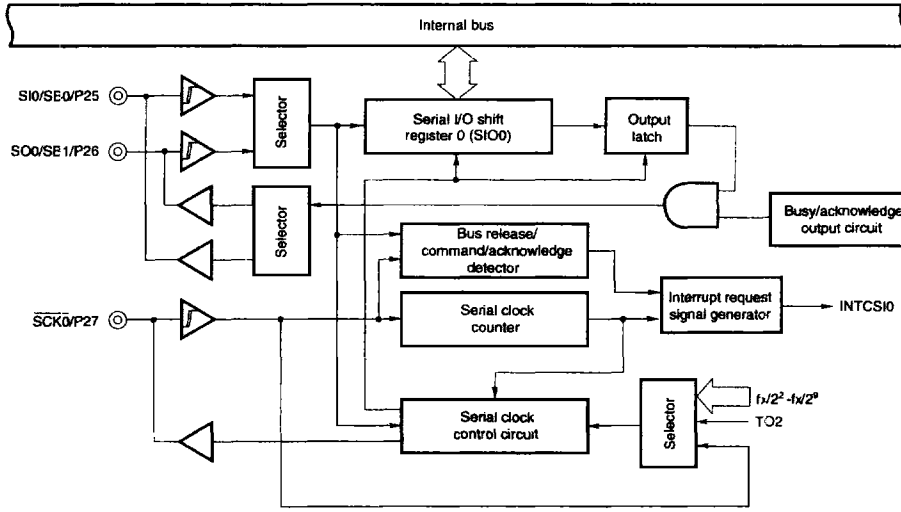
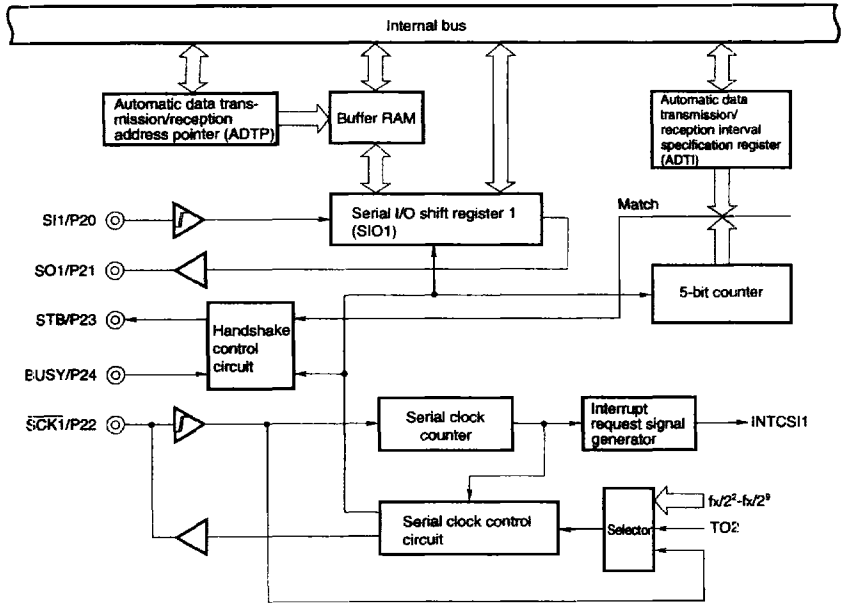


Fig. 5-11 Serial Interface Channel 1 Block Diagram

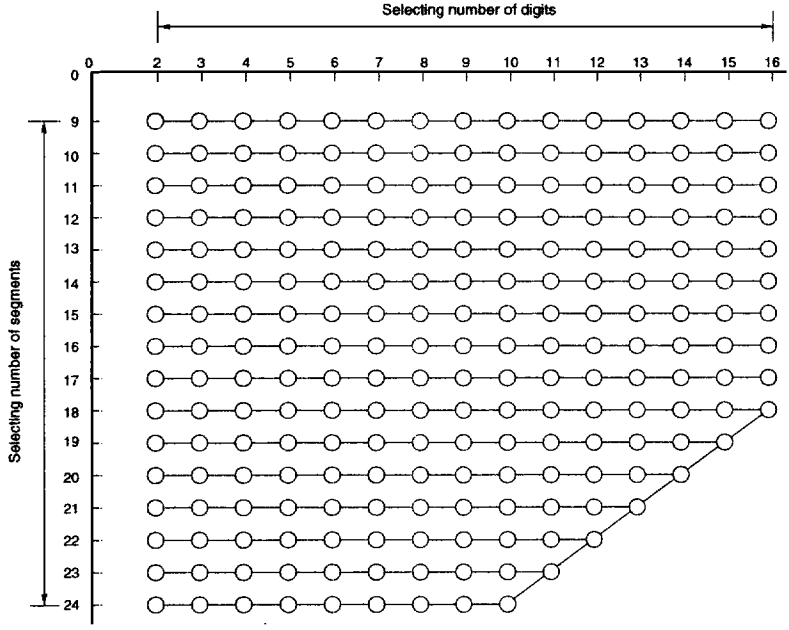


5.8 FIP CONTROLLER/DRIVER

An FIP controller/driver having the following features is provided:

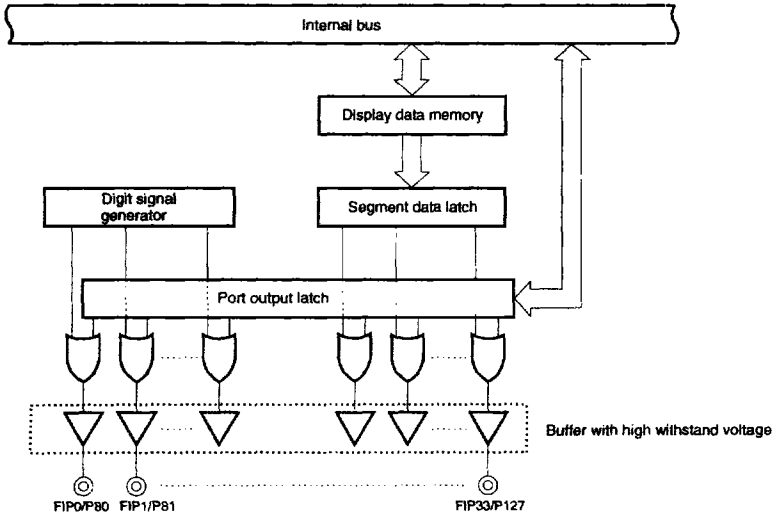
(a) Automatic output of segment signals (DMA operation) and digit signals by automatically reading display data
(b) Display mode registers (DSPM0 and DSPM1) that can control an FIP of 9 to 24 segments and 2 to 16 digits
(c) Port pins not used for FIP display can be used as output port or I/O port pins.
(d) Display mode register (DSPM1) can adjust luminance in eight steps.
(e) Hardware suitable for key scan application using segment pins
(f) High-voltage output buffer (FIP driver) that can directly drive an FIP
(g) Display output pins can be connected to a pull-down resistor by the mask option.

Fig. 5-12 Selecting Display Modes



Caution If the total number of digits and segments exceeds 34, the specified number of digits takes precedence.

Fig. 5-13 FIP Controller/Driver Block Diagram



6. INTERRUPT FUNCTION AND TEST FUNCTION

6.1 INTERRUPT FUNCTION

The following three types of interrupt functions are available:

- *Non-maskable interrupt* : 1
- Maskable interrupt : 13
- Software interrupt : 1

Table 6-1 Interrupt Source List

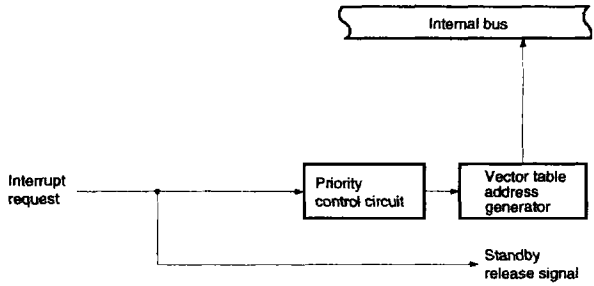
Interrupt type	Note 1 Default priority	Interrupt source		Internal/ external	Vector table address	Note 2 Basic configuration type
		Name	*Trigger*			
Non-maskable	—	INTWDT	Watchdog timer overflow (with watchdog timer mode 1 selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Watchdog timer overflow (with interval timer mode selected)			(B)
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTP1			0008H	(D)
	3	INTP2			000AH	
	4	INTP3			000CH	
		INTUD	6-bit up/down counter match signal generation	Internal		(B)
	5	INTCSI0	End of serial interface channel 0 transfer		000EH	
	6	INTCSI1	End of serial interface channel 1 transfer		0010H	
	7	INTTM3	Reference time interval signal from watch timer		0012H	
	8	INTTM0	16-bit timer/event counter match signal generation		0014H	
	9	INTTM1	8-bit timer/event counter 1 match signal generation		0016H	
	10	INTTM2	8-bit timer/event counter 2 match signal generation		0018H	
	11	INTAD	End of A/D converter conversion		001AH	
	12	INTKS	Key scan timing from FIP controller/driver		001CH	
Software	—	BRK	Execution of BRK instruction	—	003EH	(E)

Notes 1. *Default priority is the priority order when several maskable interrupts are generated at the same time.* 0 is the highest order and the 12 is the lowest order.

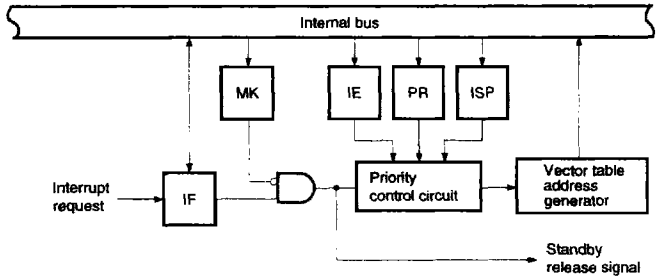
2. Basic configuration types (A) to (E) correspond to (A) to (E) in Fig. 6-1.

Fig. 6-1 Basic Configuration of Interrupt Function (1/2)

(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt (INTP0)

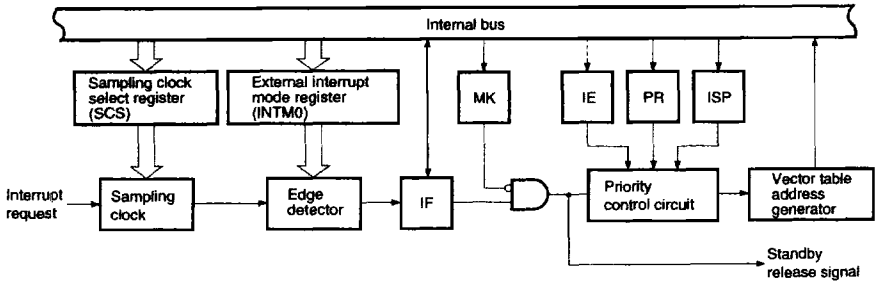
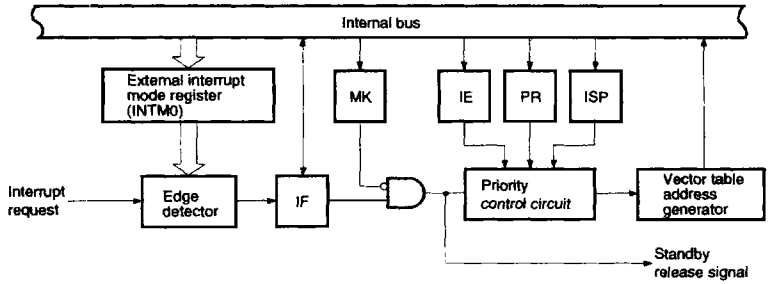
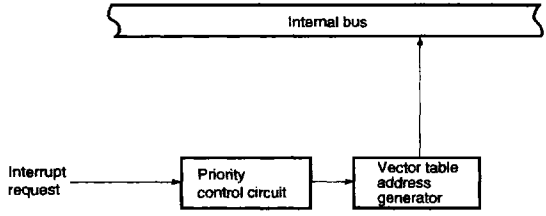


Fig. 6-1 Basic Configuration of Interrupt Function (2/2)

(D) External maskable interrupt (except INTP0)



(E) Software interrupt



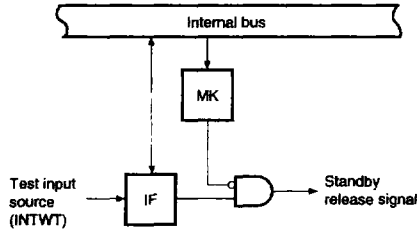
IF : Interrupt request flag
IE : Interrupt enable flag
ISP : In-service priority flag
MK : Interrupt mask flag
PR : Priority specification flag

6.2 TEST FUNCTION

The following test function is available.

Test input source		Internal/external
Name	Trigger	
INTWT	Overflow of watch timer	Internal

Fig. 6-2 Basic Configuration of Test Function



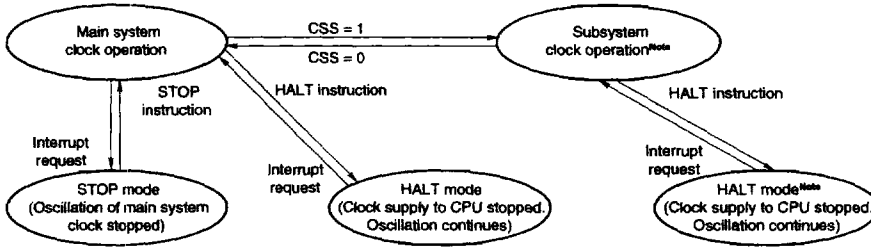
IF : Test request flag
MK : Test mask flag

7. STANDBY FUNCTION

The standby function is to reduce the current dissipation of the system and can be effected in the following two modes:

- HALT mode : In this mode, the operating clock of the CPU is stopped. By using this mode in combination with the normal operation mode, the system can be operated intermittently, so that the average current dissipation can be reduced.
- STOP mode : Oscillation of the main system clock is stopped. All the operations on the main system clock are stopped, and therefore, the current dissipation of the system can be minimized with only the subsystem clock oscillating.

Fig. 7-1 Standby Function



Note By stopping the main system clock, the current dissipation can be reduced. When the CPU operates on the subsystem clock, stop the main system clock by setting bit 7 (MCC) of the processor clock control register (PCC). The STOP instruction cannot be used.

Caution When the main system clock is stopped and the subsystem clock is operating, to switch again from the subsystem clock to the main system clock, allow sufficient time for the oscillation to settle before switching, by coding the program accordingly.

8. RESET FUNCTION

The system can be reset in the following two modes:

- External reset by $\overline{\text{RESET}}$ pin
- Internal reset by watchdog timer that detects hang up

9. INSTRUCTION SET

(1) 8-bit instruction

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

First operand \ Second operand	#byte	A	r Note	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL + byte] [HL + B] [HL + C]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
B, C											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											
[HL]		MOV											ROR4 ROL4
[HL + byte] [HL + B] [HL + C]		MOV											
X													MULU
C													DIVUW

Note Except for r = A

(2) 16-bit instruction

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

First operand \ Second operand	#word	AX	rp[Note]	sfrp	saddrp	!addr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW[Note]						INCW DECW PUSH POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

Note Only when rp = BC, DE, HL

(3) Bit manipulation instruction

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

First operand \ Second operand	A.bit	sfr.bit	saddr.bit	PSW.bit	[HL].bit	CY	$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call/Branch instruction

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

Second operand / First operand	AX	!addr16	!addr11	[addr5]	$addr16
Basic operation	BR	CALL BR	CALLF	CALLT	BR BC BNC BZ BNZ
Compound operation					BT BF BTCLR DBNZ

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

★ 10. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Parameter	Symbol	Conditions		Rating	Unit
Power supply voltage	V_{DD}			−0.3 to +7.0	V
	V_{LOAD}			V_{DD} − 40 to V_{DD} + 0.3	V
	AV_{DD}			−0.3 to V_{DD} + 0.3	V
	AV_{REF}			−0.3 to V_{DD} + 0.3	V
	AV_{SS}			−0.3 to +0.3	V
Input voltage	V_{I1}	P00-P04, P10-P17 (except when used as analog input pins), P20-P27, P30-P37, X1, X2, XT2, $\overline{RESET}$		−0.3 to V_{DD} + 0.3	V
	V_{I2}	P70-P74	N-ch open drain	−0.3 to +16[Note 1]	V
	V_{I3}	P110-P117, P120-P127	P-ch open drain	V_{DD} − 40 to V_{DD} + 0.3	V
Output voltage	V_{O1}	P01-P03, P10-P17, P20-P27, P30-P37		−0.3 to V_{DD} + 0.3	V
	V_{O2}	P70-P74		−0.3 to +16[Note 1]	V
	V_{O3}	P80, P81, P90-P97, P100-P107, P110-P117, P120-P127		V_{DD} − 40 to V_{DD} + 0.3	V
Analog input voltage	V_{AN}	ANI0-ANI7	Analog input pin	AV_{SS} − 0.3 to AV_{REF} + 0.3	V
Output current, high	I_{OH}	P01-P03, P10-P17, P20-P27, P30-P37 per pin		−10	mA
		P01-P03, P10-P17, P20-P27, P30-P37 total		−30	mA
		P80, P81, P90-P97, P100-P107, P110-P117, P120-P127 per pin		−30	mA
		P80, P81, P90-P97, P100-P107, P110-P117, P120-P127 total		−120	mA
Output current, low	I_{OL}	P01-P03, P10-P17, P20-P27, P30-P37, P70-P74 per pin	Peak value	30	mA
			rms value	15[Note 2]	mA
		P70-P74 total	Peak value	100	mA
			rms value	60[Note 2]	mA
		P01-P03, P10-P17, P20-P27, P30-P37 total	Peak value	50	mA
			rms value	20[Note 2]	mA
Total power dissipation	P_T[Note 3]	T_A = −40 to +60 °C		800	mW
		T_A = +85 °C		600	mW
Operating ambient temperature	T_A			−40 to +85	°C
Storage temperature	T_{stg}			−65 to +150	°C

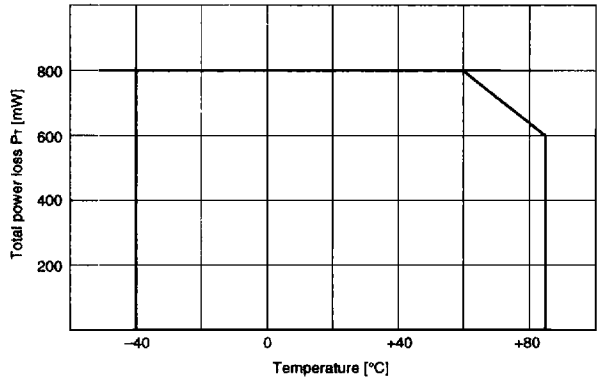
Caution Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The parameters apply independently. The device should be operated within the limits specified under DC and AC Characteristics.

Remark Unless otherwise specified, the characteristics of a shared pin are the same as those of a port pin.

Notes 1. For pins to which pull-up resistors are connected by the mask option, the rating is −0.3 to V_{DD} + 0.3.

2. *To obtain the rms value, calculate [rms value] = [peak value] × $\sqrt{duty}$.*

Notes 3. Permissible total power loss differs depending on the temperature (see the following figure).



How to calculate total power loss

The following three power consumption are available for the μPD78042F. The sum of the three power consumption should be less than the total power loss P_T (80 % or less of ratings is recommended).

① CPU power consumption: calculate V_{DD} (MAX.) × I_{DD1} (MAX.).

② Output pin power consumption: Normal output and display output are available. Power consumption when maximum current flows into each output pin.

③ Pull-down resistor power consumption: Power consumption by pull-down resistor connected to display output pin by the mask option.

The following total power consumption calculation example assumes the case where the characters shown in the figure on the next page are displayed.

Example: The operating conditions are as follows:

V_{DD} = 5 V ±10 %, operating at 5.0 MHz
Supply current (I_{DD}) = 21.6 mA
Display outputs: 11 grids × 10 segments (cut width is 1/16)
It is assumed that up to 15 mA flows to each grid pin, and that up to 3 mA flows to each segment pin.
It is also assumed that all display outputs are turned off at key scan timings.
Display output voltage: grid $V_{O3} = V_{DD} - 2$ V (Voltage drop of 2 V is assumed.)
segment $V_{O3} = V_{DD} - 0.4$ V (Voltage drop of 0.4 V is assumed.)
Voltage applied to fluorescent indication panel (V_{LOAD}) = −30 V
Mask-option pull-down resistor = 25 kΩ

The total power loss is calculated by determining power consumption ① to ③ under the above conditions.

① Power consumption of CPU: 5.5 V × 21.6 mA = 118.8 mW

② Power consumption at output pins:

$$\text{Grid:}\quad (V_{DD} - V_{O3}) \times \frac{\text{total current for all grids}}{\text{number of grids} + 1} \times \text{digit width } (1 - \text{cut width}) =$$

$$2\text{ V} \times \frac{15\text{ mA} \times 11\text{ grids}}{11\text{ grids} + 1} \times (1 - 1/16) = 25.8\text{ mW}$$

$$\text{Segment:}\quad (V_{DD} - V_{O3}) \times \frac{\text{total segment current for all dots to be lit}}{\text{number of grids} + 1} =$$

$$0.4\text{ V} \times \frac{3\text{ mA} \times 31\text{ dots}}{11\text{ grids} + 1} = 3.1\text{ mW}$$

③ Power consumption at pull-down resistors:

$$\text{Grid:}\quad \frac{(V_{O3} - V_{LOAD})^2}{\text{pull-down resistance}} \times \frac{\text{number of grids}}{\text{number of grids} + 1} \times \text{digit width} =$$

$$\frac{(5.5\text{ V} - 2\text{ V} - (-30\text{ V}))^2}{25\text{ k}\Omega} \times \frac{11\text{ grids}}{11\text{ grids} + 1} \times (1 - 1/16) = 38.6\text{ mW}$$

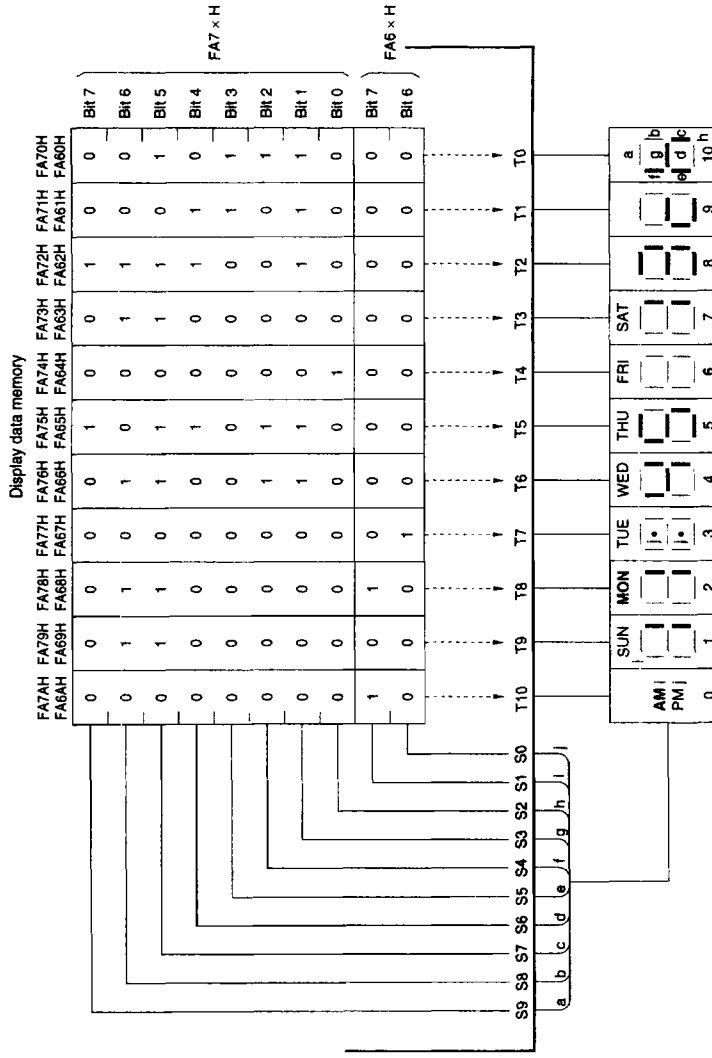
$$\text{Segment:}\quad \frac{(V_{O3} - V_{LOAD})^2}{\text{pull-down resistance}} \times \frac{\text{number of dots to be lit}}{\text{number of grids} + 1} =$$

$$\frac{(5.5\text{ V} - 0.4\text{ V} - (-30\text{ V}))^2}{25\text{ k}\Omega} \times \frac{31\text{ dots}}{11\text{ grids} + 1} = 127.3\text{ mW}$$

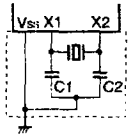
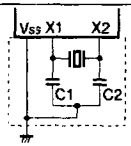
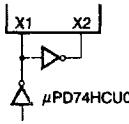
Total power consumption = ① + ② + ③ = 118.8 + 25.8 + 3.1 + 38.6 + 127.3 = 313.6 mW

In this example, the total power consumption does not exceed the rated value for the permissible total power loss shown in the graph on the previous page. Therefore, the calculation result in this example (313.6 mW) satisfies the requirement. If the total power consumption exceed the rated value for the permissible total power loss, the power consumption must be reduced, by reducing the number of built-in pull-down resistors.

10-Segment/11-Digit Display Example



MAIN SYSTEM CLOCK OSCILLATOR CHARACTERISTICS (T_A = −40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

Resonator	Recommended circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)Note 1		1		5	MHz
		Oscillation settling timeNote 2				4	ms
Crystal		Oscillation frequency (f_X)Note 1		1	4.19	5	MHz
		Oscillation settling timeNote 2	V_{DD} = 4.5 to 5.5 V			10	ms
						30	
External clock		X1 input frequency (f_X)Note 1		1		5	MHz
		X1 input high, low-level width (t_{XH}, t_{XL})		100		500	ns

Notes 1. It indicates only the oscillator characteristics. For the instruction execution time, see the AC Characteristics.

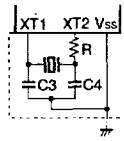
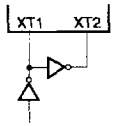
2. Time required until oscillation becomes stable after V_{DD} is applied or the STOP mode is disabled.

Cautions 1. If the main system clock oscillator is to be used, wire the area inside the broken line square as follows to avoid influence of wiring capacitance:

- **Make wiring as short as possible.**
- **Do not cross other signal lines.**
- **Do not get close to lines with fluctuating large current.**
- **Make sure that the connecting points of the capacitor of the oscillator always have the same electric potential as Vss.**
- **Do not connect the oscillator to a ground pattern that conducts a large current.**
- **Do not take out signal from the oscillator.**

2. When switching to the main system clock again after the subsystem clock has been used with the main system clock stopped, be sure to set the program to provide enough time for the oscillation to stabilize.

SUBSYSTEM CLOCK OSCILLATOR CHARACTERISTICS (T_A = −40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

Resonator	Recommended circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal		Oscillation frequency (f_{XT})Note 1		32	32.768	35	KHz
		Oscillation settling timeNote 2	V_{DD} = 4.5 to 5.5 V		12	2	s
						10	
External		XT1 input frequency (f_{XT})Note 1		32		100	kHz
		XT1 input high, low-level width (t_{XTH}, t_{XTL})		5		15	μs

Notes 1. It indicates only the oscillator characteristics. For the instruction execution time, see the AC Characteristics.

2. Time required until oscillation becomes stable after V_{DD} reaching MIN. of oscillation voltage range.

Cautions 1. If the subsystem clock oscillator is to be used, wire the area inside the broken line square as follows to avoid influence of wiring capacitance:

- **Make wiring as short as possible.**
- **Do not cross other signal lines.**
- **Do not get close to lines with fluctuating large current.**
- **Make sure that the connecting points of the capacitor of the oscillator always have the same electric potential as Vss.**
- **Do not connect the oscillator to a ground pattern that conducts a large current.**
- **Do not take out signal from the oscillator.**

2. The subsystem clock oscillator is more likely to have malfunctions due to noise than the main system clock oscillator because gain for the subsystem clock oscillator is made lower to reduce current consumption. When using the subsystem clock, be careful about how to connect wires.

RECOMMENDED OSCILLATOR CONSTANT

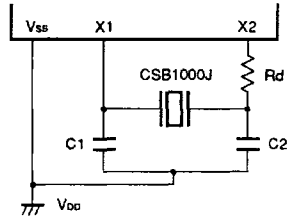
MAIN SYSTEM CLOCK: CERAMIC RESONATOR (T_A = −40 to +85 °C)

Manufacturer	Product name	Frequency (MHz)	Recommended circuit constant		Oscillator voltage range		Remark
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)	
Murata Mfg. Co., Ltd.	CSB1000J	1.00	100	100	2.7	5.5	Rd = 4.7 kΩ[Note]
	CSA2.00MG040	2.00	100	100	2.7	5.5	
	CST2.00MG040	2.00	—	—	2.7	5.5	Built-in capacitor
	CSA4.00MG	4.00	30	30	2.7	5.5	
	CST4.00MGW	4.00	—	—	2.7	5.5	Built-in capacitor
	CSA5.00MG	5.00	30	30	2.7	5.5	
	CST5.00MGW	5.00	—	—	2.7	5.5	Built-in capacitor
TDK Corp.	CCR1000K2	1.00	150	150	2.7	5.5	Surface-mount type
	CCR2.0MC3	2.00	—	—	2.7	5.5	Built-in capacitor, surface-mount type
	CCR4.0MC3	4.00	—	—	2.7	5.5	Built-in capacitor, surface-mount type
	FCR4.0MC5	4.00	—	—	2.7	5.5	Built-in capacitor
	CCR5.0MC3	5.00	—	—	2.7	5.5	Built-in capacitor, surface-mount type
	FCR5.0MC5	5.00	—	—	2.7	5.5	Built-in capacitor
Matsushita Electronics Components Co., Ltd.	EFOEC2004A4	2.00	33	33	2.7	5.5	Built-in capacitor
	EFOS2004B5	2.00	33	33	2.7	5.5	Built-in capacitor, surface-mount type
	EFOEC3584A4	3.58	33	33	2.7	5.5	Built-in capacitor
	EFOS3584B5	3.58	33	33	2.7	5.5	Built-in capacitor, surface-mount type
	EFOEC4004A4	4.00	33	33	2.7	5.5	Built-in capacitor
	EFOS4004B5	4.00	33	33	2.7	5.5	Built-in capacitor, surface-mount type
	EFOEC5004A4	5.00	33	33	2.7	5.5	Built-in capacitor
	EFOS5004B5	5.00	33	33	2.7	5.5	Built-in capacitor, surface-mount type

Note When the CSB1000J (1.00 MHz) manufactured by Murata Mfg. is used, a limiting resistor (4.7 kΩ) is necessary (see the figure in the next page). When one of other resonators is used, no limiting resistor is required.

Caution The oscillation circuit constants and oscillation voltage range indicate conditions for stable oscillation but do not guarantee accuracy of the oscillation frequency. If the application circuit requires accuracy of the oscillation frequency, it is necessary to set the oscillation frequency of the resonator in the application circuit. For this, it is necessary to directly contact the manufacturer of the resonator that being used.

Recommended sample circuit for the main system clock when the CSB1000J manufactured by Murata Mfg. is used



CAPACITANCE (T_A = 25 °C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V				15	pF
Output capacitance	C_{OUT}	f = 1 MHz Unmeasured pins returned to 0 V				35	pF
Input/output capacitance	C_{IO}	f = 1 MHz Unmeasured pins returned to 0 V	P01-P03, P10-P17, P20-P27, P30-P37			15	pF
			P70-P74			20	pF
			P110-P117, P120-P127			35	pF

Remark Unless otherwise specified, the characteristics of the shared pin are the same as the characteristics of the port pin.

POWER SUPPLY VOLTAGE (T_A = −40 to +85 °C)

Parameter	Conditions	MIN.	TYP.	MAX.	Unit
CPU[Note 1]		2.7[Note 2]		5.5	V
Display controller/driver		4.5		5.5	V
PWM mode of 16-bit timer/event counter (TM0)		4.5		5.5	V
A/D converter		4.0		5.5	V
Other hardware		2.7		5.5	V

Notes 1. *Except for system clock oscillator, display controller/driver, and PWM.*

2. *Operating power supply voltage differs depending on the cycle time. See the* **AC Characteristics**.

DC CHARACTERISTICS (T_A = −40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-level input voltage	V_{IH1}	P21, P23		0.7V_{DD}		V_{DD}	V
	V_{IH2}	P00-P03, P20, P22, P24-P27, P33, P34, $\overline{RESET}$		0.8V_{DD}		V_{DD}	V
	V_{IH3}	P70-P74	N-ch open drain	0.7V_{DD}		15[Note 1]	V
	V_{IH4}	X1, X2[Note 2]		V_{DD} − 0.5		V_{DD}	V
	V_{IH5}	XT1/P04, XT2[Note 2]	V_{DD} = 4.5 to 5.5 V	V_{DD} − 0.5		V_{DD}	V
				V_{DD} − 0.3		V_{DD}	V
	V_{IH6}	P10-P17, P30-P32, P35-P37	V_{DD} = 4.5 to 5.5 V	0.65V_{DD}		V_{DD}	V
				0.7V_{DD}		V_{DD}	V
	V_{IH7}	P110-P117, P120-P127	V_{DD} = 4.5 to 5.5 V	0.7V_{DD}		V_{DD}	V
				V_{DD} − 0.5		V_{DD}	V
Low-level input voltage	V_{IL1}	P21, P23		0		0.3V_{DD}	V
	V_{IL2}	P00-P03, P20, P22, P24-P27, P33, P34, $\overline{RESET}$		0		0.2V_{DD}	V
	V_{IL3}	P70-P74	V_{DD} = 4.5 to 5.5 V	0		0.3V_{DD}	V
				0		0.2V_{DD}	V
	V_{IL4}	X1, X2[Note 2]		0		0.4	V
	V_{IL5}	XT1/P04, XT2[Note 2]	V_{DD} = 4.5 to 5.5 V	0		0.4	V
				0		0.3	V
	V_{IL6}	P10-P17, P30-P32, P35-P37		0		0.3V_{DD}	V
	V_{IL7}	P110-P117, P120-P127		V_{DD} − 35		0.3V_{DD}	V
High-level output voltage	V_{OH}	P01-P03, P10-P17, P20-P27, P30-P37, P80, P81, P90-P97, P100-P107, P110-P117, P120-P127	V_{DD} = 4.5 to 5.5 V, I_{OH} = −1 mA	V_{DD} − 1.0			V
			I_{OH} = −100 μA	V_{DD} − 0.5			V
Low-level output voltage	V_{OL1}	P30-P37, P70-P74	V_{DD} = 4.5 to 5.5 V, I_{OL} = 15 mA		0.4	2.0	V
		P01-P03, P10-P17, P20-P27	V_{DD} = 4.5 to 5.5 V, I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	SB0, SB1, $\overline{SCK0}$	V_{DD} = 4.5 to 5.5 V, With open-drain and pull-up (R = 1 kΩ)			0.2V_{DD}	V
	V_{OL3}	P01-P03, P10-P17, P20-P27, P30-P37, P70-P74	I_{OL} = 400 μA			0.5	V

Notes 1. Pins to which pull-up resistors are connected by the mask option become V_{DD}.

2. If the X1 pin is used for high-level voltage input, the X2 pin is used for low-level voltage input, or vice versa. This is also true for the XT1/P04 pin and XT2 pin.

Remark Unless otherwise specified, the characteristics of a shared pin are the same as those of a port pin.

DC CHARACTERISTICS (T_A = −40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-level input leakage current	I_{LIH1}	$V_{IN} = V_{DD}$	P00-P03, P10-P17, P20-P27, P30-P37, $\overline{RESET}$			3	μA
	I_{LIH2}		X1, X2, XT1/P04, XT2			20	μA
	I_{LIH3}	V_{IN} = 15 V	P70-P74			20	μA
	I_{LIH4}	P110-P117, P120-P127, $V_{IN} = V_{DD}$	V_{DD} = 4.5 to 5.5 V			3 Note 1	μA
						3 Note 2	μA
Low-level input leakage current	I_{LIL1}	V_{IN} = 0 V	P00-P03, P10-P17, P20-P27, P30-P37, $\overline{RESET}$			−3	μA
	I_{LIL2}		X1, X2, XT1/P04, XT2			−20	μA
	I_{LIL3}		P70-P74			−3 Note 3	μA
	I_{LIL4}		P110-P117, P120-P127			−10	μA
High-level output leakage current Note 4	I_{LOH1}	$V_{OUT} = V_{DD}$	P01-P03, P10-P17, P20-P27, P30-P37, P80, P81, P90-P97, P100-P107, P110-P117, P120-P127			3	μA
	I_{LOH2}	V_{OUT} = 15 V	P70-74, N-ch open drain			20	μA
Low-level output leakage current Note 4	I_{LOL1}	V_{OUT} = 0 V	P01-P03, P10-P17, P20-P27, P30-P37, P70-P74			−3	μA
	I_{LOL2}	$V_{OUT} = V_{LOAD} = V_{DD} - 35$ V	P80, P81, P90-P97, P100-P107, P110-P117, P120-P127			−10	μA
Display output current	I_{OD}	V_{DD} = 4.5 to 5.5 V, $V_{OD} = V_{DD} - 2$ V		−15	−25		mA
Mask option pull-up resistor	R_1	V_{IN} = 0 V, P70-P74		20	40	90	kΩ
Software pull-up resistor	R_2	V_{IN} = 0 V, P01-P03, P10-P17, P20-P27, P30-P37	V_{DD} = 4.5 to 5.5 V	15	40	90	kΩ
				20		500	kΩ
Mask option pull-down resistor	R_3	P80, P81, P90-P97, P100-P107, P110-P117, P120-P127	$V_{OD} - V_{LOAD}$ = 35 V	25	65	135	kΩ
			$V_{OD} - V_{SS}$ = 5 V	15	40	90	kΩ
	R_4	P30-P37, $V_{IN} = V_{DD}$		40	80	150	kΩ

Notes 1. When P110 to P117 and P120 to P127 do not contain the pull-down resistors (according to the specification of the mask option), a high-level input leakage current of 150 μA (MAX.) flows only during 1.5 clocks after a read instruction has been executed to read out port 11 or 12 (P11 or P12) or port mode register 11 or 12 (PM11 or PM12). Outside the 1.5 clocks after a read instruction, the current is 3 μA (MAX.).

2. When P110 to P117 and P120 to P127 do not contain the pull-down resistors (according to the specification of the mask option), a high-level input leakage current of 90 μA (MAX.) flows only during 1.5 clocks after a read instruction has been executed to read out P11, P12, PM11, or PM12. Outside the 1.5 clocks after a read instruction, the current is 3 μA (MAX.).

3. When P70 to P74 do not contain the pull-down resistors (according to the specification of the mask option), a low-level input leakage current of −150 μA (MAX.) flows only during 1.5 clocks after a read instruction has been executed to read out port 7 (P7) or port mode register 7 (PM7). Outside the 1.5 clocks after a read out instruction, the current is −3 μA (MAX.).

4. Current which flows in the built-in pull-up or pull-down resistor is not included.

Remark Unless otherwise specified, the characteristics of a shared pin are the same as those of a port pin.

DC CHARACTERISTICS (T_A = −40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Power supply current[Note 1]	I_{DD1}	5.0 MHz crystal oscillation Operating mode	V_{DD} = 5.0 V ±10 %[Note 2]		7.2	21.6	mA
			V_{DD} = 3.0 V ±10 %[Note 3]		0.9	2.7	mA
	I_{DD2}	5.0 MHz crystal oscillation HALT mode	V_{DD} = 5.0 V ±10 %		1.3	3.9	mA
			V_{DD} = 3.0 V ±10 %		550	1650	μA
	I_{DD3}	32.768 kHz crystal oscillation Operating mode[Note 4]	V_{DD} = 5.0 V ±10 %		60	120	μA
			V_{DD} = 3.0 V ±10 %		35	70	μA
	I_{DD4}	32.768 kHz crystal oscillation HALT mode[Note 4]	V_{DD} = 5.0 V ±10 %		25	50	μA
			V_{DD} = 3.0 V ±10 %		5	10	μA
	I_{DD5}	XT1 = 0 V STOP mode Feedback resistor connected	V_{DD} = 5.0 V ±10 %		1	20	μA
			V_{DD} = 3.0 V ±10 %		0.5	10	μA
	I_{DD6}	XT1 = 0 V STOP mode Feedback resistor not connected	V_{DD} = 5.0 V ±10 %		0.1	20	μA
			V_{DD} = 3.0 V ±10 %		0.05	10	μA

Notes 1. This current excludes the AV_{REF} current, port current, and current which flows in the built-in pull-down resistor (mask option).

2. When operating at high-speed mode (when the processor clock control register (PCC) is set to 00H)

3. When operating at low-speed mode (when the PCC is set to 04H)

4. When the main system clock is stopped

AC CHARACTERISTICS

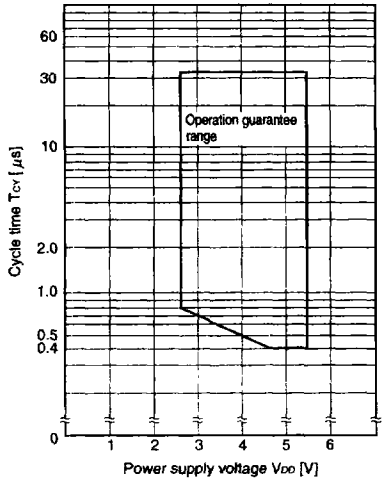
(1) Basic operation (T_A = −40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	Operated with main system clock	V_{DD} = 4.5 to 5.5 V	0.4		32	μs
				0.8		32	μs
		Operated with subsystem clock		40 Note 1	122	125	μs
TI1, 2 input frequency	f_{TI}	V_{DD} = 4.5 to 5.5 V		0		2	MHz
				0		138	kHz
TI1, 2 input high, low-level width	t_{TIH}	V_{DD} = 4.5 to 5.5 V		250			ns
	t_{TIL}			3.6			μs
Interrupt input high, low-level width	t_{INTH}	INTP0		$8/f_{sam}$ Note 2			μs
	t_{INTL}	INTP1-INTP3		10			μs
$\overline{RESET}$ low-level width	t_{RSL}			10			μs

Notes 1. Value when external clock input is used as subsystem clock. When crystal is used, the value becomes 114 μs.

2. Selection of $f_{sam} = f_X/2^{N+1}$, fx/64, fx/128 is available (N = 0 to 4) by bits 0 and 1 (SCS0, SCS1) of sampling clock select register (SCS).

T_{CY} vs. V_{DD} (with main system clock operated)



(2) Serial interface (T_A = −40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

(a) Serial interface channel 0

(i) Three-wire serial I/O mode ($\overline{SCK0}$: Internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY1}	V_{DD} = 4.5 to 5.5 V		800			ns
				3200			ns
$\overline{SCK0}$ high, low-level width	t_{KH1}	V_{DD} = 4.5 to 5.5 V		$t_{KCY1}/2 - 50$			ns
	t_{KL1}			$t_{KCY1}/2 - 150$			ns
SI0 setup time to $\overline{SCK0}$↑	t_{SIK1}			100			ns
SI0 hold time from $\overline{SCK0}$↑	t_{KSI1}			400			ns
$\overline{SCK0}$↓→ SO0 output delay time	t_{KSO1}	C = 100 pF[Note]	V_{DD} = 4.5 to 5.5 V			300	ns
						1000	ns

Note C is a load capacitance of the $\overline{SCK0}$ or SO0 output line.

(ii) Three-wire serial I/O mode ($\overline{SCK0}$: External clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY2}	V_{DD} = 4.5 to 5.5 V		800			ns
				3200			ns
$\overline{SCK0}$ high, low-level width	t_{KH2}	V_{DD} = 4.5 to 5.5 V		400			ns
	t_{KL2}			1600			ns
SI0 setup time to $\overline{SCK0}$↑	t_{SIK2}	V_{DD} = 4.5 to 5.5 V		100			ns
SI0 hold time from $\overline{SCK0}$↑	t_{KSI2}			400			ns
$\overline{SCK0}$↓→ SO0 output delay time	t_{KSO2}	C = 100 pF[Note]	V_{DD} = 4.5 to 5.5 V			300	ns
						1000	ns
$\overline{SCK0}$ rise time and fall time	t_{R2} t_{F2}					160	ns

Note C is a load capacitance of the SO0 output line.

(iii) SBI mode ($\overline{SCK0}$: Internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY3}	V_{DD} = 4.5 to 5.5 V		800			ns
				3200			ns
$\overline{SCK0}$ high, low-level width	t_{KH3}	V_{DD} = 4.5 to 5.5 V		$t_{KCY3}/2 - 50$			ns
	t_{KL3}			$t_{KCY3}/2 - 150$			ns
SB0, SB1 setup time to $\overline{SCK0}$↑	t_{SIK3}	V_{DD} = 4.5 to 5.5 V		100			ns
				300			ns
SB0, SB1 hold time from $\overline{SCK0}$↑	t_{KSI3}			$t_{KCY3}/2$			ns
$\overline{SCK0}$↓→SB0, SB1 output delay time	t_{KSO3}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 4.5 to 5.5 V	0		250	ns
				0		1000	ns
$\overline{SCK0}$↑→SB0, SB1↓	t_{KSB}			t_{KCY3}			ns
SB0, SB1↓→ $\overline{SCK0}$↓	t_{SBK}			t_{KCY3}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY3}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY3}			ns

Note R is a load resistance of the $\overline{SCK0}$, SB0, or SB1 output line, and C is its load capacitance.

(iv) SBI mode ($\overline{SCK0}$: External clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY4}	V_{DD} = 4.5 to 5.5 V		800			ns
				3200			ns
$\overline{SCK0}$ high, low-level width	t_{KH4}	V_{DD} = 4.5 to 5.5 V		400			ns
	t_{KL4}			1600			ns
SB0, SB1 setup time to $\overline{SCK0}$↑	t_{SIK4}	V_{DD} = 4.5 to 5.5 V		100			ns
				300			ns
SB0, SB1 hold time from $\overline{SCK0}$↑	t_{KSI4}			$t_{KCY4}/2$			ns
$\overline{SCK0}$↓→SB0, SB1 output delay time	t_{KSO4}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 4.5 to 5.5 V	0		300	ns
				0		1000	ns
$\overline{SCK0}$↑→SB0, SB1↓	t_{KSB}			t_{KCY4}			ns
SB0, SB1↓→$\overline{SCK0}$↓	t_{SBK}			t_{KCY4}			ns
SB0, SB1 high-level witdh	t_{SBH}			t_{KCY4}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY4}			ns
$\overline{SCK0}$ rise time and fall time	t_{R4} t_{F4}					160	ns

Note R is a load resistance of the SB0 or SB1 output line, and C is its load capacitance.

(v) Two-wire serial I/O mode ($\overline{SCK0}$: Internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY5}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 4.5 to 5.5 V	1600			ns
				3800			ns
$\overline{SCK0}$ high-level width	t_{KH5}			$t_{KCY5}/2 - 160$			ns
$\overline{SCK0}$ low-level width	t_{KL5}			$t_{KCY5}/2 - 50$			ns
SB0, SB1 setup time to $\overline{SCK0}$↑	t_{SIK5}			300			ns
SB0, SB1 hold time from $\overline{SCK0}$↑	t_{KSI5}			600			ns
$\overline{SCK0}$↓→ SB0, SB1 output delay time	t_{KSO5}		V_{DD} = 4.5 to 5.5 V	0		250	ns
				0		1000	ns

Note R is a load resistance of the $\overline{SCK0}$, SB0, or SB1 output line, and C is its load capacitance.

(vi) Two-wire serial I/O mode ($\overline{SCK0}$: External clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY6}	V_{DD} = 4.5 to 5.5 V		1600			ns
				3800			ns
$\overline{SCK0}$ high-level width	t_{KH6}			650			ns
$\overline{SCK0}$ low-level width	t_{KL6}			800			ns
SB0, SB1 setup time to $\overline{SCK0}$↑	t_{SIK6}			100			ns
SB0, SB1 hold time from $\overline{SCK0}$↑	t_{KSI6}			$t_{KCY6}/2$			ns
$\overline{SCK0}$↓→ SB0, SB1 output delay time	t_{KSO6}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 4.5 to 5.5 V	0		300	ns
				0		1000	ns
$\overline{SCK0}$ rise time and fall time	t_{R6}					160	ns
	t_{F6}						

Note R is a load resistance of the SB0 or SB1 output line, and C is its load capacitance.

(b) Serial interface channel 1

(i) Three-wire serial I/O mode ($\overline{SCK1}$: Internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY7}	V_{DD} = 4.5 to 5.5 V		800			ns
				3200			ns
$\overline{SCK1}$ high, low-level width	t_{KH7}	V_{DD} = 4.5 to 5.5 V		$t_{KCY7}/2 - 50$			ns
	t_{KL7}			$t_{KCY7}/2 - 150$			ns
SI1 setup time to $\overline{SCK1}$↑	t_{SIK7}			100			ns
SI1 hold time from $\overline{SCK1}$↑	t_{KSI7}			400			ns
$\overline{SCK1}$↓→ SO1 output delay time	t_{KSO7}	C = 100 pF[Note]	V_{DD} = 4.5 to 5.5 V			300	ns
						1000	ns

Note C is a load capacitance of the $\overline{SCK1}$ or SO1 output line.

(ii) Three-wire serial I/O mode ($\overline{SCK1}$: External clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY8}	V_{DD} = 4.5 to 5.5 V		800			ns
				3200			ns
$\overline{SCK1}$ high, low-level width	t_{KH8}	V_{DD} = 4.5 to 5.5 V		400			ns
	t_{KL8}			1600			ns
SI1 setup time to $\overline{SCK1}$↑	t_{SIK8}	V_{DD} = 4.5 to 5.5 V		100			ns
SI1 hold time from $\overline{SCK1}$↑	t_{KSI8}			400			ns
$\overline{SCK1}$↓→ SO1 output delay time	t_{KSO8}	C = 100 pF[Note]	V_{DD} = 4.5 to 5.5 V			300	ns
						1000	ns
$\overline{SCK1}$ rise time and fall time	t_{R8}					160	ns
	t_{F8}						

Note C is a load capacitance of the SO1 output line.

(iii) 3-wire serial I/O mode with automatic transmission/reception function ($\overline{SCK1}$: internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY9}	V_{DD} = 4.5 to 5.5 V		800			ns
				3200			ns
$\overline{SCK1}$ high, low-level width	t_{KH9}	V_{DD} = 4.5 to 5.5 V		$t_{KCY9}/2 - 50$			ns
	t_{KL9}			$t_{KCY9}/2 - 150$			ns
SI1 setup time to $\overline{SCK1}$↑	t_{SIK9}			100			ns
SI1 hold time from $\overline{SCK1}$↑	t_{KSI9}			400			ns
$\overline{SCK1}$↓→SO1 output delay time	t_{KSO9}	C = 100 pF[Note]	V_{DD} = 4.5 to 5.5 V			300	ns
						1000	ns
$\overline{SCK1}$↑→STB↑	t_{SBD}			$t_{KCY9}/2 - 100$		$t_{KCY9}/2 + 100$	ns
Strobe signal high level width	t_{SBW}			$t_{KCY9} - 30$		$t_{KCY9} + 30$	ns
Busy signal setup time (to busy signal detection timing)	t_{BYS}			100			ns
Busy signal hold time (to busy signal detection timing)	t_{BYH}			100			ns
Busy inactive → $\overline{SCK1}$↓	t_{SPS}					$2t_{KCY9}$	ns

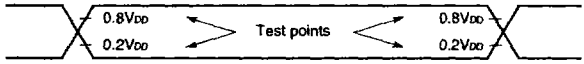
Note C is a load capacitance of the $\overline{SCK1}$ or SO1 output line.

(iv) 3-wire serial I/O mode with automatic transmission/reception function ($\overline{SCK1}$: external clock input)

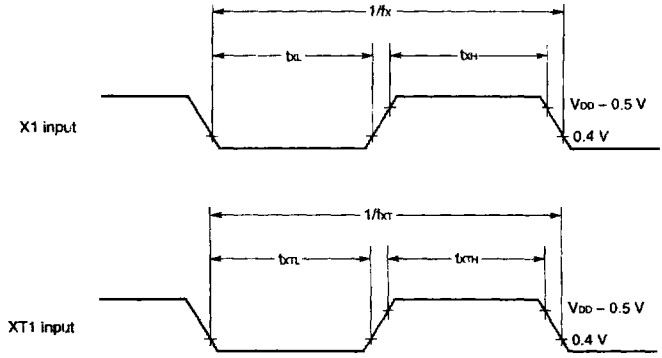
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY10}	V_{DD} = 4.5 to 5.5 V		800			ns
				3200			ns
$\overline{SCK1}$ high, low-level width	t_{KH10}	V_{DD} = 4.5 to 5.5 V		400			ns
	t_{KL10}			1600			ns
SI1 setup time to $\overline{SCK1}$↑	t_{SIK10}			100			ns
SI1 hold time from $\overline{SCK1}$↑	t_{KSI10}			400			ns
$\overline{SCK1}$↓→ SO1 output delay time	t_{KSO10}	C = 100 pF[Note]	V_{DD} = 4.5 to 5.5 V			300	ns
						1000	ns
$\overline{SCK1}$ rise time and fall time	t_{R10}					160	ns
	t_{F10}						

Note C is a load capacitance of the SO1 output line.

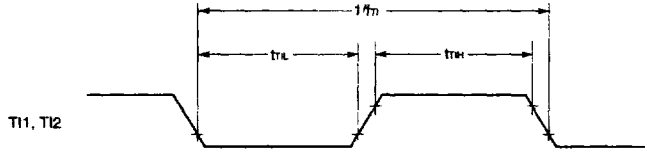
AC timing test points (except X1, XT1 input)



Clock timing

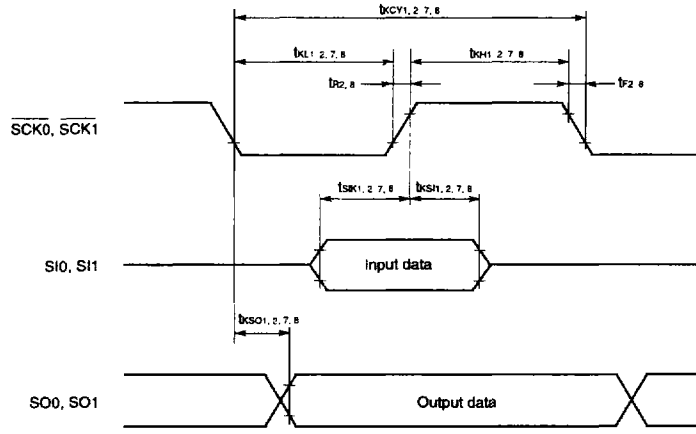


TI timing

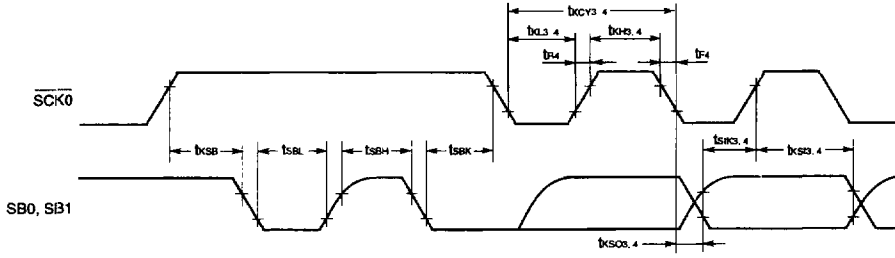


Serial transfer timing

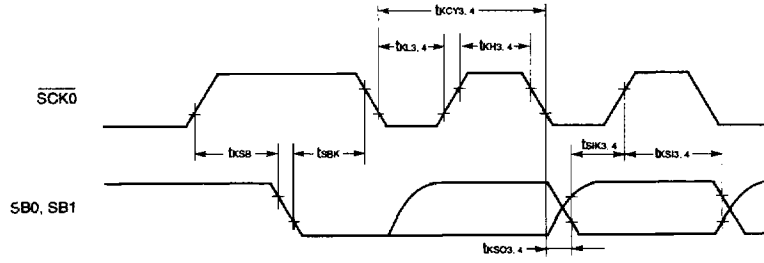
3-wire serial I/O mode:



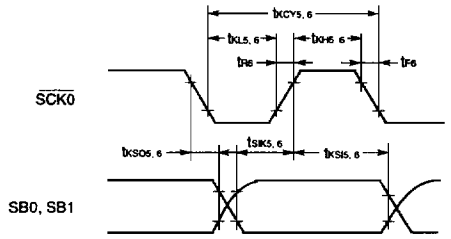
SBI mode (bus release signal transfer):



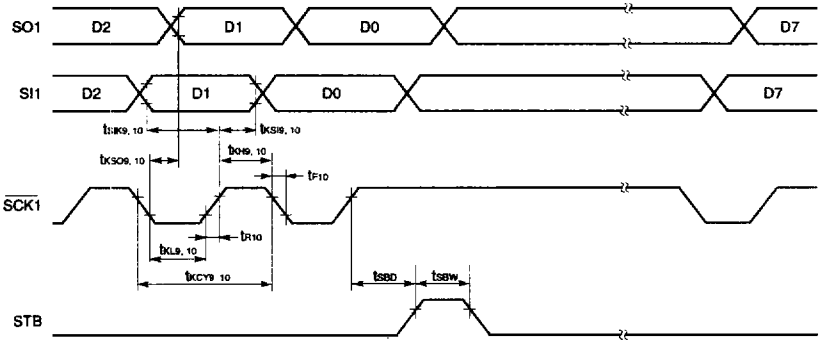
SBI mode (command signal transfer):



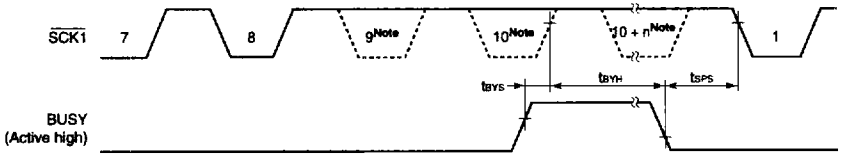
2-wire serial I/O mode:



3-wire serial I/O mode with automatic transmission/reception function:



3-wire serial I/O mode with automatic transmission/reception function (busy processing):



Note $\overline{\text{SCK}}$ does not become low actually at this point, but is indicated so to conform to the timing specification.

A/D CONVERTER CHARACTERISTICS (T_A = −40 to +85 °C, AV_{DD} = V_{DD} = 4.0 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Total error[Note 1]					0.8	%
Conversion time[Note 2]	t_{CONV}	1 MHz ≤ f_X ≤ 5.0 MHz	19.1		200	μs
Sampling time[Note 3]	t_{SAMP}		2.86		30	μs
Analog signal input voltage	V_{IAN}		AV_{SS}		AV_{REF}	V
Reference voltage	AV_{REF}		4.0		AV_{DD}	V
AV_{REF} resistor	R_{AVREF}		4	14		kΩ
AV_{DD} current	AI_{DD}			200	400	μA

Notes 1. Quantization error (±1/2LSB) is not included. This parameter is indicated as the ratio to the full-scale value.

2. Set the A/D conversion time to 19.1 μs or more.

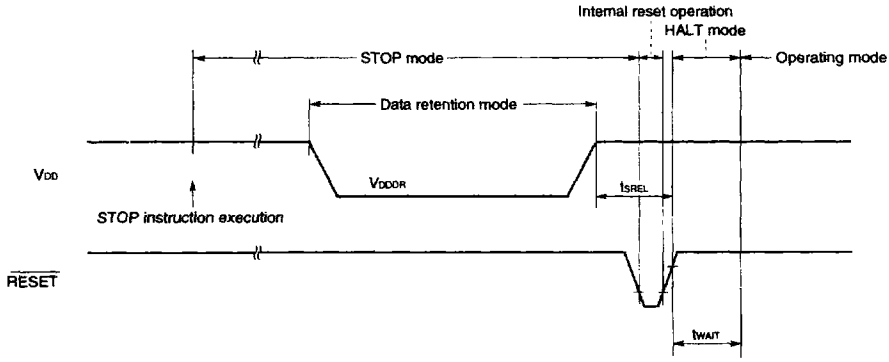
3. Sampling time depends on the conversion time.

DATA MEMORY STOP MODE LOW SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS
(T_A = −40 to +85 °C)

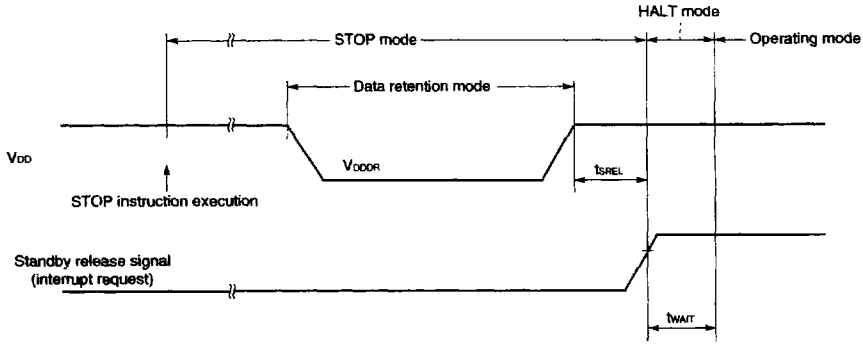
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		2.0		5.5	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 2.0 V Subsystem clock stopped Feedback resistor not connected		0.1	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{RESET}$		$2^{17}/f_X$		ms
		Release by interrupt		Note		ms

Note Selection of $2^{12}/f_X$, $2^{14}/f_X$ to $2^{17}/f_X$ is available by bits 0 to 2 (OSTS0 to OSTS2) of oscillation settling time select register (OSTS).

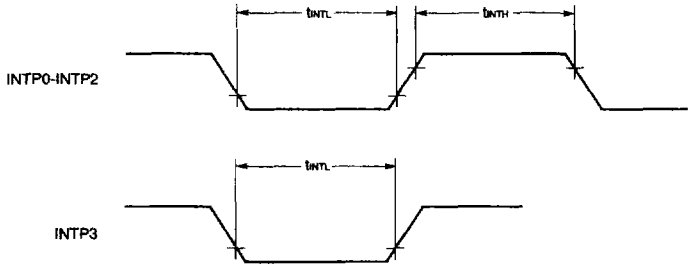
Data retention timing (STOP mode release by $\overline{RESET}$)



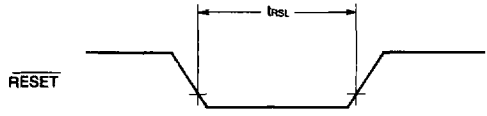
Data retention timing (standby release signal: STOP mode release by interrupt signal)



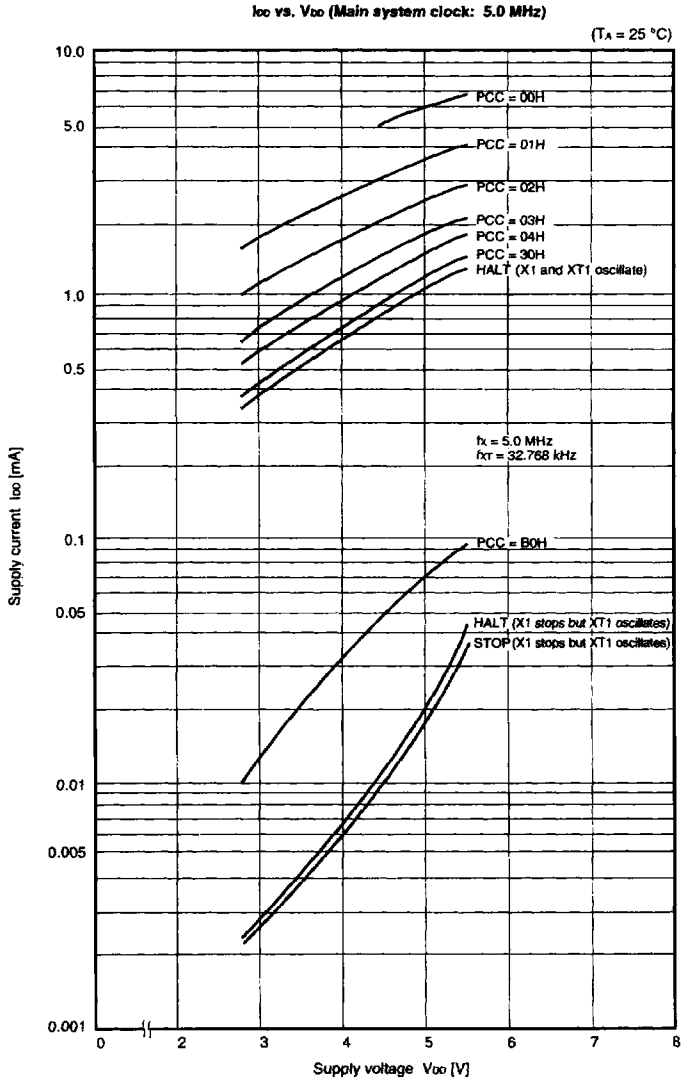
Interrupt input timing



$\overline{\text{RESET}}$ input timing

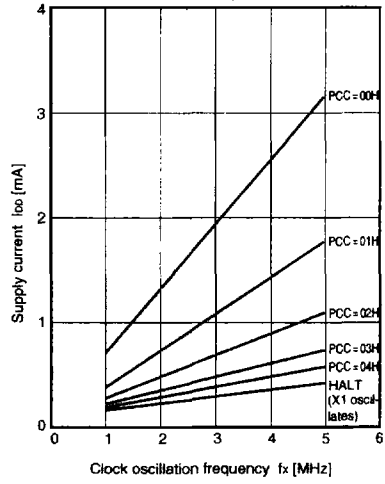


★ 11. CHARACTERISTIC CURVE (REFERENCE VALUE)



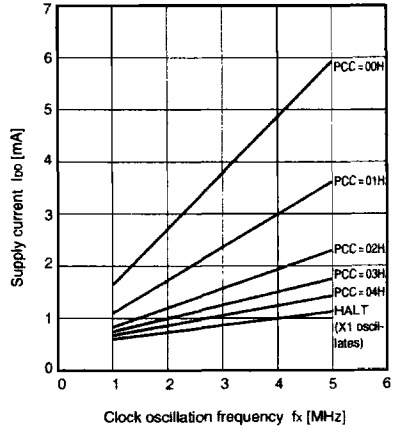
I_{DD} vs. f_X

(V_{DD} = 3 V, T_A = 25 °C)



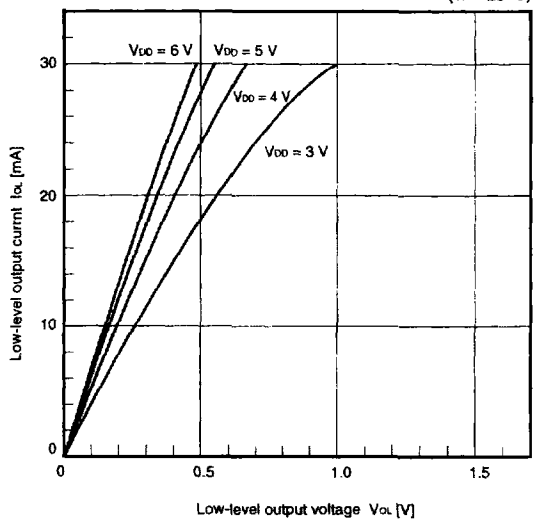
I_{DD} vs. f_X

(V_{DD} = 5 V, T_A = 25 °C)



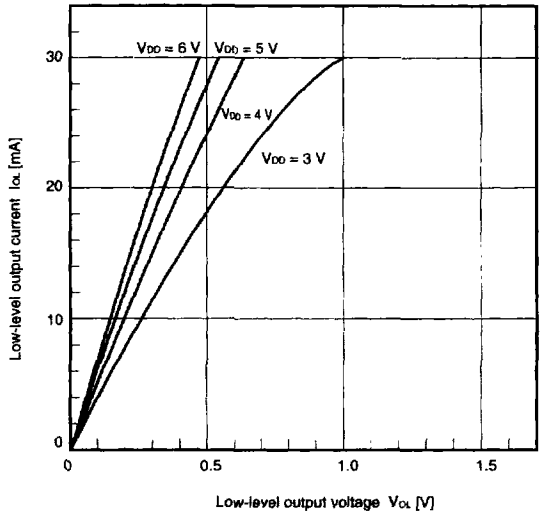
V_{OL} vs. I_{OL} (Port 1)

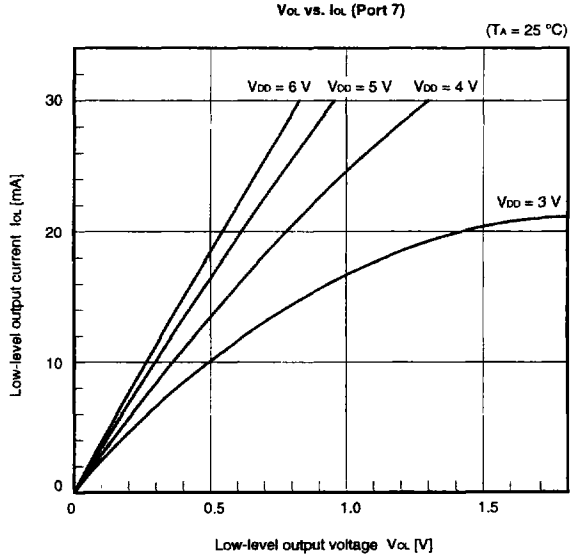
(T_A = 25 °C)

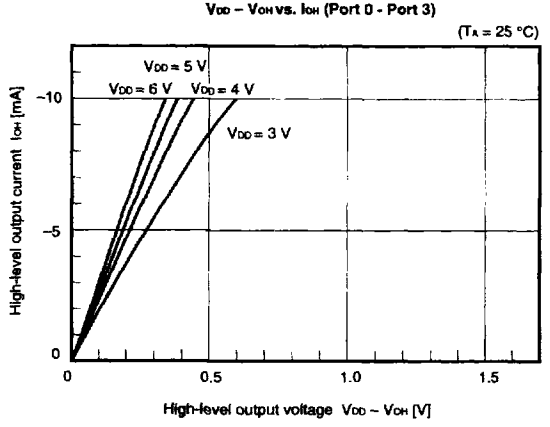


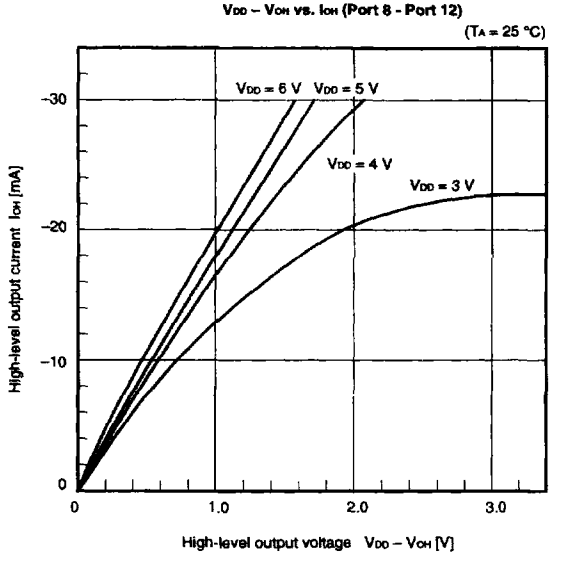
V_{OL} vs. I_{OL} (Ports 0, 2, and 3)

(T_A = 25 °C)



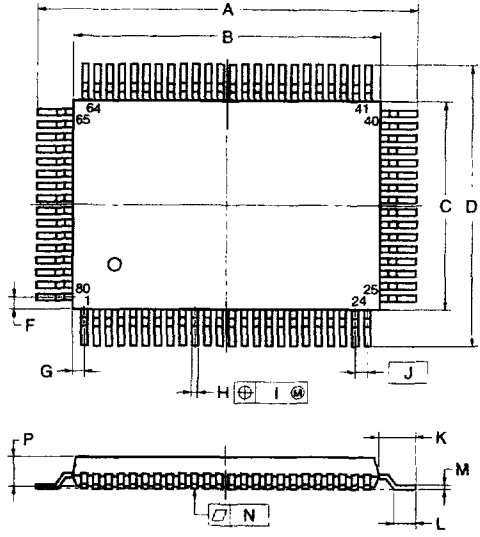

VOL vs. IOL (Port 7)
(TA = 25 °C)
VDD = 6 V
VDD = 5 V
VDD = 4 V
VDD = 3 V
30
20
10
0
0
0.5
1.0
1.5
Low-level output current IOL [mA]
Low-level output voltage VOL [V]


VDD – VOH vs. IOH (Port 0 - Port 3)
(TA = 25 °C)
VDD = 5 V
VDD = 6 V
VDD = 4 V
VDD = 3 V
High-level output current IOH [mA]
–10
–5
0
0
0.5
1.0
1.5
High-level output voltage VDD – VOH [V]


VDD – VOH vs. IOH (Port 8 - Port 12)
(TA = 25 °C)
VDD = 6 V
VDD = 5 V
VDD = 4 V
VDD = 3 V
High-level output current IOH [mA]
–30
–20
–10
0
0
1.0
2.0
3.0
High-level output voltage VDD – VOH [V]

12. PACKAGE DRAWING

80 PIN PLASTIC QFP (14×20)



NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	0.8	0.031
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

P80GF-80-3B9-3

Remark The shape and material of the ES version are the same as those of the corresponding mass-produced product.

★ 13. RECOMMENDED SOLDERING CONDITIONS

The conditions listed below shall be met when soldering the μPD78042F, μPD78043F, μPD78044F, or μPD78045F.

For details of the recommended soldering conditions, refer to our document *Semiconductor Device Mounting Technology Manual* (C10535E).

Please consult with our sales offices in case any other soldering process is used, or in case soldering is done under different conditions.

Table 13-1 Soldering Conditions for Surface-Mount Devices

μPD78042FGF-xxx-3B9: 80-pin plastic QFP (14 × 20 mm)
μPD78043FGF-xxx-3B9: 80-pin plastic QFP (14 × 20 mm)
μPD78044FGF-xxx-3B9: 80-pin plastic QFP (14 × 20 mm)
μPD78045FGF-xxx-3B9: 80-pin plastic QFP (14 × 20 mm)

Soldering process	Soldering conditions	Recommended conditions
Infrared ray reflow	Peak package's surface temperature: 235 °C Reflow time: 30 seconds or less (210 °C or more) Maximum allowable number of reflow processes: 3	IR35-00-3
VPS	Peak package's surface temperature: 215 °C Reflow time: 40 seconds or less (200 °C or more) Maximum allowable number of reflow processes: 3	VP15-00-3
Wave soldering	Solder temperature: 260 °C or less Flow time: 10 seconds or less Number of flow processes: 1 Preheating temperature : 120 °C max. (measured on the package surface)	WS60-00-1
Partial heating method	Terminal temperature: 300 °C or less Heat time: 3 seconds or less (for one side of a device)	—

Caution Do not apply two or more different soldering methods to one chip (except for partial heating method for terminal sections).