Registered ISO 9001 July,1997

Intel® (PC100) Approved

512 & 256 Megabyte Registered DIMM'S using

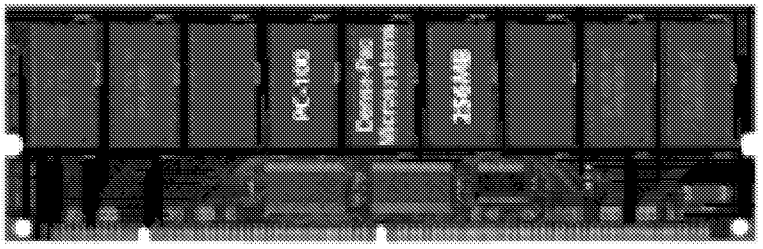
Dense-Pac's Patented Stacked Memory devices

for use in Intel® 440BX based

Chip Set NightShade & NightLlite motherboards

See Intel's web page for more information:

http://support.intel.com/support/motherboards/server/n440bx/nbx_mem.htm



For more information about Dense-Pac Stacking Memory Devices call your Dense-Pac Sales Rep. at:

(800) 642-4477

http://www.dense-pac.com

"Basic " testing approval provided by Computer Memory Test Lab (CMTL), an independent Intel certified test facility.
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DENSE-PAC
MICROSYSTEMS

512 Megabyte SDRAM DIMM
DPSD64MR72TW5-PC100

PRELIMINARY

DESCRIPTION:

The DPSD64MR72TW5-PC100 is a 64Mx72 SDRAM DIMM consisting of thirty-six 128Mbit SDRAM devices configured as 18 stacked 256Mbit modules in a 2-bank architecture. 8-bit ECC is provided for error protection. All control lines are registered; flow through buffer mode can be established by disabling the REGE signal.

These modules offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, interleave between internal banks in order to hide precharge time, and the capability to randomly change column address on each clock cycle during a burst.

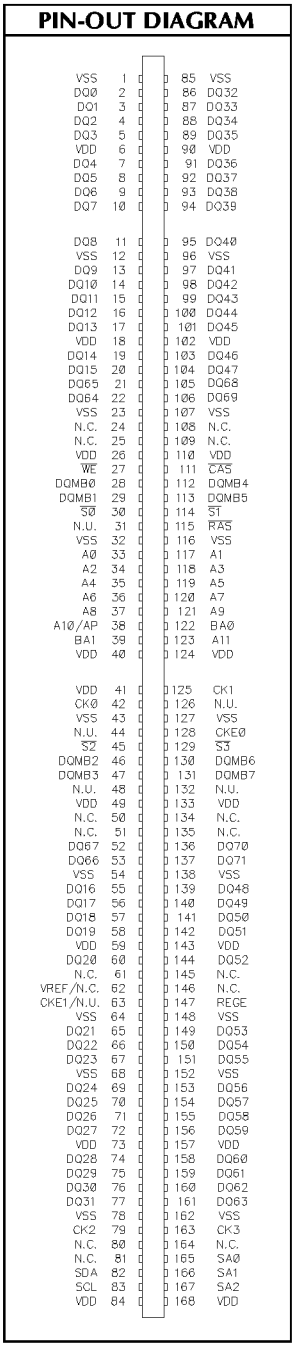
The DPSD64MR72TW5-PC100 is designed to operate in 3.3V, low power memory systems. An Auto Refresh Mode is provided along with a power saving Power-Down Mode. All inputs, outputs and clocks are LVTTL-compatible.

FEATURES:

- Configuration: 64 Meg x 72
- Module Design Compliant to Intel® Registered DIMM Specification Rev. 1.0
- PC100 Compliant Devices
- 3.3□0.3 Volt Power Requirement
- LVTTL Compatible I/O and Clock
- Programmable Burst Type, Burst Length, and CAS Latency
- Registered/Buffered Control Lines
- On-Board PLL Clock Driver
- Program Burst Lengths: 1, 2, 4, 8 or Full Page
- Internal Pipeline Operation; Column address can be changed every clock cycle
- 4096 Cycles / 64 ms Refresh
- Auto Precharge and Auto Refresh Modes
- Serial Presence-Detect (SPD)
- Utilizes 168-Pin Registered SDRAM DIMM JEDEC Standard and Intel Specification

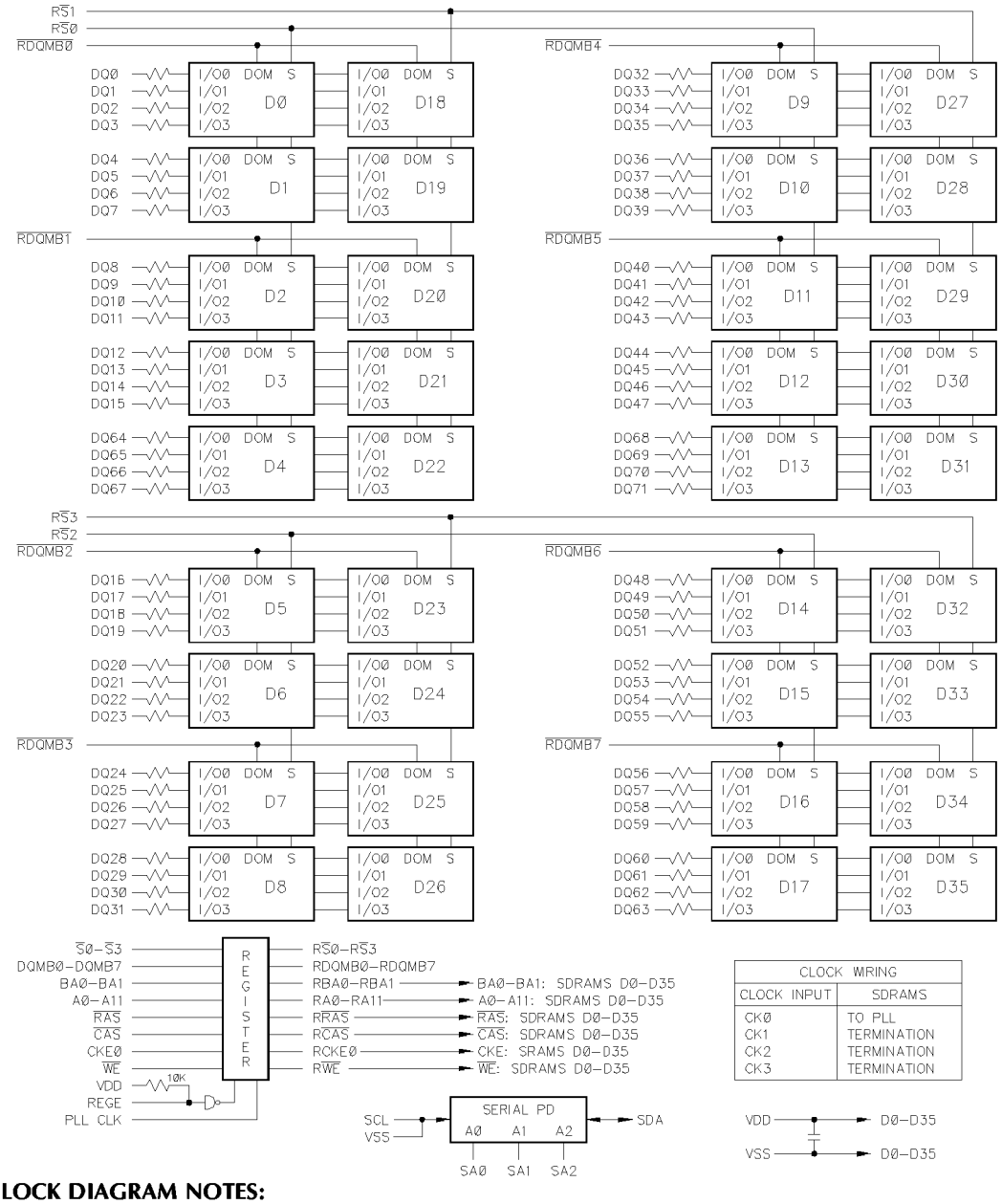
PIN NAMES	
A0 - A11	Row Address: A0 - A11 Column Address: A0 - A9, A11 Auto Precharge: A10
BA0, BA1	Bank Selects
DQ0 - DQ71	Data In / Data Out
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Enable
$\overline{WE}$	Data Write Enable
DQMB0-DQMB7	Data Input/Output Mask
CKE0, CKE1	Clock Enables
CK0 - CK3	System Clocks
$\overline{S0}$ - $\overline{S3}$	Chip Selects
REGE	Register Enable
SDA	Serial Presence-Detect Data
SCL	Serial Clock for Presence-Detect
V_{DD}	Power Supply
V_{SS}	Ground
N.C.	No Connect

PIN-OUT DIAGRAM



PRELIMINARY

FUNCTIONAL BLOCK DIAGRAM



CLOCK WIRING	
CLOCK INPUT	SDRAMS
CK0	TO PLL
CK1	TERMINATION
CK2	TERMINATION
CK3	TERMINATION

BLOCK DIAGRAM NOTES:

1. When necessary two copies of the same signals are created by doubling the register inputs.
2. Unless otherwise noted, resistors are 10 OHMs.
3. DQ wiring may differ from that described in Functional Block Diagram; however DQ/DQMB relationships are maintained as shown.

OPERATING FEATURES

$\overline{CAS}$ Latency

$\overline{CAS}$ latency defines the delay from when a Read Command is registered on a rising clock edge to when the data from the Read Command becomes available at the outputs. The $\overline{CAS}$ latency is expressed in terms of clock cycles and for this specific DIMM a value of 3 cycles is supported. Do not confuse DIMM $\overline{CAS}$ latency with SDRAM $\overline{CAS}$ latency which is one clock less. Once the appropriate $\overline{CAS}$ latency has been selected it must be programmed into the mode register after power up.

Register and DIMM Operation

All control and address signals are registered on-board and hence delayed by one cycle in arriving at the SDRAMs. The registers can be disabled (Flow-Through Buffer Mode) by pulling the REGE signal low.

The clock signal is distributed to all SDRAM's via a zero delay PLL. Note that the PLL must be given enough clock cycles to stabilize before any operation can be given (minimum stabilization time equal to 1ms).

ABSOLUTE MAXIMUM RATINGS			
Symbol	**Parameter**	**Value**	**Unit**
V_{DD}	Supply Voltage	-0.5 to +4.6	V
$V_{I/O}$	Input/Output Voltage	-0.5 to +4.6	V
T_{STG}	Storage Temperature	-55 to +125	°C
T_{OPR}	Operating Temperature	-0 to +70	°C
P_D	Power Dissipation	36	W
I_{OUT}	Short Circuit Output Current	50	mA

NOTE: Stresses greater than those under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING RANGE					
Symbol	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Unit**
V_{DD}	Supply Voltage	3.3		3.6	V
V_{IH}	Input HIGH Voltage	2.0		V_{DD}+0.3	V
V_{IL}	Input LOW Voltage	-0.3		0.8	V
T_A	Operating Temperature	0	+25	+70	°C

NOTE: All voltages reference to V_{SS} and V_{SSQ}.

CAPACITANCE*				
Symbol	**Parameter**	**Max.**	**Conditions**	**Unit**
C_{ADR}	Address Input	12	V_{DD} = 3.3V, T_A = 25°C, F = 1.0MHz	pF
C_{I1}	RAS, CAS, CKE0, DQMB, $\overline{PDE}$ Input	12		
C_S	Chip Select Input	12		
C_{WE}	Write Enable Input	12		
C_{CK}	System Clocks Input	5		
$C_{I/O}$	Data Input/Output	11		
C_{SDA}	Serial Presence Detect Data Output	10		
C_{REGE}	REGE Input	12		

* Values calculated, not measured.

SERIAL PRESENT DETECT INFORMATION				
Byte #	**Function**	**Value**	**Hex Value**	**Dec Value**
0	Number of Bytes Written into SPD	128 bytes	80	128
1	Total Number of Bytes in SPD Device	256 bytes	08	8
2	Fundamental Memory Type	SDRAM	04	4
3	Number of Row Address Bits	12	0C	12
4	Number of Column Address Bits	10	0B	11
5	Number of Banks in Module	2 Rows	02	2
6	Data Width	72 bits	40	64
7	Data Width (Continued)	-	00	0
8	Voltage Interface	LVTTL	01	1
9	SDRAM Cycle Time (t_{CYC})	10 ns	A0	160
10	SDRAM Access Time from Clock (t_{AC})	6 ns	60	96
11	Module Configuration Type	ECC	02	2
12	Refresh Rate and Type	SR/15.625	80	128
13	Primary SDRAM Width	x4	04	4
14	Error Checking SDRAM Width	x4	04	4
15	Minimum Clock Delay for Back-to-Back Random Column Address	t_{CCD} = 1 CLK	01	1
16	Burst Lengths Supported	1, 2, 4, 8 Full Page	8F	143
17	Number of Banks on SDRAM Device	4	04	4
18	$\overline{CAS}$ Latencies Supported	3	04	4
19	CS Latency	0 CLK	01	1
20	Write Latency	0 CLK	01	1
21	SDRAM Module Attributes	Buffer, Registered Control Lines	16	22
22	SDRAM Device Attributes : General	No Early $\overline{RAS}$ Precharge	0E	14
23	Minimun SDRAM Cycle Time ($\overline{CAS}$ Latency = 2)	12 ns	00	0
24	SDRAM Access from Clock ($\overline{CAS}$ Latency = 2)	7 ns	00	0
25	Minimum SDRAM Cycle Time ($\overline{CAS}$ Latency = 1)	-	00	0
26	SDRAM Access from Clock ($\overline{CAS}$ Latency = 1)	-	00	0
27	Minimum Row Precharge Time (t_{RP})	20	18	24
28	Minimum Row Active to Row Active Delay (t_{RRD})	20	14	20
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ Delay (t_{RCD})	20	18	24
30	Minimum RAS Pulse Width (t_{RAS})	50	32	50
31	Module Bank Density	128 MB	40	64
32-61	Not Used	-	00	0
62	SPD Data Revision Code	Intel SPD 1.2	12	18
63	Checksum for Bytes 0 - 62	158d - 9Eh	F6	246
64-125	Not Used	-	00	0
126	Intel® Specification Frequency	100 MHz	64	100
127	Intel® Specification CAS Latency Support	Double-Sided Norm.	85	133
128-255	Open for Customer Use	-	FF	255

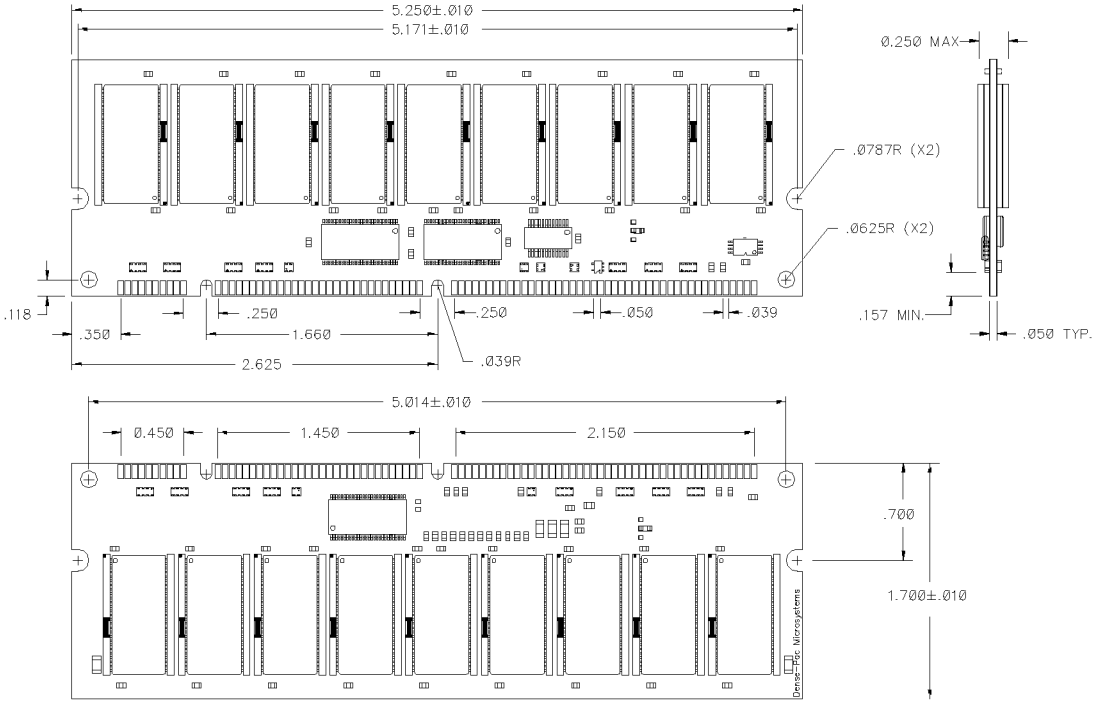
PRELIMINARY

ORDERING INFORMATION

DP	SD	64M	R	72	T	W5	–	PC100	CL3	T
PREFIX	TYPE	MEMORY DEPTH	DESIG	MEMORY WIDTH	DESIG	PACKAGE		COMPATABLE	TYPE	DESIG

- T: Blank GOLD CONTACTS; T TIN CONTACTS
- CL3: CL2 $\overline{\text{CAS}}$ LATENCY 2 (Under Development); CL3 $\overline{\text{CAS}}$ LATENCY 3
- W5: 168–PIN DIMM
- 72: 128 MEGABIT BASED
- R: REGISTERED MEMORY MODULE
- SD: SYNCHRONOUS DRAM

MECHANICAL DRAWING



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