UNITRODE

UCC1817/18
UCC2817/18
UCC3817/18
PRELIMINARY

BiCMOS Power Factor Preregulator

FEATURES

- Controls Boost Preregulator to Near-Unity Power Factor
- Limits Line Distortion
- World Wide Line Operation
- Over-voltage Protection
- Accurate Power Limiting
- Average Current Mode Control
- Improved Noise Immunity
- Improved Feed-forward Line Regulation
- Leading Edge Modulation
- 150µA Typical Start-up Current
- Low Power BiCMOS Operation
- 12V to 17V Operation

DESCRIPTION

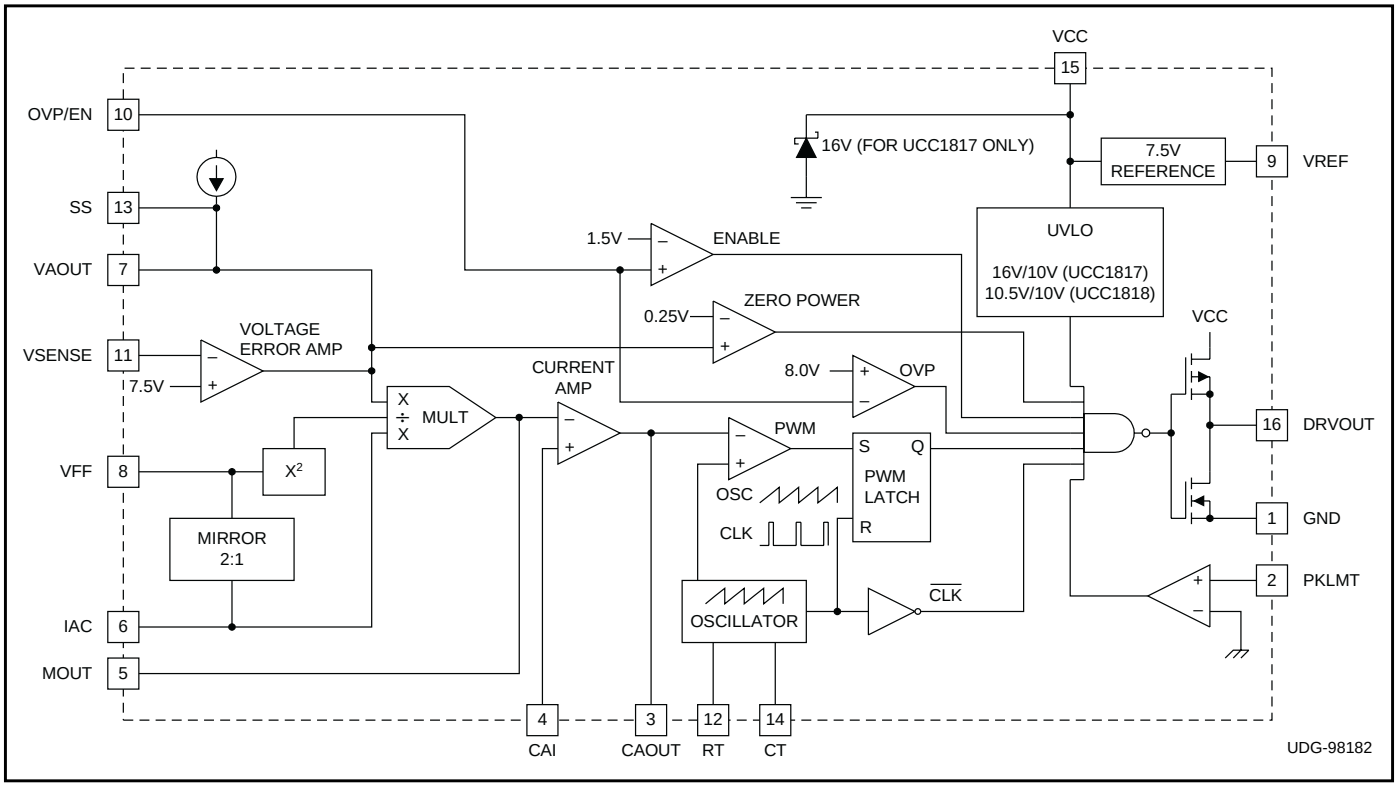
The UCC1817/UCC1818 provides all the functions necessary for active power factor corrected preregulators. The controller achieves near unity power factor by shaping the AC input line current waveform to correspond to that of the AC input line voltage. Average current mode control maintains stable, low distortion sinusoidal line current.

Designed in Unitrode's BiCMOS process, the UCC1817/UCC1818 offers new features such as lower start-up current, lower power dissipation, over-voltage protection, a shunt UVLO detect circuitry, a leading-edge modulation technique to improve ripple current in the bulk capacitor and an improved, low-offset (±2mV) current amplifier to reduce distortion at light load conditions.

UCC1817 offers an on-chip shunt regulator with low start-up current, suitable for applications utilizing a bootstrap supply. UCC1818 is intended for applications with a fixed supply (VCC).

Available in the 16-pin N, D, DW and J and 20 pin L and Q packages.

BLOCK DIAGRAM

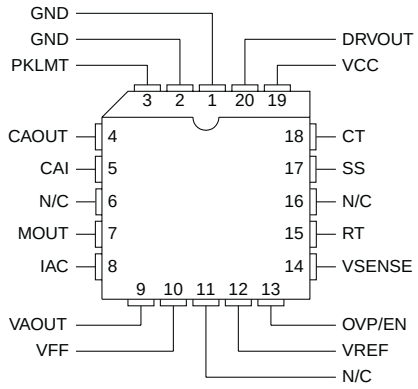


ABSOLUTE MAXIMUM RATINGS

Supply Voltage VCC 18V
Gate Drive Current,
  Continuous 0.2A
  50%Duty Cycle 1A
Input Voltage,
  CAI, MOUT 8V
  PKLMT 5V
  VSENSE, OVP/EN 10V
Input Current, RT, IAC, PKLMT 10mA
Maximum Negative Voltage, DRVOUT,PKLMT,MOUT . . –0.5V
Power Dissipation 1W

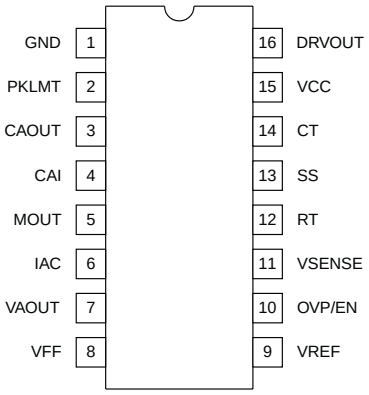
Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages. All voltages are referenced to GND.

PLCC-20, LCC-20 (TOP VIEW)
Q, L Packages

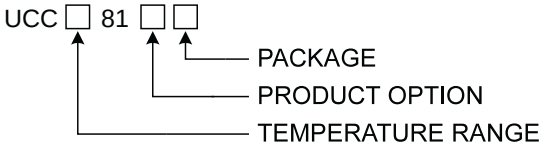


CONNECTION DIAGRAMS

SOIC-16, DIL-16 (TOP VIEW)
D, DW, N and J Packages



ORDERING INFORMATION



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, these specifications hold for T_A=0°C to 70°C for the UCC3817, –40°C to +85°C for the UCC2817, and –55°C to +125°C for the UCC1817, $T_A = T_J$. VCC = 12V, RT = 22k, CT = 330pF.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Section					
Supply Current, Off	VCC = (VCC Turnon Threshold – 0.3V)		150	300	µA
Supply Current, On	VCC = 12V, No Load on DRVOUT	2	4	6	mA
UVLO Section					
VCC Turn-On		15.4	16	16.6	V
UVLO Hysteresis		5.4	6	6.2	V
Maximum Shunt Voltage	I_{VCC} = 10mA	15.4	17	17.5	V
VCC Turn-On Threshold (UCC1818)		10.2	10.5	10.8	V
UVLO Hysteresis (UCC1818)		0.4	0.5	0.6	V
Voltage Amplifier Section					
Input Voltage	T_A = 0°C to 70°C	7.387	7.5	7.613	V
	T_A = –40° C to +85° C	7.369	7.5	7.631	V
	T_A = –55° C to 125° C	7.313	7.5	7.687	V
V_{SENSE} Bias Current	VSENSE = VREF, VAOUT = 2.5V		50	200	nA
Open Loop Gain	VAOUT = 2V to 5V		90		dB
V_{OUT} High	I_{LOAD} = –150µA	5.4	5.5	5.6	V
V_{OUT} Low	I_{LOAD} = 150µA		50	100	mV

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PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Over Voltage Protection and Enable Section					
Over Voltage Reference		7.8	8	8.2	V
Hysteresis			500		mV
Enable Threshold		1.0	1.5	2.0	V
Current Amplifier Section					
Input Offset Voltage	V_{CM} = 0V, V_{CAOUT} = 3V	–2	0	2	mV
Input Bias Current	V_{CM} = 0V, V_{CAOUT} = 3V		–50		nA
Input Offset Current	V_{CM} = 0V, V_{CAOUT} = 3V		25		nA
Open Loop Gain	V_{CM} = 0V, V_{CAOUT} = 2V to 5V		90		dB
CMRR	V_{CM} = 0V to 1.5V, V_{CAOUT} = 3V		80		dB
V_{OUT} High	I_{LOAD} = –120µA		6.3		V
V_{OUT} Low	I_{LOAD} = 1mA		0.2		V
Gain Bandwidth Product	Note 1		2.5		MHz
Voltage Reference Section					
Input Voltage	TA = 0°C to 70°C	7.387	7.5	7.613	V
	TA = –40°C to +85°C	7.369	7.5	7.631	V
	TA = –55°C to 125°C	7.313	7.5	7.687	V
Load Regulation	I_{REF} = 1mA to 2mA		3		mV
Line Regulation	VCC = 10.8V to 15V		20		mV
Short Circuit Current	VREF = 0V		–25		mA
Oscillator Section					
Initial Accuracy	T_A = 25°C	85	100	115	kHz
Voltage Stability	VCC = 10.8V to 15V		1		%
Total Variation	Line, Temp	80		120	kHz
Ramp Peak Voltage		4.5	5	5.5	V
Ramp Amplitude Voltage (peak to peak)			4		V
Peak Current Limit Section					
PKLMT Reference Voltage		–15		15	mV
PKLMT Propogation Delay			350		ns
Multiplier Section					
High Line, Low Power	I_{AC} = 500µA, V_{FF} = 4.7V, VAOUT = 1.25V		–6		µA
High Line, High Power	I_{AC} = 500µA, V_{FF} = 4.7V, VAOUT = 5V		–90		µA
Low Line, Low Power	I_{AC} = 150µA, V_{FF} = 1.4V, VAOUT = 1.25V		–19		µA
Low Line, High Power	I_{AC} = 150µA, V_{FF} = 1.4V, VAOUT = 5V		–300		µA
IAC Limited	I_{AC} = 150µA, V_{FF} = 1.3V, VAOUT = 5V		–300		µA
Gain Constant (K)	I_{AC} = 300µA, V_{FF} = 3V, VAOUT = 2.5V		1		1/V
Zero Current	I_{AC} = 150µA, V_{FF} = 1.4V, VAOUT = 0.25V		0	–2	µA
	I_{AC} = 500µA, V_{FF} = 4.7V, VAOUT = 0.25V		0	–2	µA
	I_{AC} = 500µA, V_{FF} = 4.7V, VAOUT = 0.5V		0	–3	µA
Power Limit	I_{AC} = 150µA, V_{FF} = 1.4V, VAOUT = 5V		–420		µW
Feed-Forward Section					
VFF Output Current	I_{AC} = 300µA		–150		µA
Soft Start Section					
SS Charge Current			–10		µA

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PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gate Driver Section					
Pull Up Resistance	I_{OUT} = –100mA		7		Ω
Pull Down Resistance	I_{OUT} = 100mA		3		Ω
Output Rise Time	C_{LOAD} = 1nF, R_{LOAD} = 10Ω		25		ns
Output Fall Time	C_{LOAD} = 1nF, R_{LOAD} = 10Ω		10		ns
Zero Power Section					
Zero Power Comparator Threshold	Measured on VAOUT	0.10	0.25	0.40	V

Note 1: Guaranteed by design, not 100% tested in production.

PIN DESCRIPTIONS

CAI: (current amplifier non-inverting input) This input and the inverting input (MOUT) remain functional down to and below GND.

CAOUT: (current amplifier output) This is the output of a wide bandwidth op amp that senses line current and commands the PFC pulse-width modulator (PWM) to force the correct current.

CT: (oscillator timing capacitor) A capacitor from CT to GND will set the PWM oscillator frequency according to:

$$f = \left[\frac{0.725}{(RT \bullet CT)} \right]$$

The lead from the oscillator timing capacitor to GND should be as short and direct as possible.

DRVOUT: (gate drive) The output drive for the PFC stage is a totem pole MOSFET gate driver on DRVOUT. Use a series gate resistor of at least 5Ω to prevent interaction between the gate impedance and the DRVOUT output driver that might cause the DRVOUT to overshoot excessively. Some overshoot of the DRVOUT output is always expected when driving a capacitive load.

GND: (ground) All voltages measured with respect to ground. VCC and REF should be bypassed directly to GND with a 0.1µF or larger ceramic capacitor.

IAC: (input AC current) This input to the analog multiplier is a current. The multiplier is tailored for very low distortion from this current input (I_{AC}) to multiplier output. Recommended maximum I_{AC} is 500µA.

MOUT: (multiplier output and current amplifier inverting input) The output of the analog multiplier and the inverting input of the current amplifier are connected together at MOUT. As the multiplier output is a current, this is a high impedance input so the amplifier can be configured as a differential amplifier. This configuration improves noise immunity and allows for the leading-edge modulation operation. The multiplier output current is given by the equation:

$$I_{MULT} = \frac{(VAOUT - 1) \bullet I_{AC}}{V_{FF}{}^2 \bullet K} \;;$$

Where K = 1 (multiplier gain constant.)

OVP/EN: (over-voltage/enable) A window comparator input which will disable the output driver if the boost output is 5% above nominal or will disable both the PFC output driver and reset SS if pulled below 1.5V.

PKLMT: (PFC peak current limit) The threshold for peak limit is 0V. Use a resistor divider from the negative side of the current sense resistor to VREF to level shift this signal to a voltage level defined by the value of the sense resistor and the peak current limit. Peak current limit is reached when PKLMT voltage falls below 0V.

RT: (oscillator charging current) A resistor from RT to GND is used to program oscillator charging current. A resistor between 10kΩ and 100kΩ is recommended.

SS: (soft start) SS is at ground for either enable low or VCC too low conditions. When enabled, SS will charge an external capacitor with a current source. This voltage will be used as the voltage error signal during start-up, enabling the PWM duty cycle to increase slowly. In the event of a disable command or a VCC dropout, SS will quickly discharge to disable the PWM.

PIN DESCRIPTIONS (cont.)

VAOUT: (voltage amplifier output) This is the output of the opamp that regulates output voltage. The voltage amplifier output is internally limited to approximately 5.5V to prevent overshoot.

VCC: (positive supply voltage) Connect to a stable source of at least 20mA between 10V and 17V for normal operation. Bypass VCC directly to GND to absorb supply current spikes required to charge external MOSFET gate capacitances. To prevent inadequate gate drive signals, the output devices will be inhibited unless VCC exceeds the upper under-voltage lockout voltage threshold and remains above the lower threshold.

VFF: (feed-forward signal) RMS signal generated at this pin by mirroring I_{AC} into a single pole external filter.

$$R_{VFF} = \frac{VFF_{MAX}}{\sqrt{2} \bullet \frac{IAC_{MAX}}{2} \bullet 0.9}$$

VSENSE: (voltage amplifier inverting input) This is normally connected to a compensation network and to the boost converter output through a divider network.

VREF: (voltage reference output) VREF is the output of an accurate 7.5V voltage reference. This output is capable of delivering 10mA to peripheral circuitry and is internally short circuit current limited. VREF is disabled and will remain at 0V when V_{CC} is below the UVLO threshold. Bypass VREF to GND with a 0.1µF or larger ceramic capacitor for best stability.

APPLICATION INFORMATION

The UCC3817 is a BiCMOS average current mode boost controller for high power factor, high efficiency preregulator power supplies. Fig. 1 shows the UCC3817 in a 250W PFC preregulator circuit. Off-line switching power converters normally have an input current that is not sinusoidal. The input current waveform will have high harmonic content because current is drawn in pulses at the peaks of the input voltage waveform. An active power factor correction circuit programs the input current to follow the line voltage, forcing the converter to look like a resistive load to the line. A resistive load has 0° phase displacement between the current and voltage waveforms. Power factor can be defined in terms of the phase angle between two sinusoidal waveforms of the same frequency:

$$PF = \cos\Theta$$

Therefore, a purely resistive load would have a power factor of 1. In practice, power factors of 0.999 with THD (total harmonic distortion) less than 3% are possible with a well-designed circuit. Following guidelines are provided to design PFC boost converters using the UCC3817.

Power Stage

L_{BOOST}: The boost inductor value is determined by:

$$L_{BOOST} = \frac{\left(V_{IN(\min)} \bullet D\right)}{\left(\Delta I \bullet f_S\right)}$$

Where D is the duty cycle, ΔI is the inductor ripple current and f_S is the switching frequency. For the example circuit a switching frequency of 100kHz, a ripple current of 875mA, a maximum duty cycle of 0.688 and a minimum input voltage of $85V_{RMS}$ gives us a boost inductor value of about 1mH. The values used in this equation are at the peak of low line, where the inductor current and its ripple are at a maximum.

C_{OUT}: Two main criteria, the capacitance and the voltage rating, dictate the selection of the output capacitor. The value of capacitance is determined by the hold-up time required for supporting the load after input AC voltage is removed. Hold-up is the amount of time that the output stays in regulation after the input has been removed. For this circuit, the desired hold-up time is approximately 16ms. Expressing the capacitor value in terms of output power, output voltage, and hold-up time gives the equation:

$$C_{OUT} = \frac{\left(2 \bullet P_{OUT} \bullet \Delta t\right)}{\left(V_{OUT}{}^2 - V_{OUT(\min)}{}^2\right)}$$

In practice the calculated minimum capacitor value may be inadequate because output ripple voltage specifications limit the amount of allowable output capacitor ESR. Attaining a sufficiently low value of ESR often necessitates the use of a much larger capacitor value than calculated. The amount of output capacitor ESR allowed can be determined by dividing the maximum specified output ripple voltage by the inductor ripple current.

In this design hold-up time was the dominant determining factor and a 220µF, 450V capacitor was chosen for the output voltage level of 385VDC at 250W.

Power Switch Selection

As in any power supply design, tradeoffs between performance, cost and size have to be made. When selecting a power switch it can be useful to calculate the total power

APPLICATION INFORMATION (cont.)

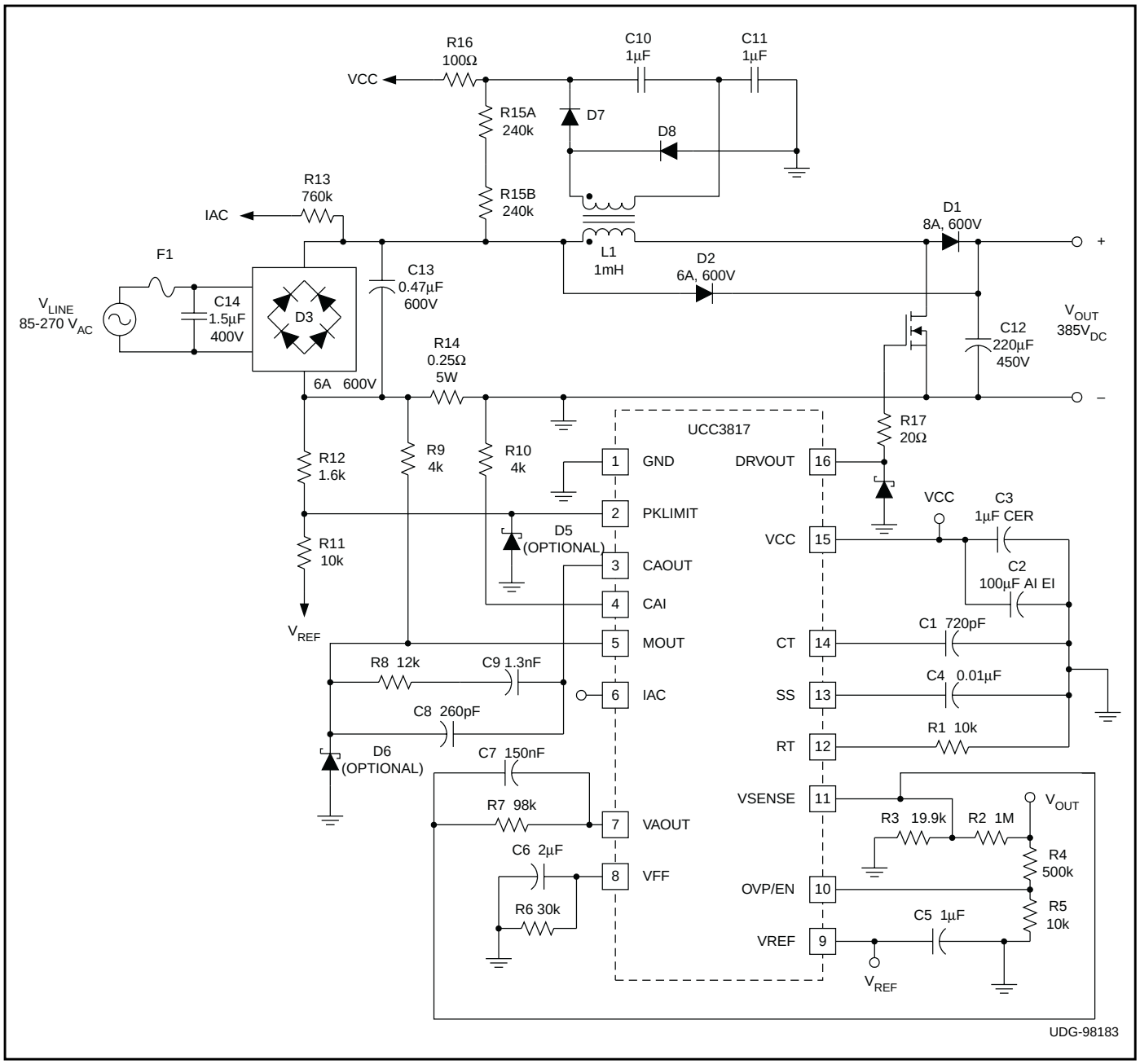

Figure 1. Typical application circuit.

dissipation in the switch for several different devices at the switching frequencies being considered for the converter. Total power dissipation in the switch is the sum of switching loss and conduction loss. Switching losses are the combination of the gate charge loss, C_{OSS} loss and turn-on and turn-off losses:

$$P_{GATE} = Q_{GATE} \bullet V_{GATE} \bullet fs$$

$$P_{COSS} = \frac{1}{2} \bullet C_{OSS} \bullet V^2_{OFF} \bullet fs$$

$$P_{ON} + P_{OFF} = \frac{1}{2} \bullet V_{OFF} \bullet I_L \bullet (t_{ON} + t_{OFF}) \bullet F_S$$

where Q_{GATE} is the total gate charge, V_{GATE} is the gate drive voltage, f_S is the clock frequency, C_{OSS} is the drain source capacitance of the MOSFET, t_{ON} and t_{OFF} are the switching times (estimated using device parameters R_{GATE}, Q_{GD} and V_{TH}) and V_{OFF} is the voltage across the switch during the off time, in this case $V_{OFF} = V_{OUT}$.

Conduction loss is calculated as the product of the $R_{DS(on)}$ of the switch (at the worst case junction temperature) and the square of RMS current:

$$P_{COND} = R_{DS(on)} \bullet K \bullet I^2_{RMS}$$

APPLICATION INFORMATION (cont.)

where K is the temperature factor found in the manufacturer's $R_{DS(on)}$ vs. junction temperature curves.

Calculating these losses and plotting against frequency gives a curve which enables the designer to determine either which manufacturer's device has the best performance at the desired switching frequency, or which switching frequency has the least total loss for a particular power switch. In this example the switch was chosen as the best trade off between performance, availability and cost. An excellent review of this procedure can be found in the Unitrode Power Supply Design Seminar SEM1200, Topic 6, Design Review: 140W, [*Multiple Output High Density DC/DC Converter*].

Multiplier

The output of the multiplier of the UCC3817 is a signal representing the desired input line current. It is an input to the current amplifier, which programs the current loop to control the input current to give high power factor operation. As such, the proper functioning of the multiplier is key to the success of the design. The inputs to the multiplier are VAOUT, the voltage amplifier error signal, IAC, a representation of the input rectified AC line voltage, and an input voltage feedforward signal, V_{FF}. The output of the multiplier, I_{MO}, can be expressed:

$$I_{MO} = \frac{I_{AC} \bullet (VAOUT - 1)}{K \bullet V_{FF}{}^2}$$

where K is a constant typically equal to 1.

The I_{AC} signal is obtained through a high value resistor connected between the rectified AC line and the IAC pin of the UCC3817. This resistor is sized to give the maximum I_{AC} current at high line. For this device the maximum I_{AC} current is about 500µA. A higher current than this can drive the multiplier out of its linear range. A smaller current level will be functional, but noise can become an issue, especially at low input line. Assuming a universal line operation of 85 to 265VAC gives a resistor value of 750kΩ Because of voltage rating constraints of standard 1/4W resistors, use a combination of lower value resistors connected in series to give the 750kΩ value and distribute the high voltage across two or more resistors.

The current through the I_{AC} resistor is mirrored internally to the VFF pin where it is filtered to produce a voltage feedforward signal proportional to line voltage and free of a 120Hz ripple component. This second harmonic ripple component at the VFF pin is one of the major contributors to harmonic distortion in the system, so adequate filtering is crucial. Refer to Unitrode Power Supply Design Seminar, SEM-700 Topic 7, [*Optimizing the Design of a High Power Factor Preregulator*.] Assuming that an allocation of 1.5% total harmonic distortion from this input is allowed, and that the second harmonic ripple is 66% of the input AC line voltage, the amount of attenuation required by this filter is:

$$\frac{1.5\%}{66\%} \; or \; .022$$

A ripple frequency (f_R)of 120Hz and an attenuation of .022 gives us a single pole filter with:

$$fp = 120\,Hz \bullet 0.022 = 2.6\,Hz$$

The range of this input to the multiplier should be 0.5V to 5.5V over the line input range. Therefore the filter resistor should be sized accordingly. Maximum I_{AC} current is 500µA, mirrored 2:1 to VFF becomes 250µA. The DC output is 90% of the RMS value of this half sine wave, or 159µA. So the filter resistor should be equal to the voltage swing of the input to the multiplier divided by the DC current or:

$$\frac{5V}{159\,\mu A} = 31.44k\Omega$$

Select 30kΩ for a standard value. Solving for the capacitor value:

$$C_f = \frac{1}{2\pi(30k)(2.6Hz)} = 2\mu F$$

This results in a single pole filter, which will adequately attenuate the harmonic distortion and also meet the DC requirement of the proper voltage swing across line conditions.

The R_{MO} resistor is sized to match the maximum current through the sense resistor to the maximum multiplier current. The maximum multiplier current, or $I_{MO(max)}$, can be determined by the equation:

$$I_{MO(\max)} = \frac{I_{AC}@V_{IN(\min)} \bullet \left(V_{EA(\max)} - 1V\right)}{K \bullet V_{FF}{}^2{}_{(\min)}}$$

$I_{MO(max)}$ for this design is approximately 315µA. The R_{MO} resistor can then be determined by

$$R_{MO} = \frac{V_{RS}}{I_{MO(\max)}}$$

In this example R_{MO} is equal to 3.91kΩ

Voltage Loop

The second major source of harmonic distortion is the ripple on the output capacitor at the second harmonic of the line frequency. This ripple is fed back through the error amplifier and appears as a 3rd harmonic ripple at the

APPLICATION INFORMATION (cont.)

input to the multiplier. The voltage loop must be compensated not just for stability but also to attenuate the contribution of this ripple to the total harmonic distortion of the system. Refer to Fig. 2.

The gain of the voltage amplifier, G_{VA}, can be determined by first calculating the amount of ripple present on the output capacitor. The peak value of the second harmonic voltage is given by the equation:

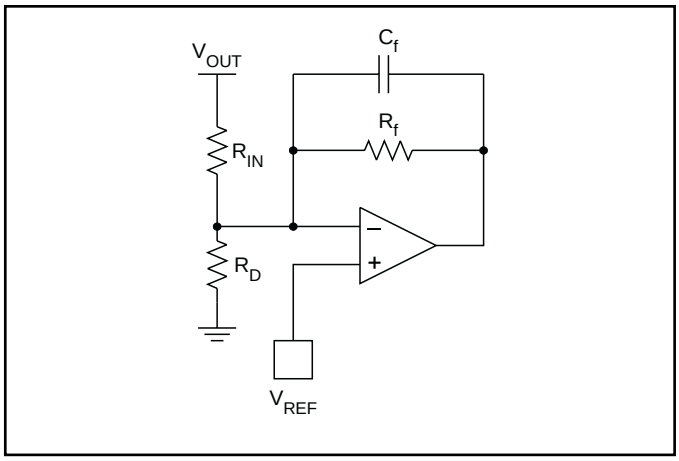

Figure 2. Voltage amplifier configuration.

$$V_{OPK} = \frac{P_{IN}}{(2\pi \bullet f_R \bullet C_{OUT} \bullet V_{OUT})}$$

In this example V_{OPK} is equal to 3.91V. Assuming an allowable contribution of 0.75% (1.5% peak to peak) from the voltage loop to the total harmonic distortion budget we set the gain equal to:

$$G_{VA} = \frac{(\Delta V_{AOUT} \bullet 1.5\%)}{V_{OPK}}$$

where V_{AOUT} is the effective output voltage range of the error amplifier (5.5V for the UCC3817). The network needed to realize this filter is comprised of an input resistor, R_{IN}, and feedback components C_f and R_f. The value of R_{IN} is already determined because of its function as one half of a resistor divider from V_{OUT} feeding back to the voltage amplifier for output voltage regulation. In this case the value was chosen to be 1MΩ. This high value was chosen to reduce power dissipation in the resistor. In practice, the resistor value would be realized by the use of two 500kΩ resistors in series because of the voltage rating constraints of most standard 1/4W resistors. The value of C_f is determined by the equation:

$$C_f = \frac{1}{(2\pi \bullet f_R \bullet G_{VA} \bullet R_{IN})}$$

In this example C_f equals 65nF. Resistor R_f sets the DC gain of the error amplifier and thus determines the frequency of the pole of the error amplifier. The location of the pole can be found by setting the gain of the loop equation to one and solving for the crossover frequency. The frequency, expressed in terms of input power, can be calculated by the equation:

$$f_{VI}^2 = \frac{P_{IN}}{(2\pi \bullet \Delta V_{AOUT} \bullet V_{OUT} \bullet R_{IN} \bullet C_{OUT} \bullet C_f)}$$

f_{VI} for this converter is 15Hz. A derivation of this equation can be found in the Unitrode Power Supply Design Seminar SEM1000, Topic 1, [*A 250kHz, 500W Power Factor Correction Circuit Employing Zero Voltage Transitions*].

Solving for R_f becomes:

$$R_f = \frac{1}{(2\pi \bullet F_{VI} \bullet C_f)}$$

or R_f equals 150kΩ

Current Loop

The gain of the power stage is:

$$G_{ID}(s) = \frac{(V_{OUT} \bullet R_{SENSE})}{(s \bullet L_{BOOST} \bullet V_P)}$$

R_{SENSE} has been chosen to give the desired differential voltage for the current sense amp at the desired current limit point. In this example a current limit of 4A and a reasonable differential voltage to the current amp of 1V gives a R_{SENSE} value of 0.25Ω. V_P in this equation is the voltage swing of the oscillator ramp, 4V for the UCC3817. Setting the crossover frequency of the system to 1/10th of the switching frequency, or 10kHz, requires a power stage gain at that frequency of 0.383. In order for the system to have a gain of 1 at the crossover frequency, the current amplifier needs to have a gain of $1/G_{PS}$ at that frequency. G_{EA}, the current amp gain is then:

$$G_{EA} = \frac{1}{G_{ID}} = \frac{1}{0.383} = 2.611$$

Refer to Fig. 3. R_I is the R_{MO} resistor, previously calculated to be 3.9kΩ. The gain of the current amp is R_f/R_I, so multiplying R_I by G_{EA} gives the value of R_f, in this case approximately 10kΩ. Setting a zero at the crossover frequency and a pole at half the switching frequency completes the current loop compensation.

$$C_Z = \frac{1}{2 \bullet \pi \bullet R_f \bullet f_C}$$

$$C_P = \frac{1}{2 \bullet \pi \bullet R_f \bullet \frac{fs}{2}}$$

APPLICATION INFORMATION (cont.)

The UCC3817 current amplifier has the input from the multiplier applied to the inverting input. This change in architecture from previous Unitrode PFC controllers improves noise immunity in the current amplifier. It also adds a phase inversion into the control loop. The UCC3817 takes advantage of this phase inversion to implement leading-edge duty cycle modulation. Synchronizing a boost PFC controller to a downstream DC to DC controller reduces the ripple current seen by the bulk capacitor between stages, reducing capacitor size and cost and reducing EMI. This is explained in greater detail in a following section. The UCC3817 current amplifier configuration is shown in Fig. 4.

Start Up Current

The UCC3818 version of the device is intended to have VCC connected to a 12V supply voltage. The UCC3817 has an internal shunt regulator enabling the device to be powered from bootstrap circuitry as shown in the typical application circuit of Fig. 1. The current drawn by the UCC3817 during under-voltage lockout, or start up current, is typically 150µA. Once VCC is above the UVLO threshold, the device is enabled and will draw 4mA typically. A resistor connected between the rectified AC line voltage and the VCC pin provides current to the shunt regulator during power-up. Once the circuit is operational the bootstrap winding of the inductor will provide the VCC voltage. Sizing of the start-up resistor is determined by the start-up time requirement of the system design.

$$I_{STARTUP} = C \bullet \frac{\Delta V}{\Delta t}$$

$$R = \frac{V_{RMS}}{I_{STARTUP}}$$

Where I is the start-up current, C is the total capacitance at the VCC pin, V is the UVLO threshold and t is the allowed startup time.

Assuming a 1 second allowed start-up time, a 16V UVLO threshold, and a total VCC capacitance of 100µF, a resistor value of 75kΩ is required at a low line input voltage of $80V_{RMS}$. The IC start-up current is sufficiently small as to be ignored in sizing the start up resistor.

Leading Edge Modulation

The UCC3817 uses leading edge modulation as opposed to traditional trailing edge modulation. Leading edge modulation in a boost PFC front end synchronized to a downstream buck converter using trailing edge modulation greatly diminishes the ripple current in the boost bulk capacitor. Refer to Fig. 5.

In a conventional synchronized system with both regulators utilizing trailing edge modulation, Q1 and Q2 would be turned on at the same time. All of the charging current for L1 would go to ground through Q1 and all of the output current would come from the bulk capacitor through Q2. Similarly, when both FETs are turned off, all the inductor current will flow into the bulk capacitor and all of the output current will be supplied by the freewheeling diode D2. By using leading edge modulation on the boost converter the FETs are turned on and off alternately. Refer to Fig. 6. When Q1 is off and Q2 is on, some of the output current is supplied through diode D1 by the boost inductor L1. When Q1 is on and Q2 off, the charge on the bulk capacitor is held up by the blocking action of Q2. It can be seen that the RMS current through the bulk capacitor is minimized when t1 and t3 are maximized with respect to t2 and t4. This greatly reduces the ripple current seen by the bulk capacitor, reducing stress and increasing reliability.

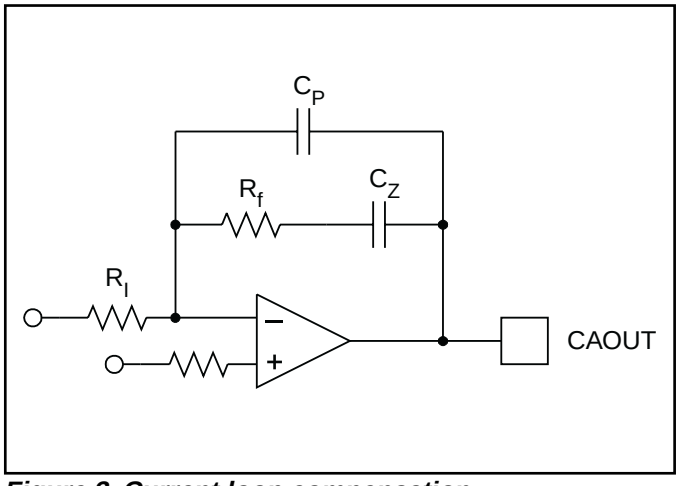

Figure 3. Current loop compensation.

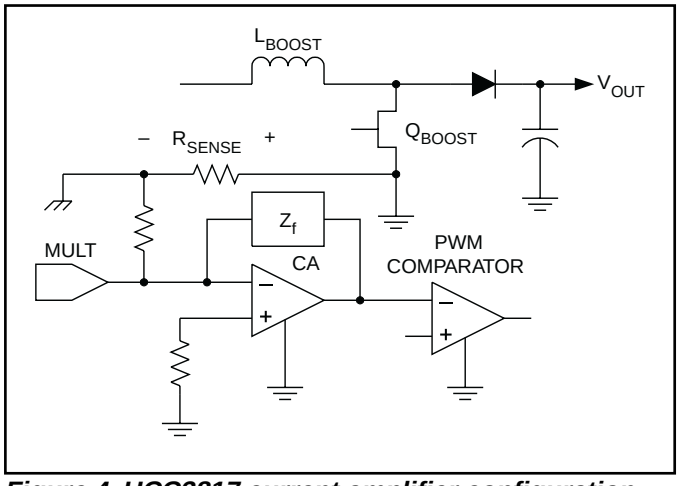

Figure 4. UCC3817 current amplifier configuration.

APPLICATION INFORMATION (cont.)

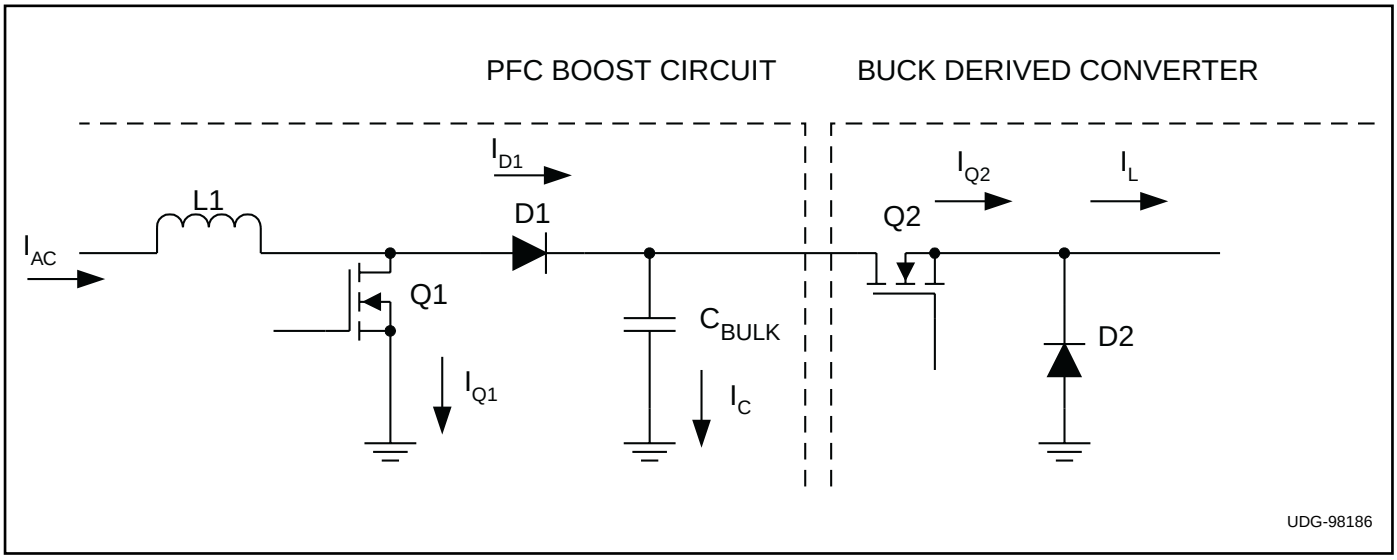

Figure 5. Leading edge modulation.

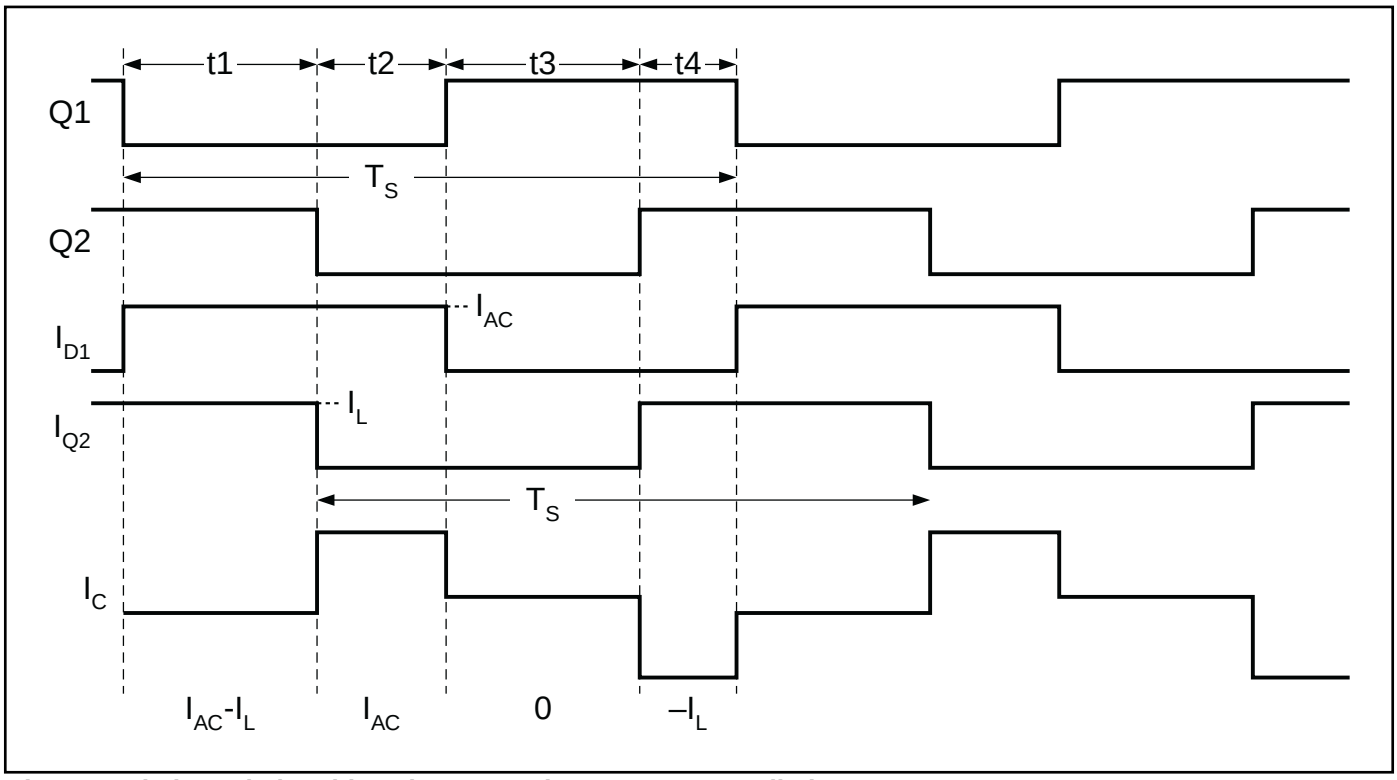

Figure 6. Timing relationships show capacitor current cancellation.

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