MP1208/9/10

Microprocessor Compatible
Double-Buffered, 12-Bit
Digital-to-Analog Converter

EXAR

FEATURES

- Lower Data Bus Feedthrough @ $\overline{CS}$ = 1
- Stable, More Accurate Segmented DAC Approach
- Ultra Stable
  - 0.2 ppm/°C Linearity Tempco
  - 2 ppm/°C Max Gain Error Tempco
- Low Sensitivity to Amplifier V_{OS}
- Low Output Capacitance
- C_{OUT1} = 80 pF at Full Scale, Gives Fastest Settling Times, and Larger Stable Bandwidth capability
- Lower Glitch Energy
- Four Quadrant Multiplication
- Guaranteed Monotonicity
- Low Feedthrough Error
- Low Power Consumption
- TTL/5 V CMOS Compatible
- Latch-Up Free
- -40°C to +85°C Operation
- 8-Bit Bus Version: MP1230A/1231A/1232A

GENERAL DESCRIPTION

The MP1208/09/10 series are 12-bit Digital-to-Analog Converters with an 8/4 bit latched input interface that provide maximum flexibility in interfacing to µP data bus. All data loading and data transfer operations are identical to the WRITE cycle of a static RAM.

The MP1208 series use a unique circuit which significantly reduces transients in the supplies during DATA bus transitions at $\overline{CS}$ = 1.

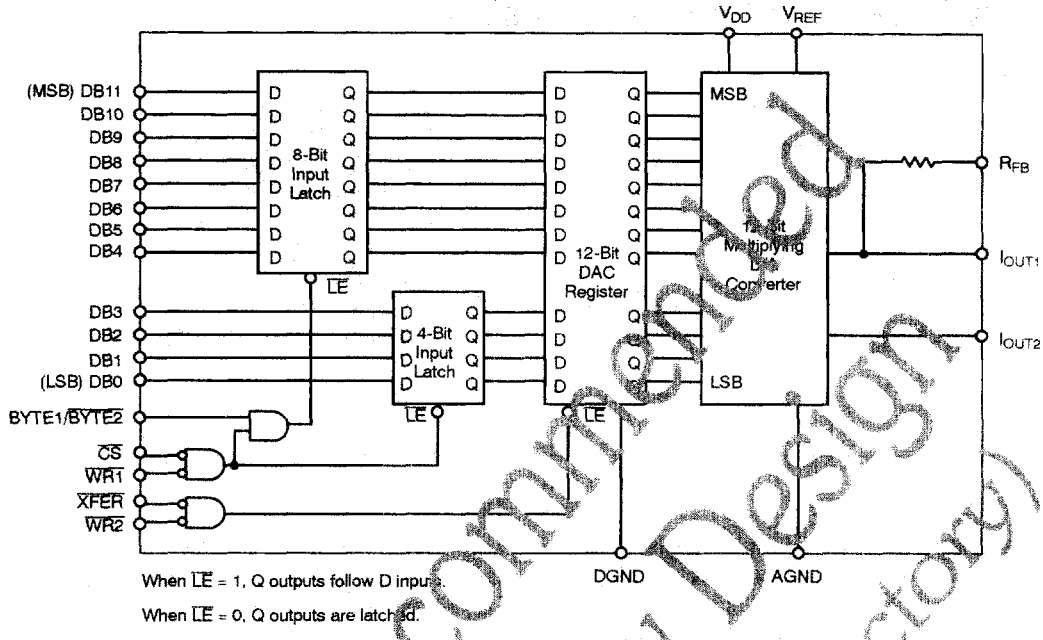
The MP1208 series are manufactured using advanced thin film resistors on a double metal CMOS process. The MP1208 series incorperates a unique bit decoding technique yielding lower glitch, higher speed and excellent accuracy over temperature and time. 12-bit linearity is achieved with minimal trimming. Outstanding features include:

Stability: Both integral and differential linearity are rated at 0.2 ppm/°C typical, and monotonicity is guaranteed over the entire temperature range (-40 to +85°C). Scale factor is a low 2 ppm/°C maximum.

Low Output Capacitance: Due to smaller MOSFET switch geometries allowed by decoding, the output capacitance at I_{OUT1} and I_{OUT2} are a low 80pF / 40pF and 25pF / 65 pF for the conditions of full/zero scale. This is over two times less than the National DAC 1208 Series. Lower capacitance allows the MP1208 series to achieve faster CMOS DAC settling times; less than 1 µsec for a 10 V step to 0.01% when utilizing a high speed output amplifier. Larger output amplifier bandwidths are available, for a given amplifier loop gain, because a smaller feedback "zero" compensating capacitor is required to offset the smaller I_{OUT} capacitance.

Low Sensitivity to Output Amplifier Offset: 4 quadrant multiplying CMOS DACs provide an output current into the virtual ground of an op amp. The additional linearity error incurred by amplifier offset is reduced by a factor of 2 in the MP1208 series over conventional R-2R DACs, to 330µV per millivolt of offset.

SIMPLIFIED BLOCK DIAGRAM



When $\overline{LE}$ = 1, Q outputs follow D inputs.

When $\overline{LE}$ = 0, Q outputs are latched.

ORDERING INFORMATION

Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (% FSR)
Plastic Dip	-40 to +85°C	MP1208JN	±2	±2	±0.4
Plastic Dip	-40 to +85°C	MP1209JN	±1	±1	±0.4
Plastic Dip	-40 to +85	MP1208KN	±1/2	±3/4	±0.4

*Contact factory for non-compliant military processing