DOUBLE DATA RATE (DDR) SDRAM

MT46V8M16 – 2 MEGX16X4 BANKS

For the latest data sheet revisions, please refer to the Micron Website: www.micron.com/dramds

Features

- 200 MHz Clock, 400 Mb/s/p data rate
- Bidirectional data strobe (DQS) transmitted/ received with data, i.e., source-synchronous data capture
- Internal, pipelined double-data-rate (DDR) architecture; two data accesses per clock cycle
- Differential clock inputs (CK and CK#)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- DLL to align DQ and DQS transitions with CK
- Four internal banks for concurrent operation
- Data mask (DM) for masking write data
- Programmable burst lengths: 2, 4, or 8
- Concurrent Auto Precharge option supported
- Auto Refresh and Self Refresh Modes
- ^{t}RAS lockout (^{t}RAP = ^{t}RCD)
- Single CAS Latency CL=3

Options	Marking
• Configuration	
8 Meg x 16 (4 Meg x 16 x 4 banks)	8M816
• Plastic Package	
66-Pin TSOP (400 mil with 0.65mm pin pitch)	TG
66-Pin TSOP (400 mil with 0.65mm pin pitch) Lead Free	P
• Timing - Cycle Time	
5ns @ CL = 3	-5G
6ns @ CL = 3	-6G
• Self Refresh	
Standard	none

General Description

The DDR SDRAM is a high-speed CMOS, dynamic random-access memory that operates at a frequency of 200 MHz (^{t}CK=5ns) with a peak data transfer rate of 400Mb/s/p DDR400 continues to use the 2*n*-prefetch architecture.

The standard DDR266 data sheet provides a complete description of DDR SDRAM functionality and operating modes. It provides full specifications and functionality unless specified herein. This addendum data sheet concentrates on the critical parameters and key differences required to support the enhanced DDR point to point speeds.

Table 1: Configuration

ARCHITECTURE	16 MEG X 8
Configuration	4 Meg x 8 x 4 banks
Refresh Count	4K
Row Addressing	4K (A0-A11)
Bank Addressing	4 (BA0, BA1)
Column Addressing	1K (A0-A9)

Table 2: Key Timing Parameters

SPEED GRADE	CLOCK RATE CL = 3[1]	DATA-OUT WINDOW[2]	ACCESS WINDOW	DQS-DQ SKEW
-5G	200 MHz	1.5ns	±0750ps	+500ps
-6G	166 MHz	1.9ns	±0750ps	+500ps

NOTE:
1. CL = CAS (Read) Latency
2. With a 50/50 clock duty cycle

Figure 1: 66-pin TSOP Package Dimension

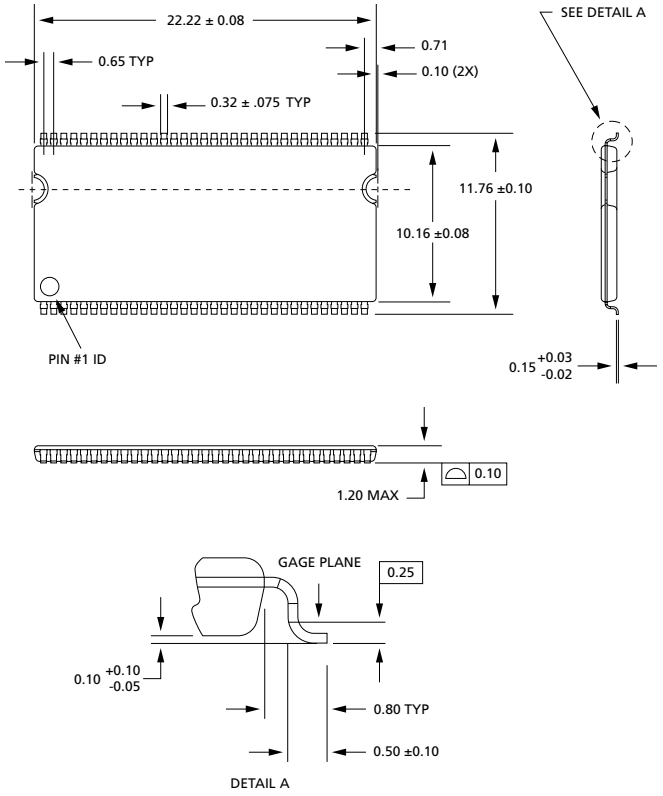
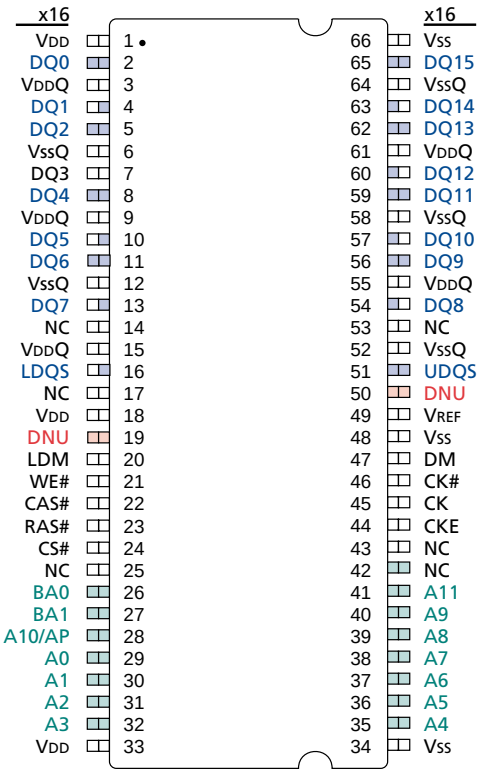


Figure 2: 66-pin TSOP Package Pin Assignment



NOTE:

1. All dimensions in millimeters.
2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.25mm per side.

Table 3: Pin Descriptions

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
45, 46	CK, CK#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQs and DQS) is referenced to the crossings of CK and CK#.
44	CKE	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates the internal clock, input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE is synchronous for POWER-DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit and for disabling the outputs. CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK, CK#, and CKE) are disabled during POWER-DOWN. Input buffers (excluding CKE) are disabled during SELF REFRESH. CKE is an SSTL_2 input but will detect an LVCMOS LOW level after V_{DD} is applied and until CKE is first brought high. After CKE is brought high it becomes an SSTL_2 input only.
24	CS#	Input	Chip Select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
23, 22, 21	RAS#,CAS#, WE#	Input	Command Inputs: RAS#, CAS#, and WE# (along with CS#) define the commandbeingentered.
20, 47	DM	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins.
26, 27	BA0, BA1	Input	Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
29-31 32, 35, 36 37, 38, 39 40, 28, 41	A0, A1, A2 A3, A4, A5 A6, A7, A8 A9, A10, A11	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA0, BA1) or all banks (A10 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which mode register (mode register or extended mode register) is loaded during the LOAD MODE REGISTER command.
2, 4, 5, 7, 8, 10, 11, 13, 54, 56, 57, 59, 60, 62, 63, 65	DQ0-15	I/O	Data Input/Output.
16, 51	LDQS/UDQS	I/O	Data Strobe: Output with read data, input with write data. DQS is edge-aligned with read data, centered in write data. It is used to capture data.
14, 17, 25, 43, 53	NC	-	No Connect: These pins should be left unconnected.
19, 50	DNU	-	Do Not Use: Must float to minimize noise on Vref
3, 9, 15, 55, 61	$V_{DD}Q$	Supply	DQ Power Supply: Isolated on the die for improved noise immunity.
6, 12, 52, 58, 64	$V_{SS}Q$	Supply	DQ Ground. Isolated on the die for improved noise immunity.
1, 18, 33	V_{DD}	Supply	Power Supply.
34, 48, 66	V_{SS}	Supply	Ground.
49	V_{REF}	Supply	SSTL_2 reference voltage.

Read Latency

The READ latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The latency should be set to 3 clocks, as shown in the CAS Latency Diagram and Mode Register Definition Diagram.

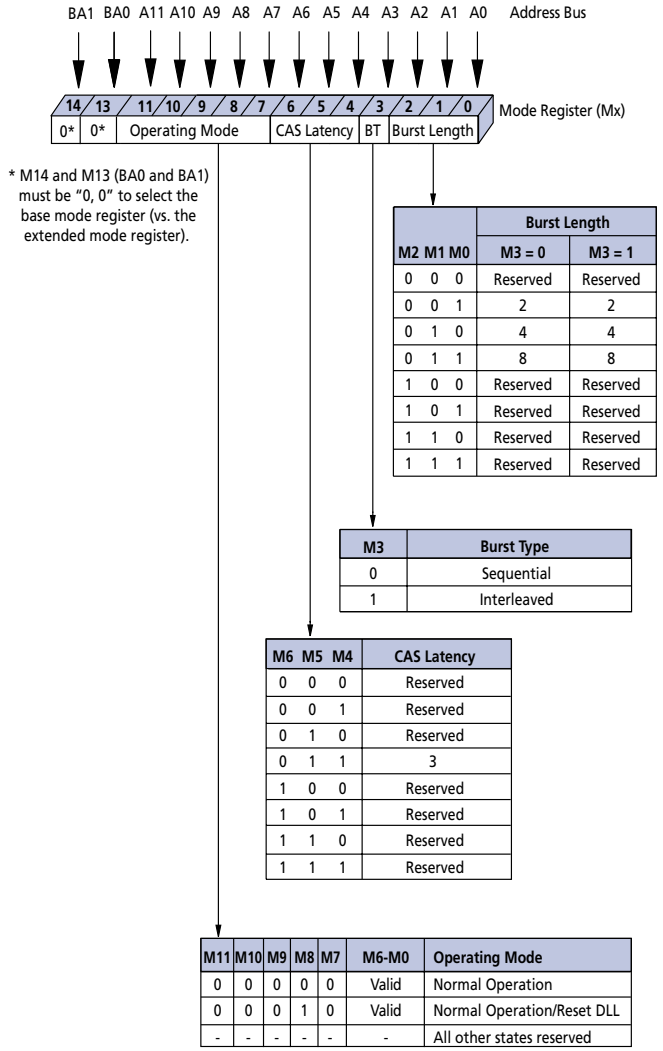
If a READ command is registered at clock edge *n*, and the latency is *m* clocks, the data will be available nominally coincident with clock edge *n* + *m*.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Table 4: CAS Latency (CL)

SPEED	ALLOWABLE OPERATING CLOCK FREQUENCY (MHz)		
	CL = 3	CL = 2.5	CL = 2
-5G	133 MHz ≤ f ≤ 200MHz	—	—
-6G	133 MHz ≤ f ≤ 166MHz	—	—

Figure 3: Mode Register Definition Diagram



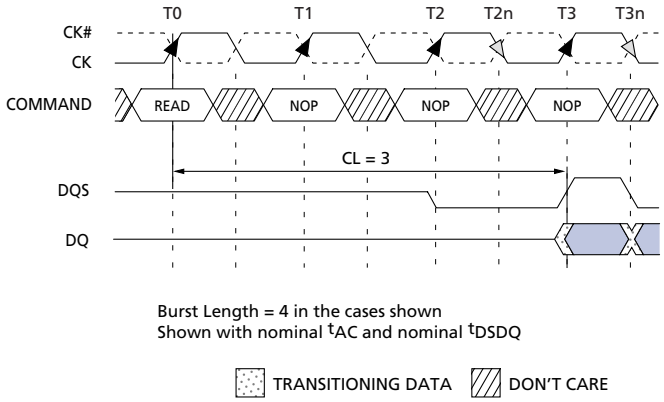
	Burst Length	
M2 M1 M0	M3 = 0	M3 = 1
0 0 0	Reserved	Reserved
0 0 1	2	2
0 1 0	4	4
0 1 1	8	8
1 0 0	Reserved	Reserved
1 0 1	Reserved	Reserved
1 1 0	Reserved	Reserved
1 1 1	Reserved	Reserved

M3	Burst Type
0	Sequential
1	Interleaved

M6 M5 M4	CAS Latency
0 0 0	Reserved
0 0 1	Reserved
0 1 0	Reserved
0 1 1	3
1 0 0	Reserved
1 0 1	Reserved
1 1 0	Reserved
1 1 1	Reserved

M11	M10	M9	M8	M7	M6-M0	Operating Mode
0	0	0	0	0	Valid	Normal Operation
0	0	0	1	0	Valid	Normal Operation/Reset DLL
-	-	-	-	-	-	All other states reserved

Figure 4: Example CAS Latency Diagram with CL=3



Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

VDD Supply Voltage
Relative to Vss ..... -1V to +3.6V
VDDQ Supply Voltage
Relative to Vss ..... -1V to +3.6V
VREF and Inputs Voltage
Relative to Vss ..... -1V to +3.6V
I/O Pins Voltage
Relative to Vss ..... -0.5V to VDDQ +0.5V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

Table 5: DC Electrical Characteristics and Operating Conditions

0°C ≤ T_A ≤ +70°C; Notes: 1–5, 16, Refer to DDR266 Data Sheet, for all notes except 53 below.

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage -5G	VDD	2.6	2.83	V	36, 41, 53
I/O Supply Voltage -5G	VDDQ	2.6	2.83	V	36, 41, 44,53
Supply Voltage -6G	VDD	2.5	2.7	V	36, 41, 53
I/O Supply Voltage -6G	VDDQ	2.5	2.7	V	36, 41, 44,53
I/O Reference Voltage	VREF	0.49 x VDDQ	0.51 x VDDQ	V	6, 44
I/O Termination Voltage (system)	VTT	VREF - 0.04	VREF + 0.04	V	7, 44
Input High (Logic 1) Voltage	VIH(DC)	VREF + 0.15	VDD + 0.3	V	28
Input Low (Logic 0) Voltage	VIL(DC)	-0.3	VREF - 0.15	V	28
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ VDD, VREF Pin 0V ≤ VIN ≤ 1.35V (All other pins not under test = 0V)	II	-2	2	µA	
OUTPUT LEAKAGE CURRENT (DQs are disabled; 0V ≤ VOUT ≤ VDDQ)	IOZ	-5	5	µA	
OUTPUT LEVELS: Full drive option - High Current (VOUT = VDDQ - 0.373V, minimum VREF, minimum VTT)	IOH	-16.8	-	mA	37, 39
	IOL	-16.8	-	mA	
OUTPUT LEVELS: Reduced drive option High Current (VOUT = VDDQ - 0.763V, minimum VREF, minimum VTT)	IOHR	-9	-	mA	38, 39
Low Current (VOUT = 0.763V, maximum VREF, maximum VTT)	IOLR	9	-	mA	

Note 53. This is the DC voltage supplied at the DRAM and is inclusive of all noise up to 20MHz. Any noise above 20MHz at the DRAM generated from any source other than the DRAM itself may not exceed the DC voltage range.

Table 6: AC Input Operating Conditions

0°C ≤ T_A ≤ +70°C; Notes: 1–5, 16, Refer to DDR266 Data Sheet for all notes.

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	$V_{IH(AC)}$	V_{REF} + 0.310	-	V	14, 28, 40
Input Low (Logic 0) Voltage	$V_{IL(AC)}$	-	V_{REF} - 0.310	V	14, 28, 40
I/O Reference Voltage	$V_{REF(AC)}$	0.49 x $V_{DD}Q$	0.51 x $V_{DD}Q$	V	6

Table 7: Capacitance (x16 TSOP)

Note: 13; Refer to DDR266 Data Sheet for all notes.

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Delta Input/Output Capacitance: DQ0-DQ7 (x8)	DC_{IO}	–	0.50	pF	24
Delta Input Capacitance: Command and Address	DC_{I1}	–	0.50	pF	29
Delta Input Capacitance: CK, CK#	DC_{I2}	–	0.25	pF	29
Input/Output Capacitance: DQs, DQS, DM	C_{IO}	4.0	5.0	pF	
Input Capacitance: Command and Address	C_{I1}	2.0	3.0	pF	
Input Capacitance: CK, CK#	C_{I2}	2.0	3.0	pF	
Input Capacitance: CKE	C_{I3}	2.0	3.0	pF	

Table 8: Electrical Characteristics and Recommended AC Operating Conditions

0°C ≤ T_A ≤ +70°C; Notes: 1-5, 14–17, 33, 46; Refer to DDR266 Data Sheet for all notes.

AC CHARACTERISTICS		-5G		-6G			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Access window of DQs from CK/CK#	^tAC	-0.75	+0.75	-0.75	+0.75	ns	
CK high-level width	^tCH	0.45	0.55	0.45	0.55	^tCK	30
CK low-level width	^tCL	0.45	0.55	0.45	0.55	^tCK	30
Clock cycle time CL=3	^tCK	5	13	6	13	ns	45, 52
DQ and DM input hold time relative to DQS	^tDH	0.6		0.6		ns	26, 31
DQ and DM input setup time relative to DQS	^tDS	0.6		0.6		ns	26, 31
DQ and DM input pulse width (for each input)	^tDIPW	1.75		2		ns	31
Access window of DQS from CK/CK#	^tDQSCK	-0.75	+0.75	-0.75	+0.75	ns	
DQS input high pulse width	^tDQSH	0.4		0.4		^tCK	
DQS input low pulse width	^tDQSL	0.4		0.4		^tCK	
DQS-DQ skew, DQS to last DQ valid, per group, per access	^tDQSQ		0.5		0.5	ns	25, 26
Write command to first DQS latching transition	^tDQSS	0.75	1.25	0.75	1.25	^tCK	
DQS falling edge to CK rising - setup time	^tDSS	0.25		0.25		^tCK	
DQS falling edge from CK rising - hold time	^tDSH	0.25		0.25		^tCK	
Half clock period	^tHP	^tCH, ^tCL		^tCH, ^tCL		ns	34
Data-out high-impedance window from CK/CK#	^tHZ		+0.50		+0.6	ns	18, 42
Data-out low-impedance window from CK/CK#	^tLZ	-0.50		-0.6		ns	18, 43
Address and control input hold time (slew rate = 1V/ns)	^tIH_F	0.9		1.1		ns	
Address and control input setup time (slew rate = 1V/ns)	^tIS_F	0.9		1.1		ns	
Address and Control input pulse width (for each input)	^tIPW	2.2		2.2		ns	14
LOAD MODE REGISTER command cycle time	^tMRD	3		3		^tCK	
DQ-DQS hold, DQS to first DQ to go non-valid, per access	^tQH	^tHP -^tQHS			^tHP -^tQHS	ns	25, 26
Data Hold Skew Factor	^tQHS		0.55		0.6	ns	
ACTIVE to READ with Auto precharge command	^tRAP	20		20		ns	
ACTIVE to PRECHARGE command	^tRAS	40	70,000	40	70,000	ns	35
ACTIVE to ACTIVE/AUTO REFRESH command period	^tRC	60		60		ns	
AUTO REFRESH command period	^tRFC	66		66		ns	50
ACTIVE to READ or WRITE delay	^tRCD	20		20		ns	
PRECHARGE command period	^tRP	20		20		ns	
DQS read preamble	^tRPRE	0.9	1.1	0.9	1.1	^tCK	42
DQS read postamble	^tRPST	0.4	0.6	0.4	0.6	^tCK	
ACTIVE bank *a* to ACTIVE bank *b* command	^tRRD	10		12		ns	
DQS write preamble	^tWPRE	0.25		0.25		^tCK	
DQS write preamble setup time	^tWPRES	0		0		ns	20, 21
DQS write postamble	^tWPST	0.4	0.6	0.4	0.6	^tCK	19
Write recovery time	^tWR	15		15		ns	
Internal WRITE to READ command delay	^tWTR	1		1		^tCK	
Data valid output window (DVW)	N/A	^tQH - ^tDQSQ				ns	25
REFRESH to REFRESH command interval	^tREFC		140.6		140.6	µs	23
Average periodic refresh interval	^tREFI		15.6		15.6	µs	23
Terminating voltage delay to V_{DD}	^tVTD	0		0		ns	
Exit SELF REFRESH to non-READ command	^tXSNR	75		75		ns	
Exit SELF REFRESH to READ command	^tXSRD	200		200		^tCK	

Table 9: IDD Specifications and Conditions (x16; -5G)

0°C ≤ T_A ≤ +70°C; Notes: 1-5, 14–17, 33, 46; Refer to DDR266 Data Sheet for all notes.

PARAMETER/CONDITION	SYMBOL	MAX -5G	MAX -6G	UNITS	NOTES
OPERATING CURRENT: One bank; Active-Precharge; $^tRC = ^tRC$ (MIN); $^tCK = ^tCK$ (MIN); DQ, DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles	IDD0	130		mA	22, 48
OPERATING CURRENT: One bank; Active-Read-Precharge; Burst = 4; $^tRC = ^tRC$ (MIN); $^tCK = ^tCK$ (MIN); IOUT = 0mA; Address and control inputs changing once per clock cycle	IDD1	145		mA	22, 48
PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; Power-down mode; $^tCK = ^tCK$ (MIN); CKE = (LOW)	IDD2P	4		mA	23, 32, 50
IDLE STANDBY CURRENT: CS# = HIGH; All banks are idle; $^tCK = ^tCK$ (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle. VIN = VREF for DQ, DQS, and DM	IDD2F	60		mA	51
ACTIVE POWER-DOWN STANDBY CURRENT: One bank active; Power-down mode; $^tCK = ^tCK$ (MIN); CKE = LOW	IDD3P	45		mA	23, 32, 50
ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; One bank active; $^tRC = ^tRAS$ (MAX); $^tCK = ^tCK$ (MIN); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	IDD3N	70		mA	22
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; $^tCK = ^tCK$ (MIN); IOUT = 0mA	IDD4R	165		mA	22, 48
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; $^tCK = ^tCK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle	IDD4W	200		mA	22
AUTO REFRESH BURST CURRENT: $^tRC = ^tRFC$(MIN)	IDD5	270		mA	50
AUTO REFRESH BURST CURRENT: ^tRFC = 7.8us,	IDD5A	6		mA	27, 50
SELF REFRESH CURRENT: CKE ≤ 0.2V; Standard	IDD6	4		mA	11
OPERATING CURRENT: Four bank interleaving READs (Burst = 4) with auto precharge, ^tRC = minimum tRC allowed; $^tCK = ^tCK$ (MIN); Address and control inputs change only during Active READ, or WRITE commands	IDD7	355		mA	22, 49

Data Sheet Designation

Preliminary: This data sheet contains initial characterization limits that are subject to change upon full characterization of production devices.

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