ADVANCE

MICRON

MT58LC64K18D7
64K x 18 SYNCBURST™ SRAM

NEW

SYNCHRONOUS PIPELINED SRAM

SYNCHRONOUS SRAM

64K x 18 SRAM
+3.3V SUPPLY, PIPELINED, BURST
COUNTER AND SINGLE CYCLE DESELECT

FEATURES
- Fast access times: 4.5, 5, 6, 7 and 8ns
- Fast $\overline{OE}$ access time: 5 and 6ns
- Single +3.3V +10%/-5% power supply
- 5V-tolerant I/O
- SNOOZE MODE for reduced power standby*
- Single cycle disable (Pentium™ BSRAM compatible)
- Common data inputs and data outputs
- Individual BYTE WRITE control and GLOBAL WRITE*
- Three chip enables for simple depth expansion and address pipelining*
- Clock controlled, registered, address, data I/O and control for fully pipelined applications
- Internally self-timed WRITE cycle
- WRITE pass-through capability
- Burst control pin (interleaved or linear burst)*
- Automatic power-down for portable applications
- High density, high speed packages
- Low capacitive bus loading
- High 30pF output drive capability at rated access time
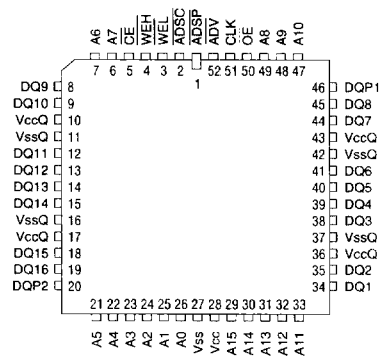- DIMMs also available

OPTIONS MARKING
- Timing
  - 4.5ns access/8ns cycle — -4.5
  - 5ns access/10ns cycle — -5
  - 6ns access/12ns cycle — -6
  - 7ns access/15ns cycle — -7
  - 8ns access/20ns cycle — -8

- Packages
  - 52-pin PLCC — EJ
  - 100-pin TQFP — LG

- Low power — P

- 2V data retention, low power — L
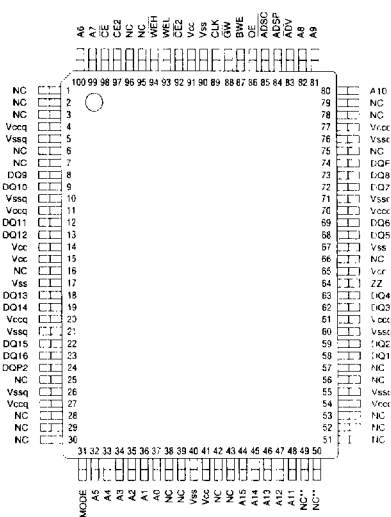
- Part Number Example: MT58LC64K18D7LG-7 P

*TQFP package only

PIN ASSIGNMENT (Top View)

52-Pin PLCC
(SA-1)

100-Pin TQFP
(SB-1)

**Pin 49 is reserved for A16, pin 50 for A17

NEW SYNCHRONOUS PIPELINED SRAM

GENERAL DESCRIPTION

The Micron SyncBurst™ SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using an advanced CMOS process.

The MT58LC64K18D7 SRAM integrates a 64K x 18 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, active LOW chip enable (CE), two additional chip enables for easy depth expansion (CE2, CE2), burst control inputs (ADSC, ADSP, ADV) byte write enables (WEH, WEL, BWE) and global write (GW).

Asynchronous inputs include the output enable (OE), clock (CLK), snooze enable (ZZ) and burst mode (MODE). The data-out (Q), enabled by OE, is also asynchronous. WRITE cycles can be from 1 to 2 bytes wide as controlled by the write control inputs.

Burst operation can be initiated with either address status processor (ADSP) or address status controller (ADSC) input pins. Subsequent burst addresses can be internally generated as controlled by the burst advance pin (ADV).

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles.

Individual byte enables allow individual bytes to be written. WEL controls DQ1-DQ8 and DQP1. WEH controls DQ9-DQ16 and DQP2, conditioned by BWE being LOW. GW LOW causes all bytes to be written. WRITE pass-through makes written data immediately available at the output register during the READ cycle following a WRITE as controlled solely by OE to improve cache system response. The device incorporates an additional pipelined enable register to allow depth expansion without penalizing system performance.

The "L" version of this device has a data retention option which is useful for battery backup mode of operation. Although the part is not guaranteed to operate functionally below Vcc MIN, it will retain data with a minimum of power dissipation.

The MT58LC64K18D7 operates from a +3.3V power supply and all inputs and outputs are TTL-compatible and 5V tolerant. The device is ideally suited for Pentium™ and PowerPC™ pipelined systems and systems that benefit from a very wide high-speed data bus. The device is also ideal in generic 18-, 36- and 72-bit-wide applications.

FUNCTIONAL BLOCK DIAGRAM
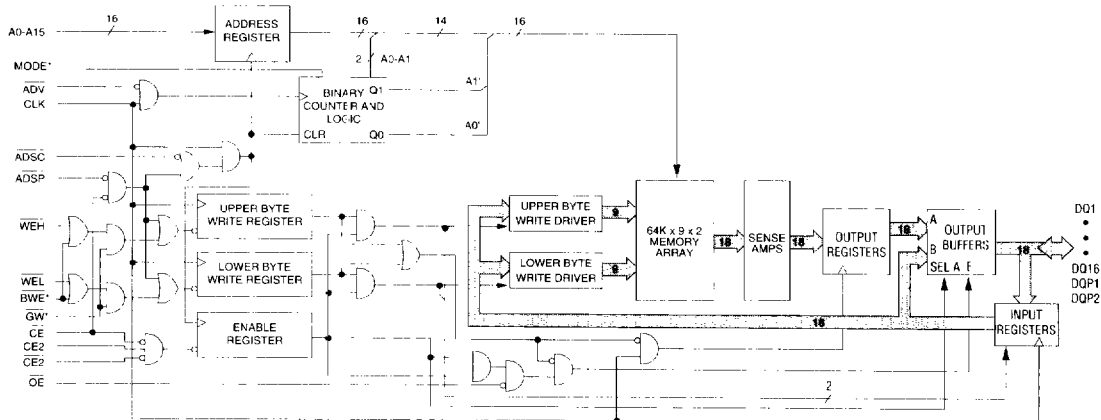
*LG package only

NOTE: 1. The Functional Block Diagram illustrates simplified device operation. See Truth Table, Pin Descriptions and timing diagrams for detailed information.

PIN DESCRIPTIONS

PLCC PINS	TQFP PINS	SYMBOL	TYPE	DESCRIPTION
26, 25, 24, 23, 22, 21, 7, 6, 49, 48, 47, 33, 32, 31, 30, 29	37, 36, 35, 34, 33, 32, 100, 99, 82, 81, 80, 48, 47, 46, 45, 44	A0-A15	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
4, 3	94, 93	W̅E̅H̅, W̅E̅L̅	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A byte write enable is LOW for a WRITE cycle and HIGH for a READ cycle. W̅E̅L̅ controls DQ1-DQ8 and DQP1. W̅E̅H̅ controls DQ9-DQ16 and DQP2. Data I/O are tristated if either of these inputs are LOW.
n/a	87	B̅W̅E̅	Input	Byte Write Enable: This active LOW input permits byte write operations and must meet the setup and hold times around the rising edge of CLK.
n/a	88	G̅W̅	Input	Global Write: This active LOW input allows a full 18-bit WRITE to occur independent of the B̅W̅E̅ and W̅E̅n̅ lines and must meet the setup and hold times around the rising edge of CLK.
51	89	CLK	Input	Clock: This signal registers the address, data, chip enable, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
5	98	C̅E̅	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and conditions internal use of A̅D̅S̅P̅. This input is sampled only when a new external address is loaded.
n/a	92	C̅E̅2̅	Input	Synchronous Chip Enable: This active LOW input is used to enable the device. This input is sampled only when a new external address is loaded.
n/a	97	CE2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device. This input is sampled only when a new external address is loaded.
50	86	O̅E̅	Input	Output Enable: This active LOW asynchronous input enables the data I/O output drivers.
52	83	A̅D̅V̅	Input	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). This pin must be HIGH at the rising edge of the first clock after an A̅D̅S̅P̅ cycle is initiated if a WRITE cycle is desired (to ensure use of correct address).
1	84	A̅D̅S̅P̅	Input	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ is performed using the new address, independent of the byte write enables and A̅D̅S̅C̅ but dependent upon C̅E̅ being LOW.

NEW

SYNCHRONOUS PIPELINED SRAM

PIN DESCRIPTIONS (continued)

PLCC PINS	TQFP PINS	SYMBOL	TYPE	DESCRIPTION
2	85	ADSC	Input	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ or WRITE is performed using the new address if CE is LOW. ADSC is also used to place the chip into power-down state when CE is HIGH.
n/a	31	MODE	Input	Mode: This input selects the burst sequence. A LOW on this pin selects LINEAR BURST. A NC or HIGH on this pin selects INTERLEAVED BURST. Do not alter input state while device is operating.
n/a	64	ZZ	Input	Snooze Enable: This active HIGH asynchronous input causes the device to enter a low-power standby mode in which all data in the memory array is retained.
34, 35, 38, 39, 40, 41, 44, 45, 8, 9, 12, 13, 14, 15, 18, 19	58, 59, 62, 63, 68, 69, 72, 73, 8, 9, 12, 13, 18, 19, 22, 23	DQ1-DQ16	Input/ Output	SRAM Data I/O: Low Byte is DQ1-DQ8. High Byte is DQ9-DQ16. Input data must meet setup and hold times around the rising edge of CLK.
46, 20	74, 24	DQP1, DQP2	Input/ Output	Parity Data I/O: Low Byte Parity is DQP1. High Byte Parity is DQP2.
10, 17, 28, 36, 43	4, 11, 14, 15, 20, 27, 41, 54, 61, 65, 70, 77, 91	Vcc	Supply	Power Supply: +3.3V +10%/-5%
11, 16, 27, 37, 42	5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	Vss	Supply	Ground: GND
	1, 2, 3, 6, 7, 16, 25, 28, 29, 30, 38*, 39*, 42*, 43*, 49, 50, 51, 52, 53, 56, 57, 66, 75, 78, 79, 95, 96	NC	-	No Connect: These signals are not internally connected. These signals may be connected to ground to improve package heat dissipation.

*These pins are reserved as DNU pins (Do Not Use) on the 2 Meg and 4 Meg versions of the SyncBurst family. It is recommended that these pins be left unconnected in any designs to allow for future upgradability.

BURST ADDRESS TABLE (MODE = NC OR HIGH)

First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X00	X...X11	X...X10
X...X10	X...X11	X...X00	X...X01
X...X11	X...X10	X...X01	X...X00

BURST ADDRESS TABLE (MODE = GND)

First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X10	X...X11	X...X00
X...X10	X...X11	X...X00	X...X01
X...X11	X...X00	X...X01	X...X10

PARTIAL TRUTH TABLE FOR WRITE COMMANDS

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{WEL}$	$\overline{WEH}$
READ	H	H	X	X
READ	H	L	H	H
WRITE Low Byte	H	L	L	H
WRITE High Byte	H	L	H	L
WRITE all bytes	H	L	L	L
WRITE all bytes	L	X	X	X

PASS-THROUGH TRUTH TABLE

PREVIOUS CYCLE[1]		PRESENT CYCLE				NEXT CYCLE
OPERATION	$\overline{WEs}$	OPERATION	$\overline{CE}$	$\overline{WEs}$	$\overline{OE}$	OPERATION
Initiate WRITE cycle, all bytes Address = A(n-1), data = D(n-1)	All L[2,3]	Initiate READ cycle Register A(r), Q = D(n-1)	L	H	L	Read D(n)
Initiate WRITE cycle, all bytes Address = A(n-1), data = D(n-1)	All L[2,3]	No new cycle Q = D(n-1)	H	H	L	No carry-over from previous cycle
Initiate WRITE cycle, all bytes Address = A(n-1), data = D(n-1)	All L[2,3]	No new cycle Q = HIGH-Z	H	H	H	No carry-over from previous cycle
Initiate WRITE cycle, one byte Address = A(n-1), data = D(n-1)	One L[2]	No new cycle Q = D(n-1) for one byte	H	H	L	No carry-over from previous cycle

NOTE:
1. Previous cycle may be either BURST or NONBURST cycle.
2. $\overline{BWE}$ is LOW when one or two $\overline{WEn}$ is LOW.
3. $\overline{GW}$ LOW will yield identical results.

NEW

SYNCHRONOUS PIPELINED SRAM

TRUTH TABLE

OPERATION	ADDRESS USED	CE̅	CE̅2̅	CE2	ZZ	ADSP̅	ADSC̅	ADV̅	WRITE̅	OE̅	CLK	DQ
Deselected Cycle, Power-down	None	H	X	X	L	X	L	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	X	L	L	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	H	X	L	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	X	L	L	H	L	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	H	X	L	H	L	X	X	X	L-H	High-Z
SNOOZE MODE, Power-down	None	X	X	X	H	X	X	X	X	X	X	High-Z
READ Cycle, Begin Burst	External	L	L	H	L	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	External	L	L	H	L	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	L	H	L	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	X	X	L	H	H	L	L	X	L-H	D
WRITE Cycle, Continue Burst	Next	H	X	X	L	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	H	L-H	High-Z
READ Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	L	X	L-H	D

NOTE:

1. X means "don't care." H means logic HIGH. L means logic LOW. WRITE̅=L means any one or more byte write enable signals (WEL̅ or WEH̅) and BWE̅ are LOW or GW̅ is LOW. WRITE̅=H means all byte write enable signals are HIGH.
2. WEL̅ enables WRITEs to DQ1-DQ8, DQP1. WEH̅ enables WRITEs to DQ9-DQ16, DQP2.
3. All inputs except OE̅ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
4. Wait states are inserted by suspending burst.
5. For a WRITE operation following a READ operation, OE̅ must be HIGH before the input data required setup time and held HIGH throughout the input data hold time.
6. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
7. ADSP̅ LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals and BWE̅ LOW or GW̅ LOW for the subsequent L-H edge of CLK. Refer to WRITE timing diagram for clarification.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -0.5V to +4.6V
V$_{IN}$ .... -0.5V to +6V
Storage Temperature (plastic) .... -55°C to +150°C
Junction Temperature** .... +150°C
Short Circuit Output Current 100mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See technical note TN-05-14 for more information.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T$_A$ ≤ 70°C; Vcc = +3.3V +10%/-5% unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V$_{IH}$	2.0	5.5	V	1, 2
Input High (Logic 1) Voltage	For MODE and ZZ	V$_{IH}$	2.4	5.5	V	1, 2
Input Low (Logic 0) Voltage		V$_{IL}$	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V$_{IN}$ ≤ Vcc	I$_{LI}$	-1	1	µA	14
Output Leakage Current	Output(s) disabled, 0V ≤ V$_{OUT}$ ≤ Vcc	I$_{LO}$	-1	1	µA	
Output High Voltage	I$_{OH}$ = -4.0mA	V$_{OH}$	2.4		V	1, 11, 17
Output Low Voltage	I$_{OL}$ = 8.0mA	V$_{OL}$		0.4	V	1, 11
Supply Voltage		Vcc	3.135	3.6	V	1

DESCRIPTION	CONDITIONS	SYM	VER	TYP	MAX					UNITS	NOTES
					-4.5	-5	-6	-7	-8		
Power Supply Current: Operating	Device selected; all inputs ≤ V$_{IL}$ or ≥ V$_{IH}$; cycle time ≥ ^{t}KC MIN; Vcc = MAX; outputs open	Icc	ALL	180	425	360	325	275	235	mA	3, 12, 13
Power Supply Current: Idle	Device selected; Vcc = MAX; ADSC, ADSP, GW, BWs, ADV ≥ V$_{IH}$; all inputs ≤ Vss +0.2 or ≥ Vcc -0.2; cycle time ≥ ^{t}KC MIN	Icc1	ALL	30	76	71	66	61	51	mA	12, 13
CMOS Standby	Device deselected; Vcc = MAX; all inputs ≤ Vss +0.2 or ≥ Vcc -0.2; all inputs static; CLK frequency = 0	ISB2	STD	0.5	5	5	5	5	5	mA	12, 13
			P	0.2	2	2	2	2	2	mA	
TTL Standby	Device deselected; Vcc = MAX; all inputs ≤ V$_{IL}$ or ≥ V$_{IH}$; all inputs static; CLK frequency = 0	ISB3	STD	15	25	25	25	25	25	mA	12, 13
			P	8	18	18	18	18	18	mA	
Clock Running	Device deselected; Vcc = MAX; all inputs ≤ Vss +0.2 or ≥ Vcc -0.2; CLK cycle time ≥ ^{t}KC MIN	ISB4	ALL	30	76	71	66	61	51	mA	12, 13

NEW ■ SYNCHRONOUS PIPELINED SRAM

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Control Input Capacitance	$T_A = 25°C$; $f = 1$ MHz	C_I	3	4	pF	4
Input/Output Capacitance (DQ)	$V_{CC} = 3.3V$	C_O	6	8	pF	4
Address and Clock Input Capacitance		C_A	2.5	3	pF	4

THERMAL CONSIDERATIONS

DESCRIPTION	CONDITIONS	SYMBOL	PLCC TYP	TQFP TYP	UNITS	NOTES
Thermal resistance - Junction to Ambient	Still air, soldered on 4.25 x	θ_{JA}	45	20	°C/W	
Thermal resistance - Junction to Case	1.125 inch 4-layer PCB	θ_{JC}	15	1	°C/W	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Note 5) ($0°C \leq T_A \leq 70°C$; $V_{CC} = +3.3V +10\%/-5\%$)

DESCRIPTION	SYM	-45 MIN	-45 MAX	-5 MIN	-5 MAX	-6 MIN	-6 MAX	-7 MIN	-7 MAX	-8 MIN	-8 MAX	UNITS	NOTES
Clock													
Clock cycle time	^tKC	8		10		12		15		20		ns	
Clock HIGH time	^tKH	3		4		4.5		5		6		ns	
Clock LOW time	^tKL	3		4		4.5		5		6		ns	
Output Times													
Clock to output valid	^tKQ		4.5		5		6		7		8	ns	
Clock to output invalid	^tKQX	2		2		2		2		2		ns	
Clock to output in Low-Z	^tKQLZ	2		2		2		2		2		ns	4, 6, 7
Clock to output in High-Z	^tKQHZ		4.5		5		5		6		6	ns	4, 6, 7
$\overline{OE}$ to output valid	^tOEQ		4.5		5		5		5		6	ns	9
$\overline{OE}$ to output in Low-Z	^tOELZ	0		0		0		0		0		ns	4, 6, 7
$\overline{OE}$ to output in High-Z	^tOEHZ		3		4		5		6		6	ns	4, 6, 7
Setup Times													
Address	^tAS	2.5		2.5		2.5		2.5		3.5		ns	8, 10
Address Status ($\overline{ADSC}$, $\overline{ADSP}$)	^tADSS	2.5		2.5		2.5		2.5		3.5		ns	8, 10
Address Advance ($\overline{ADV}$)	^tAAS	2.5		2.5		2.5		2.5		3.5		ns	8, 10
Write Signals ($\overline{WEL}$, $\overline{WEH}$, $\overline{BWE}$, $\overline{GW}$)	^tWS	2.5		2.5		2.5		2.5		3.5		ns	8, 10
Data-in	^tDS	2.5		2.5		2.5		2.5		3.5		ns	8, 10
Chip Enables ($\overline{CE}$, $\overline{CE2}$, CE2)	^tCES	2.5		2.5		2.5		2.5		3.5		ns	8, 10
Hold Times													
Address	^tAH	0.5		0.5		0.5		0.5		0.8		ns	8, 10
Address Status ($\overline{ADSC}$, $\overline{ADSP}$)	^tADSH	0.5		0.5		0.5		0.5		0.8		ns	8, 10
Address Advance ($\overline{ADV}$)	^tAAH	0.5		0.5		0.5		0.5		0.8		ns	8, 10
Write Signals ($\overline{WEL}$, $\overline{WEH}$, $\overline{BWE}$, $\overline{GW}$)	^tWH	0.5		0.5		0.5		0.5		0.8		ns	8, 10
Data-in	^tDH	0.5		0.5		0.5		0.5		0.8		ns	8, 10
Chip Enables ($\overline{CE}$, $\overline{CE2}$, CE2)	^tCEH	0.5		0.5		0.5		0.5		0.8		ns	8, 10

MT58LC64K18D7
Y26.pm5 – Rev 6/95

1-24

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AC TEST CONDITIONS

Input pulse levels .... Vss to 3.0V	
Input rise and fall times 2.5ns	
Input timing reference levels 1.5V	
Output reference levels 1.5V	
Output load .... See Figures 1 and 2	
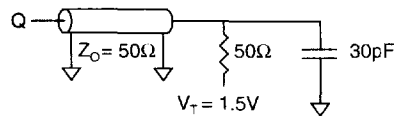
Fig. 1 OUTPUT LOAD EQUIVALENT
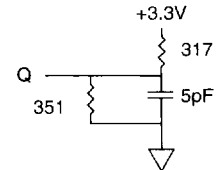
Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tKC/2$.
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tKC/2$.
   Power-up: $V_{IH} \leq +6.0V$ and $V_{CC} \leq 3.135V$ for $t \leq 200ms$.
3. Icc is given with no output current. Icc increases with greater output loading and faster cycle times.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with $C_L = 5pF$ as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^tKQHZ is less than ^tKQLZ and ^tOEHZ is less than ^tOELZ.
8. A WRITE cycle is defined by at least one byte write enable LOW and $\overline{ADSP}$ HIGH for the required setup and hold times. A READ cycle is defined by all byte write enables HIGH and ($\overline{ADSC}$ or $\overline{ADV}$ LOW) or $\overline{ADSP}$ LOW for the required setup and hold times.
9. $\overline{OE}$ is a "don't care" when a byte write enable is sampled LOW.

10. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW and chip enabled. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when the chip is enabled. Chip enable must be valid at each rising edge of CLK (when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW) to remain enabled.
11. The load used for V_{OH}, V_{OL} testing is shown in Fig. 2. AC load current is higher than the shown DC values. AC I/O curves are available upon request.
12. "Device Deselected" means device is in POWER-DOWN mode as defined in the Truth Table. "Device Selected" means device is active (not in POWER-DOWN mode).
13. Typical values are measured at 3.3V, 25°C and 20ns cycle time.
14. MODE pin has an internal pull-up and exhibits an input leakage current of ±10µA.
15. Typical values are measured at 25°C.
16. The device must have a deselect cycle applied at least two clock cycles before data retention mode is entered.
17. DQs are guaranteed to meet V_{OH} min. for up to 10 ms after outputs become static.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Vcc for Retention Data		V_{DR}	2		V	
Data Retention Current Method 1	$\overline{CE}$, $\overline{CE2} \geq$ (Vcc -0.2V), CE2 ≤ 0.2V $V_{IN} \geq$ (Vcc -0.2V) or ≤ 0.2V Vcc = 2V, ZZ ≤ 0.2V	I_{CCDR}		TBD	μA	15
Data Retention Current Method 2	ZZ ≥ Vcc -0.2V Vcc = 2V	I_{CCDR}		TBD	μA	15
Chip Deselect to Data Retention Time		^tCDR	2(^tKC)		ns	4, 16
Operation Recovery Time		^tR		2(^tKC)	ns	4

LOW Vcc DATA RETENTION WAVEFORM

//// DON'T CARE

▨▨ UNDEFINED
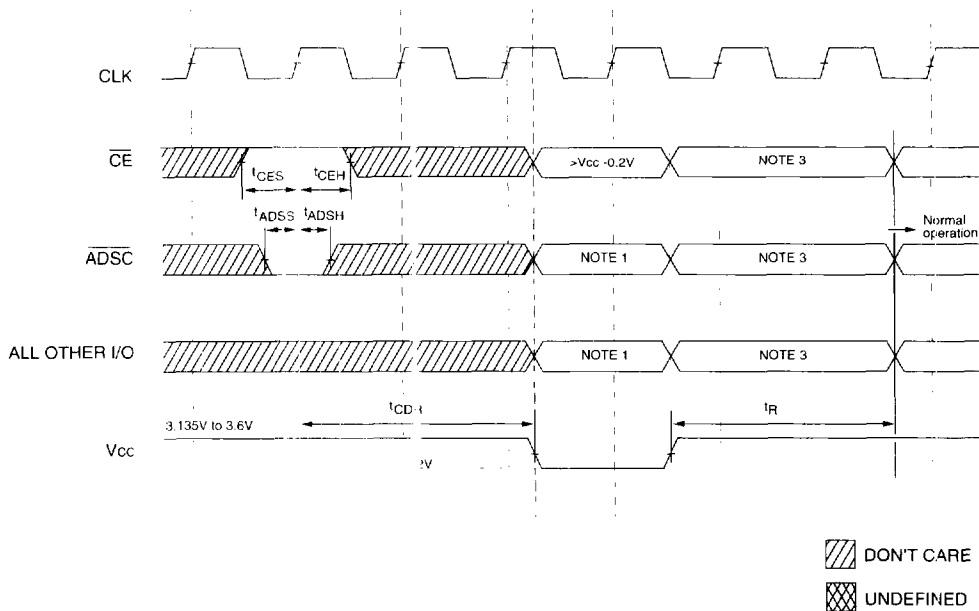
NOTE: 1. If ZZ is inactive (ZZ ≤ 0.2V), $\overline{CE}$ > Vcc -0.2V and other inputs must be ≥ Vcc -0.2V or ≤ 0.2V to guarantee I_{CCDR} in data retention mode. If inputs are between these levels or left floating, I_{CCDR} may be exceeded. If ZZ is active (ZZ ≥ Vcc -0.2V), then this restriction on input may be ignored.

2. Only one of the available deselect cycle sequences is shown above ($\overline{CE}$ = HIGH, $\overline{ADSC}$ = LOW). Any of the other deselect cycle sequences may also be used.

3. The device control signals should be in a deselect state between the rising edge of Vcc and until ^tR is met.

4. All inputs must be ≤ Vcc +0.3V while the device is in data retention mode.

SNOOZE MODE

SNOOZE MODE is a low current, "power down" mode in which the device is deselected and current is reduced to I_{SB2}. The duration of SNOOZE MODE is dictated by the length of time the ZZ pin is in a HIGH state. After entering SNOOZE MODE, the clock and all other inputs are ignored.

The ZZ pin (pin 64) is an asynchronous, active HIGH input that causes the device to enter SNOOZE MODE.

When the ZZ pin becomes a logic HIGH, I_{SB2} is guaranteed after the setup time ^tZZ is met. Any access pending when entering SNOOZE MODE is not guaranteed to successfully complete. Therefore, SNOOZE MODE must not be initiated until valid pending operations are completed.
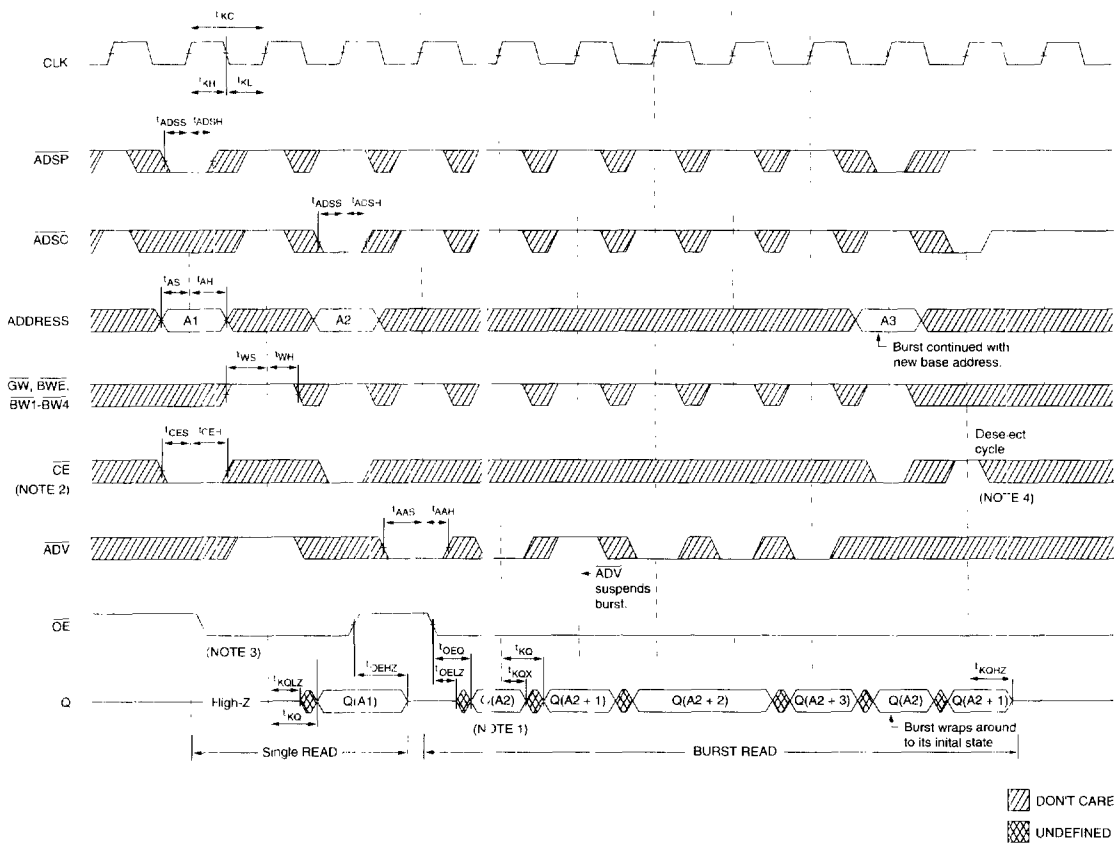
SNOOZE MODE ELECTRICAL CHARACTERISTICS

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Current during SNOOZE MODE	$ZZ \geq V_{IH}$	I_{SB2}		5	mA	
Current during SNOOZE MODE (P Version)	$ZZ \geq V_{IH}$	I_{SB2}		2	mA	
ZZ HIGH to SNOOZE MODE time		^tZZ	$2(^tKC)$		ns	4
SNOOZE MODE Operation Recovery Time		^tRZZ		$2(^tKC)$	ns	4

SNOOZE MODE WAVEFORM
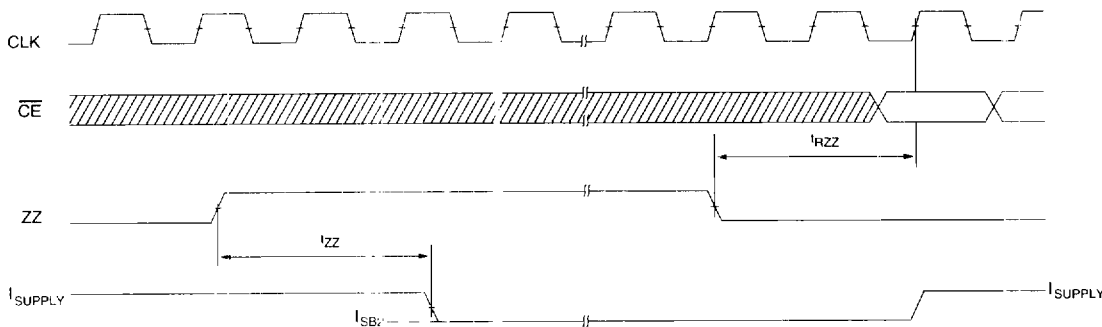
NOTE: 1. The $\overline{CE}$ signal shown above refers to a TRUE state on all chip selects for the device.

NEW | **SYNCHRONOUS PIPELINED SRAM**

READ TIMING

Burst continued with new base address.

Deselect cycle

ADV suspends burst.

Burst wraps around to its inital state

Single READ

BURST READ

▨ DON'T CARE
▧ UNDEFINED

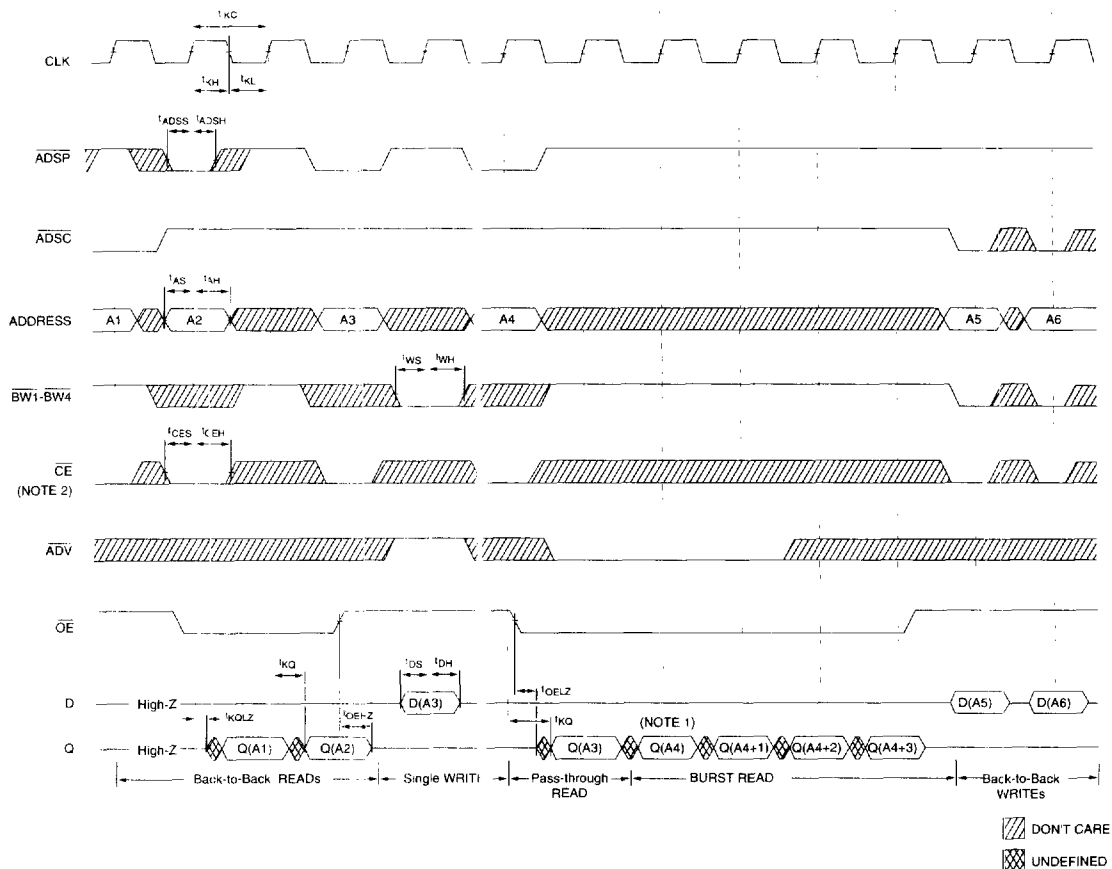**NOTE:**
1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.
2. CE2 and CE2 have timing identical to CE. On this diagram, when CE is LOW, CE2 is LOW and CE2 is HIGH. When CE is HIGH, CE2 is HIGH and CE2 is LOW.
3. Timing is shown assuming that the device was not enabled before entering into this sequence. OE does not cause Q to be driven until after the following clock rising edge.
4. Outputs are disabled within one clock cycle after deselect.

WRITE TIMING

▨ DON'T CARE
▨ UNDEFINED
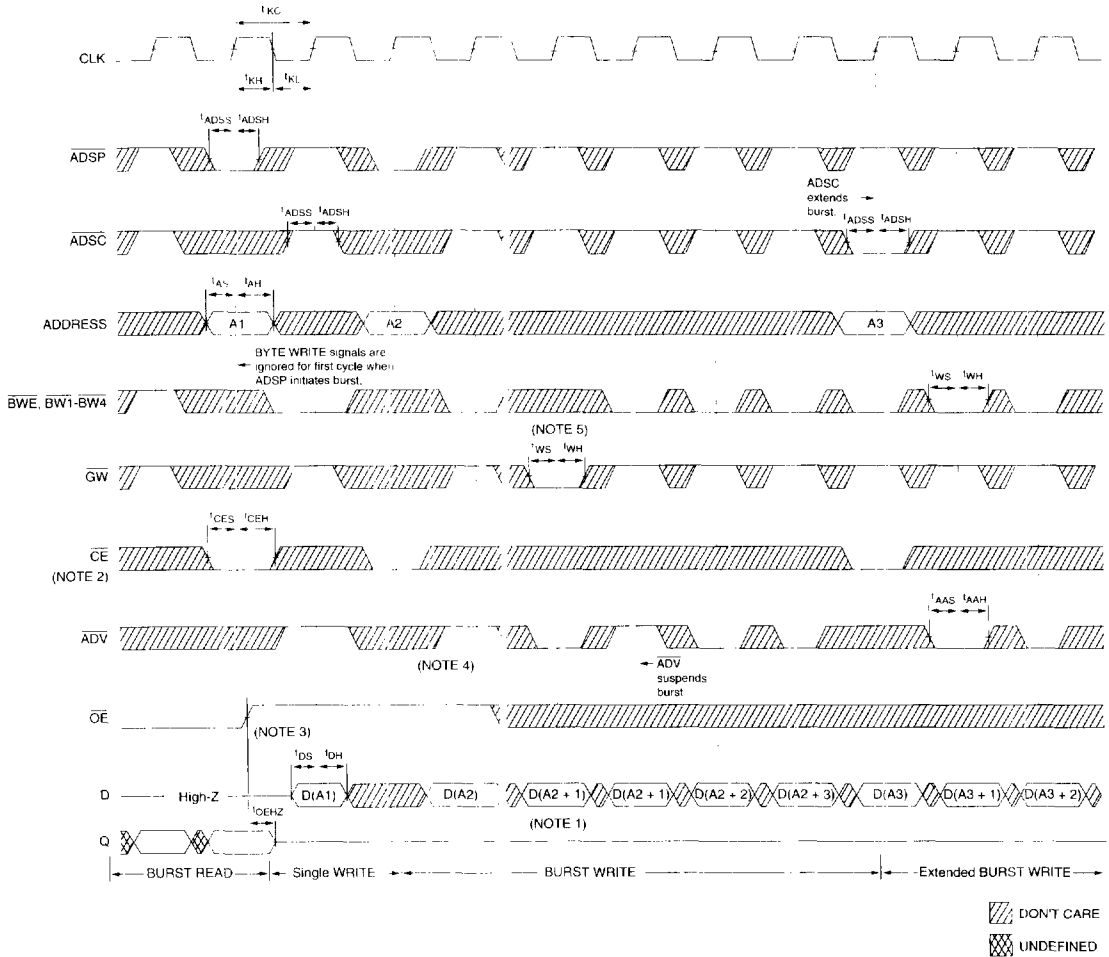
NOTE:
1. D(A2) refers to input for address A2. Q(A2+1) refers to input for the next internal burst address following A2.
2. CE2 and CE2 have timing identical to CE. On this diagram, when CE is LOW, CE2 is LOW and CE2 is HIGH. When CE is HIGH, CE2 is HIGH and CE2 is LOW.
3. OE must be HIGH before the input data setup and held HIGH throughout the data hold time. This prevents input/output data contention for the time period prior to the byte write enable inputs being sampled.
4. ADV must be HIGH to permit a WRITE to the loaded address.
5. Full width WRITE can be initiated by GW LOW or GW HIGH and BWE, WEL and WEH LOW.

NEW

SYNCHRONOUS PIPELINED SRAM

READ/WRITE TIMING

DON'T CARE

UNDEFINED

NOTE:
1. Q(A4) refers to output from address A4. Q(A4+1) refers to output from the next internal burst address following A4.
2. $\overline{CE2}$ and CE2 have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE2}$ is LOW and CE2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE2}$ is HIGH and CE2 is LOW.
3. The data bus (Q) remains in High-Z following a WRITE cycle unless an $\overline{ADSP}$, $\overline{ADSC}$ or $\overline{ADV}$ cycle is performed.
4. $\overline{GW}$ is HIGH.
5. Back-to-back READs may be controlled by either $\overline{ADSP}$ or $\overline{ADSC}$.

APPLICATION INFORMATION

LOAD DERATING CURVES

The Micron 64K x 18 Synchronous SRAM timing is dependent upon the capacitive loading on the outputs. The data sheet is written assuming a load of 30pF. Access time changes with load capacitance as follows:

$$\Delta {}^tKQ = 0.016 \text{ ns/pF} \times \Delta C_L \text{ pF}.$$
(Note: this is preliminary information subject to change.)

For example, if the SRAM loading is 22pF, ΔC_L is -8pF (8pF less than rated load). The clock to valid output time of the SRAM is reduced by 0.016 x 8 = 0.128ns. If the device is an 8ns part, the worst case ${}^tKQ$ becomes 7.87ns (approximately).

Consult the factory for copies of I/O current versus voltage curves. For capacitive loading derating curves see technical note TN-05-20, "3.3V SRAM Capacitive Loading."