74HCT612

FEATURES

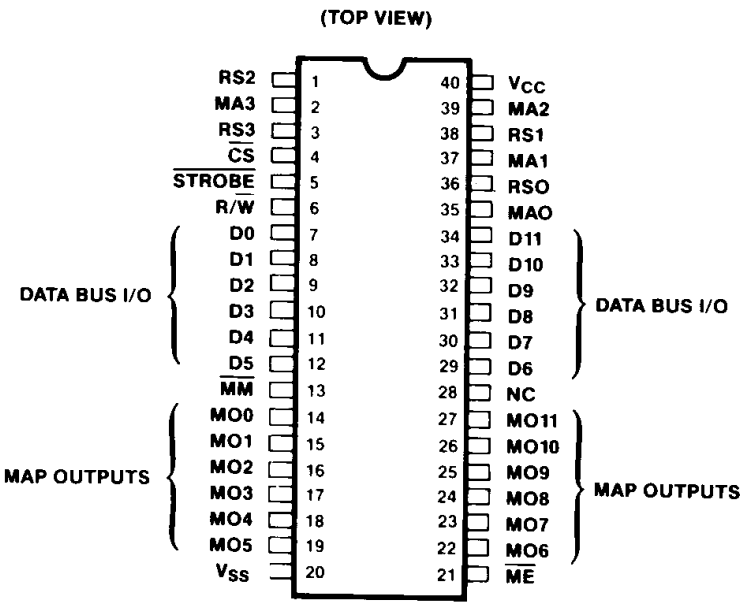
- Expands 4 Address Lines to 12 Address Lines
- Designed for Paged Memory Mapping
- 3-State Map Outputs
- Compatible with iAPX286 and Other Microprocessors.
- Guaranteed Latch-Up Protection 100mA min
- Designed in 1.8 Micron, Double Metal CHMO3

DESCRIPTION

The 74HCT612 Memory Mapper is intended for use in applications requiring paged memory expansion. It can expand an address bus by 8 bits. In a typical application, 4 bits of the source address bus are used to select 1 of the 16, twelve bit map registers in the 74HCT612. These registers are normally programmed (through software) with the starting address of each memory page. The register data is output directly for use as the most significant bits of the expanded address bus. The 12 bits from the 74HCT612, are used along with the unused source address bits to form the expanded address bus.

As summarized in Table 1, the 74HCT612 has four modes of operation including; read, write, map and pass. Data may be written into, or read from the Memory Mapper when chip select ($\overline{CS}$) is low. The register select inputs (RS0 through RS3) select one of the sixteen map registers. When R/$\overline{W}$ is low, data is written into a register from the data bus. When R/$\overline{W}$ is high data is output from a Memory Mapper register to the data bus.

The map mode of operation is selected when chip select ($\overline{CS}$) is high and map mode control ($\overline{MM}$) is low. In this mode, the register data selected by the map

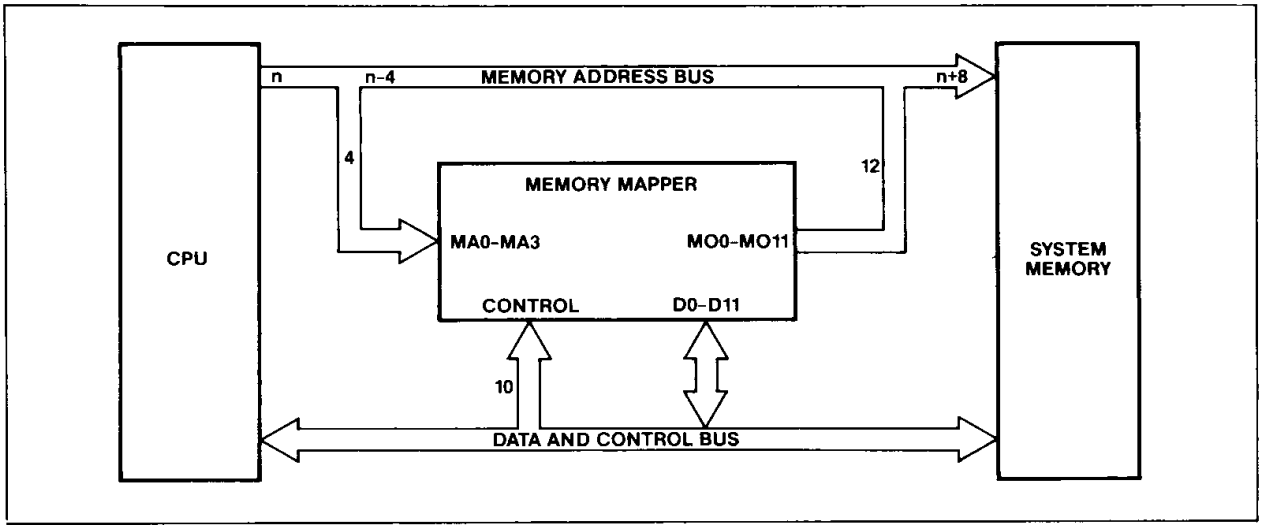


74HCT612 Pin Diagram

address inputs (MA0 through MA3) will be available on the map outputs (MO0 through MO11). Note that the map registers are addressed by either the RS inputs or the MA inputs depending upon the operating mode.

The pass mode of operation is selected when both chip select ($\overline{CS}$) and map mode control ($\overline{MM}$) are high. In this operating mode, the inputs MA0 through MA3 are output directly to the outputs MO8 through MO11, respectively. Outputs MO0 through MO7 take a low level.

When $\overline{ME}$ (Map Enable) is lwo the map outputs (MO0–MO11) are active. When $\overline{ME}$ is high, the map outputs are at high impedance.



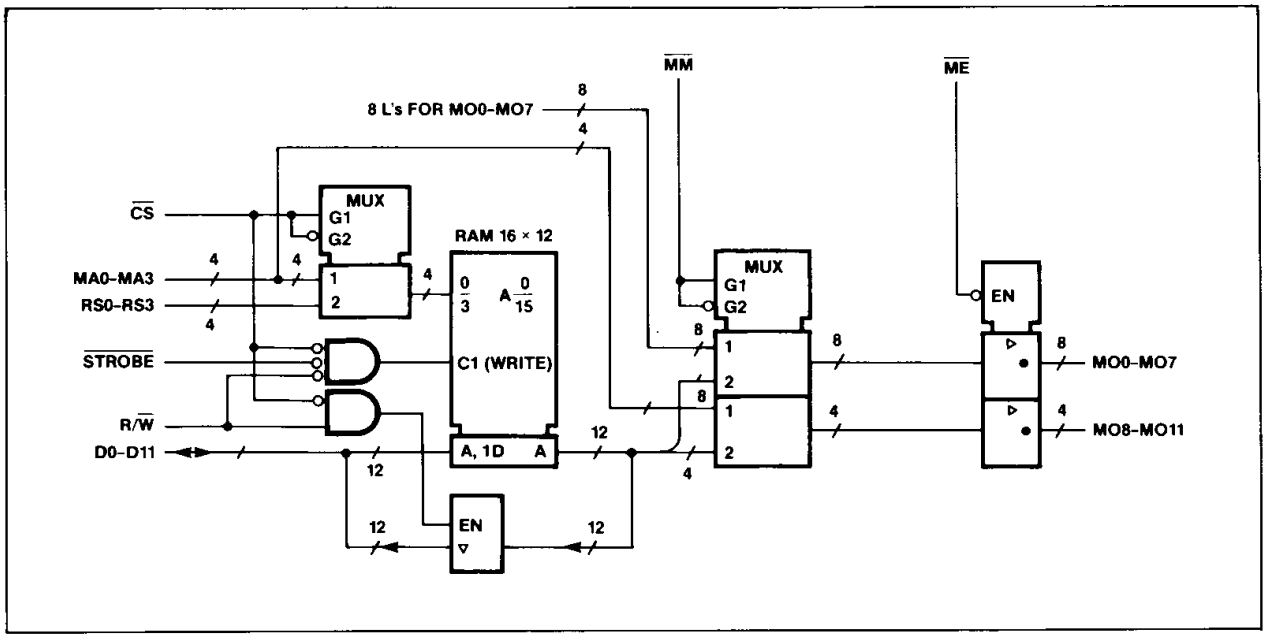


TABLE 1			
$\overline{CS}$	$\overline{MM}$	R/$\overline{W}$	MODE
0	X	0	Write to register selected by RSx inputs.
0	X	1	Read from register selected RSx inputs.
1	0	X	Output on MOx the register selected by MAx inputs.
1	1	X	Output MO0 through MO7 are low, MO8 through MO11 equal MA0 through MA3 respectively.

PIN DESCRIPTION

PIN	PIN NAME	FUNCTIONAL DESCRIPTION
7–12, 29–34	D0 thru D11	I/O connections to data and control bus used for reading from and writing to the map register selected by RS0–RS3 when $\overline{CS}$ is low. Mode controlled by R/$\overline{W}$.
36,38,1,3	RS0 thru RS3	Register select inputs for I/O operations.
6	R/$\overline{W}$	Read or write control used in I/O operations to select the condition of the data bus. When high, the data bus outputs are active for reading the map register. When low, the data bus is used to write into the register.
5	$\overline{STROBE}$	Strobe input used to enter data into the selected map register during I/O operations.
4	$\overline{CS}$	Chip select input. A low input level selects the memory mapper (assuming more than one used) for an I/O operation.
35,37,39,2	MA0 thru MA3	Map address inputs to select one of 16 map registers when in map mode ($\overline{MM}$ is low and $\overline{CS}$ high).
14–19, 22–27	MO0 thru MO11	Map outputs. Present the map register contents to the system memory address bus in the map mode. In the pass mode, these outputs provide the map address on MO8–MO11 and low levels on MO0–MO7.
13	$\overline{MM}$	Map mode input. When low, map mode 12 bits of data are transferred from the selected map register to the map outputs. When high (pass mode), the 4 bits present on the map address inputs MA0–MA3 are passed to the map outputs MO8–MO11, respectively, while MO0–MO7 are set low.
21	$\overline{ME}$	Map enable for the map outputs. A low level allows the outputs to be active while a high input level puts the outputs at high impedance.
28	NC	No connect
40	V_{CC}, GND	5-V power supply.
20	V_{SS}	Ground.

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC} 7V
Input voltage ..... V_{CC} + .3V
Ambient temperature under bias ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
I_{OH}	High-level output current				−15	mA
I_{OL}	Low-level output current				+24	mA
t_{SLSH}	Width of strobe input pulse	See Figure 1	75			ns
t_{CSLSL}	$\overline{CS}$ setup ($\overline{CS}$ low to strobe low)		20			ns
t_{WLSL}	R/$\overline{W}$ setup time (R/$\overline{W}$ low to strobe low)		20			ns
t_{RVSL}	RS setup time (RS valid to strobe low)		20			ns
t_{DVSH}	Data setup time (D0–D11 valid to strobe high)		75			ns
t_{SHCSH}	$\overline{CS}$ hold time (Strobe high to $\overline{CS}$ high)		20			ns
t_{SHWH}	R/$\overline{W}$ hold time (Strobe high to R/$\overline{W}$ high)		20			ns
t_{SHRX}	RS hold time (Strobe high to RS invalid)		20			ns
t_{SHDX}	Data hold time (Strobe high to D0–D11 invalid)		20			ns
T_A	Ambient temperature under bias		0		70	°C

ELECTRICAL CHARACTERISTICS OVER AMBIENT TEMPERATURE UNDER BIAS (unless otherwise noted)

PARAMETER		CONDITIONS		MIN	TYP[2]	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = -18mA				-1.5	V
V_{OH}	High-level output voltage/current	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = .8V/I_{OH} = -15mA		2.4			V
V_{OL}	Low-level output voltage/current	V_{CC} = MIN, V_{IH} = 2V, V_{OL} = .8V/I_{OH} = 12mA			.25	.4	V
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2V, V_{IL} = .8V V_O = 2.7V				20	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IH} = 2V, V_{IL} = .8V V_O = 0.4V				-20	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V to V_{CC}		-20		20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4V				-25	μA
I_{OS}	Short circuit output current[3]	V_{CC} = MAX		-30		-130	mA
I_{CC}	Supply Current	V_{CC} = MAX	Dynamic			10	mA
			Static			1	

[1] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[2] All typical values are at V_{CC} = 5V, T_A = 25°C.

[3] Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 50pF to GND)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{CSLDV} Access (enable) time	$\overline{CS}$↓	D0–D11	LOAD = 6TTL See Figure 1 See Note 1		26	50	ns
t_{WHDV} Access (enable) time	R/$\overline{W}$↑	D0–D11			25	35	ns
t_{RVDV} Access time	RS	D0–D11			39	75	ns
t_{WLDZ} Disable time	R/$\overline{W}$↓	D0–D11			30	50	ns
t_{CSHDZ} Disable time	$\overline{CS}$↑	D0–D11			38	65	ns
t_{ELQV} Access (enable) time	$\overline{ME}$↓	MO0–11	LOAD = 6TTL See Figure 2 See Note 1		17	30	ns
t_{CSHQV} Access time	$\overline{CS}$↑	MO0–11			25	50	ns
t_{MLQV} Access time	$\overline{MM}$↓	MO0–11			22	40	ns
t_{AVQV1} Access time ($\overline{MM}$ low)	MA	MO0–11			39	70	ns
t_{MHQV} Access time					22	40	ns
t_{AVQV2} Propagation time ($\overline{MM}$ high)	MA	MO8–11			13	30	ns
t_{EHQZ} Disable time	$\overline{ME}$↑	MO0–11			14	25	ns

Note 1: Access time are tested as t_{PLH} and t_{PHL} or t_{PZH} or t_{PZL}. Disable times are tested at t_{PHZ} and t_{PLZ}.

EXPLANATION OF LETTER SYMBOLS

This data sheet uses a type of letter symbol to describe time intervals. The format is:

$$t_{AB\cdot CD}$$

where:

subscripts A and C indicate the names of the signals for which changes of state or level or establishment of state or level constitute signal events assumed to occur first and last, respectively, that is, at the beginning and end of the time interval.

Subscripts B and D indicate the direction of the transitions and/or the final states or levels of the signals represented by A and C, respectively. One or two of the following is used:

H = high or transition to high
L = low or transition to low
V = a valid steady-state level
X = unknown, changing, or "don't care" level
Z = high-impedance (off) state.

The hyphen between the B and C subscripts is omitted when no confusion is likely to occur. For these letter symbols on this data sheet, the signal names are further abbreviated as follows:

SIGNAL NAME	A AND C SUBSCRIPT
$\overline{CS}$	CS
D0–11	D
MA0–MA3	A
MO0–MO11	Q
$\overline{ME}$	E
$\overline{MM}$	M
R/$\overline{W}$	W
$\overline{RS0–RS3}$	R
$\overline{STROBE}$	S

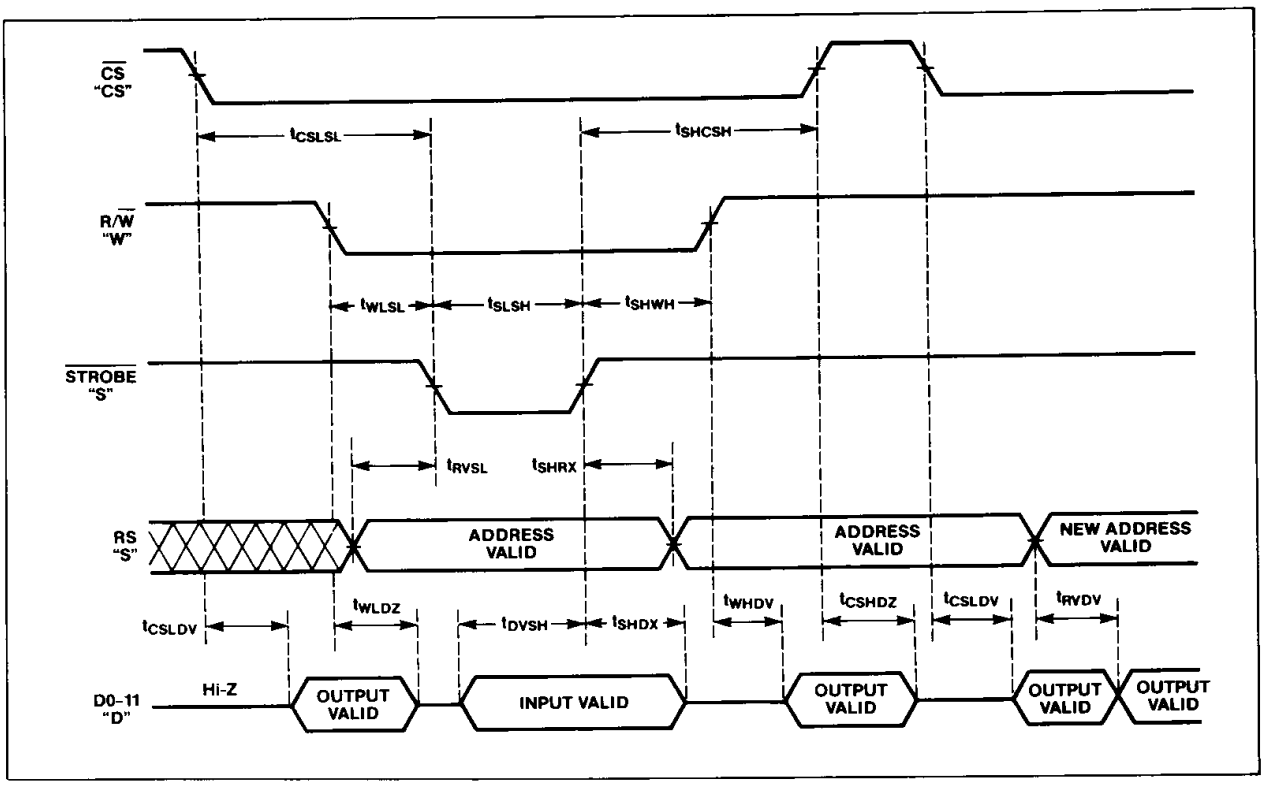


Figure 1. Write and Read Modes

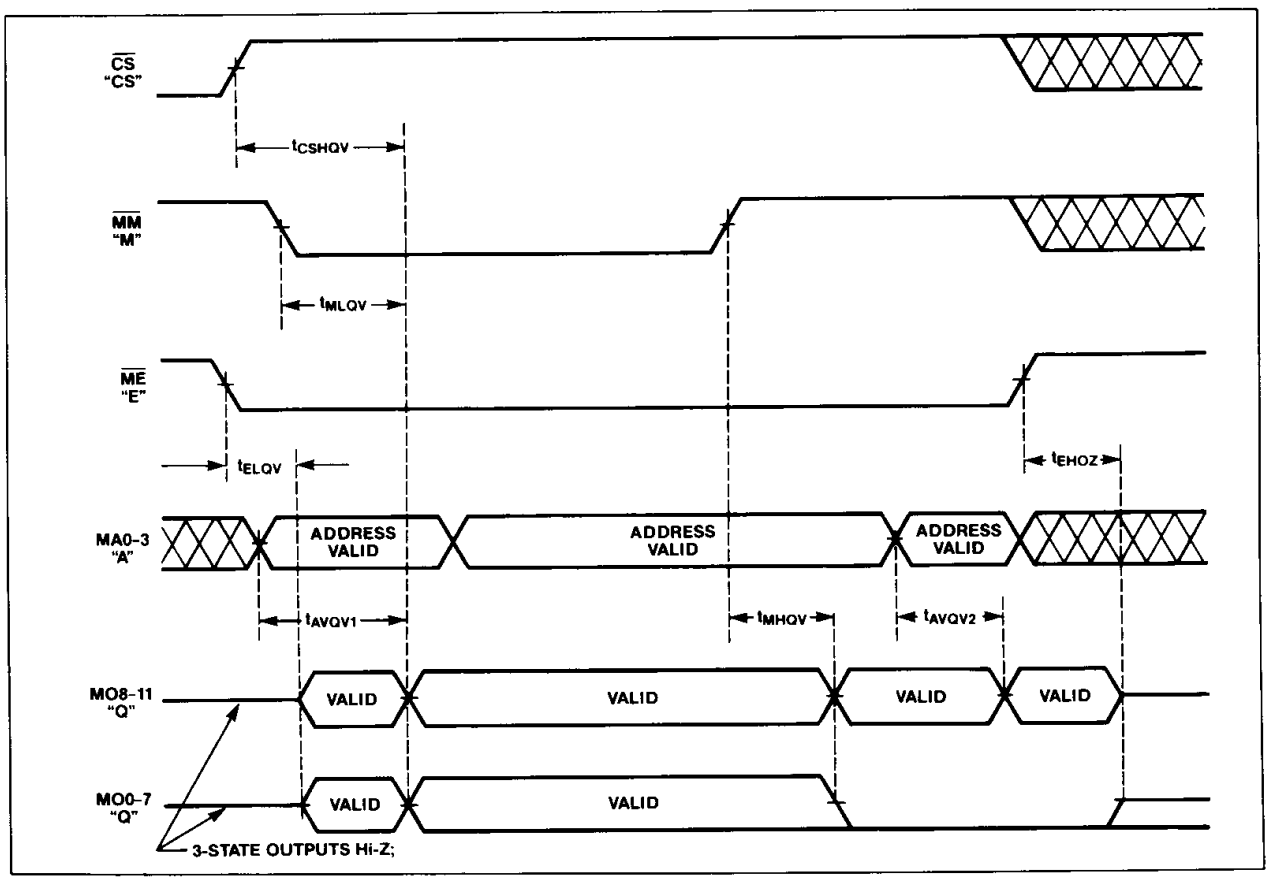


Figure 2. Map and Pass Modes

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