88SF9210

6 Gbps Serial Attached SCSI to Serial ATA Protocol Converter

Preliminary Datasheet

Doc No. MV-S106632-00 Rev. B

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CONFIDENTIAL

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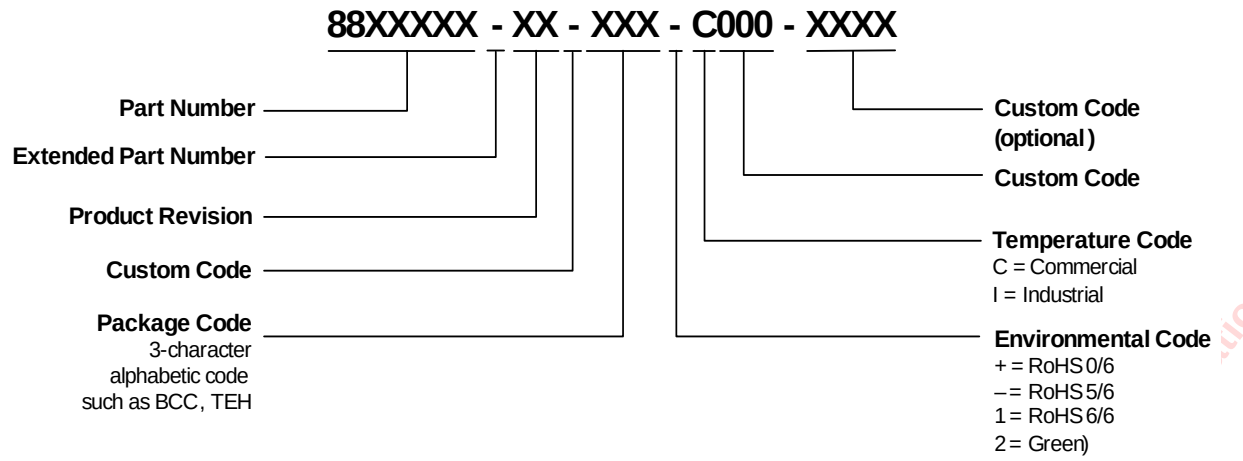
ORDERING INFORMATION

Ordering Part Numbers and Package Markings

The following figure shows the ordering part numbering scheme for the 88SF9210 part. For complete ordering information, contact your Marvell FAE or sales representative.

Sample Ordering Part Number



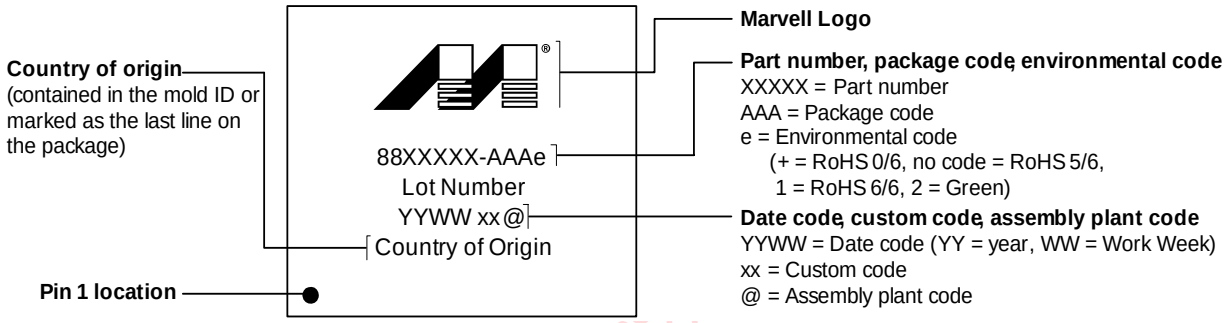
The standard ordering part numbers for the respective solutions are indicated in the following table.

Ordering Part Numbers

Part Number	Description
88SF9210B0-NNR2C000	84-pin QFN, 10 x 10 mm. Package height 1.0 mm maximum, 0.85 mm nominal.

The next figure shows a typical Marvell package marking.

88SF9210 Package Marking and Pin 1 Location



Note: The above drawing is not drawn to scale. The location of markings is approximate. Add-on marks are not represented. Flip chips vary widely in their markings and flip chip examples are not shown here. For flip chips, the markings may be omitted per customer requirement.

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CHANGE HISTORY

The following table identifies the document change history for Rev. B.

Document Changes *

Location	Type	Description	Date
Page -iii	Update	Updated Ordering Information as follows: from 88SF9210A0-NNR2C000 to 88SF9210B0-NNR2C000	5-Oct-10
Page 3-7	Update	Updated Table 3-5, GPIO Interface Signals. Changed the description of T[15]–T[8] from Reserved to GPIO pins.	8-Sep-10

* The type of change is categorized as: Parameter, Revision, or Update. A Parameter change is a change to a spec value, a Revision change is one that originates from the chip Revision Notice, and an Update change includes all other document updates.

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CONTENTS

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1 OVERVIEW

This chapter contains the following sections:

1.1 Block Overview

The 88SF9210 is a SCSI-to-SATA protocol bridge chip. It contains two integrated SAS target ports, and two integrated SATA Host ports.

The 88SF9210 allows one or two standard single port SATA HDDs or SSDs to function as a single, dual port SAS Serial SCSI Protocol (SSP) target device. All protocol translation is performed on-chip. The 88SF9210 provides support for all SAS connectivity and functionality that is not native to a SATA Device.

In SAS Target mode, the 88SF9210 internally terminates the SAS SSP protocol. All SCSI commands that do not have corresponding functions in the SATA protocol, such as Mode Select and Mode Sense, are serviced by the 88SF9210's internal microprocessor. SCSI commands that have corresponding functions, such as Read Command (ReadCmd) and Write Command (WriteCmd), are forwarded to one of the two SATA devices using the SATA protocol. The embedded microprocessor performs internal error handling.

The 88SF9210 provides full ANSI compliant SAS 2.0 target functionality, including Speed Negotiation Window 3 (SNW-3) and PHY training, at data rates of 1.5, 3, and 6 Gbps on its two fully independent SAS target ports.

The 88SF9210 supports concurrent active-to-active full duplex command and data transfers, and up to 128 concurrent I/O operations from up to 32 SAS Initiators.

The dual SATA interfaces provide full ANSI compliant SATA host functionality (SATA 1.0A, SATA-2 and SATA-3) on the 88SF9210's SATA ports. NCQ is supported.

Internal sector size translation is provided. SATA devices do not support non-512-byte sector sizes. This allows SAS initiators to configure the device for sector sizes of 520, 524, or 528 bytes per sector. Other sector sizes are also supported. All sector size translation and mapping is performed internally by the 88SF9210, and is transparent to the SATA device.

The 88SF9210 also provides support for XDREAD, XDWRITE, and XPWRITE commands, as well as the Write/Verify command.

The 88SF9210 provides full support for the T10 Protection Information Model. Protection information fields, also known as PIF fields, can be verified, inserted, or deleted from the data stream by the 88SF9210, transparent to the SATA device. Figure 1-1 shows the system block diagram.

Figure 1-1 88SF9210 System Block Diagram

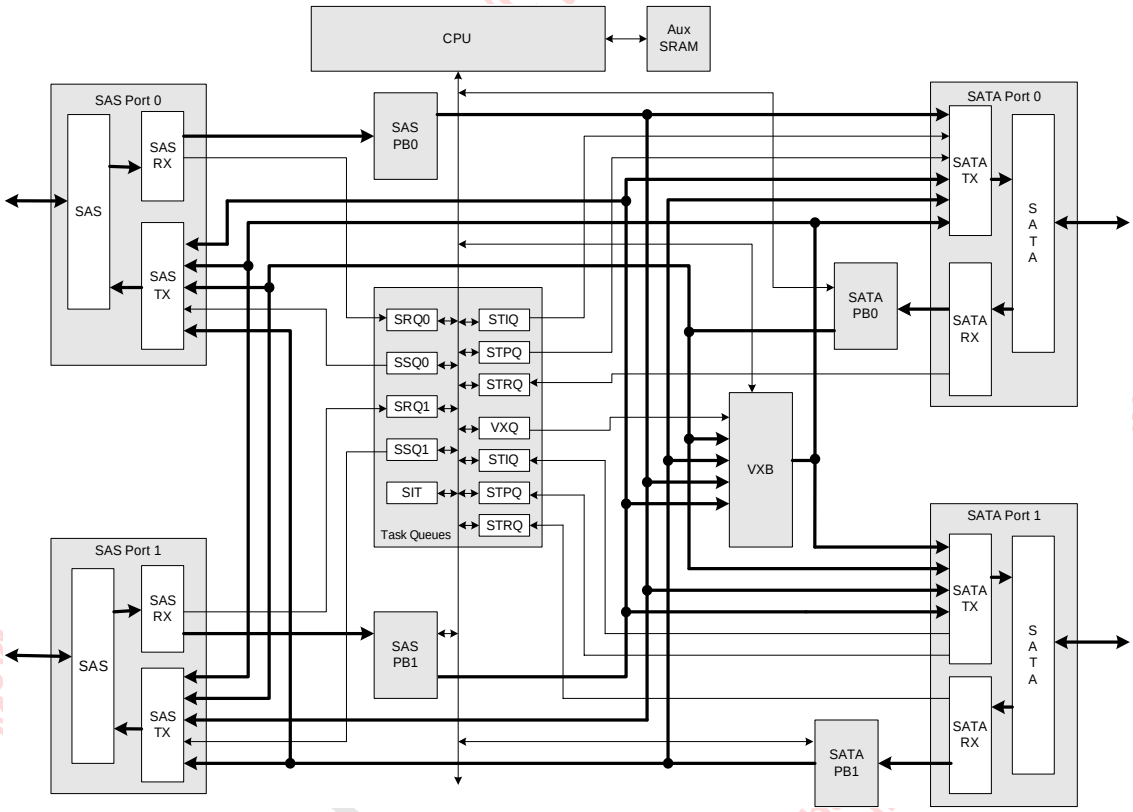

Table 1-1 defines the acronyms used in Figure 1-1.

Table 1-1 Legend for Figure 1-1

Block	Acronym	Definition
General	Aux SRAM	Auxiliary SRAM
	CPU	Central Processing Unit
	VXB	Verify XOR Buffer
Payload Buffer	SAS PBx	SAS Payload Buffer
	SATA PBx	SATA Payload Buffer
SAS Port 0 and SAS Port 1	SAS	SAS PHY and Link Control
	SAS RX	SAS Receive Control
	SAS TX	SAS Send Control

Table 1-1 Legend for Figure 1-1 (continued)

Block	Acronym	Definition
SATA Port 0 and SATA Port 1	SATA	SATA PHY and Link Control
	SATA RX	SATA Receive Control
	SATA TX	SATA Send Control
Task Queues	SIT	SAS Initiator Table
	SRQx	SAS Receive Queue
	SSQx	SAS Send Queue
	STIQ	SATA Send Internal Queue
	STPQ	SATA Pass-Through Queue
	STRQ	SATA Receive Queue
	VXQ	Verify XOR Queue

1.2 SATA Bypass Mode

In SATA Bypass mode, the 88SF9210 acts as a transparent forwarding engine for the SATA protocol. SAS Port 0, which is normally connected to a SAS initiator, is configured as a SATA device port. The port can then be connected to a SATA host. SATA traffic received on the port is transparently bridged through the 88SF9210 to the device connected to SATA port 0. This mode enables SATA manufacturing and test equipment to access the SATA device without first being translated to SCSI and then back to SATA. Similarly, SAS port 1 is transparently bridged to SATA port 1.

This feature allows the SATA Device to toggle between SAS mode and native SATA mode by simply inverting a single configuration pin, and then power cycling the bridge. SATA Bypass mode operates almost entirely in hardware, requiring only a small number of PHY registers to be re-programmed for SATA operation.

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2 FEATURES

This chapter contains the following sections:

2.1 General

- Embedded SERDES for all ports.
- Embedded Feroceon™ processor (ARM966E-S equivalent).
  - 96 KB instruction RAM.
  - 32 KB data RAM.
  - 256 KB auxiliary RAM.
- Downloadable firmware (UART or SAS Interface).
- Requires a single crystal oscillator at 20, 50, 75, 100 MHz.
- 55 nm CMOS process.
- 84-pin QFN package.

2.2 Serial Attached SCSI (SAS)

- Dual-port SAS target controller.
- Supports Serial SCSI Protocol (SSP), Initiator and Target mode.
- ANSI Serial Attached SCSI, Revision 2.0 (SAS-2.0) Specification compliant.
- Supports 6 Gbps, 3 Gbps, and 1.5 Gbps devices.
- Supports OOB signaling, Speed Negotiation (SNW 3, Final SNW), and PHY Training.
- Supports SSC, with independent control for each PHY.
- Supports concurrent, full-duplex, dual port transfers (active-to-active).
- Fully automated SAS connection management.
- Supports four PHY event counters per PHY (per SAS-2.0 specification).
- Supports independent duplicate TAG checking on each port.

2.3 Serial ATA (SATA)

- Dual SATA host controller.
- Compliant with Serial ATA Revision 3.0 Specification
- Supports communication speeds of 6.0 Gbps, 3.0 Gbps, and 1.5 Gbps
- Supports OOB signaling and speed negotiation.
- Supports HDD spin-up control.
- Supports First Party DMA (FPDMA) commands for Native Command Queueing (NCQ).
- Affiliations (Tag mapping) handled transparently.

2.4 SCSI

- Supports up to 128 concurrent I/O operations.
- Supports up to 32 initiators.
- Internal management for logical sector sizes of 520, 524, and 528 bytes per sector.
- Hardware support for XDWRITE, XDREAD, XPWRITE commands.
- Supports Write/Content Verify command.
- Supports insertion, verification, and/or removal of T10 protection information (data integrity fields).

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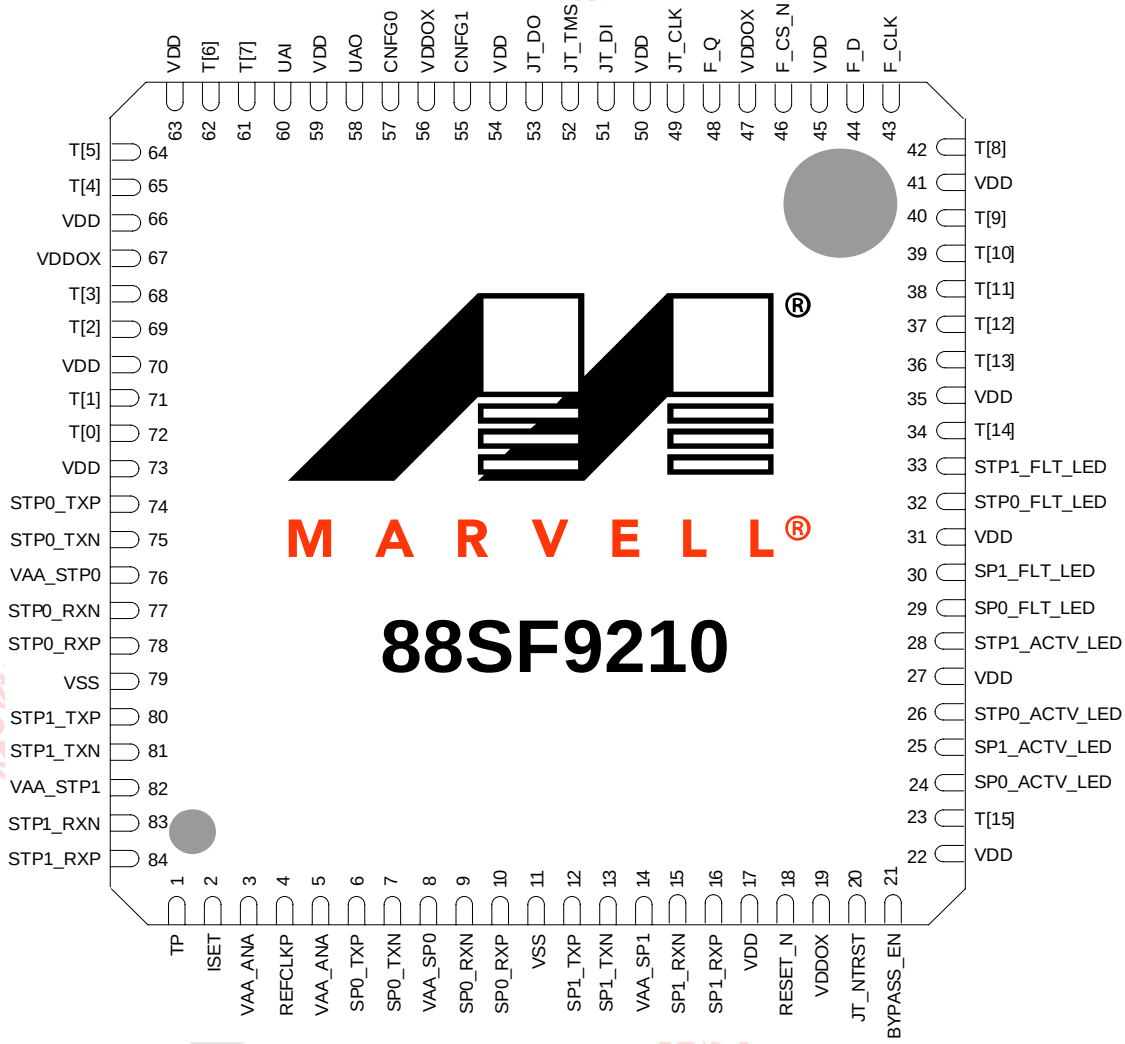
3 PACKAGE

This chapter contains the following sections:

3.1 Pin Diagram

The 84-pin QFN package diagram is illustrated in Figure 3-1.

Figure 3-1 84-Pin QFN Package Diagram

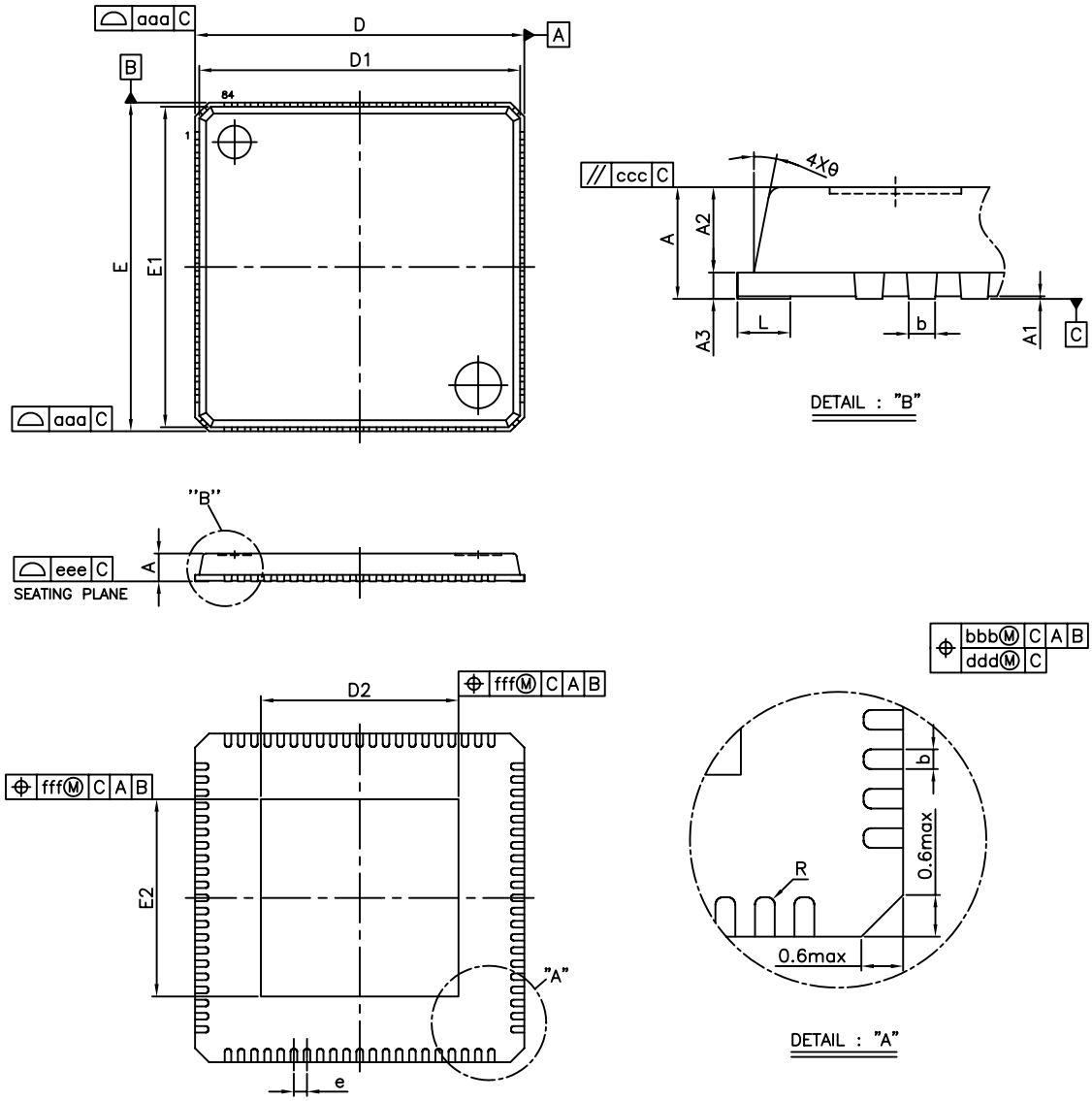


Note: The center area beneath the chip is the Exposed Die Pad (Epad). When designing the PCB, create a solder pad for the Epad and connect the Epad to ground.

3.2 Mechanical Dimensions

The 84-pin package mechanical drawing is shown in Figure 3-2.

Figure 3-2 84-Pin QFN Package Mechanical Diagram



The package mechanical dimensions are shown in Figure 3-3.

Figure 3-3 84-Pin QFN Package Mechanical Dimensions

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	1.00	0.031	0.033	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	0.60	0.65	0.80	0.024	0.026	0.031
A3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	10.00 BSC			0.394 BSC		
D1/E1	9.75 BSC			0.384 BSC		
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
θ	0°	---	14°	0°	---	14°
R	0.075	---	---	0.003	---	---
aaa	---	---	0.15	---	---	0.006
bbb	---	---	0.10	---	---	0.004
ccc	---	---	0.10	---	---	0.004
ddd	---	---	0.05	---	---	0.002
eee	---	---	0.08	---	---	0.003
fff	---	---	0.10	---	---	0.004

Die Pad Size Options (D2/E2)				Shape Option
	Symbol	Dimension in mm	Dimension in inch	
	D_2	4.60 BSC	.181 BSC	Square
	E_2	4.60 BSC	.181 BSC	

3.3 Signal Descriptions

This section contains the pin types and signal descriptions for the 88SF9210 package.

3.3.1 Pin Type Definitions

Pin type definitions are shown in Table 3-1.

Table 3-1 Pin Type Definitions

Pin Type	Definition
I/O	Input and Output
I	Input only
O	Output only

3.3.2 Signal Descriptions

This section outlines the 88SF9210 pin descriptions.

Table 3-2 Serial Flash Interface Signals

Signal Name	84-pin QFN Signal Number	Type	Description
F_CLK	43	O	Serial Flash Clock Out.
F_CS_N	46	O	Serial Flash Chip Select. Active-low signal to enable the Flash Access
F_D	44	O	Serial Flash Data Out. Transfers instructions, addresses, and write data serially to the Flash device. It changes on the falling edge of F_CLK.
F_Q	48	I	Serial Flash Data In. Transfers read data serially from the Flash device. Data is sampled by the rising edge of F_CLK.

Table 3-3 JTAG and Configuration Interface Signals

Signal Name	84-pin QFN Signal Number	Type	Description
BYPASS_EN	21	I	SATA Bypass Mode. **0:** Disable Bypass mode. **1:** Enable Bypass mode.
CNFG0 CNFG1	57 55	i	Chip Operation Mode. **0:** Normal Functional mode. **Others:**Test mode.
JT_CLK	49	I	JTAG Clock In.
JT_DI	51	I	JTAG Data In.
JT_DO	53	O	JTAG Data Out.
JT_NTRST	20	I	JTAG Reset.
JT_TMS	52	I	JTAG Test Mode Select.

Table 3-4 UART Serial Interface Signals (Baud Rate = 57,600 bps)

Signal Name	84-pin QFN Signal Number	Type	Description
UAI	60	I	UART Input (pull-up if not used).
UAO	58	O	UART Output.

Table 3-5 GPIO Interface Signals

Signal Name	84-pin QFN Signal Number	Type	Description
T[15]	23	I/O	GPIO Pins.
T[14]	34		Test pins T[15]–T[0] can be used as GPIO pins. After power-up, the default mode for the pins is Input mode. Change the value and direction of the test pins by programming TEST_OUT (R3008h [15:0]) and TEST_OE (R300Ch [15:0]) after reset.
T[13]	36		
T[12]	37		
T[11]	38		
T[10]	39		
T[9]	40		
T[8]	42		
T[7]	61	I/O	Boot Mode.
T[6]	62		***Note:*** *Input value latched at power up. Determines Boot mode. May be used as a GPIO thereafter.*
T[5]	64		
T[4]	65	I/O	Reserved.
T[3]	68	I/O	UART Baud Rate. **0:** 57600 bps. **1:** Reserved.
T[2]	69	I/O	UART Mode. **0:** Reserved. **1:** Terminal mode.
T[1]	71	I/O	Chip Reference Clock Selection.
T[0]	72		**00**: 20 MHz. **01**: 50 MHz. **10**: 100 MHz. **11**: 75 MHz.

Table 3-6 SAS Port 0 Interface Signals

Signal Name	84-pin QFN Signal Number	Type	Description
SP0_ACTV_LED	24	O	SAS0 Active LED.
SP0_FLT_LED	29	O	SAS0 Fault LED.
SP0_RXN	9	I	SAS0 Receive Data, differential analog input.
SP0_RXP	10		
SP0_TXN	7	O	SAS0 Transmit Data, differential analog output.
SP0_TXP	6		

Table 3-7 SAS Port 1 Interface Signals

Signal Name	84-pin QFN Signal Number	Type	Description
SP1_ACTV_LED	25	O	SAS1 Active LED.
SP1_FLT_LED	30	O	SAS1 Fault LED.
SP1_RXN	15	I	SAS1 Receive Data, differential analog input.
SP1_RXP	16		
SP1_TXN	13	O	SAS1 Transmit Data, differential analog output.
SP1_TXP	12		

Table 3-8 SATA Port 0 Interface Signals

Name	84-pin QFN Signal Number	Type	Description
STP0_ACTV_LED	26	O	SATA0 Active LED.
STP0_FLT_LED	32	O	SATA0 Fault LED.
STP0_RXN	77	I	SATA0 Receive Data, differential analog input.
STP0_RXP	78		
STP0_TXN	75	O	SATA0 Transmit Data, differential analog output.
STP0_TXP	74		

Table 3-9 SATA Port 1 Interface Signals

Name	84-pin QFN Signal Number	Type	Description
STP1_ACTV_LED	28	O	SATA1 Active LED.
STP1_FLT_LED	33	O	SATA1 Fault LED.
STP1_RXN	83	I	SATA1 Receive Data, differential analog input.
STP1_RXP	84		
STP1_TXN	81	O	SATA1 Transmit Data, differential analog output.
STP1_TXP	80		

Table 3-10 Clock and Reset Interface Signals

Signal Name	84-pin QFN Signal Number	Type	Description
REFCLKP	4	I	Reference Clock differential input, single-ended input.
RESET_N	18	I	Chip Power-On Reset. Active-low.

Table 3-11 Power Pins

Signal Name	84-pin QFN Signal Number	Type	Description
ISET	2	I	6 KΩ Bias current resistor. A 6 KΩ resistor must be connected between this pin and a via in the digital ground plane.
TP	1	O	Analog test port.
VAA_ANA	3 5	I	2.5V Power for Chip PLL, Current Source.
VAA_SP0	8	I	2.5V Power for SAS0 PHY.
VAA_SP1	14	I	2.5V Power for SAS1 PHY.
VAA_STP0	76	I	2.5V Power for SATA0 PHY.
VAA_STP1	82	I	2.5V Power for SATA1 PHY.
VDDOX	19 47 56 67	I	2.5V Power for I/O.

Table 3-11 Power Pins (continued)

Signal Name	84-pin QFN Signal Number	Type	Description
VDD	17 22 27 31 35 41 45 50 54 59 63 66 70 73	I	1.0V Digital Logic Power Supply.
VSS	11 79	Ground	Ground.

4 ELECTRICAL SPECIFICATIONS

This chapter contains the following sections:

4.1 Power Requirements

Table 4-1 describes the 88SF9210 power requirements.

Table 4-1 Total Power Dissipation

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Absolute digital I/O pad power supply	VDDOX				100	mA
Absolute digital power supply	VDD				500	mA
Absolute analog power supply for TBG	VAA_ANA				20	mA
Absolute analog power supply for SATA PHY 0	VAA_STP0				100	mA
Absolute analog power supply for SATA PHY 1	VAA_STP1				100	mA
Absolute analog power supply for SAS PHY 0	VAA_SP0				100	mA
Absolute analog power supply for SAS PHY 1	VAA_SP1				100	mA

4.2 Absolute Maximum Ratings

Table 4-2 describes the absolute maximum ratings for the 88SF9210.

Table 4-2 Absolute Maximum Ratings

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Absolute Digital Power Supply Voltage	VDD_{ABS}		-0.5		1.1	V
Absolute Digital I/O pad Supply Voltage	$VDDIO_{ABS}$		-0.4		2.75	V
Absolute Analog Power Supply Voltage for TBG	VAA_{ABS}		-0.5		2.75	V
Absolute Analog Power Supply Voltage for SATA PHY 0	VAA_STP0_{ABS}		-0.5		2.75	V
Absolute Analog Power Supply Voltage for SATA PHY 1	VAA_STP1_{ABS}		-0.5		2.75	V
Absolute Analog Power Supply Voltage for SAS PHY 0	VAA_SP0_{ABS}		-0.5		2.75	V
Absolute Analog Power Supply Voltage for SAS PHY 1	VAA_SP1_{ABS}		-0.5		2.75	V
Absolute Input Voltage	Vin_{ABS}		-0.4		3.63	V
Absolute Storage Temperature	$Tstor_{ABS}$		-55		+85	°C
Absolute Junction Temperature	$Tjunc_{ABS}$				125	°C

4.3 Recommended/Typical Operating Conditions

Table 4-3 describes the recommended and typical operating conditions for the 88SF9210.

Table 4-3 Recommended/Typical Operating Conditions

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Ambient Operating Temperature			0		70	°C
Junction Operating Temperature			0		125	°C
Operating Digital Power Supply Voltage	VDD_{OP}		0.9	1.0	1.1	V
Operating Digital I/O Pad Supply Voltage	$VDDIO_{OP}$		2.25	2.5	2.75	V
Operating Analog Power Supply Voltage for TBG	VAA_{OP}		2.5 - 8%	2.5	2.7	V
Operating Analog Power Supply Voltage for SATA PHY 0	VAA_STP0_{OP}		2.5 - 8%	2.5	2.7	V
Operating Analog Power Supply Voltage for SATA PHY 1	VAA_STP1_{OP}		2.5 - 8%	2.5	2.7	V
Operating Analog Power Supply Voltage for SAS PHY 0	VAA_SP0_{OP}		2.5 - 8%	2.5	2.7	V
Operating Analog Power Supply Voltage for SAS PHY 1	VAA_SP1_{OP}		2.5 - 8%	2.5	2.7	V

4.4 DC Characteristics

Table 4-4 lists the DC characteristics of the 88SF9210.

Table 4-4 DC Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Low Voltage	V_{IL}		-0.4		0.3 x VDDIO	V
Input High Voltage	V_{IH}		0.7 x VDDIO		3.63	V
Output Low Voltage	V_{OL}	I_{OL}=7 mA, VDDIO=2.46V	-0.4	0.13	0.4	V
Output High Voltage	V_{OH}	I_{OH}=7 mA, VDDIO=2.46V	2.25	2.5	VDDIO	V

4.5 Thermal Data

It is recommended to read application note *AN-63 Thermal Management for Selected Marvell® Products* (Document Number MV-S300281-00) and the *ThetaJC, ThetaJA, and Temperature Calculations White Paper*, available from Marvell, before designing a system. These documents describe the basic understanding of thermal management of integrated circuits (ICs) and guidelines to ensure optimal operating conditions for Marvell products.

Table 4-5 provides the thermal data for the 88SF9210. The simulation was performed according to JEDEC standards.

Table 4-5 shows the values for the package thermal parameters for the 84-lead Quad Flat Non-Lead package (QFN 84) mounted on a 6-layer PCB.

Table 4-5 Package Thermal Data, 6-Layer PCB*

Parameter	Definition	Airflow Value			
		0 m/s	1 m/s	2 m/s	3 m/s
θ_{JA}	Thermal resistance: junction to ambient	28.6 C/W	25.7 C/W	23.3 C/W	22.1 C/W
θ_{JB}	Thermal resistance: junction to board	1.7 C/W	–	–	–
θ_{JC}	Thermal resistance: junction to case	10.6 C/W	–	–	–

* All data is based on parts mounted on a 1” x 4” 6L PCB.

Table 4-6 shows the values for the package thermal parameters for the 84-lead Quad Flat Non-Lead package (QFN 84) mounted on a 4-layer PCB.

Table 4-6 Package Thermal Data, 4-Layer PCB*

Parameter	Definition	Airflow Value			
		0 m/s	1 m/s	2 m/s	3 m/s
θ_{JA}	Thermal resistance: junction to ambient	25.2 C/W	24.2 C/W	23.2 C/W	21.9 C/W
θ_{JB}	Thermal resistance: junction to board	1.7 C/W	–	–	–
θ_{JC}	Thermal resistance: junction to case	10.2 C/W	–	–	–

* All data is based on parts mounted on a 4” x 4.5” JEDEC 4L PCB.

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