32KX8 Bit High-Speed CMOS Static RAM(3.3V Operating)

FEATURES

- **Fast Access Time : 15, 17, 20, 25ns (Max.)**
- **Low Power Dissipation**
  Standby (TTL) : 30mA (MaX.)
  (CMOS) : 100μA (Max.)
  Operating : KM68V257-15 : 110mA (Max.)
  KM68V257-17 : 100mA (Max.)
  KM68V257-20 : 90mA (Max.)
  KM68V257-25 : 80mA (Max.)
- **Single 3.3V±0.3V power supply**
- **TTL compatible inputs and outputs**
- **2V Minimum Data Retention**
- **Fully Static Operation**
  - No clock or refresh required
- **Three State Output**
- **Standard Pin Configuration**
  KM68V257P : 28-DIP-300
  KM68V257J : 28-SOJ-300

GENERAL DESCRIPTION

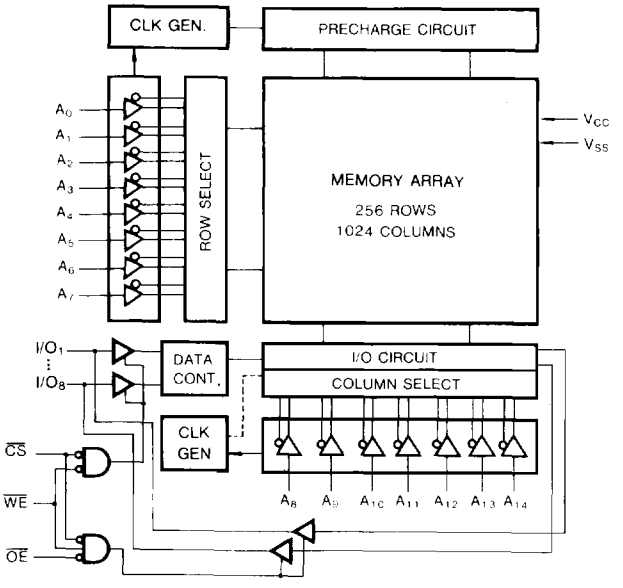
The KM68V257 is a 262,144-bit high-speed Static Random Access Memory organized as 32,768 words by 8 bits.

The KM68V257 uses eight common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using Samsung's advanced CMOS process and designed for high-speed system applications.

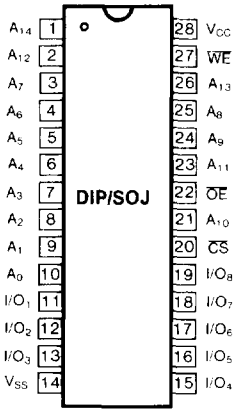
The KM68V257 is designed to operate at 3.3 volts. It is particularly well suited for use in high-density high-speed system applications.

The KM68V257 is packaged in a 300mil 28-pin plastic DIP or SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top View)



Pin Name	Pin Function
A_0-A_{14}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O_1~I/O_8	Data Inputs/Outputs
V_{CC}	Power (+3.3V)
V_{SS}	Ground

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−0.5 to 4.6	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 5.5	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	−65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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RECOMMENDED DC OPERATING CONDITIONS (T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.3*	—	0.8	V

*V_{IL}(min.) = −3.0V for ≤10 ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70°C, V_{CC}=3.3±0.3V, unless otherwise specified)

Item	Symbol	Test Condition		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to V_{CC}		-	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IN} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, $V_{I/O}$=Vss to V_{CC}		-	2	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty $\overline{CS}$=V_{IL}, I_{out}=0mA	15ns	-	110	mA
			17ns	-	100	mA
			20ns	-	90	mA
			25ns	-	80	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, Min Cycle.		-	30	mA
	I_{SB1}	$\overline{CS}$≥V_{CC}-0.2V, f= oMHz V_{IN}≥V_{CC}-0.2 or V_{IN}≤0.2V		-	100	μA
Output Low Voltage	V_{OL}	I_{OL}=8.0mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4.0mA		2.4	-	

CAPACITANCE (f=1MHz, T_A=25°C)*

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	—	6	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	—	8	pF

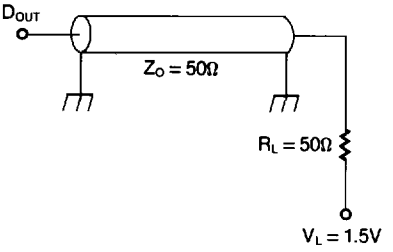
*Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS

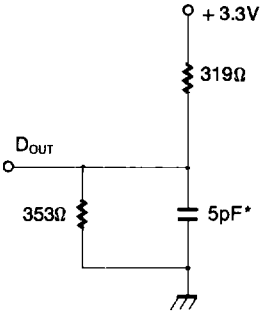
TEST CONDITIONS (T_A=0 to 70°C, V_{CC}=3.3±0.3V, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW}, t_{OLZ} & t_{OHZ})



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM68V257P-15 KM68V257J-15		KM68V257P-17 KM68V257J-17		KM68V257P-20 KM68V257J-20		KM68V257P-25 KM68V257J-25		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	15		17		20		25		ns
Address Access Time	t_{AA}		15		17		20		25	ns
Chip Select to Output	t_{CO}		15		17		20		25	ns
Output Enable to Valid Output	t_{OE}		8		8		10		12	ns
Chip Select to Low-Z Output	t_{LZ}	3		3		3		3		ns
Output Enable to Low-Z Output	t_{OLZ}	0		0		0		0		ns
Chip Disable to High-Z Output	t_{HZ}	0	10	0	10	0	10	0	10	ns
Output Disable to High-Z Output	t_{OHZ}	0	6	0	6	0	8	0	10	ns
Output Hold from Address Change	t_{OH}	3		3		3		3		ns
Chip Selection to Power Up Time	t_{PU}	0		0		0		0		ns
Chip Selection to Power Down Time	t_{PD}		15		17		20		25	ns

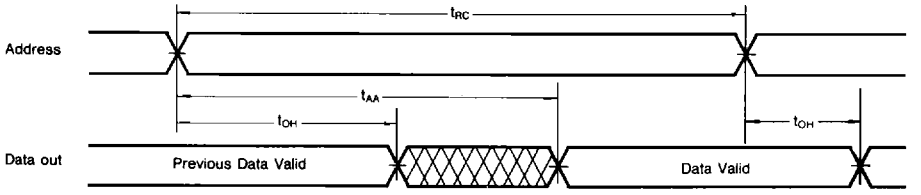
WRITE CYCLE

Parameter	Symbol	KM68V257P-15 KM68V257J-15		KM68V257P-17 KM68V257J-17		KM68V257P-20 KM68V257J-20		KM68V257P-25 KM68V257J-25		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	15		17		20		25		ns
Chip Select to End of Write	t_{CW}	12		12		13		14		ns
Address Set-up Time	t_{AS}	0		0		0		0		ns
Address Valid to End of Write	t_{AW}	12		12		13		14		ns
Write Pulse Width	t_{WP}	12		12		13		14		ns
Write Recovery Time	t_{WR}	0		0		0		0		ns
Write to Output High-Z	t_{WZ}	0	6	0	6	0	8	0	10	ns
Data to Write Time Overlap	t_{DW}	8		8		10		12		ns
Data Hold from Write Time	t_{DH}	0		0		0		0		ns
End Write to Output Low-Z	t_{OW}	0		0		0		0		ns

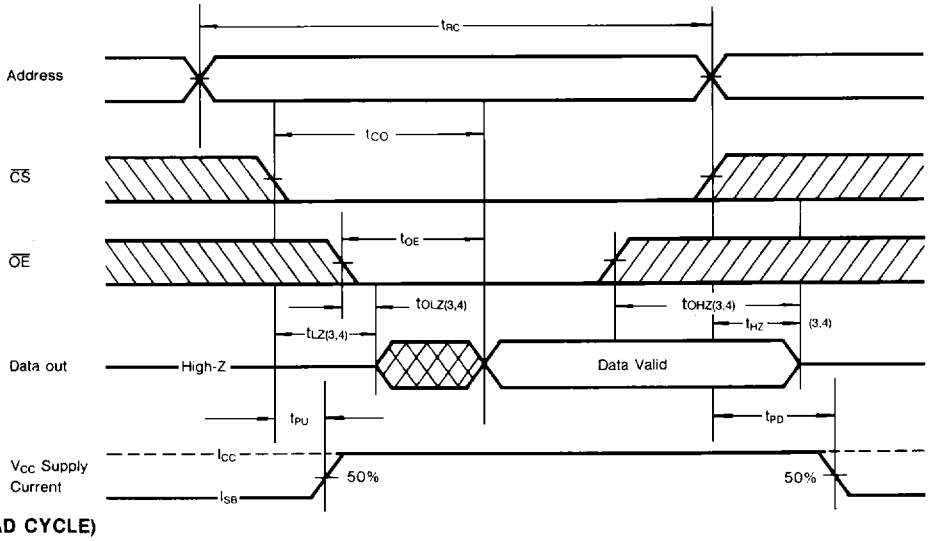
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (Address Controlled)

($\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH})



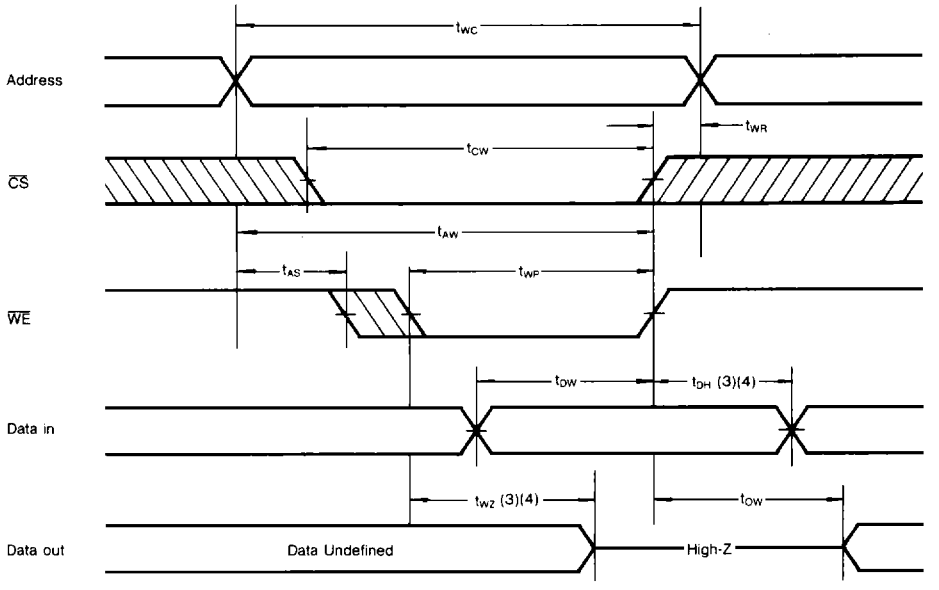
TIMING WAVEFORM OF READ CYCLE



Note (READ CYCLE)

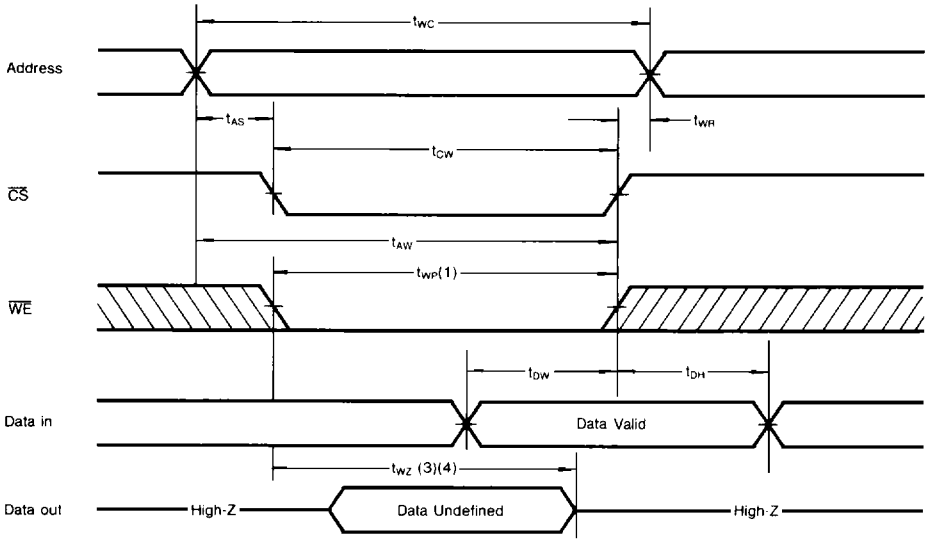
1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
5. Address valid prior to or conincident with $\overline{CS}$ transition low
6. Device is continuously selected with $\overline{CS}$=VIL.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



SAMSUNG ELECTRONICS

TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltage with Load (B).
   This parameter is sampled and not 100% tested.
4. At any given temperature and voltage condition, t_{WZ}(max.) is less than t_{OW}(min.) both for a given device and from device to device.
5. $\overline{CS}$ or $\overline{WE}$ must be in high during address transition.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X *	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

* Note: X means Don't Care

DATA RETENTION CHARACTERISTICS* (T_A=0 to 70°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}$-0.2V	2	-	3.6	V
Data Retention Current	I_{DR}	V_{CC}=0.3V, $\overline{CS} \geq V_{CC}$-0.2V $V_{IN} \geq 0.2V$ or $V_{IN} \leq 0.2V$	-	1**	50	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention	0	-	-	ns
Recovery Time	t_{RDR}	Wave forms(below)	t_{RC}*	-	-	ns

* t_{RC}=Read Cycle time
**Temp=25° C

DATA RETENTION WAVEFORM