M5M5408P,FP,TP,RT-55L,-70L,-10L, -55LL,-70LL,-10LL

4194304-BIT (524288-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5408 is 4194304-bit CMOS static RAM organized as 524288-words by 8-bit, fabricated using high-performance quadruple-polysilicon and double metal CMOS technology.

The use of thin film transistor (TFT) load cells and CMOS periphery results in a high density and low power static RAM. The M5M5408 is designed for memory applications where the high performance, high reliability, large storage, simple interfacing and battery back-up are important design objectives.

The M5M5408 is offered in a 32-pin plastic dual-in-line package (DIP), 32-pin plastic small outline package (SOP) as well as 32-pin thin small outline package (TSOP), providing high board level packing densities. Two types of TSOP packages are available, M5M5408TP (normal lead bend type package) and M5M5408RT (reverse lead bend type package). Using both two types makes it easy to design a printed circuit board.

FEATURES

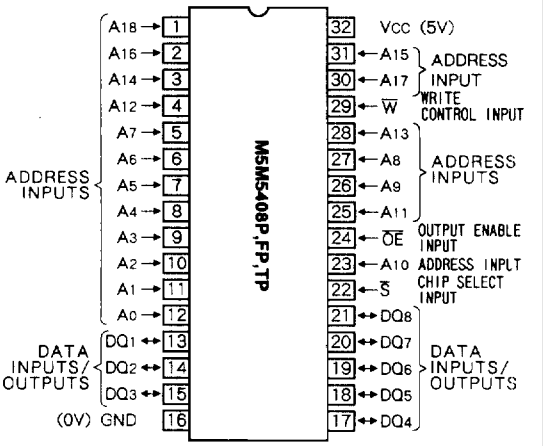
Type name	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M5408P, FP, TP, RT-55L M5M5408P, FP, TP, RT-70L M5M5408P, FP, TP, RT-10L	55ns 70ns 100ns	30mA (1MHz)	100 μA (Vcc = 5.5V)
M5M5408P, FP, TP, RT-55LL M5M5408P, FP, TP, RT-70LL M5M5408P, FP, TP, RT-10LL	55ns 70ns 100ns		20 μA (Vcc = 5.5V) 0.4 μA (Vcc = 3V, typ)

- Single +5V power supply
- No clocks, no refresh
- All inputs and outputs are TTL compatible
- Easy memory expansion and power down by $\overline{S}$
- Data retention supply voltage = 2.0V to 5.5V
- Three-state outputs : OR-tie capability
- $\overline{OE}$ prevents data contention in the I/O bus
- Common data I/O
- Small stand-by current ..... 0.4 μA (typ)
- Battery back-up capability
- Package
  - M5M5408P : 32-pin 600mil DIP
  - M5M5408FP : 32-pin 525mil SOP
  - M5M5408TP : 32-pin 400mil TSOP (II)
  - M5M5408RT : 32-pin 400mil TSOP (II)

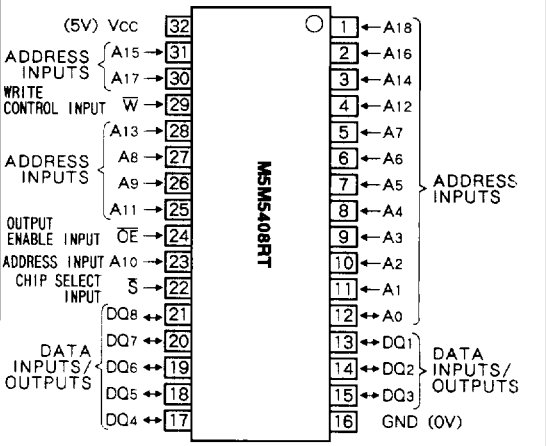
APPLICATION

Small capacity memory units, IC card, battery operating system

PIN CONFIGURATION (TOP VIEW)



Outline 32P4(P)
32P2M-A(FP)
32P3Y-H(TP)

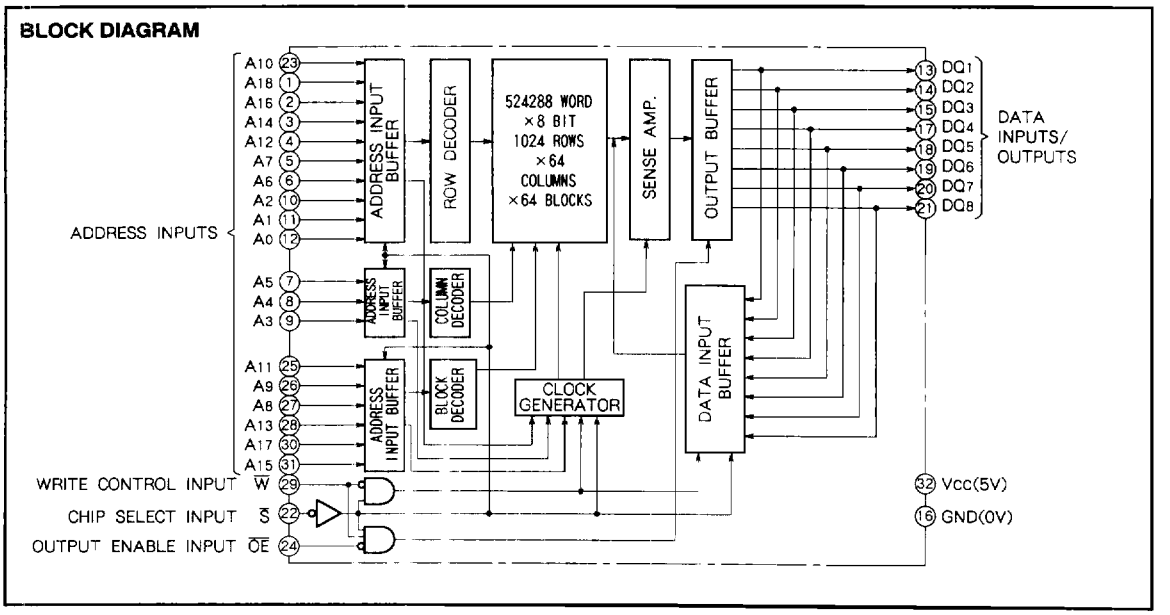


Outline 32P3Y-J

M5M5408P,FP,TP,RT-55L,-55LL M5M5408P-70L,-70LL,-10L,-10LL : Under development

MITSUBISHI ELECTRIC

BLOCK DIAGRAM



FUNCTION

The operation mode of the M5M5408 is determined by a combination of the device control inputs $\overline{S}$, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S}$. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, or $\overline{S}$ whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input $\overline{OE}$ directly controls the output state. Setting the $\overline{OE}$ at a high level, the output state is in a highimpedance state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S}$ is in an active state ($\overline{S}$ = L).

When setting $\overline{S}$ at a high level, the chips are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output state is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S}$. The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4}, and the memory data can be held at – 2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S}$	$\overline{W}$	$\overline{OE}$	Mode	DQ	Icc
H	X	X	Non selection	High-impedance	Stand-by
L	L	X	Write	Din	Active
L	H	L	Read	Dout	Active
L	H	H		High-impedance	Active

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	− 0.3~7	V
V_I	Input voltage	With respect to GND	− 0.3 * ~V_{CC} + 0.3	V
V_O	Output voltage	With respect to GND	0~V_{CC}	V
P_c	Power dissipation	T_a = 25℃	700	mW
T_{opr}	Operating temperature		0~70	℃
T_{stg}	Storage temperature		− 65~150	℃

* − 3.0V in case of AC (Pulse width ≤ 50ns)

DC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, Vcc = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High-level input voltage			2.2		V_{CC}+0.3	V
V_{IL}	Low-level input voltage			− 0.3 *		0.8	V
V_{OH}	High-level output voltage	I_{OH} = − 1mA		2.4			V
		I_{OH} = − 0.1mA		V_{CC}−0.5			
V_{OL}	Low-level output voltage	I_{OL} = 2.1mA				0.4	V
I_I	Input leakage current	V_I = 0~V_{CC}				± 1	μA
I_O	Output leakage current	$\overline{S}$ = V_{IH}, $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0~V_{CC}				± 1	μA
I_{CC1}	Active supply current (AC, MOS level)	$\overline{S}$ ≦ 0.2, other inputs ≦ 0.2V or ≧ V_{CC}−0.2V, Output-open (duty 100%)	minimum cycle		50	80	mA
			1MHz		25	30	
I_{CC2}	Active supply current (AC, TTL level)	$\overline{S}$ = V_{IL}, other inputs = V_{IH} or V_{IL}, Output-open (duty 100%)	minimum cycle		60	90	mA
			1MHz		30	40	
I_{CC3}	Stand by current	$\overline{S}$ ≧ V_{CC} − 0.2V, other inputs = 0~V_{CC}	P,FP,TP, RT-L			100	μA
			P,FP,TP, RT-LL		1.0	20	
I_{CC4}	Stand by current	$\overline{S}$ = V_{IH}, other inputs = 0~V_{CC}				3	mA

* − 3.0V in case of AC (Pulse width ≤ 50ns)

CAPACITANCE (Ta = 0~70℃, Vcc = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
C_I	Input capacitance	V_I = GND, V_I = 25mVrms, f = 1MHz			6	pF
C_O	Output capacitance	V_O = GND, V_O = 25mVrms, f = 1MHz			8	pF

Note 1. Direction for current flowing into an IC is positive (no mark).
2. Typical value is Vcc = 5V, Ta = 25℃.

AC ELECTRICAL CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse levels ····· V_{IH} = 2.4V, V_{IL} = 0.6V (P, FP, TP, RT / -70L, -10L, -70LL, -10LL)

V_{IH} = 3.0V, V_{IL} = 0V (P, FP, TP, RT-55L, -55LL)

Input rise and fall time ····· 5ns

Reference levels ····· V_{OH} = V_{OL} = 1.5V

Transition in measured ± 500mV from steady state voltage. (for t_{en}, t_{dis})

Output loads ····· Fig.1, C_L = 100pF (P, FP, TP, RT-10L, -10LL)

C_L = 30pF (P, FP, TP, RT-55L, -70L, -55LL, -70LL)

C_L = 5pf (for t_{en}, t_{dis})

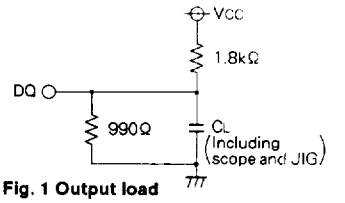


Fig. 1 Output load

(2) READ CYCLE

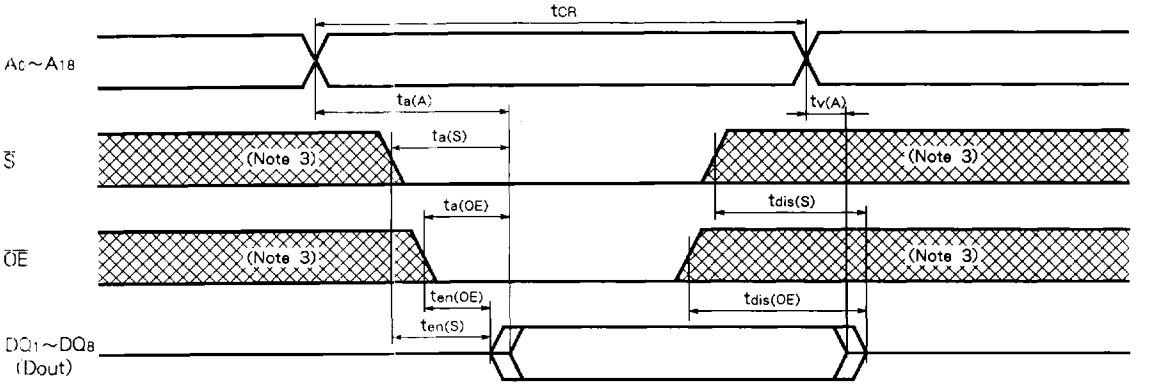
Symbol	Parameter	Limits						Unit
		M5M5408P, FP, TP, RT-55L, -55LL		M5M5408P, FP, TP, RT-70L, -70LL		M5M5408P, FP, TP, RT-10L, -10LL		
		Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	55		70		100		ns
$t_{a(A)}$	Address access time		55		70		100	ns
$t_{a(S)}$	Chip select access time		55		70		100	ns
$t_{a(OE)}$	Output enable access time		25		35		50	ns
$t_{dis(S)}$	Output disable time after $\overline{S}$ high		20		25		35	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high		20		25		35	ns
$t_{en(S)}$	Output enable time after $\overline{S}$ low	10		10		10		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5		5		5		ns
$t_{v(A)}$	Data valid time after address	10		10		10		ns

(3) WRITE CYCLE

Symbol	Parameter	Limits						Unit
		M5M5408P, FP, TP, RT-55L, -55LL		M5M5408P, FP, TP, RT-70L, -70LL		M5M5408P, FP, TP, RT-10L, -10LL		
		Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time	55		70		100		ns
$t_{w(W)}$	Write pulse width	40		50		60		ns
$t_{su(A)}$	Address set up time	0		0		0		ns
$t_{su(A-WH)}$	Address set up time with respect to $\overline{W}$ high	50		60		80		ns
$t_{su(S)}$	Chip select set up time	50		60		80		ns
$t_{su(D)}$	Data set up time	25		30		35		ns
$t_{h(D)}$	Data hold time	0		0		0		ns
$t_{rec(W)}$	Write recovery time	0		0		0		ns
$t_{dis(W)}$	Output disable time from $\overline{W}$ low		20		25		35	ns
$t_{dis(OE)}$	Output disable time from $\overline{OE}$ high		20		25		35	ns
$t_{en(W)}$	Output enable time from $\overline{W}$ high	5		5		5		ns
$t_{en(OE)}$	Output enable time from $\overline{OE}$ low	5		5		5		ns

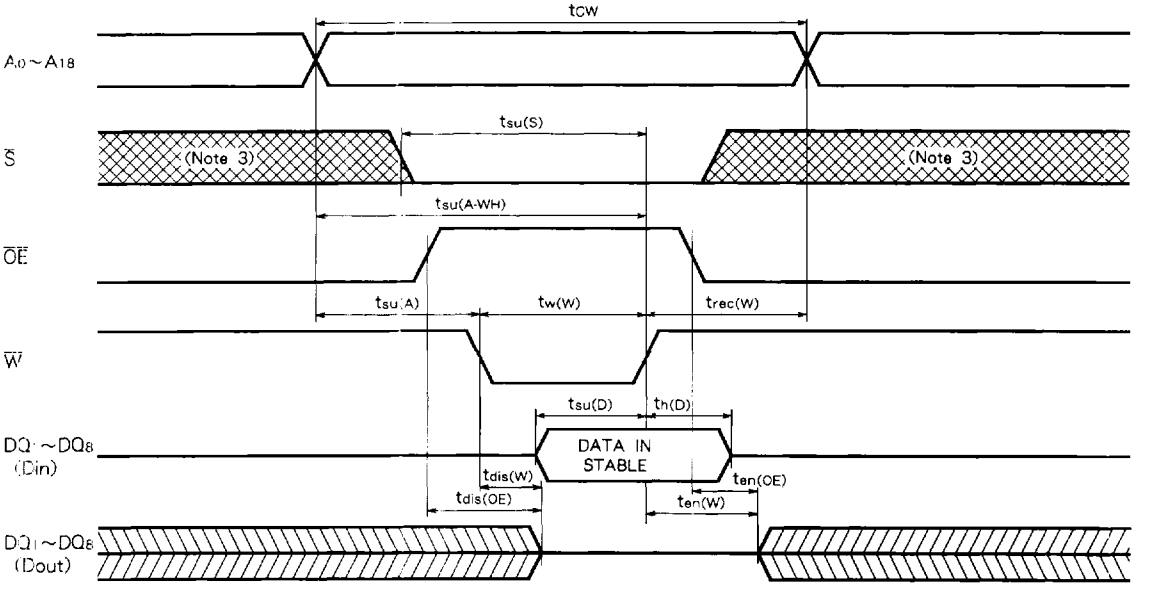
(4) TIMING DIAGRAMS

Read cycle

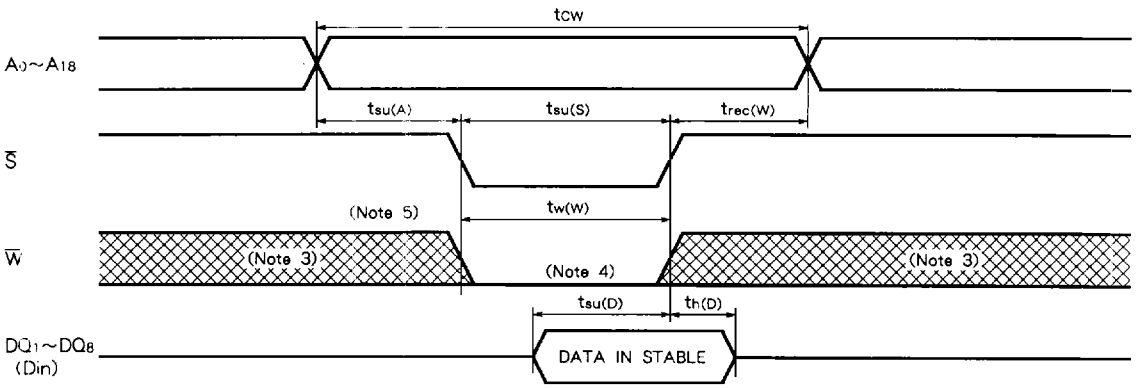


W = "H" level

Write cycle (W control mode)



Write cycle ($\overline{S}$ control mode)



Note 3. Hatching indicates the state is "don't care".
4. A write occurs during the overlap of a low $\overline{S}$ and low $\overline{W}$.
5. If $\overline{W}$ goes low simultaneously with or prior to $\overline{S}$, the output remains in the high impedance state.
6. Don't apply inverted phase signal externally when DQ pin is in output mode.

POWER DOWN CHARACTERISTICS

ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage			2			V
$V_{I(S)}$	Chip select input $\overline{S}$	2.2 ≦ $V_{CC(PD)}$		2.2			V
		2V ≦ $V_{CC(PD)}$ ≦ 2.2V			$V_{CC(PD)}$		
$I_{CC(PD)}$	Power down supply current	V_{CC} = 3V, $\overline{S}$ ≧ V_{CC} − 0.2V, other inputs = 0~3V	P,FP,TP, RT-L			50	μA
			P,FP,TP, RT-LL		0.4	10 *	

Note 7. When $\overline{S}$ is at 2.2V (V_{IH} min) and the supply voltage is at any level between 4.5V and 2.4V, supply current is defined as I_{CC4}.
* $I_{CC(PD)}$ = 1 μA at Ta = 25℃.

TIMING REQUIREMENTS (Ta = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(PD)}$	Power down set up time		0			ns
$t_{rec(PD)}$	Power down recovery time		5			ms

POWER DOWN CHARACTERISTICS

$\overline{S}$ control mode