FUJITSU MICROELECTRONICS
DATA SHEET

DS04–27270–1E

*ASSP for Power Management Applications (General-Purpose DC/DC Converter)*

# 2ch DC/DC converter IC with synchronous rectification

# MB39A138

## ■ DESCRIPTION

MB39A138 is a 2ch step-down DC/DC converter equipped with a bottom detection comparator and N-ch/N-ch synchronous rectification. It supports low on-duty operation to allow stable output of low voltages when there is a large difference between input and output voltages. MB39A138 realizes ultra-rapid response and high efficiency with built-in enhanced protection features.

## ■ FEATURES

- High efficiency
- High accurate reference voltage : ±1.0% (indoor temperature )
- Input voltage range : 6 V to 24 V
- Output voltage setting range : CH1 0.7 V to 5.2 V
  : CH2 2.0 V to 5.2 V
- Built-in diode for boot strap
- Built-in over voltage protection function
- Built-in under voltage protection function
- Built-in over current detection function
- Built-in over temperature protection function
- Built-in soft-start circuit without load dependence
- Built-in discharge control circuit
- Built-in synchronous rectification type output steps for N-ch MOS FET
- Standby current : 0 μA (Typ)
- Small package : TSSOP-24

## ■ APPLICATIONS

- Digital TV
- Photocopiers
- STB
- BD, DVD players/recorders
- Projectors
  Various other advanced devices


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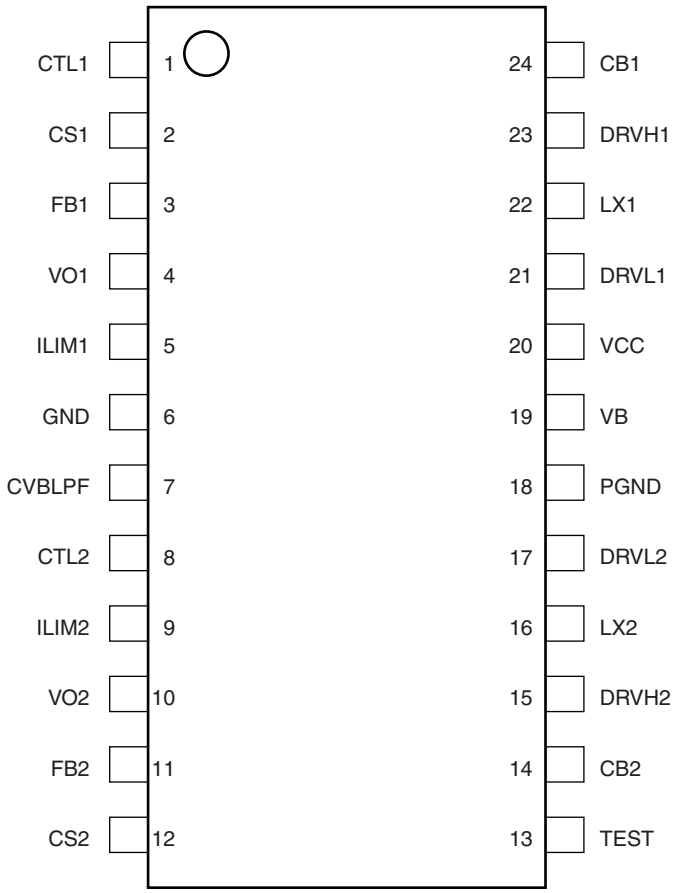
## ■ PIN ASSIGNMENT

(TOP VIEW)

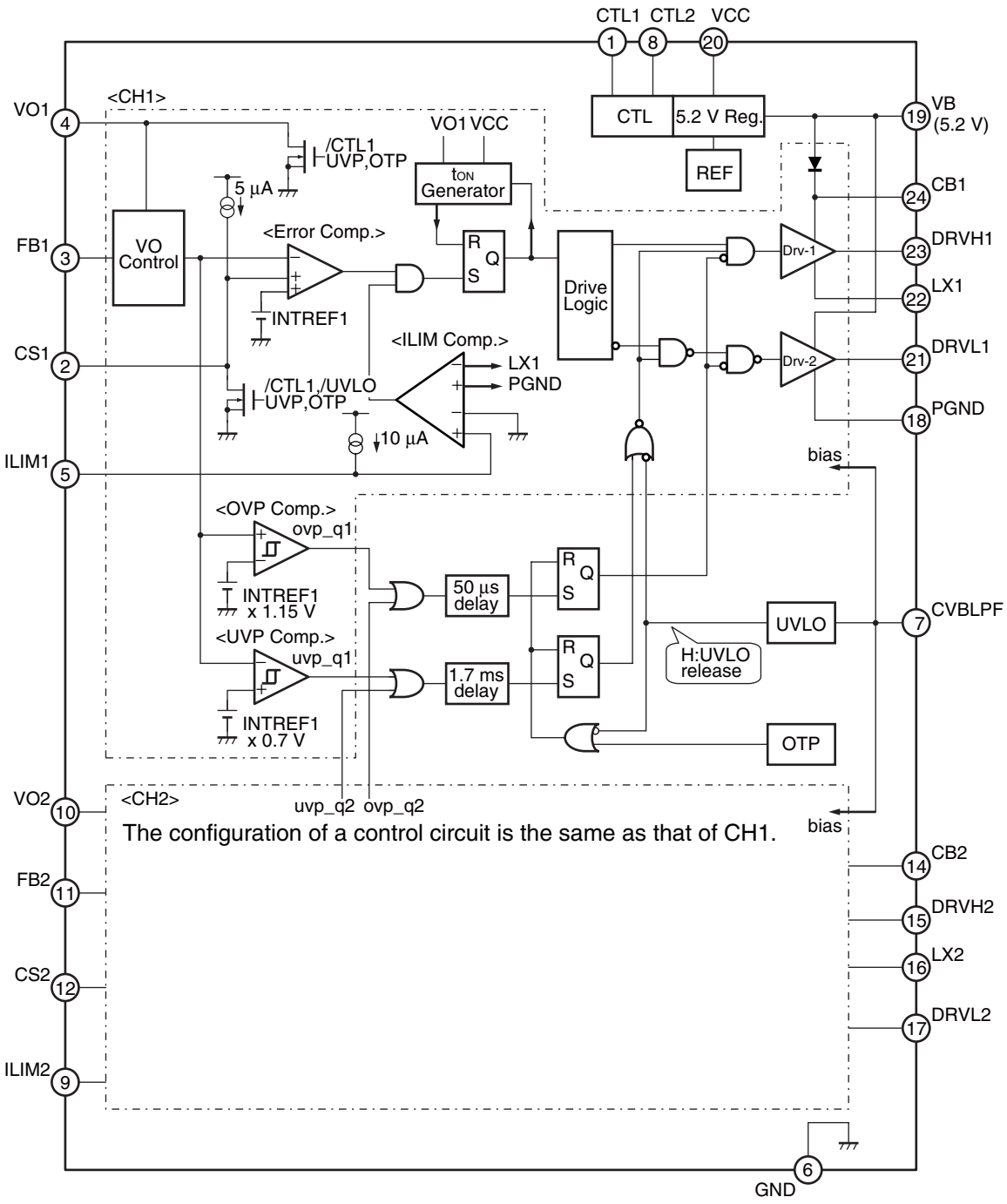



(FPT-24P-M10)

## ■ PIN DESCRIPTIONS

| Pin No. | Pin Name | I/O | Description |
|---|---|---|---|
| 1 | CTL1 | I | CH1 control pin. |
| 2 | CS1 | I | CH1 start time setting capacitor connection pin. |
| 3 | FB1 | I | CH1 feedback pin for DC/DC output voltage. |
| 4 | VO1 | I | CH1 input pin for DC/DC output voltage. |
| 5 | ILIM1 | I | CH1 over current detection level setting voltage input pin. |
| 6 | GND | — | Ground pin. |
| 7 | CVBLPF | I | Control circuit bias input pin. |
| 8 | CTL2 | I | CH2 control pin. |
| 9 | ILIM2 | I | CH2 over current detection level setting voltage input pin. |
| 10 | VO2 | I | CH2 input pin for DC/DC output voltage. |
| 11 | FB2 | I | CH2 feedback pin for DC/DC output voltage. |
| 12 | CS2 | I | CH2 soft-start time setting capacitor connection pin. |
| 13 | TEST | I | Pin for IC test. Connect to GND in the DC/DC operation. |
| 14 | CB2 | — | CH2 connection pin for boot strap capacitor. |
| 15 | DRVH2 | O | CH2 output pin for external high-side FET drive. |
| 16 | LX2 | — | CH2 inductor and external high-side FET source connection pin. |
| 17 | DRVL2 | O | CH2 output pin for external low-side FET gate drive. |
| 18 | PGND | — | Ground pin for output circuit. |
| 19 | VB | O | Output circuit bias output pin. |
| 20 | VCC | I | Power supply pin for reference voltage and control circuit. |
| 21 | DRVL1 | O | CH1 output pin for external low-side FET gate drive. |
| 22 | LX1 | — | CH1 inductor and external high-side FET source connection pin. |
| 23 | DRVH1 | O | CH1 output pin for external high-side FET gate drive. |
| 24 | CB1 | — | CH1 connection pin for boot strap capacitor. |

## ■ BLOCK DIAGRAM



## ■ ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Condition | Rating | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| Power supply voltage | $V_{VCC}$ | — | — | 26 | V |
| CB pin input voltage | $V_{CB}$ | CB1, CB2 pins | — | 32 | V |
| LX pin input voltage | $V_{LX}$ | LX1, LX2 pins | — | 26 | V |
| Voltage between CB and LX | $V_{CBLX}$ | — | — | 7 | V |
| Control input voltage | $V_I$ | CTL1, CTL2 pins | — | 26 | V |
| Input voltage | $V_{CVBLPF}$ | CVBLPF pin | — | VB + 0.3 | V |
| | $V_{FB}$ | FB1, FB2 pins | — | VB + 0.3 | V |
| | $V_{VO}$ | VO1, VO2 pins | — | VB + 0.3 | V |
| | $V_{CS}$ | CS1, CS2 pins | — | VB + 0.3 | V |
| | $V_{ILIM}$ | ILIM1, ILIM2 pins | — | VB + 0.3 | V |
| | $V_{TEST}$ | TEST pin | — | VB + 0.3 | V |
| Output current | $I_{OUT}$ | DRVH1, DRVH2 pins, DRVL1, DRVL2 pins | — | 60 | mA |
| Power dissipation | $P_D$ | Ta ≤ + 25 °C | — | 1333 | mW |
| Storage temperature | $T_{STG}$ | — | − 55 | + 125 | °C |

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## ■ RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| Power supply voltage | $V_{VCC}$ | — | 6 | — | 24 | V |
| CB pin input voltage | $V_{CB}$ | — | — | — | 30 | V |
| Bias output current | $I_{VB}$ | — | − 1 | — | — | mA |
| CTL pin input voltage | $V_I$ | CTL1, CTL2 pins | 0 | — | 24 | V |
| Input voltage | $V_{CVBLPF}$ | CVBLPF pin | 0 | — | VB | V |
| | $V_{FB}$ | FB1, FB2 pins | 0 | — | VB | V |
| | $V_{VO}$ | VO1, VO2 pins | 0 | — | VB | V |
| | $V_{ILIM}$ | ILIM1, ILIM2 pins | 30 | — | 200 | mV |
| Peak output current | $I_{OUT}$ | DRVH1, DRVH2 pins, DRVL1, DRVL2 pins Duty ≤ 5% ($t = 1/f_{OSC} \times Duty$) | − 1200 | — | + 1200 | mA |
| Soft start capacitor | $C_{CS}$ | — | — | 0.018 | — | µF |
| CB pin capacitor | $C_{CB}$ | — | — | 0.1 | 1.0 | µF |
| Bias voltage output capacitor | $C_{VB}$ | — | — | 2.2 | 10.0 | µF |
| Bias voltage input capacitor | $C_{CVBLPF}$ | — | — | 1.0 | 4.7 | µF |
| Operating ambient temperature | Ta | — | − 30 | + 25 | + 85 | °C |

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

## ■ ELECTRICAL CHARACTERISTICS

(Ta = + 25 °C, VCC pin = 12 V, CTL1, CTL2 pins = 5 V = CVBLPF pin : VB pin connected)

| Parameter | | Symbol | Pin No. | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| Bias Voltage Block [VB Reg.] | Output voltage | $V_{VB}$ | 19 | — | 5.04 | 5.20 | 5.36 | V |
| | Input stability | LINE | 19 | VCC pin = 6 V to 24 V | — | 10 | 100 | mV |
| | Load stability | LOAD | 19 | VB pin = 0 A to –1 mA | — | 10 | 100 | mV |
| | Short-circuit output current | $I_{OS}$ | 19 | VB pin = 0 V | – 200 | – 140 | – 100 | mA |
| Under voltage Lockout Protection Circuit Block [UVLO] | Threshold voltage | $V_{TLH}$ | 7 | CVBLPF pin | 4.0 | 4.2 | 4.4 | V |
| | | $V_{THL}$ | 7 | CVBLPF pin | 3.4 | 3.6 | 3.8 | V |
| | Hysteresis width | $V_H$ | 7 | CVBLPF pin | — | 0.6* | — | V |
| Soft-Start/ Discharge Block [Soft-Start, Discharge] | Charge current | $I_{CS}$ | 2, 12 | CS1, CS2 pins = 0 V | – 7.1 | – 5.0 | – 3.8 | µA |
| | Electrical discharge resistance | $R_D$ | 4, 10 | CTL1, CTL2 pins = 0 V, VO1, VO2 pins = 0.5 V | — | 35 | 70 | Ω |
| | Discharge end voltage | $V_{VOVTH}$ | 4, 10 | CTL1, CTL2 pins = 0 V, VO1, VO2 pins | 0.1 | 0.2 | 0.3 | V |
| ON/OFF Time Generator Block [tON Generator] | ON time | $t_{ON11}$ | 23 | VCC pin = 12 V, VO1 pin = 1.2 V | 256 | 320 | 384 | ns |
| | | $t_{ON12}$ | 15 | VCC pin = 12 V, VO2 pin = 3.3 V | 470 | 587 | 704 | ns |
| | Minimum ON time | $t_{ONMIN}$ | 23, 15 | VCC pin = 12 V, VO1, VO2 pins = 0 V | — | 100 | — | ns |
| | Minimum OFF time | $t_{OFFMIN}$ | 23, 15 | — | — | 380 | — | ns |
| Output Voltage Block [VO Control, Error Comp.] | Feedback voltage (CH1) | $V_{TH1}$ | 3 | Ta = + 25 °C | 0.693 | 0.700 | 0.707 | V |
| | | $V_{THT1}$ | 3 | Ta = 0 °C to + 85 °C | 0.690* | — | 0.710* | V |
| | Feedback voltage (CH2) | $V_{TH2}$ | 11 | Ta = + 25 °C | 1.980 | 2.000 | 2.020 | V |
| | | $V_{THT2}$ | 11 | Ta = 0 °C to +85 °C | 1.970* | — | 2.030* | V |
| | Bottom detection voltage (CH1) | $V_{TH3}$ | 4 | Ta = + 25 °C | 1.202 | 1.226 | 1.250 | V |
| | | $V_{THT3}$ | 4 | Ta = 0 °C to + 85 °C | 1.196 | — | 1.256 | V |
| | Bottom detection voltage (CH2) | $V_{TH4}$ | 10 | Ta = + 25 °C | 3.381 | 3.450 | 3.519 | V |
| | | $V_{THT4}$ | 10 | Ta = 0 °C to + 85 °C | 3.364 | — | 3.536 | V |
| | FB pin input current | $I_{FB}$ | 3, 11 | FB1, FB2 pins = 0.8 V | – 0.1 | 0 | + 0.1 | µA |
| | VO pin input current | $I_{VO1}$ | 4 | VO1 pin = 1.226 V | — | 80 | 115 | µA |
| | | $I_{VO2}$ | 10 | VO2 pin = 3.450 V | — | 225 | 325 | µA |
| Over-voltage Protection Circuit Block [OVP Comp.] | Over-voltage detecting voltage | $V_{OVP}$ | 3, 11 (4, 10) | Error Comp. input | INTREF × 1.11 | INTREF × 1.15 | INTREF × 1.19 | V |
| | Over-voltage detection time | $t_{OVP}$ | 3, 11 (4, 10) | — | — | 50 | — | µs |

*(Continued)*

(Ta = + 25 °C, VCC pin = 12 V, CTL1, CTL2 pins = 5 V = CVBLPF pin : VB pin connected)

| Parameter | | Symbol | Pin No. | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| Under-voltage Protection Circuit Block [UVP Comp.] | Under-voltage detecting voltage | $V_{UVP}$ | 3, 11 (4, 10) | Error Comp. input | INTREF × 0.65 | INTREF × 0.70 | INTREF × 0.75 | V |
| | Under-voltage detection time | $t_{UVP}$ | 3, 11 (4, 10) | — | 1.2* | 1.7* | 2.2* | ms |
| Over-temperature Protection Circuit Block [OTP] | Protection temperature | $T_{OTPH}$ | — | — | — | + 150* | — | °C |
| | | $T_{OTPL}$ | — | — | — | + 125* | — | °C |
| Output Block [DRV] | High-side output on-resistance | $R_{OH}$ | 23, 15 | DRVH1, DRVH2 pins = −100 mA | — | 5 | 7 | Ω |
| | | $R_{OL}$ | 23, 15 | DRVH1, DRVH2 pins = 100 mA | — | 1.5 | 2.5 | Ω |
| | Low-side output on-resistance | $R_{OH}$ | 21, 17 | DRVL1, DRVL2 pins = −100 mA | — | 4 | 6 | Ω |
| | | $R_{OL}$ | 21, 17 | DRVL1, DRVL2 pins = 100 mA | — | 1 | 2 | Ω |
| | Output source current | $I_{SOURCE}$ | 23, 15 | LX1, LX2 pins = 0 V, CB1, CB2 pins = VB DRVH1, DRVH2 pins = 2.5 V Duty ≤ 5% | — | − 0.4* | — | A |
| | | | 21, 17 | LX1, LX2 pins = 0 V, CB1, CB2 pins = VB DRVL1, DRVL2 pins = 2.5 V Duty ≤ 5% | — | − 0.5* | — | A |
| | Output sink current | $I_{SINK}$ | 23, 15 | LX1, LX2 pins = 0 V, CB1, CB2 pins = VB DRVH1, DRVH2 pins = 2.5 V Duty ≤ 5% | — | 0.7* | — | A |
| | | | 21, 17 | LX1, LX2 pins = 0 V, CB1, CB2 pins = VB DRVL1, DRVL2 pins = 2.5 V Duty ≤ 5% | — | 0.9* | — | A |
| | Dead time | $t_D$ | 23, 21 15, 17 | LX1, LX2 pins = 0 V, CB1, CB2 pins = VB pin DRVL1, DRVL2 pins-low to DRVH1, DRVH2 pins-on | — | 40 | — | ns |
| | | | | LX1, LX2 pins = 0 V, CB1, CB2 pins = VB pin DRVH1, DRVH2 pins-low to DRVL1, DRVL2 pins-on | — | 80 | — | ns |
| | Diode voltage | $V_F$ | 24, 14 | $I_F$ = 10 mA | 0.7 | 0.8 | 0.9 | V |
| | Leak current | $I_{LEAK}$ | 24, 14 | CB1, CB2 pins = 30 V, LX1, LX2 pins = 24 V Ta = + 25 °C | — | 0.1 | 1 | µA |

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*(Continued)*

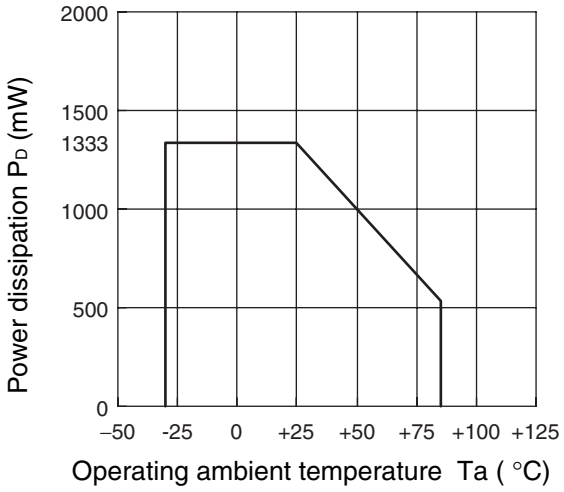
(Ta = + 25 °C, VCC pin = 12 V, CTL1, CTL2 pins = 5 V = CVBLPF pin : VB pin connected)

| Parameter | | Symbol | Pin No. | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| Over Current Detection Block [Current Sense] | ILIM pin source current | $I_{ILIM}$ | 5, 9 | ILIM1, ILIM2 pins = 0.1 V, Ta = + 25 °C | − 12.5 | − 10.0 | − 8.3 | µA |
| | ILIM pin source current temperature slope | $T_{ILIM}$ | 5, 9 | Ta = + 25 °C (reference) | — | 4200* | — | ppm / °C |
| | Over current detection offset voltage | $V_{OFFILIM}$ | 5, 9 | ILIMx − (PGND − LXx) PGND − LXx = 60 mV | − 20 | 0 | + 20 | mV |
| | Over current detection setting range | $V_{ILIM}$ | 5, 9 | ILIM pin input range | 30 | — | 200 | mV |
| Control Block [CTL1, CTL2] | ON condition | $V_{ON}$ | 1, 8 | CTL1, CTL2 pins | 2 | — | 24 | V |
| | OFF condition | $V_{OFF}$ | 1, 8 | CTL1, CTL2 pins | 0 | — | 0.8 | V |
| | Hysteresis width | $V_H$ | 1, 8 | CTL1, CTL2 pins | — | 0.4* | — | V |
| | Input current | $I_{CTLH}$ | 1, 8 | CTL1, CTL2 pins = 5 V | — | 25 | 40 | µA |
| | | $I_{CTLL}$ | 1, 8 | CTL1, CTL2 pins = 0 V | — | 0 | 1 | µA |
| General | Standby current | $I_{CCS}$ | 20 | CTL1, CTL2 pins = 0 V | — | 0 | 10 | µA |
| | Power supply current | $I_{CC}$ | 20 | LX1, LX2 pins = 0 V, FB1, FB2 pins = 1.0 V | — | 1.5 | 2.0 | mA |

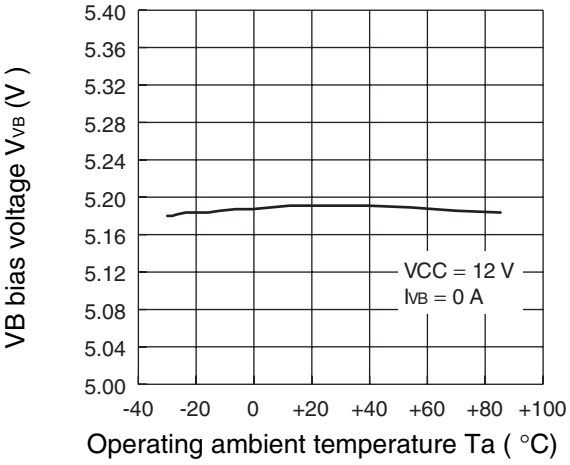
* : This parameter is not be specified. This should be used as a reference to support designing the circuits.

## ■ TYPICAL CHARACTERISTICS

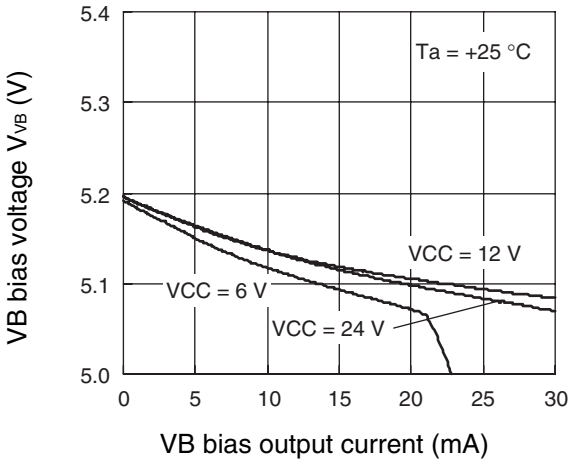
Power dissipation vs.
Operating ambient temperature



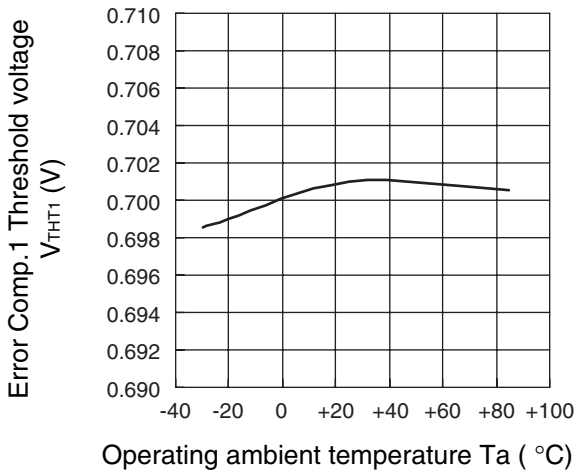

VB bias voltage vs.
Operating ambient temperature



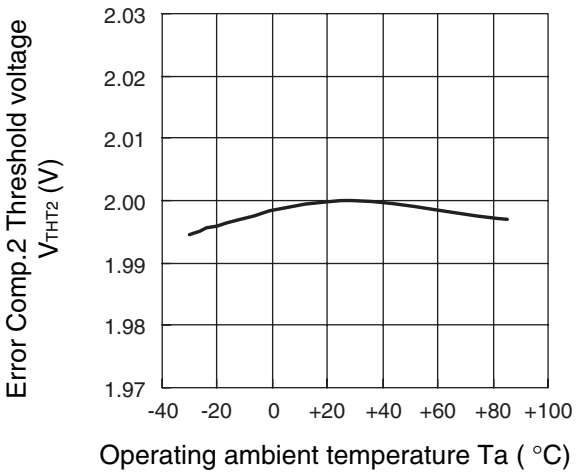

VB bias voltage vs.
VB bias output current




Error Comp.1 Threshold voltage vs.
Operating ambient temperature




Error Comp.2 Threshold voltage vs.
Operating ambient temperature

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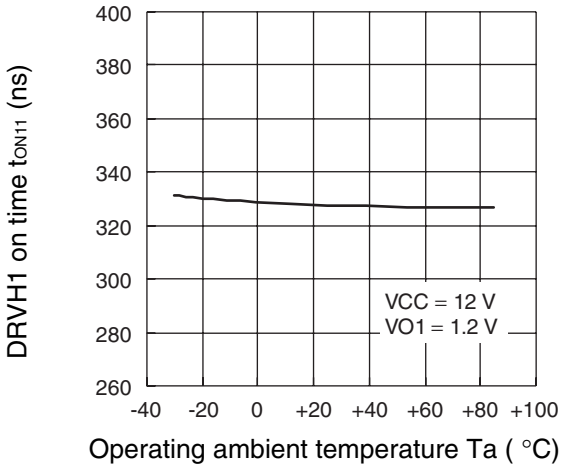
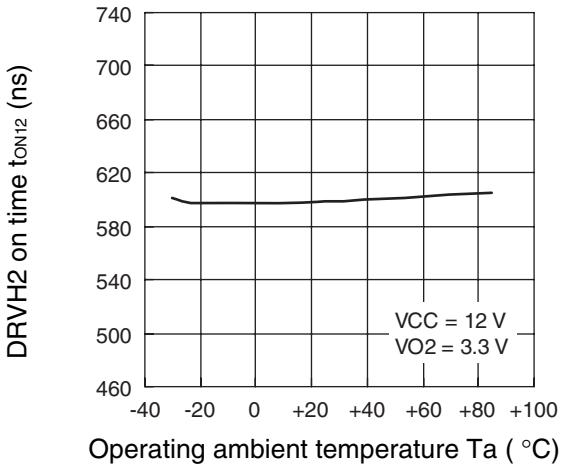
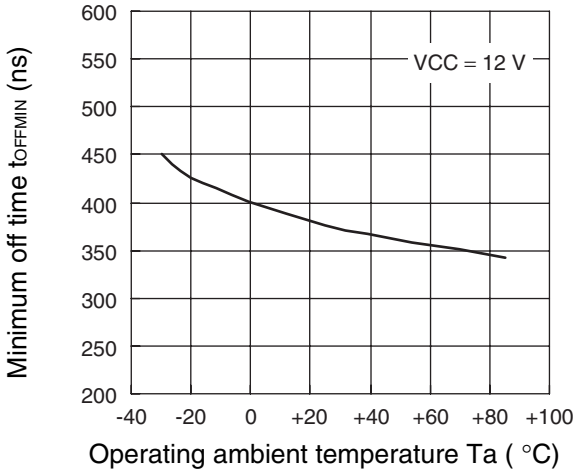
DRVH1 on time vs.
Operating ambient temperature



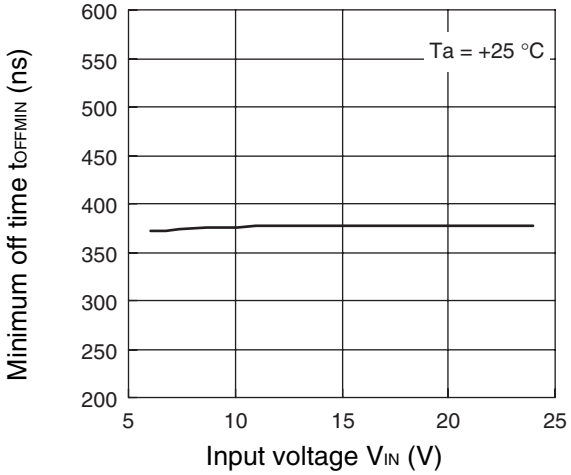

DRVH2 on time vs.
Operating ambient temperature



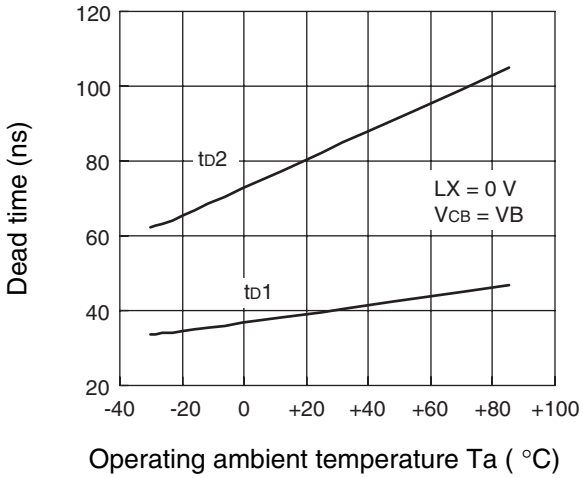

Minimum off time vs.
Operating ambient temperature



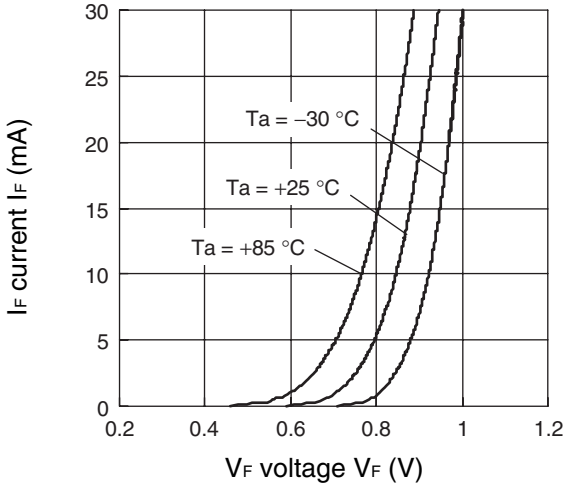

Minimum off time vs.
Input voltage




Dead time vs.
Operating ambient temperature




Bootstrup diode IF vs. VF

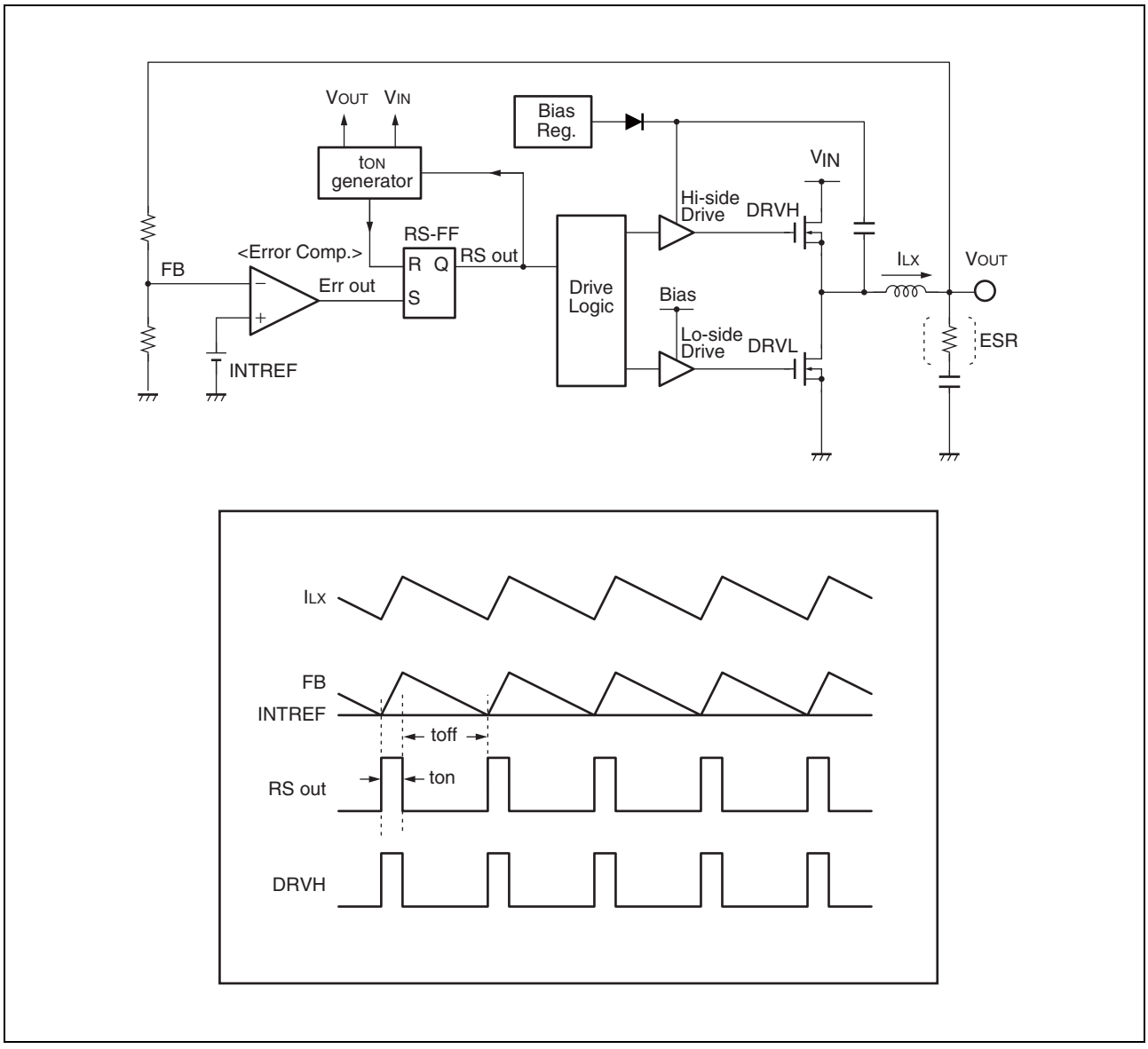


## ■ FUNCTION

### 1. Bottom detection comparator system

The bottom detection comparator system uses fixed ON time ($t_{ON}$) and the switching ripple voltage which superimposed the output voltage ($V_{OUT}$).
The $t_{ON}$ time is uniquely defined by the power supply voltage ($V_{IN}$) and the output voltage ($V_{OUT}$). During the $t_{ON}$ period, a current is supplied from the power supply voltage ($V_{IN}$). This results in an increased inductor current ($I_{LX}$) and also an increased output voltage ($V_{OUT}$) due to the parasitic resistance (ESR) of the output capacitor.
And when the $t_{OFF}$ period arrives, the energy accumulated in the inductor is supplied to the load to decrease the inductor current ($I_{LX}$) gradually. Consequently, the output voltage ($V_{OUT}$), which has been increasing due to the parasitic resistance (ESR) of the output capacitor, also decreases. When the output voltage is below a certain level, RS-FF is set and the $t_{ON}$ period arrives again. Switching is repeated as described above.

Error Comp. is used to compare the reference voltage (INTREF) with the output period voltage $V_{FB}$ to control the off-duty condition in order to stabilize the output voltage.



**(1) Bias Voltage Block (VB Reg.)**

It outputs 5.2 V (Typ) for setting of the output circuit's power supply and the bootstrap voltage. The bias power supply is supplied from the CVBLPF pin (pin 7) to the control circuit, which is smoothed with the RC filter of the resistor and the capacitor connected outside of the IC.

**(2) Under Voltage Lockout Protection Circuit Block (UVLO)**

A bias voltage ($V_{CVBLPF}$) of the control IC, a transitional state at startup, or a sudden drop leads to malfunction of the control IC, causing system destruction/deterioration. To prevent such malfunction, the under voltage lockout protection circuit detects a voltage drop at the CVBLPF pin (pin 7) and fixes DRVH1 pin (pin 23), DRVH2 pin (pin 15) and DRVL1 pin (pin 21), DRVL2 pin (pin 17) to the "L" level. When voltages at the CVBLPF pin exceed the threshold voltage of the under voltage lockout protection circuit, the system is restored.

**(3) Soft-start/Discharge Block (Soft-Start, Discharge)**

The soft-start block is the circuit to prevent a rush current when turning power on.

When the CTL1 pin (pin 1) and CTL2 pin (pin 8) are set to the "H" level, the capacitor connected to the CS1 pin (pin 2) and, CS2 pin (pin 12) starts charging and its lamp voltage is input to the error comparator (Error Comp.) of each channel. This allows for the setting of the soft-start time that does not depend on the output load of the DC/DC converter.

The discharge block is the circuit to discharge electrical charges stored in an output capacitor at output stop.

When setting the CTL1 pin (pin 1) and the CTL2 pin (pin 8) "L" level, FET for discharge ($R_{ON}$ = 35 Ω (Typ)) which is connected between the VO1 pin (pin 4), VO2 pin (pin 10), and GNDs will turn on and discharge the output capacitors. When VO1 pin voltage and VO2 pin voltage go down below 0.2 V (Typ) after discharging starts, FET for discharge is turned off and the discharge operation stops. Also, the discharge block works when detecting low voltage at the under-voltage protection circuit block (UVP Comp.) and detecting IC junction temperature increase at the over-temperature protection circuit block (OTP).

**(4) ON/OFF Time Generator Block ($t_{ON}$ Generator)**

The ON/OFF time generator block ($t_{ON}$ generator) contains a capacitor for timing setting and a resistor for timing setting and generates ON time which depends on input voltage and output voltage. ON time for each CH is obtained by the following formula.

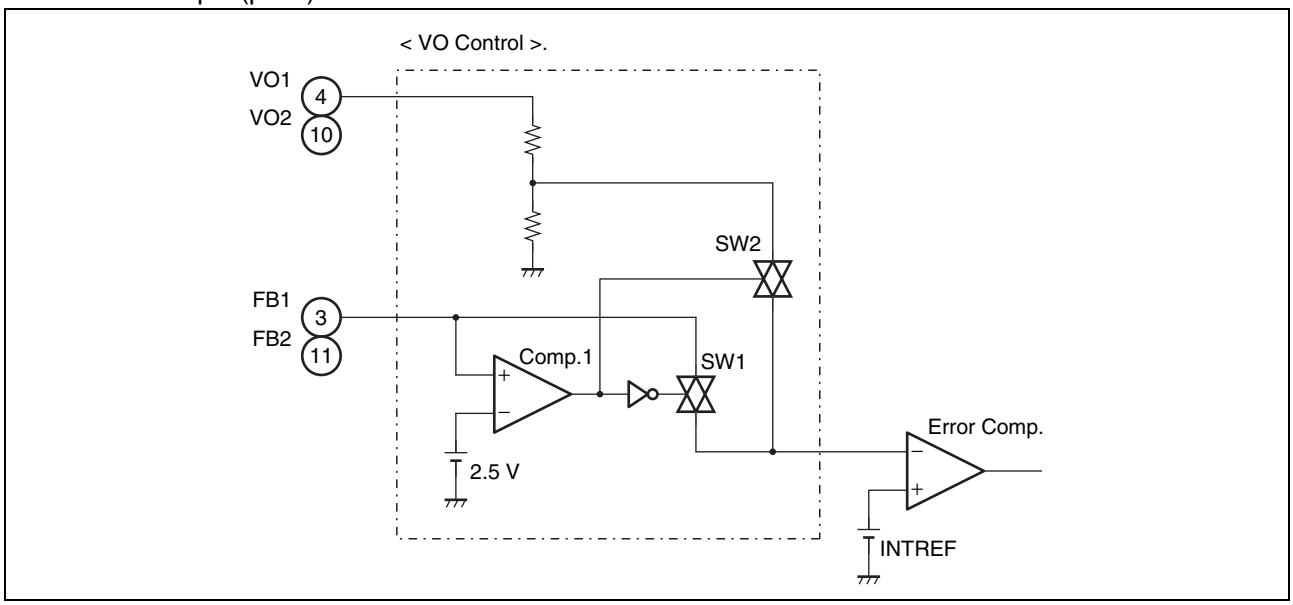
$$t_{ON11}\ (\text{ns}) = \frac{V_{VO1}}{V_{VCC}} \times 3200\ (f_{OSC1} \approx 310\ \text{kHz})$$

$$t_{ON12}\ (\text{ns}) = \frac{V_{VO2}}{V_{VCC}} \times 2133\ (f_{OSC2} \approx 465\ \text{kHz})$$

The oscillation frequency of CH2 is set to 1.5 times that of CH1 to prevent the beat by the frequency difference among channels.

### (5) Output Voltage Setting Block (VO Control, Error Comp.)

The output voltage setting block (VO Control, Error Comp.) detects the bottom value of ripple voltage that superimposed output voltage for DC/DC converter at the error comparator. The optional output voltage can be set by connecting the external output voltage setting resistor to the FB1 pin (pin 3) and the FB2 pin (pin 11). Also, the output setting resistor of the built-in IC can be used by connecting the FB1 pin and the FB2 pin to the CVBLPF pin (pin 7).




Output Voltage Setting Table

| Connection state of FB1 and FB2 pins | SW state | Remarks |
|---|---|---|
| Connected to an external resistor | SW1 : ON<br>SW2 : OFF | The DC/DC output voltage can be set freely by the external resistor |
| Connected to CVBLPF pin (pin 7) | SW1 : OFF<br>SW2 : ON | The external resistor for output voltage setting is unnecessary because DC/DC output voltage setting resistor embedded in the IC is used.<br>Set VO1 = 1.23 V, VO2 = 3.45 V. |

### (6) Over-voltage Protection Circuit Block (OVP Comp.)

It compares 1.15 times (Typ) of the internal reference voltage INTREF (CH1/CH2: 0.7V/2.0V) with the feedback voltage that is input to the FB1 pin (pin 3) and the FB2 pin (pin 11). The RS latch is set and the DRVH1 pin (pin 23) and the DRVH2 pin (pin 15) set to "L" level and the DRVL1 pin (pin 21) and the DRVL2 pin (pin 17) set to "H" level, when the feedback voltage detects a higher state at 50 µs (Typ) or more. The voltage output stops to fixes the high-side FET to the off-state and the low-side FET to the on-state, of both channels in the DC/DC converter.
The over-voltage protection state can be cancelled by setting the IC to standby state first and then resetting the latch using the UVLO signal.

### (7) Under-voltage Protection Circuit Block (UVP Comp.)

It compares 0.7 times (Typ) of the internal reference voltage INTREF (CH1/CH2: 0.7V/2.0V) with the feedback voltage that is input to the FB1 pin (pin 3) and the FB2 pin (pin 11). The RS latch is set and the DRVH1 pin (pin 23) and the DRVH2 pin (pin 15) go to "L" level and the DRVL1 pin (pin 21) and the DRVL2 pin (pin 17) go to "L" level, when the feedback voltage detects a lower state at 1.7 ms (Typ) or more. The discharge function internal in the IC operates and the voltage output of both channels stops, in synchronization with setting the latch of under voltage protection.
The under-voltage protection state can be cancelled by setting the IC to standby state first and then resetting the latch using the UVLO signal.

### (8) Over-temperature Protection Circuit Block (OTP)

If the junction temperature reaches +150 °C, the over-temperature protection circuit block makes the discharge function internal in the IC operate and makes voltage output of both channels stop. The soft start activates again when the junction temperature goes down to +125 °C.

### (9) Output Block (DRV1, DRV2)

The output circuit is configured in CMOS type for both of the high-side and the low-side, allowing the external N-ch MOS FET to drive.

### (10) Over Current Detection Block (ILIM)

The over current detection block (ILIM) compares the difference voltage between the PGND pin (pin 18) and the LX1 pin (pin 22) during the synchronous rectification period with the ILIM1 pin (pin 5) voltage, and compares the difference voltage between the PGND pin and the LX2 pin (pin 16) with the ILIM2 pin (pin 9) voltage, and detects over current at each cycle.

The high-side FET remains the off state until the voltage difference between the PGND pin and the LXx pin becomes below the ILIMx pin voltage and ON in the high-side FET is allowed after the voltage difference has been below the ILIMx pin voltage. This protects a circuit from flowing over current. This protection operates to drop the output voltage.

The difference voltage between PGND and LXx caused during the synchronous rectification period is described as the voltage waveform by sensing the inductor current, as the ON-resistance of the low-side FET is regarded as the sense resistor.

The optional limit value for over current can be set by setting a resistor to the ILIMx pin because $I_{ILIM}$ current which is 10 μA (Typ) is supplied from the ILIMx pin. As for $I_{ILIM}$ current, the temperature slope which is 4200 ppm/ °C is set to compensate the temperature dependence characteristics of the low-side FET on-resistance.

Note: x is each channel number.

### (11) Control Block (CTL)

On and off for CH1 is set by the CTL1 pin (pin 1) and on and off for CH2 is set by the CTL2 pin (pin 8). If setting CTL1 and CTL2 to "L" level at the same time, this IC turns to the standby state. (The maximum power-supply current at standby is 10 μA.)

**Control Function Table**

| CTL1 | CTL2 | DC/DC converter (CH1) | DC/DC converter (CH2) |
|---|---|---|---|
| L | L | OFF | OFF |
| H | L | ON | OFF |
| L | H | OFF | ON |
| H | H | ON | ON |

## ■ PROTECTION FUNCTION TABLE

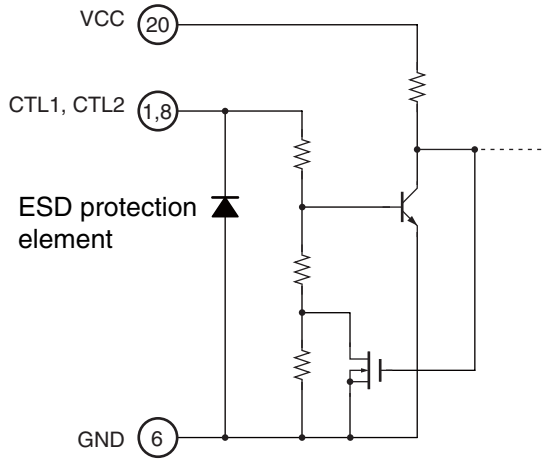
The following table shows the state of DRVH1, DRVH2 pins (pin 23, pin 15) and DRVL1, DRVL2 pins (pin 21, pin 17) when each protection function operates.

| Protection function | Detection condition | Output of each pin after detection | | | DC/DC output dropping operation |
|---|---|---|---|---|---|
| | | VB | DRVHx | DRVLx | |
| Under Voltage Lockout Protection (UVLO) | $V_{CVBLPF}$ < 3.6 V | — | L | L | Electrical discharge by discharge function |
| Under Voltage Protection (UVP) | $V_{FBx}$ < INTREFx × 0.7 V | 5.2 V | L | L | Electrical discharge by discharge function |
| Over Voltage Protection (OVP) | $V_{FBx}$ > INTREFx × 1.15 V | 5.2 V | L | H | 0 V clamping |
| Over Current Protection (ILIM) | $V_{PGNDx} - V_{LXx} > V_{ILIMx}$ | 5.2 V | switching | switching | The voltage is dropped by the constant current |
| Over Temperature Protection (OTP) | Tj > + 150 °C | 5.2 V | L | L | Electrical discharge by discharge function |
| CONTROL (CTL) | CTLx : H → L (VOx > 0.2 V) | 5.2 V | L | L | Electrical discharge by discharge function |

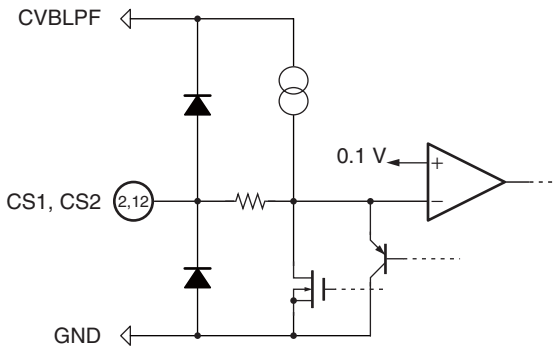
Note: x is each channel number.

## ■ I/O PIN EQUIVALENT CIRCUIT DIAGRAM

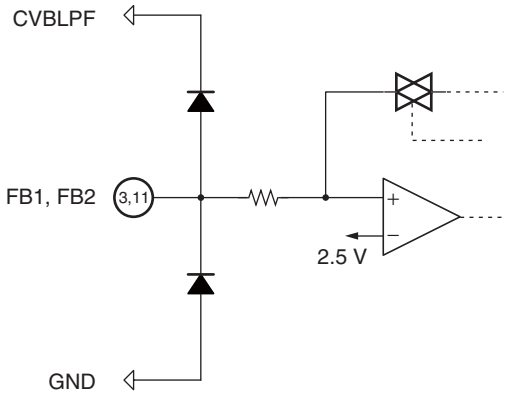
CTL1, CTL2 pins



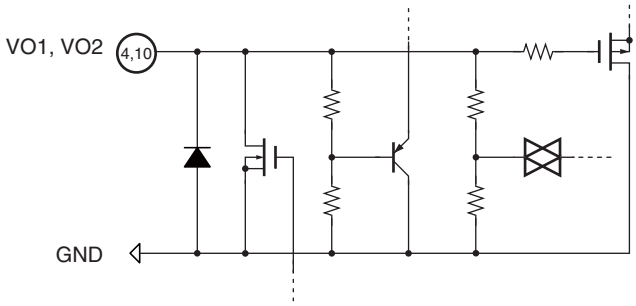

CS1, CS2 pins



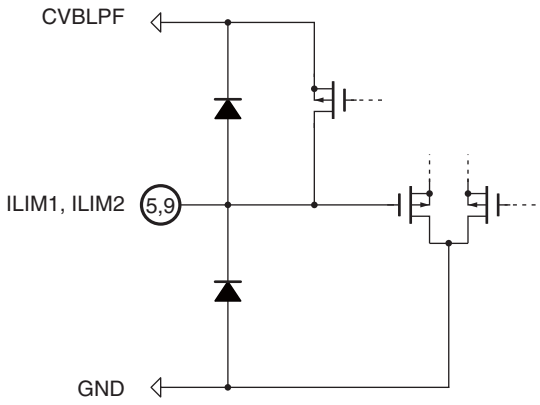

FB1, FB2 pins



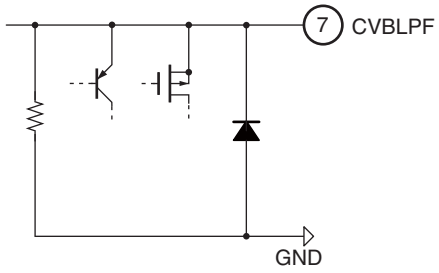

VO1, VO2 pins




ILIM1, ILIM2 pins




CVBLPF pin

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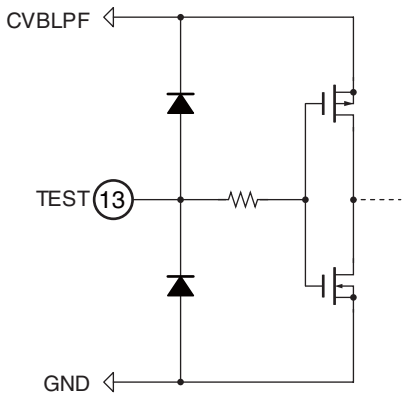
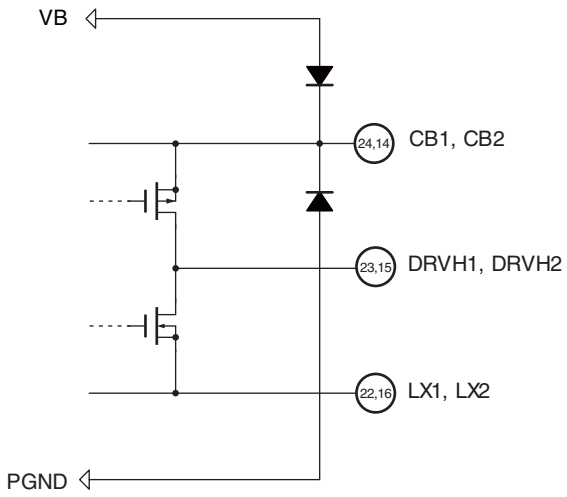
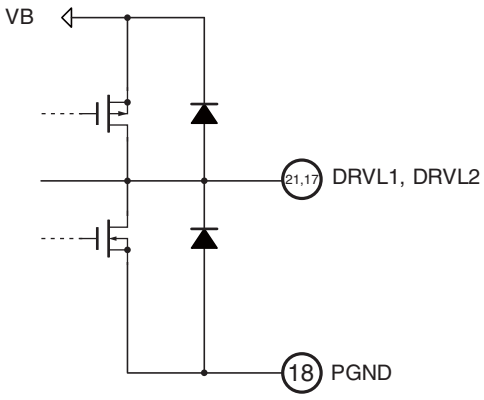
TEST pin



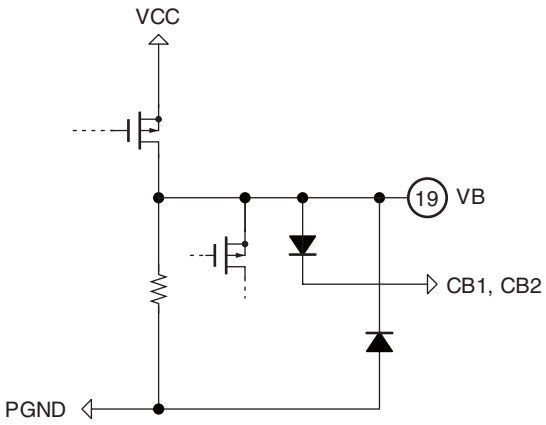

DRVH1, DRVH2, CB1, CB2 and LX1, LX2 pins



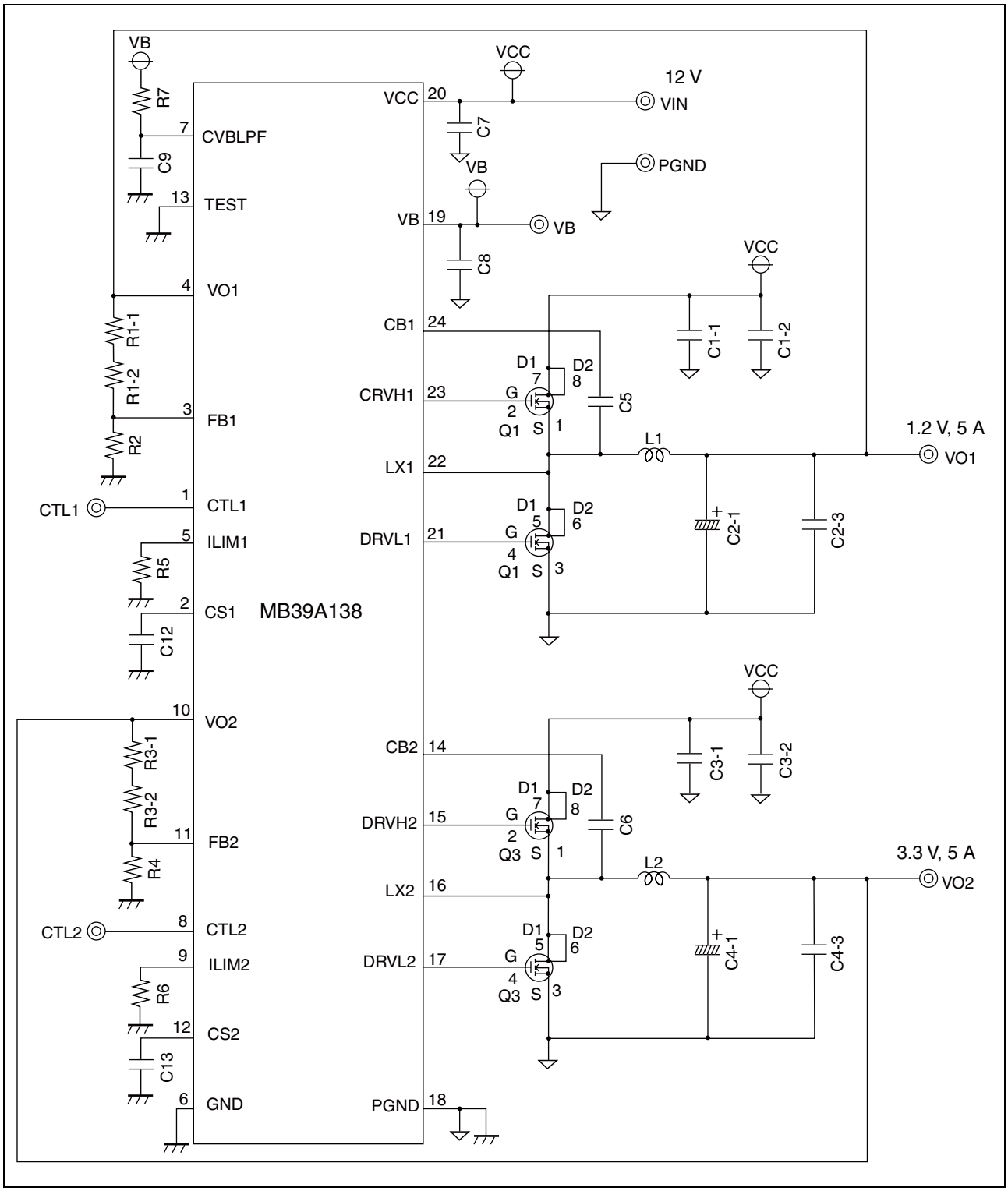

DRVL1, DRVL2 pins




VB pin



## ■ EXAMPLE APPLICATION CIRCUIT



## ■ PARTS LIST

| Compo-nent | Item | Specification | Vendor | Package | Part number | Remarks |
|---|---|---|---|---|---|---|
| Q1 | N-ch FET | VDS = 30 V, ID = 8 A, Ron = 21 mΩ | NEC | SO-8 | μPA2755 | Dual type (2 elements) |
| Q3 | N-ch FET | VDS = 30 V, ID = 8 A, Ron = 21 mΩ | NEC | SO-8 | μPA2755 | Dual type (2 elements) |
| L1 | Inductor | 1.5 μH (6.8 mΩ, 9.0 A) | TDK | — | VLF10045T-1R5N9R0 | |
| L2 | Inductor | 2.2 μH (10.2 mΩ, 7.4 A) | TDK | — | VLF10045T-2R2N7R4 | |
| C1-1 | Ceramic capacitor | 10 μF (25 V) | TDK | 3216 | C3216JB1E106K | |
| C1-2 | Ceramic capacitor | 10 μF (25 V) | TDK | 3216 | C3216JB1E106K | |
| C2-1 | OS-CON | 220 μF (6.3 V, 15 mΩ Max) | SANYO | C6 | 6SVPC220MV | |
| C2-3 | Ceramic capacitor | 1000 pF (50 V) | TDK | 1608 | C1608CH1H102J | |
| C3-1 | Ceramic capacitor | 10 μF (25 V) | TDK | 3216 | C3216JB1E106K | |
| C3-2 | Ceramic capacitor | 10 μF (25 V) | TDK | 3216 | C3216JB1E106K | |
| C4-1 | OS-CON | 220 μF (6.3 V, 15 mΩ Max) | SANYO | C6 | 6SVPC220MV | |
| C4-3 | Ceramic capacitor | 1000 pF (50 V) | TDK | 1608 | C1608CH1H102J | |
| C5 | Ceramic capacitor | 0.1 μF (50 V) | TDK | 1608 | C1608JB1H104K | |
| C6 | Ceramic capacitor | 0.1 μF (50 V) | TDK | 1608 | C1608JB1H104K | |
| C7 | Ceramic capacitor | 0.1 μF (50 V) | TDK | 1608 | C1608JB1H104K | |
| C8 | Ceramic capacitor | 2.2 μF (16 V) | TDK | 1608 | C1608JB1C225K | |
| C9 | Ceramic capacitor | 1.0 μF (16 V) | TDK | 1608 | C1608JB1C105K | |
| C12 | Ceramic capacitor | 0.015 μF (50 V) | TDK | 1608 | C1608JB1H153K | |
| C13 | Ceramic capacitor | 4700 pF (50 V) | TDK | 1608 | C1608JB1H472K | |
| R1-1 | Resistor | 1 kΩ | SSM | 1608 | RR0816P102D | |
| R1-2 | Resistor | 24 kΩ | SSM | 1608 | RR0816P243D | |
| R2 | Resistor | 36 kΩ | SSM | 1608 | RR0816P363D | |
| R3-1 | Resistor | 1.1 kΩ | SSM | 1608 | RR0816P112D | |
| R3-2 | Resistor | 22 kΩ | SSM | 1608 | RR0816P223D | |
| R4 | Resistor | 36 kΩ | SSM | 1608 | RR0816P363D | |
| R5 | Resistor | 18 kΩ | SSM | 1608 | RR0816P183D | |
| R6 | Resistor | 18 kΩ | SSM | 1608 | RR0816P183D | |
| R7 | Resistor | 5.6 Ω | KOA | 1608 | RK73H1JTTD5R6F | |

NEC : NEC Electronics Corporation
SANYO : SANYO Electric Co., Ltd.
TDK : TDK Corporation
SSM : SUSUMU CO., LTD.
KOA : KOA Corporation

## ■ APPLICATION NOTE

### 1. Setting Operating Conditions

**Setting output voltages**

1. When the output setting voltages are Vo1 = 1.23 V, Vo2 = 3.45 V:

They can be set by the internal preset function. In this case, the smallest number of parts is required for the setting, as it is not necessary to use a resistor to set the output voltage.

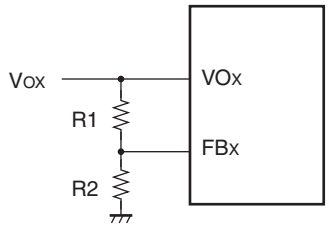
| | **Pin connection** | Output voltage setting value (Vo) |
|---|---|---|
| CH1 | FB1 = CVBLPF | Vo1 = 1.23 V |
| CH2 | FB2 = CVBLPF | Vo2 = 3.45 V |

2. When the output setting voltages are other Vo1 = 1.23 V, Vo2 = 3.45 V:

They can be set by adjusting the ratio of the output voltage setting resistor value. The output setting voltage is calculated by the following formula.

$$V_{OX} = \frac{R1 + R2}{R2} \times INTREF + \frac{\Delta V_{OX}}{2}$$

$V_{OX}$ : Output setting voltage [V]
INTREF : Internal reference voltage (CH1/CH2 : 0.7 V/2.0 V)
$\Delta V_{OX}$ : Output ripple voltage value [V]




The output ripple voltage value ($\Delta V_{OX}$) is calculated by the following formula.

$$\Delta V_{OX} = ESR \times \frac{V_{IN} - V_{OX}}{L} \times \frac{V_{OX}}{V_{IN} \times f_{OSC}}$$

$\Delta V_{OX}$ : Output ripple voltage value [V]
L : Inductor value [H]
$V_{IN}$ : Power supply voltage [V]
$V_{OX}$ : Output setting voltage [V]
$f_{OSC}$ : Oscillation frequency [Hz] (CH1 : 310 kHz, CH2 : 465 kHz)

Note: x is each channel number.

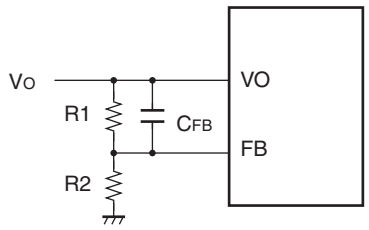
When not using the following feedback capacitor (CFB), select a resistor value that achieves R1//R2 ≤ 15 kΩ as a target.
Set so that the on-time ($t_{ON}$) is more than 100 ns.
(For how to calculate the on-time, see (4) ON/OFF Time Generator Block in "■ FUNCTION")

As the output voltage gets higher, the resistor value ratio of output voltage setting is getting higher. Moreover, the oscillation frequency may become unstable as a result. This occurs because the value of the ripple voltage applied to the FB pin is reduced by the R1/R2 ratio. In this case, a stable oscillation frequency can be achieved by increasing the output ripple voltage or adding a capacitor ($C_{FB}$) in parallel to R1.

Select an additional capacitor using the following formula as a guide.

$$C_{FB} \geq \frac{10 \times (R1 + R2)}{2\pi \times fosc \times R1 \times R2}$$

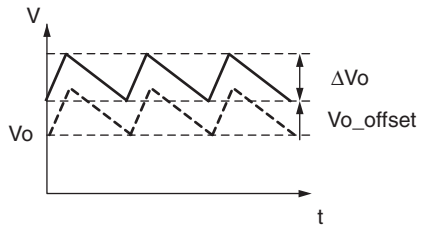
$C_{FB}$ : Capacitor value of feedback capacitor [F]
R1, R2 : Output voltage setting resistor value [Ω]
$f_{OSC}$ : Oscillation frequency [Hz]




Moreover, adding a capacitor increases the output voltage according to the output ripple voltage.
The following formula is used to calculate the output voltage value to be increased.

$$Vo\_{offset} = \frac{(V_O - INTREF) \times \Delta V_O}{2 \times INTREF}$$

$Vo\_{offset}$ : Output setting voltage offset value [V]
$V_O$ : Output setting voltage [V]
ΔVo : Output ripple voltage value [V]
INTREF : Internal reference voltage (CH1/CH2 : 0.7 V/2.0 V)




Use the following formula to calculate the output setting voltage when considering the output setting voltage offset value.

$$V_{OX} = \frac{R1 + R2}{R2} \times INTREF + \frac{\Delta V_{OX}}{2} + Vo\_{offset}$$

$V_{OX}$ : Output setting voltage[V]
INTREF : Internal reference voltage (CH1/CH2 : 0.7 V/2.0 V)
$\Delta V_{OX}$ : Output ripple voltage value [V]
$V_{O\_offset}$ : Output setting voltage offset value [V]

Note: x is each channel number.

**Consideration of output ripple voltage**

This device requires an output ripple voltage value as an operating principle. It must secure about 15 mV at the FB pin. Calculate the output ripple voltage required for the output of the DC/DC converter by the following formula.

$$\Delta V_{OX} \geq K \times 15\ mV$$

$\Delta V_{OX}$ : Output ripple voltage value [V]

K : Coefficient When $C_{FB}$ is used : K = 1;

$C_{FB}$ is not used : $K = \frac{V_O}{INTREF}$

$V_O$ : Output setting voltage [V]

INTREF : Internal reference voltage (CH1/CH2 : 0.7 V/2.0 V)

A stable oscillation frequency can be achieved by increasing the output ripple voltage.
The output ripple voltage can be increased by selecting a larger output capacitor's ESR or a smaller inductor value.
However, if the output ripple voltage is increased excessively, the slope of the output ripple voltage during the off-period ($t_{OFF}$) becomes steeper, which affects the bottom detection voltage more. As a result, it affects the output voltage. This become prominent, if it increase on-duty. Ensure that the ripple voltage at the FB pin is not excessively large.

### Setting soft-start time

Calculate the soft-start time by the following formula.

$$t_s = \frac{INTREF \times C_{CS}}{5 \times 10^{-6}}$$

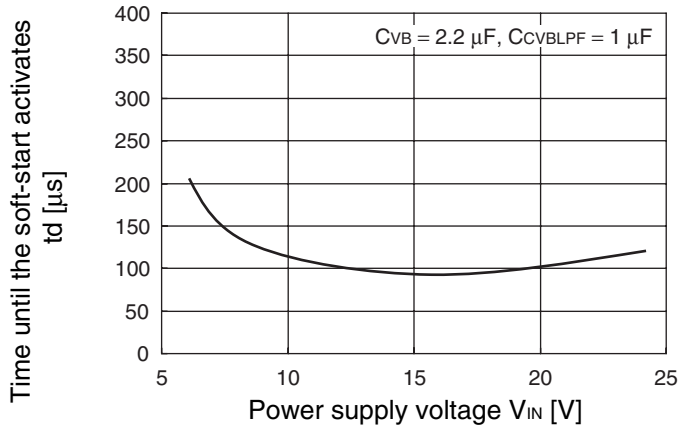
| | |
|---|---|
| $t_s$ | : Soft-start time [s] (time until output reaches 100%) |
| INTREF | : Internal reference voltage (CH1/CH2 : 0.7 V/2.0 V) |
| $C_{CS}$ | : CS pin capacitor value [F] |

Calculate the delay time until the soft-start activation by the following formula.

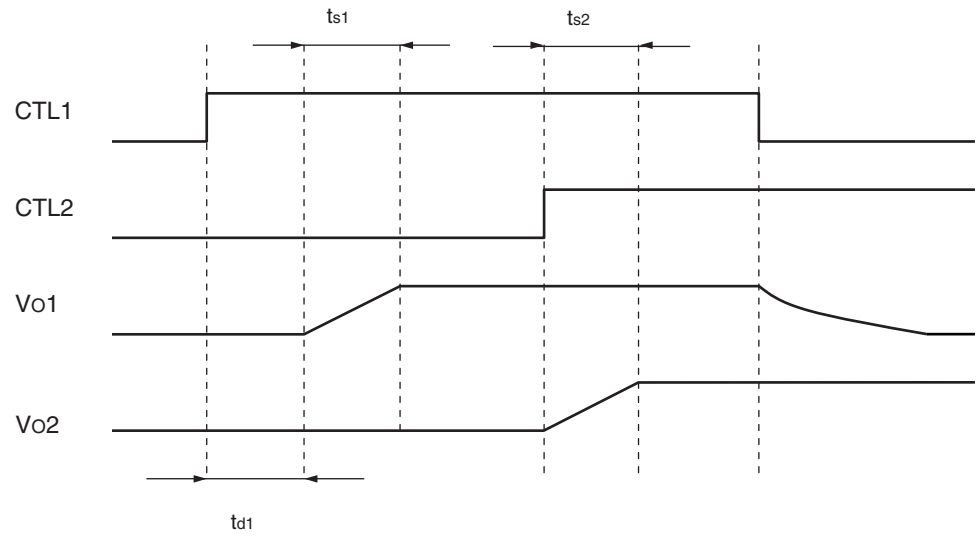
$$t_d = 30 \times (C_{VB} + C_{CVBLPF})$$

| | |
|---|---|
| $t_d$ | : VB voltage delay time [s] |
| $C_{VB}$ | : VB capacitor value [F] |
| $C_{CVBLPF}$ | : CVBLPF capacitor value [F] |

Reference characteristics : Time until the soft-start activates vs. power supply voltage




In almost all cases, no delay time is generated when the soft-start activates in the state that one side channel has already activated (UVLO release: VB output already).



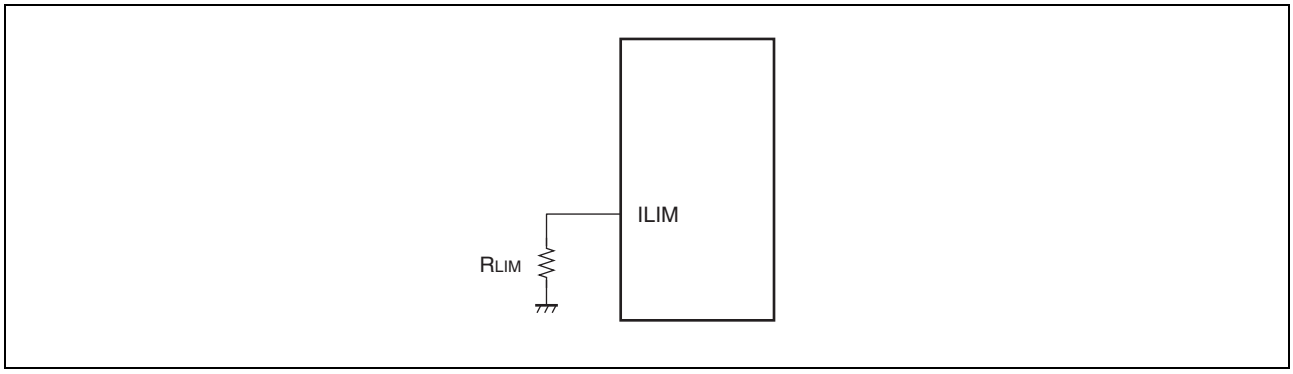

Note : Set the slew rate of 750 V/s or more to the input-signal to CTL1 and CTL2 pins.

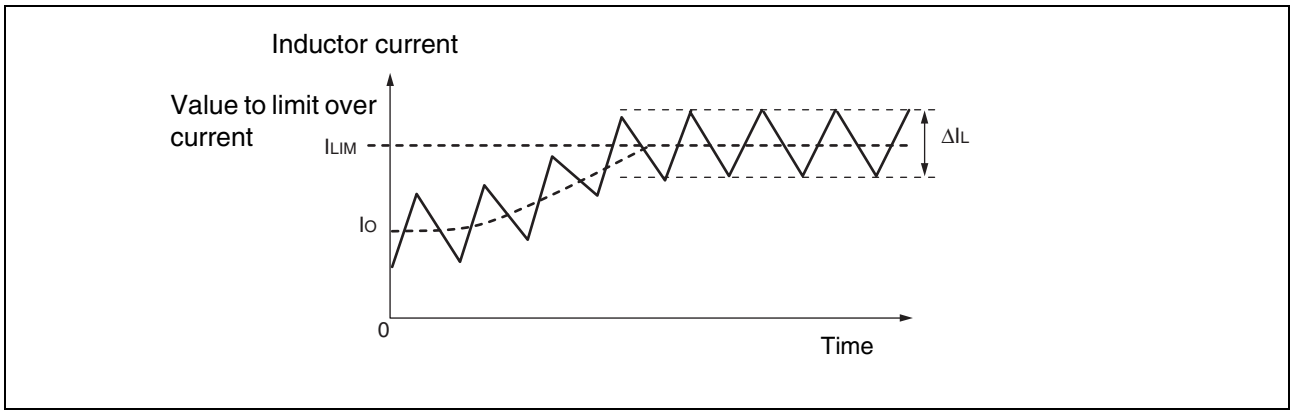
### Setting over current detection value

The over current detection value can be set by adjusting the over current detection resistor value connected to the ILIM pin.
Calculate the resistor value by the following formula.

$$R_{LIM} = \frac{R_{ON\_Sync} \times \left(I_{LIM} - \frac{\Delta IL}{2} + \frac{V_O \times 260 \times 10^{-9}}{L}\right)}{10 \times 10^{-6}}$$

| | |
|---|---|
| $R_{LIM}$ | : Over current detection value setting resistor [Ω] |
| $I_{LIM}$ | : Over current detection value [A] |
| $\Delta IL$ | : Ripple current peak-to-peak value of inductor [A] |
| $R_{ON\_Sync}$ | : ON resistance of low-side FET [Ω] |
| $V_O$ | : Output setting voltage [V] |
| L | : Inductor value [H] |



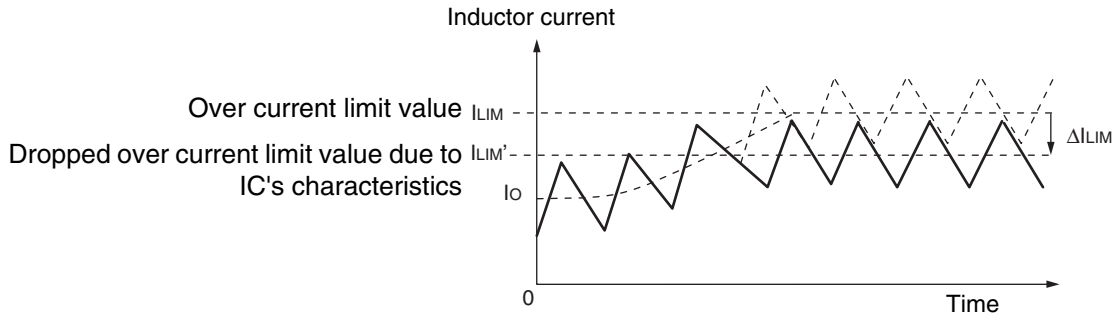




If the rate of inductor saturation current is small, the inductor value decreases and the ripple current of inductor increase when the over-current flows. At that time there is a possibility that the limited output current increases or is not limited, because the bottom of inductor current is detected. It is necessary to use the inductor that has enough large rate of inductor saturation current to prevent the overlap current.

The over current limit value is affected by ILIM pin source current and over current detection offset voltage in the IC except for the on resistance of the low-side FET and the inductor value. The variation of dropped over current limit value caused by IC characteristics is calculated by the following formula.

$$\Delta I_{LIM} = - \frac{1.7 \times 10^{-6} \times R_{LIM} + 0.02}{R_{ON\_Sync}}$$

$\Delta I_{LIM}$ : The variation of dropped over current limit value [A]
$R_{LIM}$ : Resistor to set over current limit [Ω]
$R_{ON\_Sync}$ : Low-side FET on resistance [Ω]




The over current detection value needs to set a sufficient margin against the maximum load current.

### VB Regulator

In the condition for which the potential difference between VCC and VB is insufficient, the decrease in the voltage of VB happens because of power output on-resistance and load current (mean current of all external FET gate driving current and load current of internal IC) of the VB regulator. Stop the switching operation when the voltage of VB decreases and it reaches threshold voltage (VTHL) of the under voltage lockout protection circuit.
Therefore, set oscillation frequency or external FET or I/O potential difference of the VB regulator using the following formula as a target when you use this IC. When using it in the condition for which the I/O potential difference is insufficient, check the operation on an actual device carefully during normal operation, startup and shutdown.

$$V_{IN} \geq VB\ (V_{THL}) + (Qg \times f_{OSC} + I_{CC}) \times R_{VB}$$

| | |
|---|---|
| VB ($V_{THL}$) | : Threshold voltage of under-voltage lockout protection circuit = 3.8 [V] Max |
| Qg | : Total amount of gate charge of external FET [C] |
| $f_{OSC}$ | : Oscillation frequency [Hz] |
| $I_{CC}$ | : Power supply current = $2 \times 10^{-3}$ [A] ( ≈ Load current of VB (LDO)) |
| $R_{VB}$ | : VB Output on-resistance = 75 [Ω] (The reference value at $V_{IN}$ = 6 V) |

### Power dissipation and the thermal design

As for this IC, considerations of the power dissipation and thermal design are not necessary in most cases because of its high efficiency. However, they are necessary for the use at the conditions of a high power supply voltage, a high oscillation frequency, high load, and the high temperature. Calculate IC internal loss by the following formula.

$$P_{IC} = V_{CC} \times (I_{CC} + Q_{g1} \times f_{OSC1} + Q_{g2} \times f_{OSC2})$$

| | |
|---|---|
| $P_{IC}$ | : IC internal loss [W] |
| $V_{CC}$ | : Power supply voltage ($V_{IN}$) [V] |
| $I_{CC}$ | : Power supply current [A] (2 mA Max) |
| $Q_{g1}$, $Q_{g2}$ | : Total quantity of charge for the high-side FET and the low-side FET of each CH [C] (Total at Vgs = VB) |
| $f_{OSC1}$, $f_{OSC2}$ | : Oscillation frequency of each CH [Hz] |

Calculate junction temperature (Tj) by the following formula.

$$T_j = T_a + \theta_{ja} \times P_{IC}$$

| | |
|---|---|
| $T_j$ | : Junction temperature [ °C] ( + 125 °C Max) |
| $T_a$ | : Operation ambient temperature [ °C] |
| $\theta_{ja}$ | : TSSOP-24 Package thermal resistance ( + 75 °C/W) |
| $P_{IC}$ | : IC internal loss [W] |

## 2. Selecting parts

### Selection of smoothing inductor

The inductor value selects the value that the ripple current peak-to-peak value of the inductor is 50% or less of the maximum load current as a rough standard. Calculate the inductor value in this case by the following formula.

$$L \geq \frac{V_{IN} - V_O}{LOR \times I_{OMAX}} \times \frac{V_O}{V_{IN} \times f_{OSC}}$$

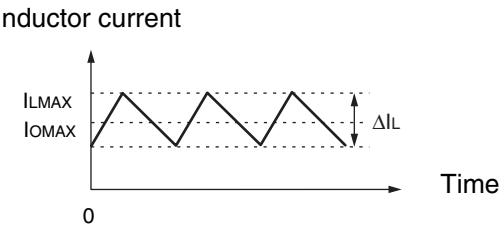
| | |
|---|---|
| L | : Inductor value [H] |
| $I_{OMAX}$ | : Maximum load current [A] |
| LOR | : Ripple current peak-to-peak value of inductor / Maximum load current ratio (=0.5) |
| $V_{IN}$ | : Power supply voltage [V] |
| $V_O$ | : Output setting voltage [V] |
| $f_{OSC}$ | : Oscillation frequency [Hz] |

It is necessary to calculate the maximum current value that flows to the inductor to judge whether the electric current that flows to the inductor is a rated value or less. Calculate the maximum current value of the inductor by the following formula.

$$I_{LMAX} \geq I_{OMAX} + \frac{\Delta IL}{2}$$

$$\Delta IL = \frac{V_{IN} - V_O}{L} \times \frac{V_O}{V_{IN} \times f_{OSC}}$$

| | |
|---|---|
| $I_{LMAX}$ | : Maximum current value of inductor [A] |
| $I_{OMAX}$ | : Maximum load current [A] |
| ΔIL | : Ripple current peak-to-peak value of inductor [A] |
| L | : Inductor value [H] |
| $V_{IN}$ | : Power supply voltage[V] |
| $V_O$ | : Output setting voltage[V] |
| $f_{OSC}$ | : Oscillation frequency [Hz] |



### Selection of Switching FET

Select the low-side FET ON resistance from the below range in order to operate the over current limit function normally.

$$\frac{0.03}{(I_{LIM} - \frac{\Delta IL}{2})} \leq R_{ON\_Sync} \leq \frac{0.2}{(I_{LIM} - \frac{\Delta IL}{2})}$$

$R_{ON\_Sync}$ : Low-side FET ON resistance [Ω]
$\Delta IL$ : Ripple current peak-to-peak value of inductor [A]
$I_{LIM}$ : Over current detection value [A]

The maximum value of the current that flows to the switching FET must be calculated in order to determine whether the current flowing to the switching FET is within the rated value. Calculate the maximum value of the current that flows to the switching FET by the following formula.

$$I_D = I_{OMAX} + \frac{\Delta IL}{2}$$

$I_D$ : Drain current [A]
$I_{OMAX}$ : Maximum load current [A]
$\Delta IL$ : Ripple current peak-to-peak value of inductor [A]

Moreover, it is necessary to calculate the loss of switching FET to judge whether a power dissipation of switching FET is a rated value or less. Calculate the loss on high-side FET by the following formula.

$$P_{MainFET} = P_{RON\_Main} + P_{SW\_Main}$$

$P_{MainFET}$ : High-side FET loss [W]
$P_{RON\_Main}$ : High-side FET conduction loss [W]
$P_{SW\_Main}$ : High-side FET switching loss [W]

High-side FET conduction loss

$$P_{RON\_Main} = I_{OMAX}^2 \times \frac{V_O}{V_{IN}} \times R_{ON\_Main}$$

$P_{RON\_Main}$ : High-side FET conduction loss [W]
$I_{OMAX}$ : Maximum load current[A]
$V_{IN}$ : Power supply voltage[V]
$V_O$ : Output voltage[V]
$R_{ON\_Main}$ : High-side FET ON resistance [Ω]

High-side FET switching loss

$$P_{SW\_Main} = \frac{V_{IN} \times f_{OSC} \times (I_{btm} \times t_r + I_{top} \times t_f)}{2}$$

$P_{SW\_Main}$ : Switching loss [W]
$V_{IN}$ : Power supply voltage [V]
$f_{OSC}$ : Oscillation frequency (Hz)
$I_{btm}$ : Ripple current bottom value of inductor [A]
$I_{top}$ : Ripple current top value of inductor [A]

$$I_{btm} = I_{OMAX} - \frac{\Delta IL}{2},\ I_{top} = I_{OMAX} + \frac{\Delta IL}{2}$$

$\Delta IL$ : Ripple current peak-to-peak value of inductor [A]
$I_{OMAX}$ : Maximum load current [A]

$t_r$ : Turn-on time on high-side FET [s]

$t_f$ : Turn-off time on high-side FET [s]

$t_r$ and $t_f$ is calculated by the following formula.

$$t_r = \frac{Q_{gd} \times 4}{V_B - V_{gs}\ (on)},\ t_f = \frac{Q_{gd} \times 1}{V_{gs}\ (on)}$$

$Q_{gd}$ : Quantity of charge between gate and drain on high-side FET [C]
$V_{gs}$ (on) : Voltage between gate and sources in Qgd on high-side FET [V]
$V_B$ : VB voltage [V]

The loss of the low-side FET is calculated by the following formula. (The transition voltage of the voltage between drain and source on low-side FET is generally small, and the switching loss is omitted here for the small one as it is possible to disregard it.)

$$P_{SyncFET} = R_{Ron\_Sync} = I_{OMAX}^2 \times \left(1 - \frac{V_O}{V_{IN}}\right) \times R_{on\_Sync}$$

$P_{Ron\_Sync}$ : Low-side FET conduction loss [W]
$I_{OMAX}$ : Maximum load current [A]
$V_{IN}$ : Power supply voltage [V]
$V_O$ : Output voltage [V]
$R_{on\_Sync}$ : Low-side FET on-resistance [Ω]

The gate drive power of switching FET is supplied by LDO in IC, therefore all of the allowable maximum total gate charge (QgTotalMax) of all switching FET for 2 channels is calculated by the following formula.

$$Qg_{TotalMax} \leq \frac{140000}{f_{OSC2}}$$

$Qg_{TotalMax}$ : All of the allowable maximum total gate charge of all switching FET for 2 channels [nC]
$f_{OSC2}$ : CH2 oscillation frequency [kHz]

### Selection of fly-back diode

Fly-back diode is not needed in general. However, it is possible to enhance the conversion efficiency by building in the fly-back diode, thought it is usually unnecessary. The effect is achieved in the condition where the oscillation frequency is high or output voltage is lower. Select schottky barrier diode (SBD) that the forward current is as small as possible. In this DC/DC control IC, the period for the electric current flows to fly-back diode is limited to synchronous rectification period (120 [ns]) because of using the synchronous rectification method. Therefore, select the one that the electric current of fly-back diode does not exceed ratings of forward current surge peak ($I_{FSM}$).Calculate the forward current surge peak ratings of fly-back diode by the following formula.

$$I_{FSM} \geq I_{OMAX} + \frac{\Delta IL}{2}$$

$I_{FSM}$ : Forward current surge peak ratings of SBD [A]
$I_{OMAX}$ : Maximum load current [A]
$\Delta IL$ : Ripple current peak-to-peak value of inductor [A]

Calculate ratings of the fly-back diode by the following formula:

$$V_{R\_Fly} > V_{IN}$$

$V_{R\_Fly}$ : Reverse voltage of fly-back diode direct current [V]
$V_{IN}$ : Power supply voltage [V]

### Selection of output capacitor

A certain level of ESR is required for stable operation of this IC. Use a tantalum capacitor or polymer capacitor as the output capacitor. If using a ceramic capacitor with low ESR, a resistor should be connected in series with it to increase ESR equivalently.

Calculate the required ESR for the smoothing capacitor by the following formula.

$$ESR \geq \frac{\Delta IL}{\Delta V_O}$$

ESR : Series resistance of output capacitor [Ω]
$\Delta V_O$ : Output ripple voltage [V]
$\Delta IL$ : Ripple current peak-to-peak value of inductor [A]

Select the capacitance of the output capacitor with the following condition to a target.

$$C_O \geq \frac{1}{4 \times f_{OSC} \times ESR}$$

$C_O$ : Output capacitor value [F]
$f_{OSC}$ : Oscillation frequency [Hz]
ESR : Series resistance of output capacitor [Ω]

When using a capacitor where the capacity demanded by the above formula is unfulfilled, use it after intensively operation check that there is no problem with the jitter level.

Moreover, the output capacitor values are also derived from the allowable amount of overshoot and undershoot. The following formula is represented as the worst condition in which the shift time for a sudden load change is 0s. For a longer shift time, the smaller amount of output capacitor is acceptable than the value calculated by the following formula.

Overshoot condition

$$C_O \geq \frac{\Delta I_O^2 \times L}{2 \times V_O \times \Delta V_{O\_OVER}}$$

Undershoot condition

$$C_O \geq \frac{\Delta I_O^2 \times L \times (V_O + V_{IN} \times f_{OSC} \times 380 \times 10^9)}{2 \times V_O \times \Delta V_{O\_UNDER} \times (V_{IN} - V_O - V_{IN} \times f_{OSC} \times 380 \times 10^9)}$$

| | |
|---|---|
| $C_O$ | : Output capacitor value [F] |
| $\Delta V_{O\_OVER}$ | : Allowable amount of output voltage overshoot [V] |
| $\Delta V_{O\_UNDER}$ | : Allowable amount of output voltage undershoot [V] |
| $\Delta I_O$ | : Current difference in sudden load change [A] |
| L | : Inductor value [H] |
| $V_{IN}$ | : Power supply voltage [V] |
| $V_O$ | : Output setting voltage[V] |
| $f_{OSC}$ | : Oscillation frequency [Hz] |

The capacitor has frequency, operating temperature, and bias voltage characteristics, etc. Therefore, it must be noted that its effective capacitor value may be significantly smaller, depending on the use conditions.

Calculate voltage rating of the output capacitor by the following formula.

$$V_{CO} > V_O$$

| | |
|---|---|
| $V_{CO}$ | : Withstand voltage of the output capacitor [V] |
| $V_O$ | : Output voltage [V] |

Capacitor voltage rating should have a sufficient margin to withstand the output voltage.

Calculate the allowable ripple current of the output capacitor by the following formula.

$$Irms \geq \frac{\Delta IL}{2\sqrt{3}}$$

| | |
|---|---|
| Irms | : Allowable ripple current (effective value) [A] |
| $\Delta$IL | : Ripple current peak-to-peak value of inductor [A] |

**Selection of input capacitor**

Select the input capacitor whose ESR is as small as possible. The ceramic capacitor is an ideal. Use the tantalum capacitor and the polymer capacitor of the low ESR when a mass capacitor is needed as the ceramic capacitor can not support.
If a inductor is connected as a noise filter between the power supply and the input capacitor, and the cut-off frequency for this inductor and input capacitor is set to a value lower than the oscillation frequency, the ripple voltage by the switching operation of DC/DC is generated.
Discuss the lower bound of input capacitor according to an allowable ripple voltage. Calculate the ripple voltage of the power supply from the following formula.

$$\Delta V_{IN} = \frac{I_{OMAX}}{C_{IN}} \times \frac{V_O}{V_{IN} \times f_{OSC}} + ESR \times \left(I_{OMAX} + \frac{\Delta IL}{2}\right)$$

| | |
|---|---|
| $\Delta V_{IN}$ | : Power supply ripple voltage peak-to-peak value [V] |
| $I_{OMAX}$ | : Maximum load current value [A] |
| $C_{IN}$ | : Input capacitor value [F] |
| $V_{IN}$ | : Power supply voltage [V] |
| $V_O$ | : Output setting voltage [V] |
| $f_{OSC}$ | : Oscillation frequency [Hz] |
| ESR | : Series resistance component of input capacitor [Ω] |
| $\Delta IL$ | : Ripple current peak-to-peak value of inductor [A] |

Capacitor has frequency characteristic, the temperature characteristic, and the bias voltage characteristic, etc. The effective capacitor value might become extremely small depending on the use conditions. Note the effective capacitor value in the use conditions.

Calculate ratings of the input capacitor by the following formula:

$$V_{CIN} > V_{IN}$$

| | |
|---|---|
| $V_{CIN}$ | : Withstand voltage of the input capacitor [V] |
| $V_{IN}$ | : Power supply voltage [V] |

Select the capacitor voltages rating with withstand voltage with margin enough for the input voltage.

In addition, use the allowable ripple current with an enough margin, if it has a rating. Calculate an allowable ripple current by the following formula.

$$Irms \geq I_{OMAX} \times \frac{\sqrt{V_O \times (V_{IN} - V_O)}}{V_{IN}}$$

| | |
|---|---|
| Irms | : Ripple current (effective value) [A] |
| $I_{OMAX}$ | : Maximum load current value [A] |
| $V_{IN}$ | : Power supply voltage [V] |
| $V_O$ | : Output setting voltage [V] |

### Selection of boot strap capacitor

To drive the gate of high-side FET, the bootstrap capacitor must have enough stored charge. Therefore, a minimum value as a target is assumed the capacitor which can store electric charge 10 times that of the Qg on high-side FET. And select the boot strap capacitor.

$$C_{BOOT} \geq 10 \times \frac{Q_g}{V_B}$$

$C_{BOOT}$ : Boot strap capacitor value [F]
$Q_g$ : Amount of gate charge on high-side FET [C]
$V_B$ : VB voltage [V]

Calculate ratings of the boot strap capacitor by the following formula:

$$V_{CBOOT} > V_B$$

$V_{CBOOT}$ : Withstand voltage of the boot strap capacitor[V]
$V_B$ : VB voltage [V]

### VB pin capacitor

2.2 µF is assumed to be a standard, and when Qg of switching FET used is large, it is necessary to adjust it. To drive the gate of high-side FET, the bootstrap capacitor must have enough stored charge. Therefore, a minimum value as a target is assumed the capacitor value which can store electric charge 100 times that of the Qg on switching FET. And select it.

Moreover, capacitor change may cause an overshoot when CTL was turned on.

Although the overshoot does not affect DC/DC operation, check that the VB pin does not exceed its rating before applying the capacitors.

$$C_{VB} \geq 100 \times \frac{Qg}{V_B}$$

$C_{VB}$ : VB pin capacitor value [F]
$Q_g$ : Total amount of gate charge of high-side FET and low-side FET for 2ch [C]
$V_B$ : VB voltage [V]

Calculate ratings of the VB pin capacitor by the following formula:

$$V_{CVB} > V_B$$

$V_{CVB}$ : Withstand voltage of the VB pin capacitor [V]
$V_B$ : VB voltage [V]

### CVBLPF pin capacitor and resistor

LPF to power supply from the VB regulator (VB pin) to the control system power supply (CVBLPF pin) is made by the CVBPF pin's capacitor and the resistor between the VB pin and the CVBPF pin. The cut-off frequency is set to one tenth of oscillation frequency as a target (1 µF is the standard of the capacitor value).

Select as small a value as possible (the recommended value is about 5 Ω).

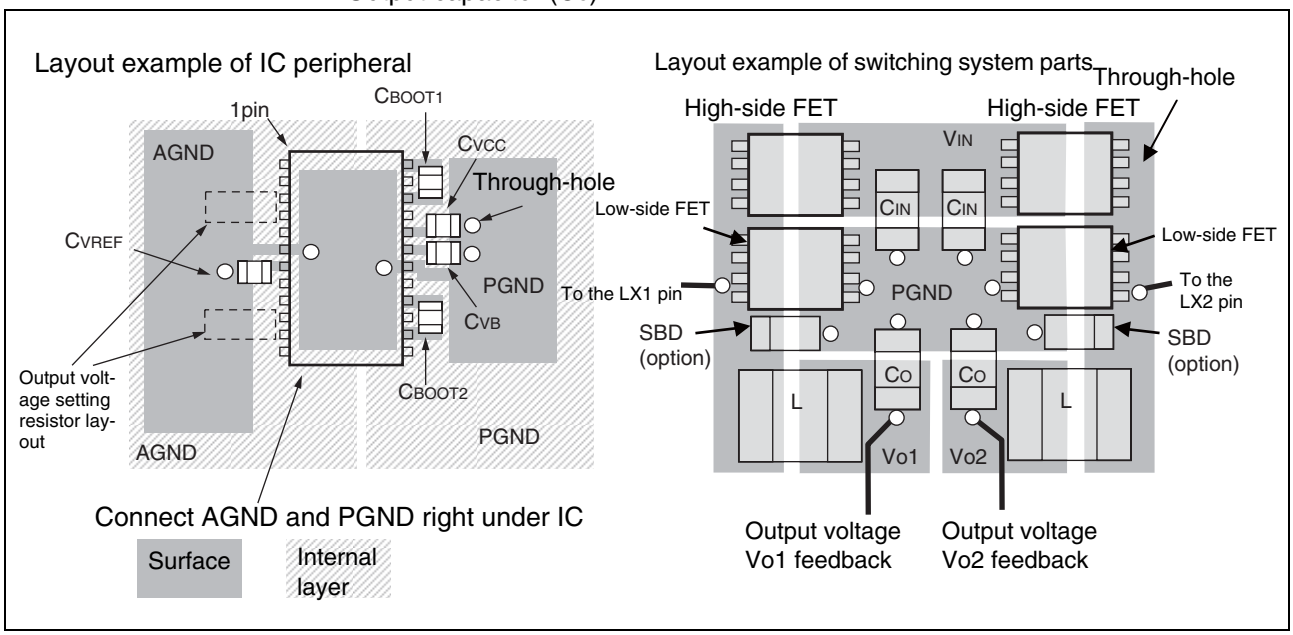
Because the voltages drop to the control system power supply is occurred when setting the resistor value to extremely large value.

## 3. Layout

Consider the points listed below and do the layout design.

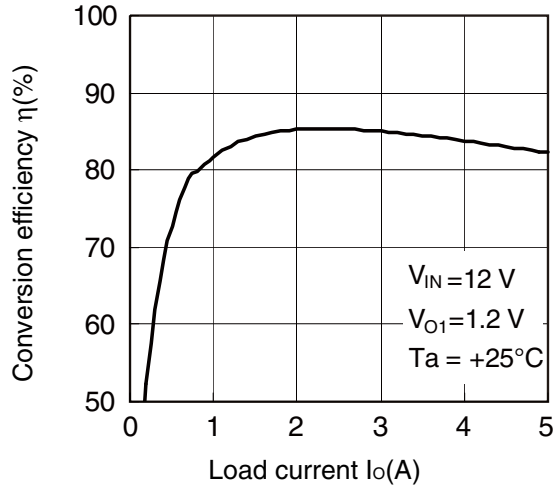
- Provide the ground plane as much as possible on the IC mounted face. Connect bypass capacitor connected with the VCC and VB pins, and GND pin of the switching system parts with switching system GND (PGND). Connect other GND connection pins with control system GND (AGND), and separate each GND, and try not to pass the heavy current path through the control system GND (AGND) as much as possible. In that case, connect control system GND (AGND) and switching system GND (PGND) at the single point of GND (PGND) in IC.
- Connect the switching system parts as much as possible on the surface. Avoid the connection through the through-hole as much as possible.
- As for GND pins of the switching system parts, provide the through hole at the proximal place, and connect it with GND of internal layer.
- Pay the most attention to the loop composed of input capacitor ($C_{IN}$), switching FET, and fly-back diode (SBD). Consider making the current loop as small as possible.
- Place the boot strap capacitor ($C_{BOOT1}$, $C_{BOOT2}$) proximal to CBx and LXx pins of IC as much as possible.
- Large electric current flows momentary in the net of DRVHx and DRVLx pins connected with the gate of switching FET. Wire the linewidth of about 0.8 mm to be a standard, as short as possible.
- By-pass capacitor ($C_{VBLPF}$, $C_{VCC}$, $C_{VB}$) connected with CVBLPF, VCC, and VB should be placed close to the pin as much as possible. Also connect the GND pin of the bypass capacitor with GND of internal layer in the proximal through-hole.
- Pull the feedback line to be connected to the VOx pin of the IC separately from near the output capacitor pin, whenever possible, in order to feed back it to the IC more accurately. It is the ripple voltage which is generated from ESR of the output capacitor. Consider the net connected with VOx and FBx pins to keep away from a switching system parts as much as possible because it is sensitive to the noise.
  Moreover, place the output voltage setting resistor connected with this net close to the IC as much as possible, and try to make the net as short as possible. In addition, for the internal layer right under the component mounting place, provide the control system GND (AGND) of few ripple and few spike noises, or provide the ground plane of the power supply as much as possible.

Switching system parts : Input capacitor ($C_{IN}$), Switching FET, Fly-back diode (SBD), Inductor (L), Output capacitor ($C_O$)

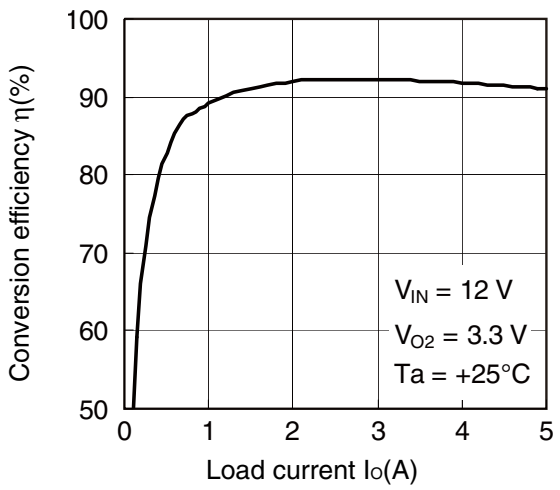


## ■ REFERENCE DATA

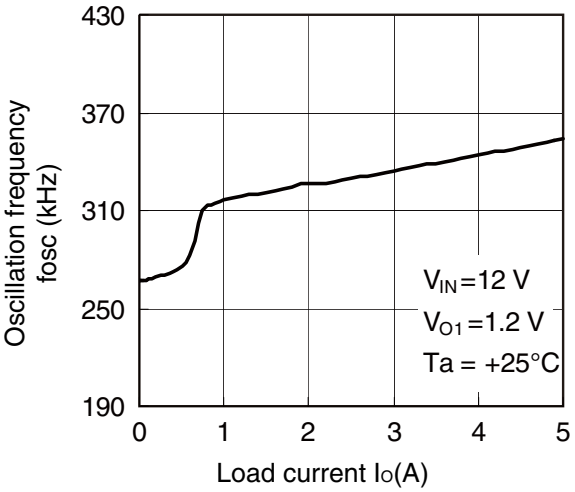
Conversion efficiency vs. Load current



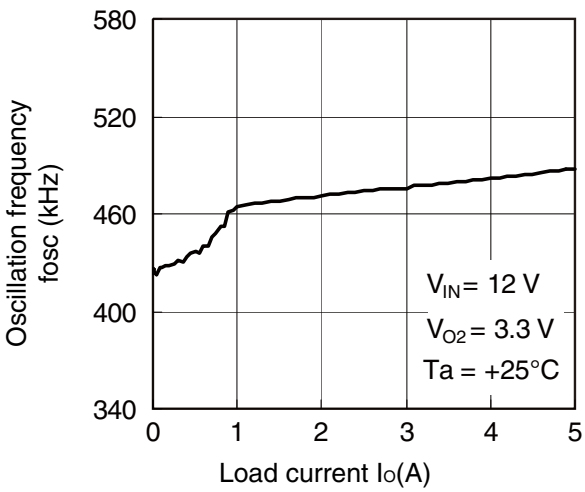

Conversion efficiency vs. Load current



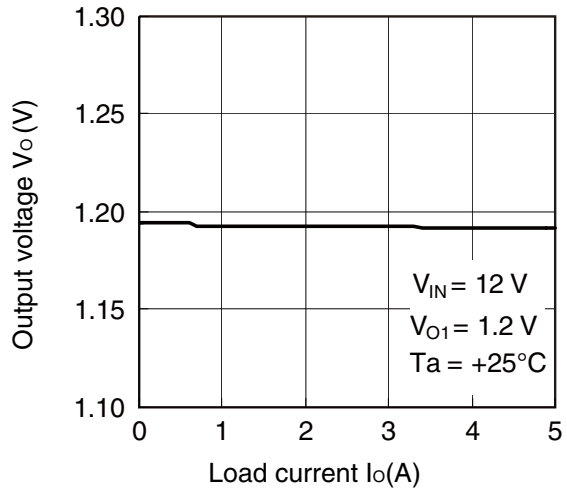

Oscillation frequency vs. Load current



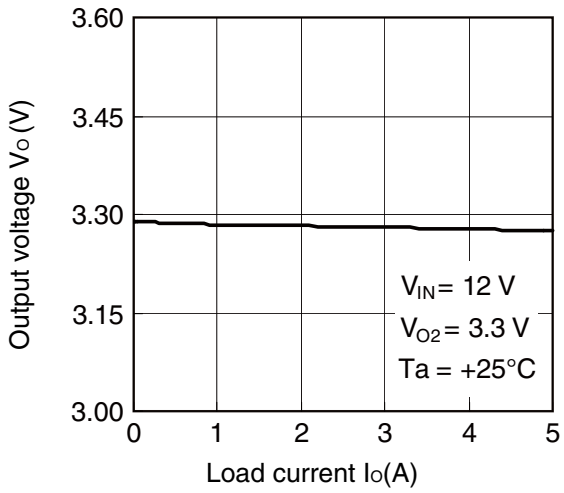

Oscillation frequency vs. Load current




Output voltage vs. Load current




Output voltage vs. Load current

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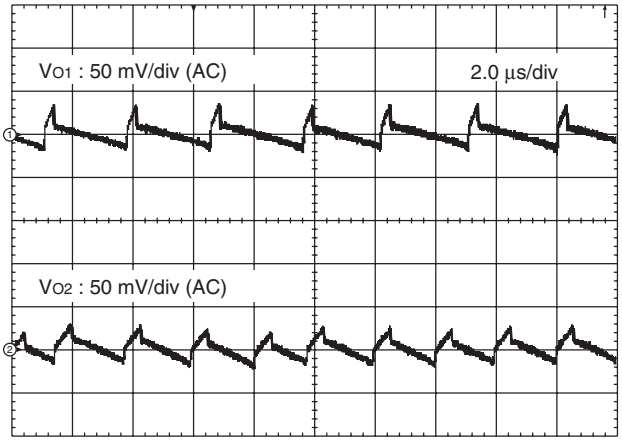
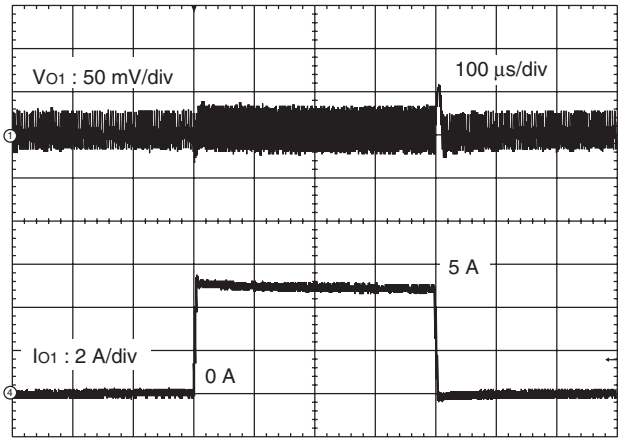
Ripple Waveform



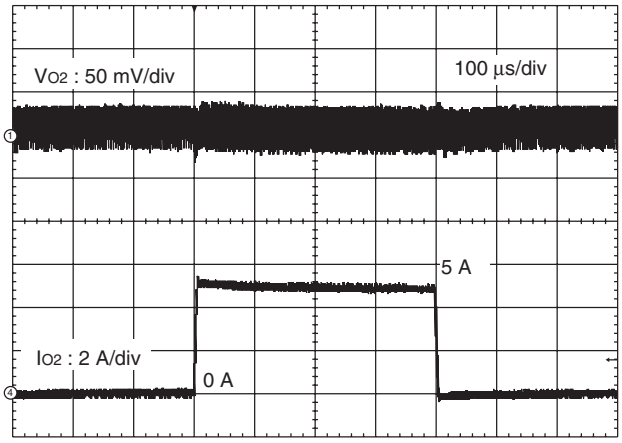

$V_{IN}$ = 12 V, $V_{O1}$ = 1.2 V, $I_{O1}$ = 5 A, $V_{O2}$ = 3.3 V, $I_{O2}$ = 5 A,
Ta = + 25 °C

CH1 Load Sudden Change Waveform



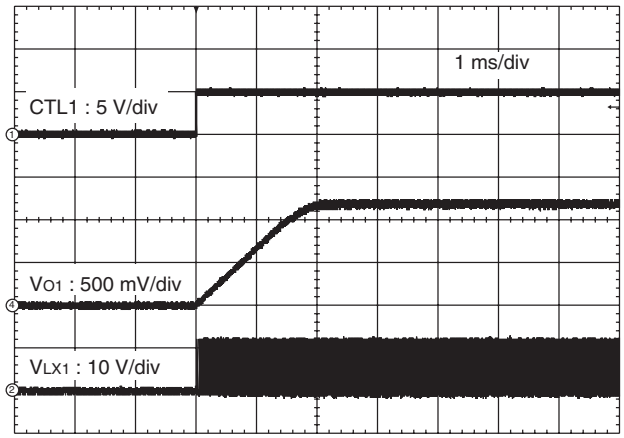

$V_{IN}$ = 12 V, $V_{O1}$ = 1.2 V, SR SET = 0.75 A/µs
$I_{O2}$ = 0 A ⇔ 5 A, Ta = + 25 °C

CH2 Load Sudden Change Waveform



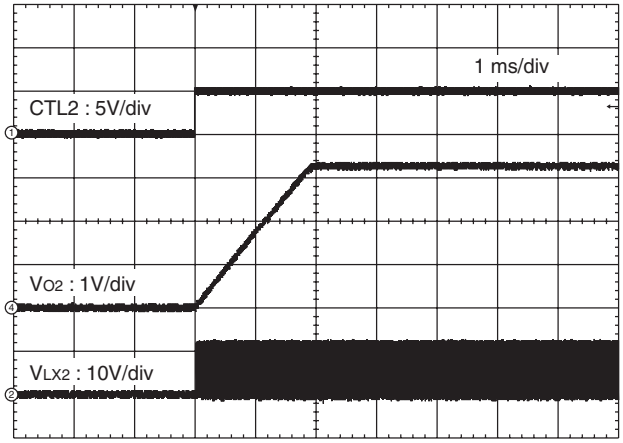

$V_{IN}$ = 12 V, $V_{O2}$ = 3.3 V, SR SET = 0.75 A/µs
$I_{O2}$ = 0 A ⇔ 5 A, Ta = + 25 °C

CH1 CTL Startup Waveform




$V_{IN}$ = 12 V, $V_{O1}$ = 1.2 V, $I_{O1}$ = 5 A (0.24 Ω),
Softstart setting time = 2.1 ms, Ta = + 25 °C

CH2 CTL Startup Waveform




$V_{IN}$ = 12 V, $V_{O2}$ = 3.3 V, $I_{O2}$ = 5 A (0.66 Ω),
Softstart setting time = 1.9 ms, Ta = + 25 °C

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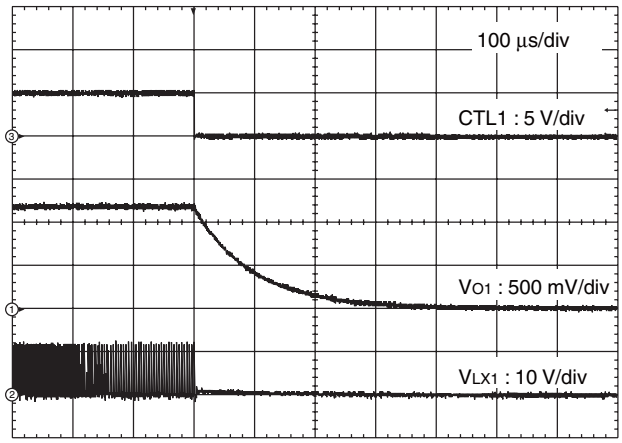
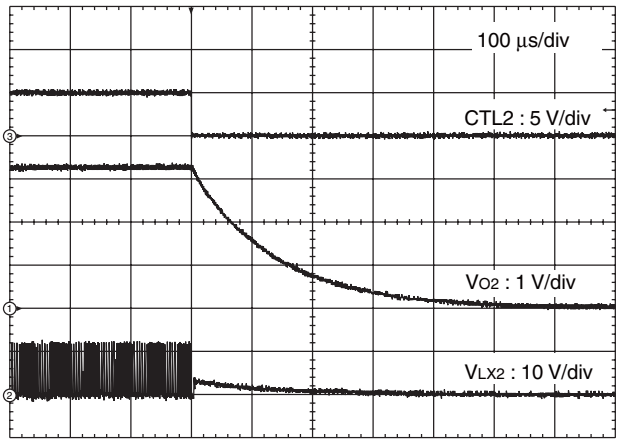
CH1 CTL Shutdown Waveform



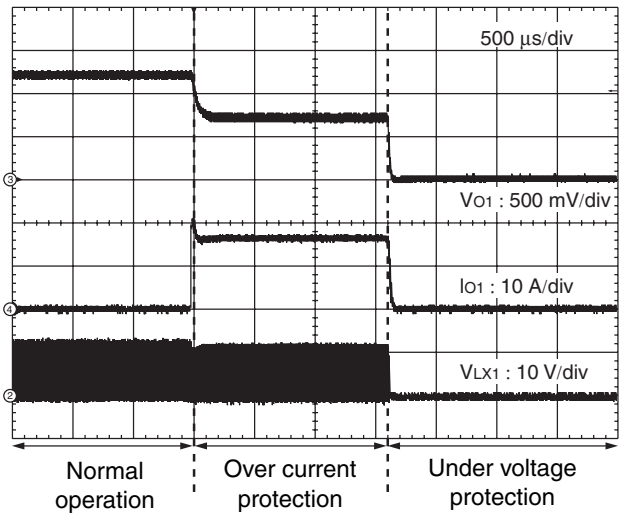

$V_{IN}$ = 12 V, $V_{O1}$ = 1.2 V, $I_{O1}$ = 5 A (0.24 Ω), Ta = + 25 °C

CH2 CTL Shutdown Waveform



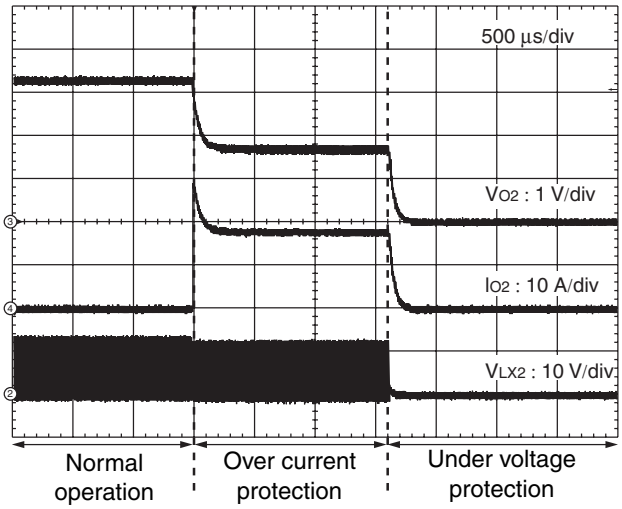

$V_{IN}$ = 12 V, $V_{O2}$ = 3.3 V, $I_{O2}$ = 5 A (0.66 Ω), Ta = + 25 °C

CH1 Output Over Current Waveform




$V_{IN}$ = 12 V, $V_{O1}$ = 1.2 V, Ta = + 25°C

CH2 Output Over Current Waveform




$V_{IN}$ = 12 V, $V_{O2}$ = 3.3 V, Ta = + 25°C

## ■ USAGE PRECAUTION

### 1. Do not configure the IC over the maximum ratings.

If the IC is used over the maximum ratings, the LSI may be permanently damaged.
It is preferable for the device to normally operate within the recommended usage conditions. Usage outside of these conditions can have an adverse effect on the reliability of the LSI.

### 2. Use the device within the recommended operating conditions.

The recommended values guarantee the normal LSI operation under the recommended operating conditions. The electrical ratings are guaranteed when the device is used within the recommended operating conditions and under the conditions stated for each item.

### 3. Printed circuit board ground lines should be set up with consideration for common impedance.

### 4. Take appropriate measures against static electricity.

- Containers for semiconductor materials should have anti-static protection or be made of conductive material.
- After mounting, printed circuit boards should be stored and shipped in conductive bags or containers.
- Work platforms, tools, and instruments should be properly grounded.
- Working personnel should be grounded with resistance of 250 kΩ to 1 MΩ in serial body and ground.

### 5. Do not apply negative voltages.

The use of negative voltages below −0.3 V may make the parasitic transistor activated to the LSI, and can cause malfunctions.

## ■ ORDERING INFORMATION

| Part number | Package | Remarks |
|---|---|---|
| MB39A138PFT-❑❑❑E1 | 24-pin plastic TSSOP<br>(FPT-24P-M10) | Lead free version |

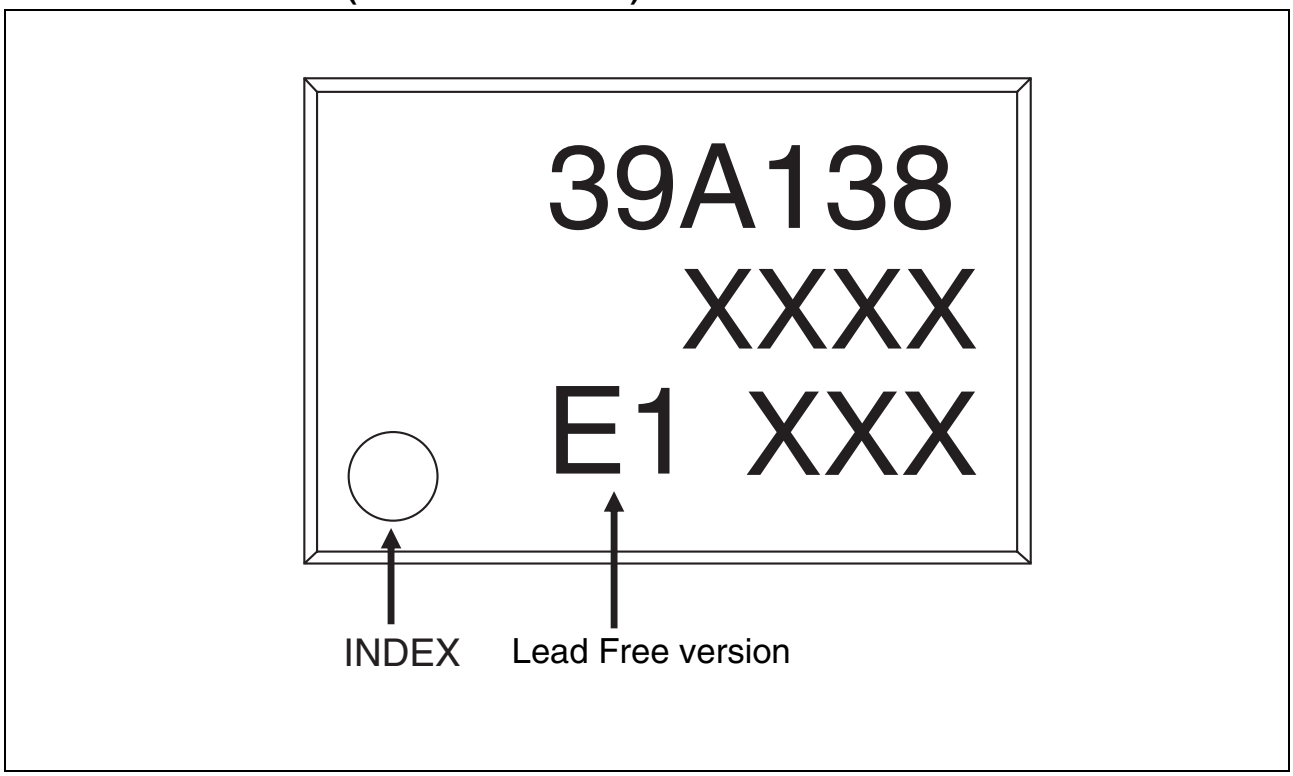
## ■ EV BOARD ORDERING INFORMATION

| EV board number | EV board version No. | Remarks |
|---|---|---|
| MB39A138EVB-01 | MB39A138EVB-01 Rev.2.0 | TSSOP-24 |

## ■ RoHS COMPLIANCE INFORMATION OF LEAD (Pb) FREE VERSION

The LSI products of Fujitsu Microelectronics with “E1” are compliant with RoHS Directive, and has observed the standard of lead, cadmium, mercury, Hexavalent chromium, polybrominated biphenyls (PBB) , and polybrominated diphenyl ethers (PBDE) . A product whose part number has trailing characters “E1” is RoHS compliant.

## ■ MARKING FORMAT (Lead Free version)



## ■ LABELING SAMPLE (Lead free version)

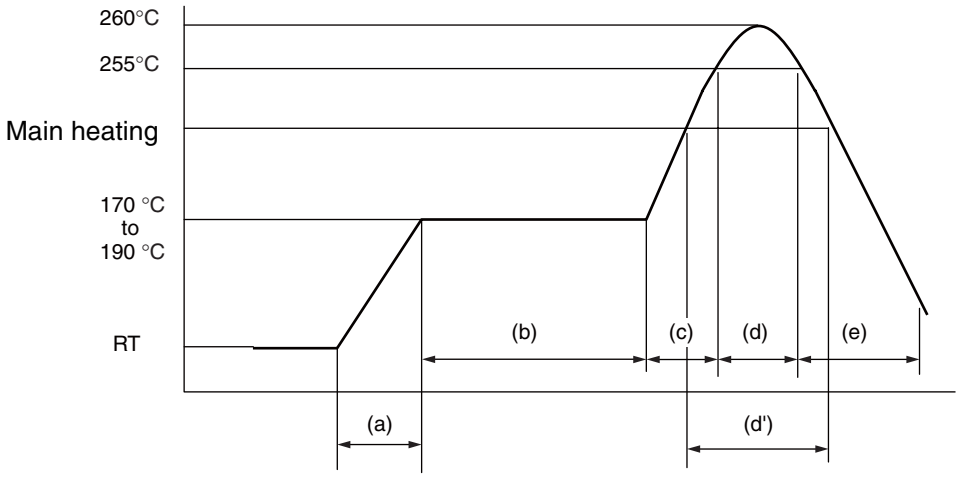
## ■ MB39A138PFT-❑❑❑ E1
## RECOMMENDED CONDITIONS OF MOISTURE SENSITIVITY LEVEL

**[Fujitsu Microelectronics Recommended Mounting Conditions]**

| Item | Condition | |
|---|---|---|
| Mounting Method | IR (infrared reflow) , Manual soldering (partial heating method) | |
| Mounting times | 2 times | |
| Storage period | Before opening | Please use it within two years after Manufacture. |
| | From opening to the 2nd reflow | Less than 8 days |
| | When the storage period after opening was exceeded | Please process within 8 days after baking (125 °C, 24h) |
| Storage conditions | 5 °C to 30 °C, 70%RH or less (the lowest possible humidity) | |

**[Mounting Conditions]**

**(1) IR (infrared reflow)**



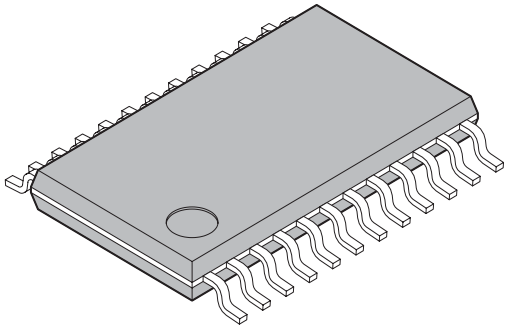

"H" level : 260 °C Max
(a) Temperature increase gradient : Average 1 °C/s to 4 °C/s
(b) Preliminary heating : Temperature 170 °C to 190 °C, 60 s to 180 s
(c) Temperature increase gradient : Average 1 °C/s to 4 °C/s
(d) Peak temperature : Temperature 260 °C Max; 255 °C or more, 10 s or less
(d') Main heating : Temperature 230 °C or more, 40 s or less
or
Temperature 225 °C or more, 60 s or less
or
Temperature 220 °C or more, 80 s or less
(e) Cooling : Natural cooling or forced cooling

Note: Temperature : on the top of the package body

**(2) Manual soldering (partial heating method)**

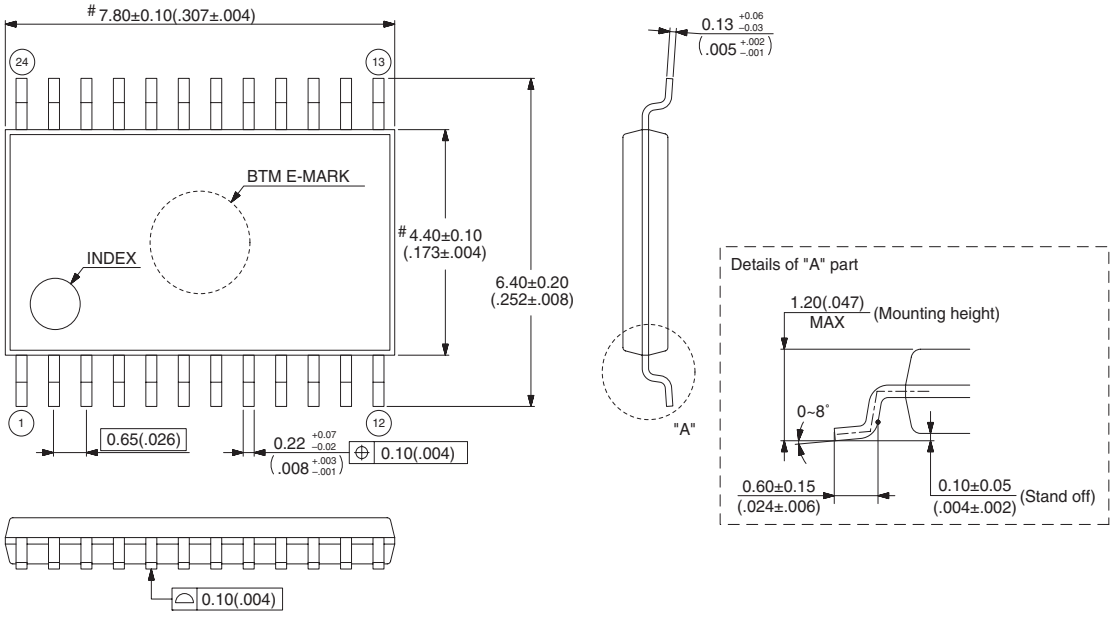
Temperature at the tip of an soldering iron: 400 °C max
Time: Five seconds or below per pin

## ■ PACKAGE DIMENSIONS

| 24-pin plastic TSSOP | | |
|---|---|---|
|  (FPT-24P-M10) | Lead pitch | 0.65 mm |
| | Package width × package length | 4.40 mm × 7.80 mm |
| | Lead shape | Gullwing |
| | Sealing method | Plastic mold |
| | Mounting height | 1.20 mm MAX |
| | Weight | 0.10 g |
| | | |

24-pin plastic TSSOP
(FPT-24P-M10)

Note 1) Pins width and pins thickness include plating thickness.
Note 2) Pins width do not include tie bar cutting remainder.
Note 3) #: These dimensions do not include resin protrusion.






Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

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