NANDxxxxNx

Large page NAND flash memory and low power SDRAM, 1.8/2.6 V MCP and PoP

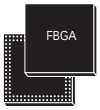
Features

- MCP (multichip package) and PoP (package on package)
  - NAND flash memory
  - 1-, 2-, 4-, 2x2-Gbit large page size NAND flash memory
  - 256-, 512-, 2x512-, 128+256/512-Mbit or 1-Gbit (x16/x32) SDR/DDR LPSDRAM
- Temperature range: -30 up to 85 °C
- Supply voltage
  - NAND flash: V_{DDF}= 1.7-1.95 V or 2.5-3.6 V
  - LPSDRAM: V_{DDD} = V_{DDQD} = 1.7-1.95 V
- Electronic signature
- ECOPACK® packages

Flash memory

- Nand interface
  - x8 or x16 bus width
  - Multiplexed address/data
- Page size
  - x8 device: (2048 + 64 spare) bytes
  - x16 device: (1024 + 32 spare) words
- Block size
  - x8 device: (128K + 4K spare) bytes
  - x16 device: (64K + 2K spare) words
- Page read/program
  - Random access: 25 µs (max)
  - Sequential access: 25/30 ns (min)
  - Page program time: 200 µs (typ)
- Copy back program mode
- Fast block erase: 1.5/2 ms (typ)
- Chip Enable ‘don’t care’
- Status register
- Data integrity
  - 100 000 program/erase cycles
  - 10 years data retention

TFBGA107 10.5 × 13 × 1.2 mm
TFBGA137 10.5 x 13 x 1.2 mm
LFBGA137 10.5 x 13 x 1.4 mm
TFBGA149 10 × 13.5 × 1.2 mm
VFBGA160 15 x 15 x 1 mm



VFBGA152 14 x 14 x 0.9 mm
TFBGA152 14×14 × 1.1 mm
TFBGA152 14 × 14 × 1.2 mm
TFBGA128 12 x 12 x 1.1 mm

Single or double data rate LPSDRAM

- Interface: x16/32 bus width
- Deep power-down mode
- 1.8 V LVCMOS interface
- Quad internal banks controlled by BA0, BA1
- Wrap sequence: sequential/interleaved
- Automatic and controlled precharge
- Auto refresh and self refresh
  - 8192 or 4096 (for 128 Mbits) refresh cycles/64 ms
  - Programmable partial array self refresh
  - Auto temperature compensated self refresh

Table 1. Device summary

NANDxxxxNx		
NANDA0R3N0	NANDA8R3N0	NANDA9R3Nx
NANDA9R4Nx	NANDA9WxN1	NANDB0R3N0
NANDBAR3Nx	NANDBAR4Nx	NANDB1R3N0
NANDB9R3N0	NANDB9R4Nx	NANDC9R4N0
NANDBAW4N1	NANDCAW4N1	NANDCBR4N3
NANDC3R4N5	NANDD3R4N5	NANDDBR3N5

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1 Description

The NANDxxxxNx devices combine multiple memory devices in a multichip package or a package-on-package solution that includes:

- 1.8/2.6 V supply 1- or 2-Gbit (x8/x16) or 4-Gbit (x16), or 1.8 V supply 2 x 2-Gbit (×16), NAND flash memories (NAND01GWxB2B, NAND01GRxB2B, NAND01GRxB2C, NAND02GRxB2C, NAND02GRxB2D, NAND04GxxB2D)
- 128-Mbit (x16) SDR (single data rate) LPSDRAM (M65KA128AJ) + 256-Mbit (x16) SDR LPSDRAM (M65KA256AJ), or
- 128-Mbit (x16) SDR LPSDRAM (M65KA128AJ) + 512-Mbit (x16) SDR LPSDRAM (M65KA512AC), or
- 256-Mbit (x16) SDR LPSDRAM (M65KA256AG), or
- 512-Mbit (x16) SDR LPSDRAM (M65KA512AB, or M65KA512AC, or M65KA512AH, or M65KA512AM), or
- 2 x 512-Mbit (x16) SDR LPSDRAMs (M65KA512AB, or M65KA512AM, or M65KA512AC, or M65KA512AJ), or
- 512-Mbit (x32) SDR LPSDRAM (M65KC512AB or M65KC512AC), or
- 1-Gbit (x32) SDR LPSDRAM (M65KC001AJ), or
- 512-Mbit (x16) DDR (double data rate) LPSDRAM (M65KG512AB, or M65KG512AH, or M65KG512AM, or M65KG512AC), or
- 512-Mbit (x32) DDR LPSDRAM (M65KD512AC), or
- 1-Gbit (x16) DDR LPSDRAM (M65KG001AJ), or
- 1-Gbit (x32) DDR LPSDRAM (M65KD001AJ)
- 2 x 1-Gbit (x32) DDR LPSDRAM (M65KD001AJ).

The NAND flash memory and LPSDRAM components have separate power supplies. They also have separate control, address and input/output signals, which allows simultaneous access to both devices at any moment. They may or not share the same grounds, depending on the package in which they are offered.

They are distinguished by a Chip Enable input, $\overline{E}_F$, for the NAND flash memory and a Chip Select, $\overline{E}_D$, for the LPSDRAM. See *Figure 1: Block diagram for TFBGA107, TFBGA137, and TFBGA149 packages*, *Figure 3: Block diagram for TFBGA128, TFBGA152 (NANDA8R3N0, NANDA9R3N0, NANDBAR3N, NANDB9R3N0), VFBGA152, and VFBGA160 packages*, *Figure 4: Block diagram for TFBGA152 package (NANDBAR3N0, NANDB0R3N0, NANDB1R3N0, NANDA0R3N0)*, and *Table 3: Signal names* for an overview of the signals associated with each component.

This datasheet should be read in conjunction with the SLC large page NAND flash datasheets (NAND01G-B2B_NAND02G-B2C, NAND01G-B2C, NAND02G-B2D, and NAND04G-B2D_NAND08G-BxC) and LPSDRAM datasheets (M65KA256AG, M65KA512AB, M65KA512AC, M65KG512AB, M65KC512AB, M65KC512AC, M65KD512AC, M65KAxxxAJ, M65KA512AH, M65KG512AH, M65KGxxxAJ, M65KAxxxAM, M65KCxxxAJ, M65KDxxxAJ, M65KGxxxAM, and M65KG512AC).

The NANDxxxxNx devices are available with a 1.8 V or 2.6 V voltage supply and are offered in the following packages as shown in *Table 2: Product list*:

- TFBGA107 (10.5 × 13 × 1.2 mm)
- TFBGA137 (10.5 x 13 x 1.2 mm)
- LFBGA137 (10.5 x 13 x 1.4 mm)
- TFBGA152 (14 × 14 × 1.1 mm) and TFBGA152 (14 × 14 × 1.2 mm)
- VFBGA152 (14 x 14 x 0.9 mm)
- TFBGA149 (10 × 13.5 × 1.2 mm)
- TFBGA128 (12 x 12 x 1.1 mm)
- VFBGA160 (15 x 15 x 1 mm)

The memories are supplied with all the NAND flash memory bits erased (set to ‘1’).

Table 2. Product list

Reference	Part number	NAND product	Datasheet	LPSDRAM product(1)(2)	LPSDRAM name	Package
NANDA0R3N0	NANDA0R3N0	1 Gbit (x8) - 1.8 V	NAND01G-B2B_NAND02G-B2C NAND01G-B2C	SDR 128 + 512 Mbits (x16), 1.8 V, 133 MHz	M65KA128AJ + M65KA512AC	TFBGA152
NANDA8R3N0	NANDA8R3N0	1 Gbit (x8) - 1.8 V	NAND01G-B2B_NAND02G-B2C	SDR 256 Mbits (x16), 1.8 V, 133 MHz	M65KA256AG	TFBGA152
NANDA9R3Nx	NANDA9R3N0	1 Gbit (x8) - 1.8 V	NAND01G-B2B_NAND02G-B2C	SDR 512 Mbits (x16), 1.8 V, 133 MHz	M65KA512AB or M65KA512AH	TFBGA107
			NAND01G-B2C		M65KA512AB	TFBGA152
					M65KA512AC	TFBGA128
	NANDA9R3N1	1Gbit (x8) - 1.8 V	NAND01G-B2B_NAND02G-B2C	SDR 512 Mbits (x32) 1.8 V, 133 MHz	M65KC512AC	TFBGA137
	NANDA9R3N2	1Gbit (x8) - 1.8 V		DDR 512 Mbits (x16) 1.8 V, 133 MHz	M65KG512AH	TFBGA107
	NANDA9R3N3	1Gbit (x8) - 1.8 V		DDR 512 Mbits (x32) 1.8 V, 133 MHz	M65KD512AC	TFBGA137
	NANDA9R3N6	1Gbit (x8) - 1.8 V	NAND01G-B2C	SDR 512 Mbits (x16) 1.8 V, 166 MHz	M65KA512AM	TFBGA107
NANDA9R4Nx	NANDA9R4N0	1 Gbit (x16) - 1.8 V	NAND01G-B2B_NAND02G-B2C	SDR 512 Mbits (x16), 1.8 V, 133 MHz	M65KA512AB or M65KA512AH	TFBGA149
	NANDA9R4N1	1 Gbit (x16) - 1.8 V		SDR 512 Mbits (x32) 1.8 V, 133 MHz	M65KC512AC	TFBGA137
	NANDA9R4N2	1 Gbit (x16) - 1.8 V		DDR 512 Mbits (x16), 1.8 V, 133 MHz	M65KG512AB or M65KG512AH	TFBGA149
	NANDA9R4N3	1 Gbit (x16) - 1.8 V		DDR 512 Mbits (x32), 1.8 V, 133 MHz	M65KD512AC	TFBGA137
	NANDA9R4N4	1 Gbit (x16) - 1.8 V	NAND01G-B2C	DDR 512 Mbits (x16), 1.8 V, 166 MHz	M65KG512AM	TFBGA149
	NANDA9R4N6	1 Gbit (x16) - 1.8 V		SDR 512 Mbits (x16), 1.8 V, 166 MHz	M65KA512AM	TFBGA149

Table 2. Product list (continued)

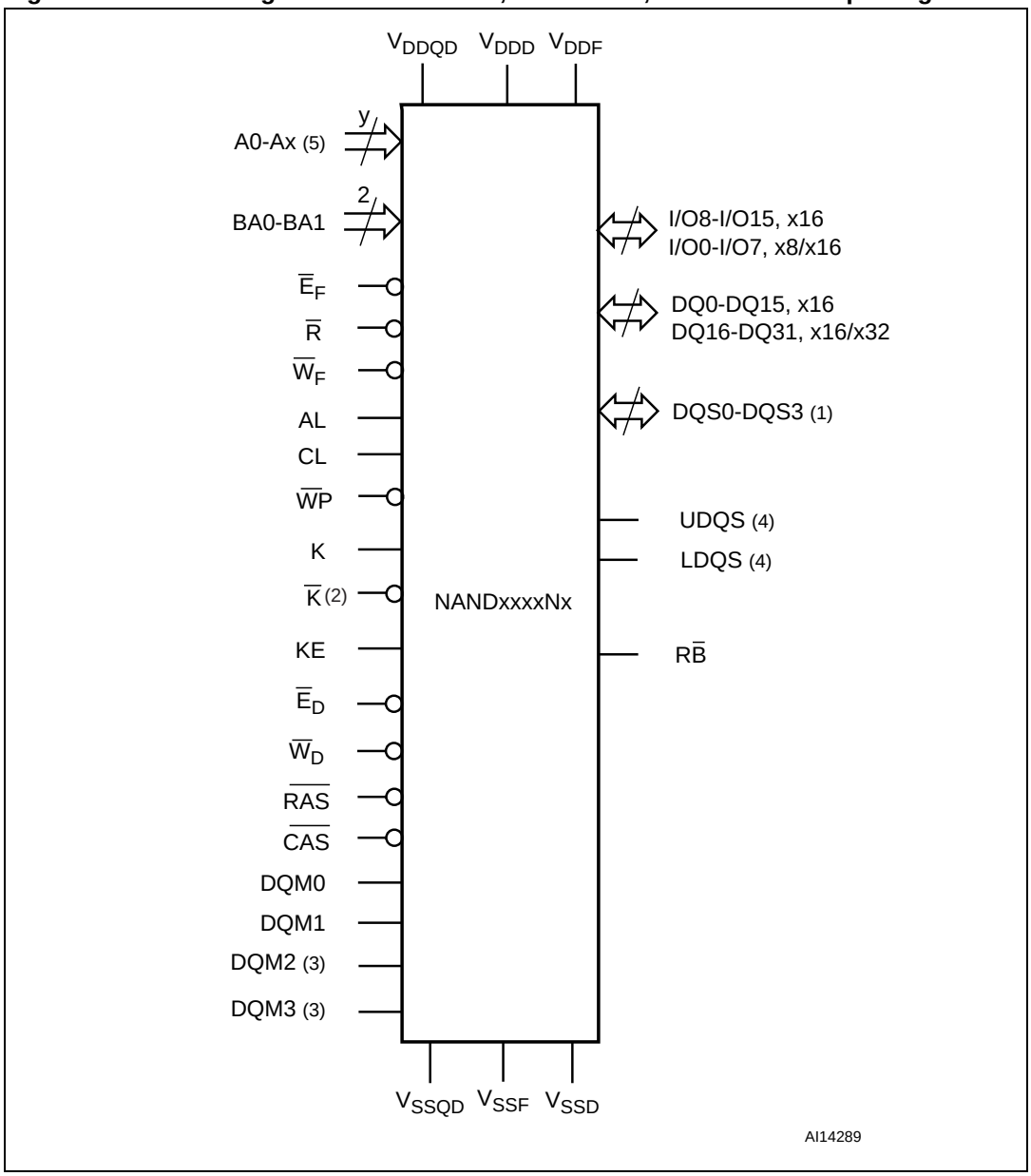
NANDA9WxN1	NANDA9W3N1	1 Gbit (x8) - 2.6 V	NAND01G-B2B_NAND02G-B2C	SDR 512 Mbits (x32) 1.8 V, 133 MHz	M65KC512AB	TFBGA137
	NANDA9W4N1	1 Gbit (x16) - 2.6 V			M65KC512AC	
NANDB0R3N0	NANDB0R3N0	2 Gbits (x8) - 1.8 V	NAND02G-B2D	SDR 128 + 512 Mbits (x16) 1.8 V, 133 MHz	M65KA128AJ + M65KA512AC	TFBGA152
NANDBAR3Nx	NANDBAR3N1	2 Gbits (x8) - 1.8 V	NAND02G-B2D	SDR 1 Gbit (x 32) [2 x 512 Mbits x16], 1.8 V, 133 MHz	M65KA512AB	TFBGA152
	NANDBAR3N6	2 Gbits (x8) - 1.8 V		SDR 1 Gbit (x32) [2 x 512 Mbits x16], 1.8 V, 166 MHz	M65KA512AM	TFBGA128
NANDBAR4Nx	NANDBAR4N0	2 Gbits (x16) - 1.8 V	NAND02G-B2D	SDR 1 Gbit (x16), 1.8 V, 133 MHz	M65KA001AJ	TFBGA149
	NANDBAR4N1	2 Gbits (x16)- 1.8 V		SDR 1 Gbit (x32)(2 x 512 Mbits x16), 1.8 V, 166 MHz	M65KA512AJ	TFBGA137
	NANDBAR4N2	2 Gbits (x16)- 1.8 V		DDR 1 Gbit (x16), 1.8 V, 133 MHz	M65KG001AJ	VFBGA160
						TFBGA149
	NANDBAR4N5	2 Gbits (x16)- 1.8 V		DDR 1 Gbit (x32), 1.8 V, 166 MHz	M65KD001AJ	TFBGA137
						VFBGA152
	NANDBAR4N7	2 Gbits (x16)- 1.8 V		SDR 1 Gbit (x32), 1.8 V, 166 MHz	M65KC001AJ	TFBGA137
NANDBAW4N1	NANDBAW4N1	2 Gbits (x16)- 2.6 V	NAND02G-B2D	SDR 1 Gbit (x32), 1.8 V, 133 MHz	M65KA512AJ	TFBGA137
TBD	TBD	2 Gbits (x8)- 1.8 V	NAND02G-B2D	DDR 1 Gbit (x16), 1.8 V	M65KG001AM	TFBGA137
NANDB1R3N0	NANDB1R3N0	2 Gbits (x8) - 1.8 V	NAND02G-B2D	SDR 128 + 256 Mbits (x16) 1.8 V, 133 MHz	M65KA128AJ + M65KA256AJ	TFBGA152
NANDB9R3N0	NANDB9R3N0	2 Gbits (x8) - 1.8 V	NAND01G-B2B_NAND02G-B2C	SDR 512 Mbits (x16), 1.8 V, 133 MHz	M65KA512AB	TFBGA128
			NAND02G_B2D		M65KA512AC	TFBGA152

Table 2. Product list (continued)

NANDB9R4Nx	NANDB9R4N0	2 Gbits (x16) - 1.8 V	NAND01G-B2B_NAND02G-B2C	SDR 512 Mbits (x16), 1.8 V, 133 MHz	M65KA512AB	TFBGA149
	NANDB9R4N2	2 Gbits (x16) - 1.8 V	NAND02G_B2D	DDR 512 Mbits (x16), 1.8 V, 133 MHz	M65KG512AC	TFBGA149
	NANDB9R4N5	2 Gbits (x16) - 1.8 V	NAND01G-B2B_NAND02G-B2C	DDR 512 Mbits (x32) 1.8 V, 166 MHz	M56KD512AC	TFBGA137
NANDC3R4N5	NANDC3R4N5	4 Gbits (x16) - 1.8 V	NAND04GR4B2D	DDR 1G (x32) 2x 1G DDR (x16)	M65KD001AM M65KG001AM	LFBGA137
NANDCAW4N1	NANDCAW4N1	4 Gbits (x16)- 2.6 V	NAND04G-B2D_NAND08G-BxC	SDR 1 Gbit (x32)(2 x 512 Mbits x16), 1.8 V, 133 MHz	M65KA512AJ	TFBGA137
NANDCBR4N3	NANDCBR4N3	4 Gbits (x16)- 1.8 V	NAND04G-B2D_NAND08G-BxC	DDR 2 Gbits (x32)(2 x 1 Gbit x32), 1.8 V, 133 MHz	M65KD001AJ	LFBGA137
NANDC9R4N0	NANDC9R4N0	2x2 Gbits (x16) - 1.8 V	NAND01G-B2B_NAND02G-B2C	SDR 512 Mbits (x16), 1.8 V, 133 MHz	M65KA512AB	TFBGA149
NANDD3R4N5	NANDD3R4N5	2x4 Gbits (x16) - 1.8 V	NAND08GR4B2C	DDR 1G (x32) 2x 1G DDR (x16)	M65KD001AM M65KG001AM	LFBGA137
NANDDBR3N5	NANDDBR3N5	2x4 Gbits (x16) - 1.8 V	NAND08GR4B2C	2x 1G DDR (x16)	M65KG001AM	LFBGA137

1. SDR = single data rate.
2. DDR = double data rate.

Figure 1. Block diagram for TFBGA107, TFBGA137, and TFBGA149 packages



1. Only available in MCP with DDR x32.
2. Only available in MCP with DDR.
3. Only available in MCP with SDR/DDR x32.
4. Only available in MCP with DDR x16.
5. x = 12 (width bus DRAM y = 13 bits) except for NANDBAR4N0 and NANDBAR4N2, which have x = 13 (width bus DRAM y = 14 bits).

Figure 2. Block diagram for LFBGA137 package

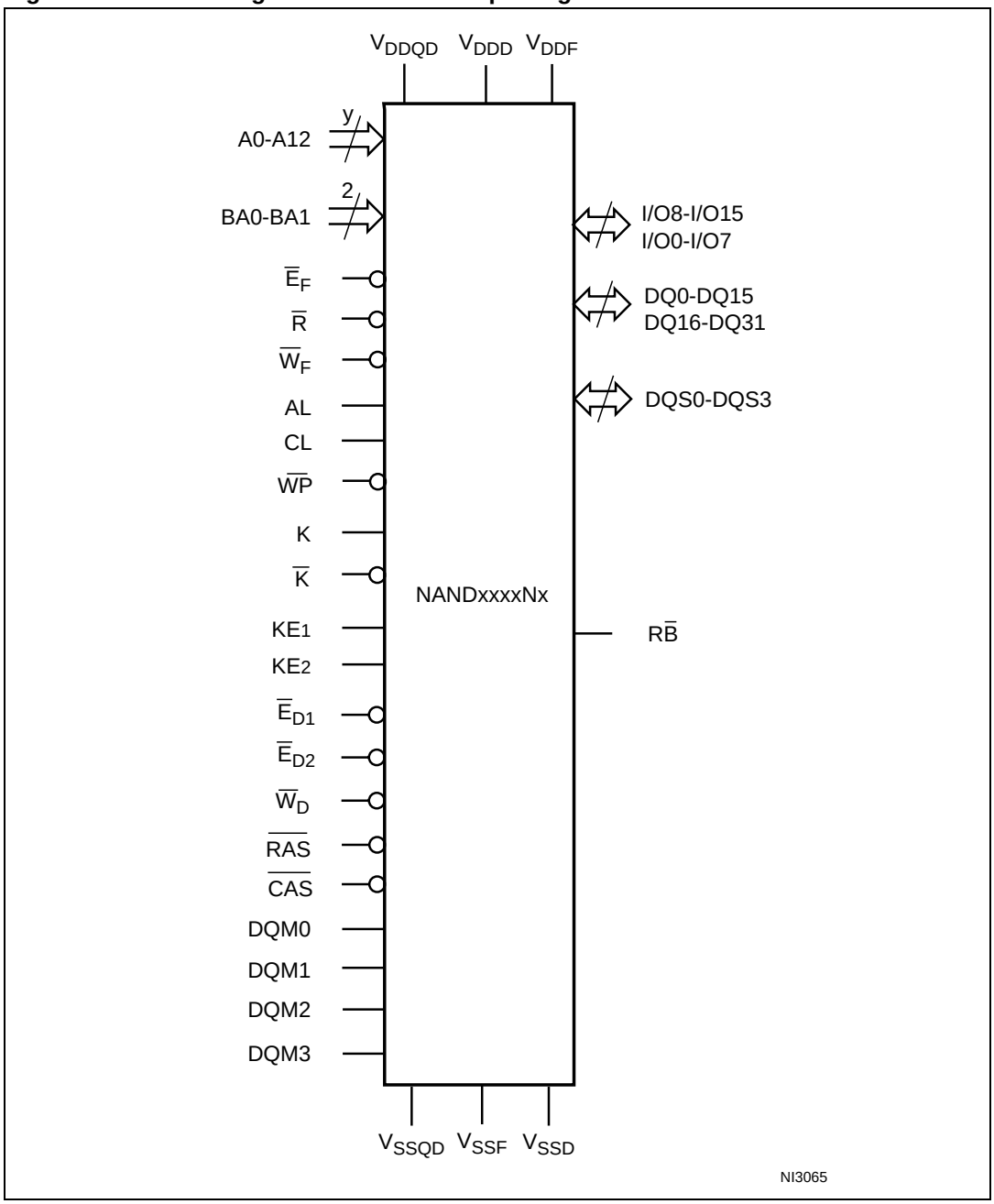
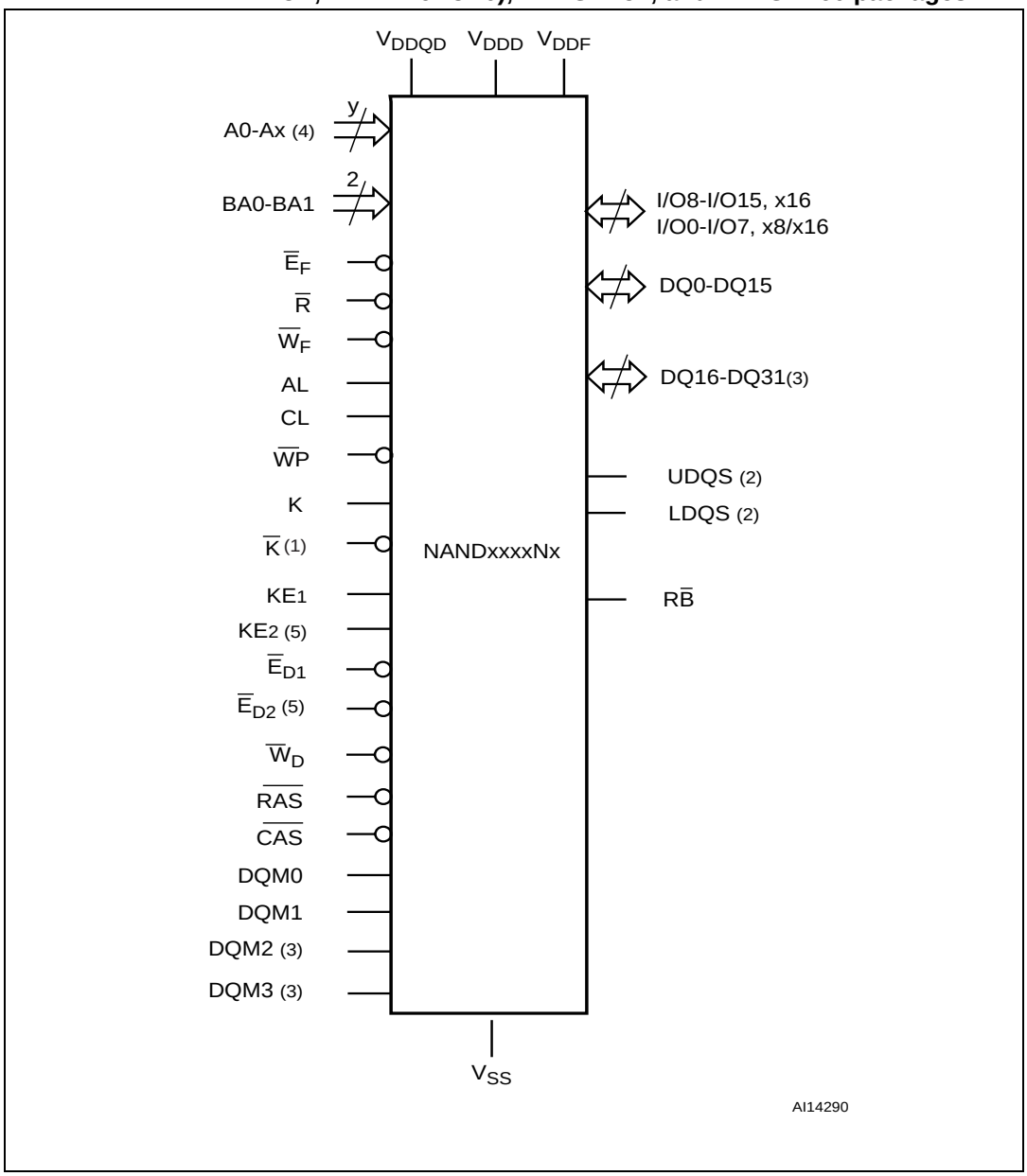
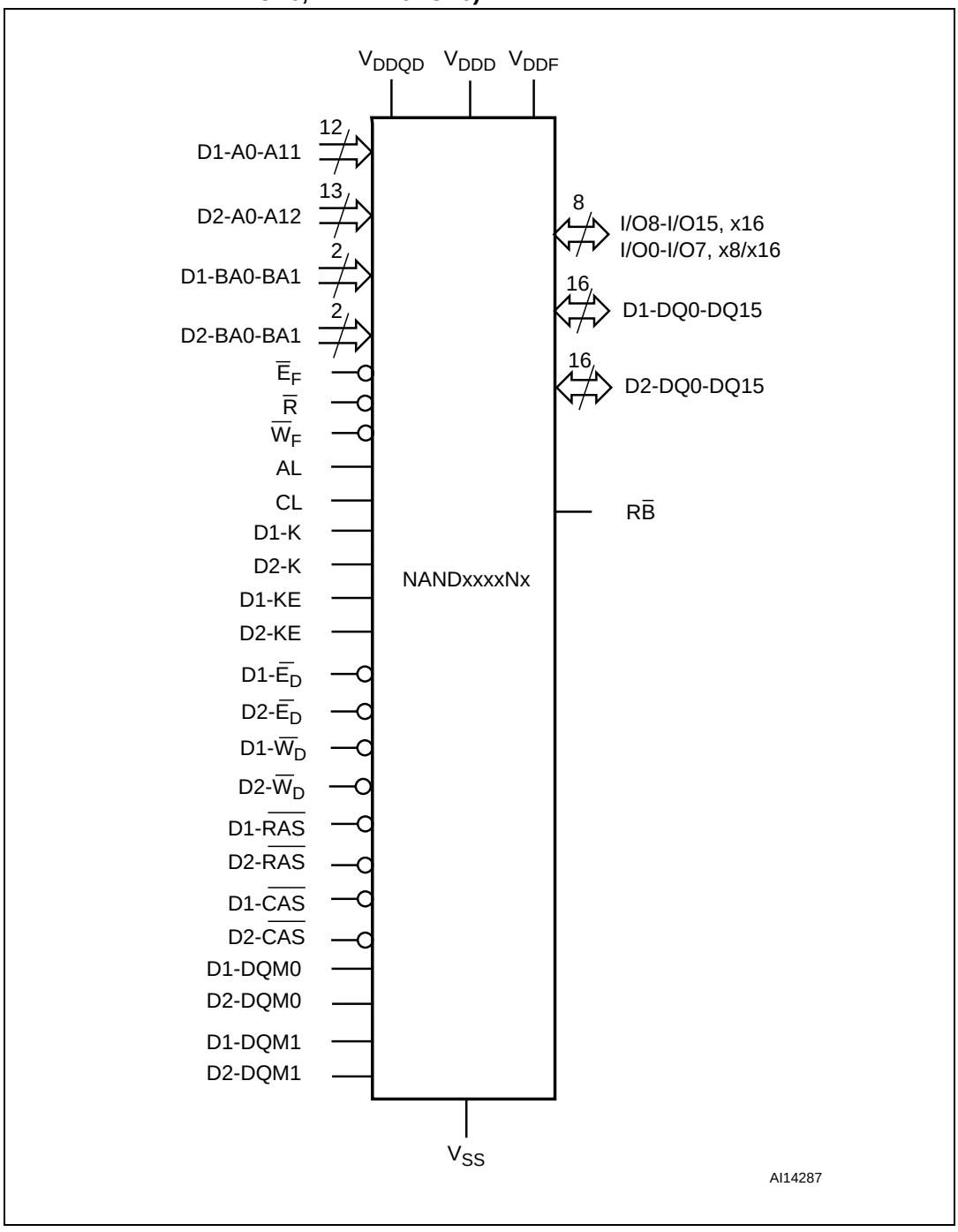


Figure 3. Block diagram for TFBGA128, TFBGA152 (NANDA8R3N0, NANDA9R3N0, NANDBAR3N, NANDB9R3N0), VFBGA152, and VFBGA160 packages



1. Only available in PoP with DDR.
2. Only available in PoP with DDRx16.
3. Only available in PoP with SDR/DDR x32.
4. x = 12 (width bus DRAM y = 13 bits) except for NANDBAR4N2, which has x = 13 (width bus DRAM y = 14 bits).
5. KE_2 and $\overline{E}_{D2}$ are only used for the possible second LPSDRAM (NANDBAR3N6).

Figure 4. Block diagram for TFBGA152 package (NANDBAR3N0, NANDB0R3N0, NANDB1R3N0, NANDA0R3N0)



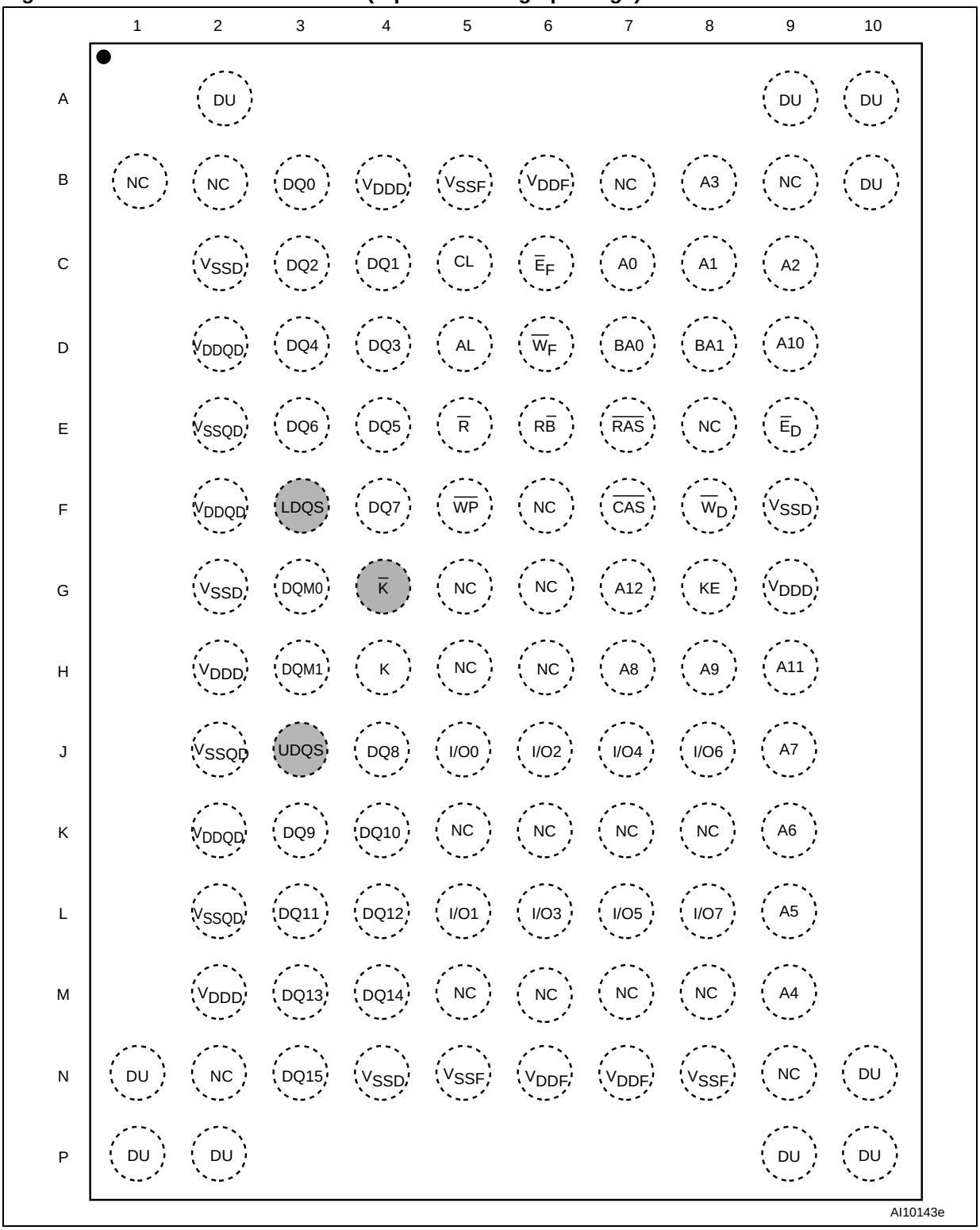
1. D1-X signals are related to the 128-Mbit SDR, while D2-X signals are related to the 256- or 512-Mbit SDR.

Table 3. Signal names

Signal	Function	Direction
NAND flash memory		
I/O0-I/O7	Data input/outputs (x8/x16)	Input/output
I/O8-I/O15	Data inputs/outputs (x16)	Input/output
AL	Address Latch Enable	Input
CL	Command Latch Enable	Input
$\overline{E_F}$	Chip Enable	Input
$\overline{R}$	Read Enable	Input
$\overline{RB}$	Ready/Busy (open-drain output)	Output
$\overline{W_F}$	Write Enable	Input
$\overline{WP}$	Write Protect	Input
V_{DDF}	Supply voltage	Power supply
V_{SSF}	Ground	Ground
LPSDRAM		
A0-Ax	Address inputs - A10 determines the precharge mode	Input
BA0-BA1	Bank Select inputs	Input
DQ0-DQ15	Data inputs/outputs (x16/x32)	Input/output
DQ16-DQ31	Data inputs/outputs (x32)	Input/output
DQS0(1)	Data Read/Write Strobe for DQ0-DQ7	Input/output
DQS1(1)	Data Read/Write Strobe for DQ8-DQ15	Input/output
DQS2(1)	Data Read/Write Strobe for DQ15-DQ23	Input/output
DQS3(1)	Data Read/Write Strobe for DQ24-DQ31	Input/output
K	Clock inputs	Input
$\overline{K}$ (2)	Clock inputs	Input
KE	Clock Enable input	Input
$\overline{E_D}$	Chip Select inputs	Input
$\overline{W_D}$	Write Enable input	Input
$\overline{RAS}$	Row Address Strobe input	Input
$\overline{CAS}$	Column Address Strobe input	Input
DQM0	DQ Mask Enable input controls DQ0-DQ7	Input
DQM1	DQ Mask Enable input controls DQ8-DQ15	Input
DQM2(3)	DQ Mask Enable input controls DQ16-DQ23	Input
DQM3(3)	DQ Mask Enable input controls DQ24-DQ31	Input
LDQS/UDQS(4)	Lower/Upper Data Read/Write Strobe I/O	Input/output
V_{DDD}	Supply voltage	Power supply
V_{DDQD}	Input/output supply voltage	Power supply
V_{SSQD}	Input/output ground	Ground
V_{SSD}	Ground	Ground
NC	Not connected internally	
DU	Do not use	

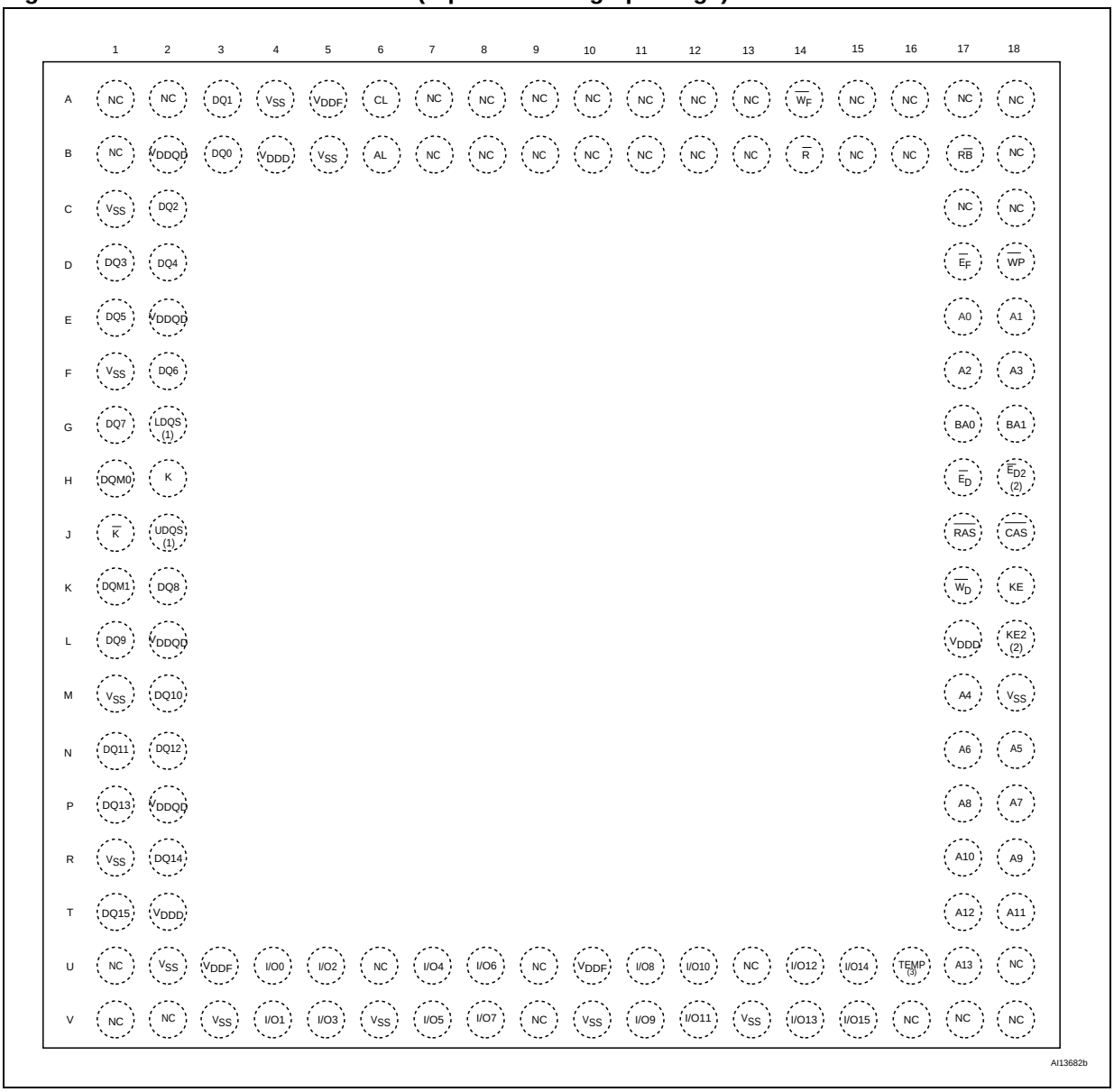
1. Only available with DDR x32.
2. Only available with DDR.
3. Only available with SDR/DDR x32.
4. Only available with DDR x16.

Figure 5. TFBGA107 connections (top view through package)



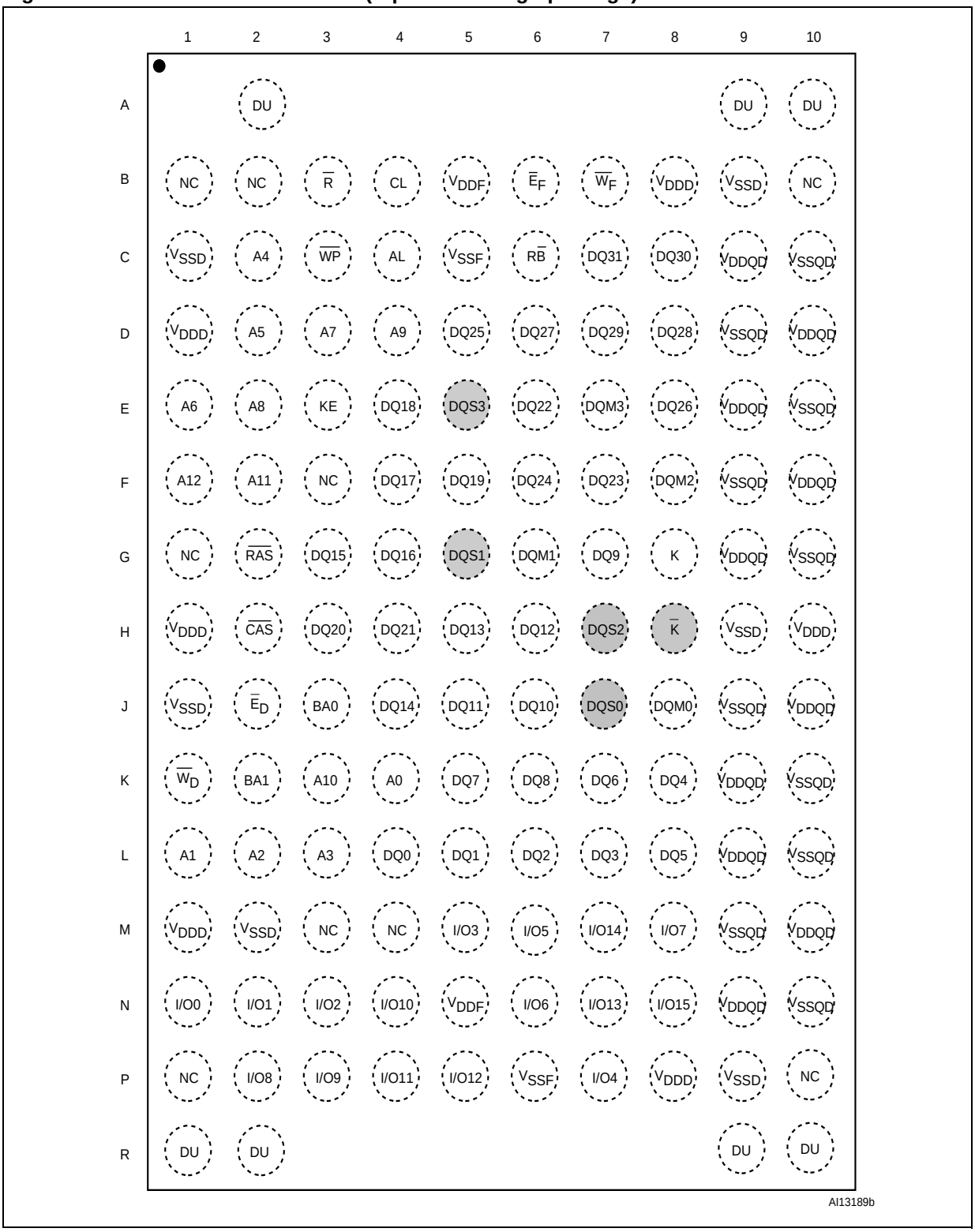
1. All voltage balls must be connected to the power supply (the internal connection is not guaranteed). All ground balls must be connected to the ground.
2. Balls shaded in gray are only used for NAND and DDR devices.

Figure 6. TFBGA128 connections (top view through package)



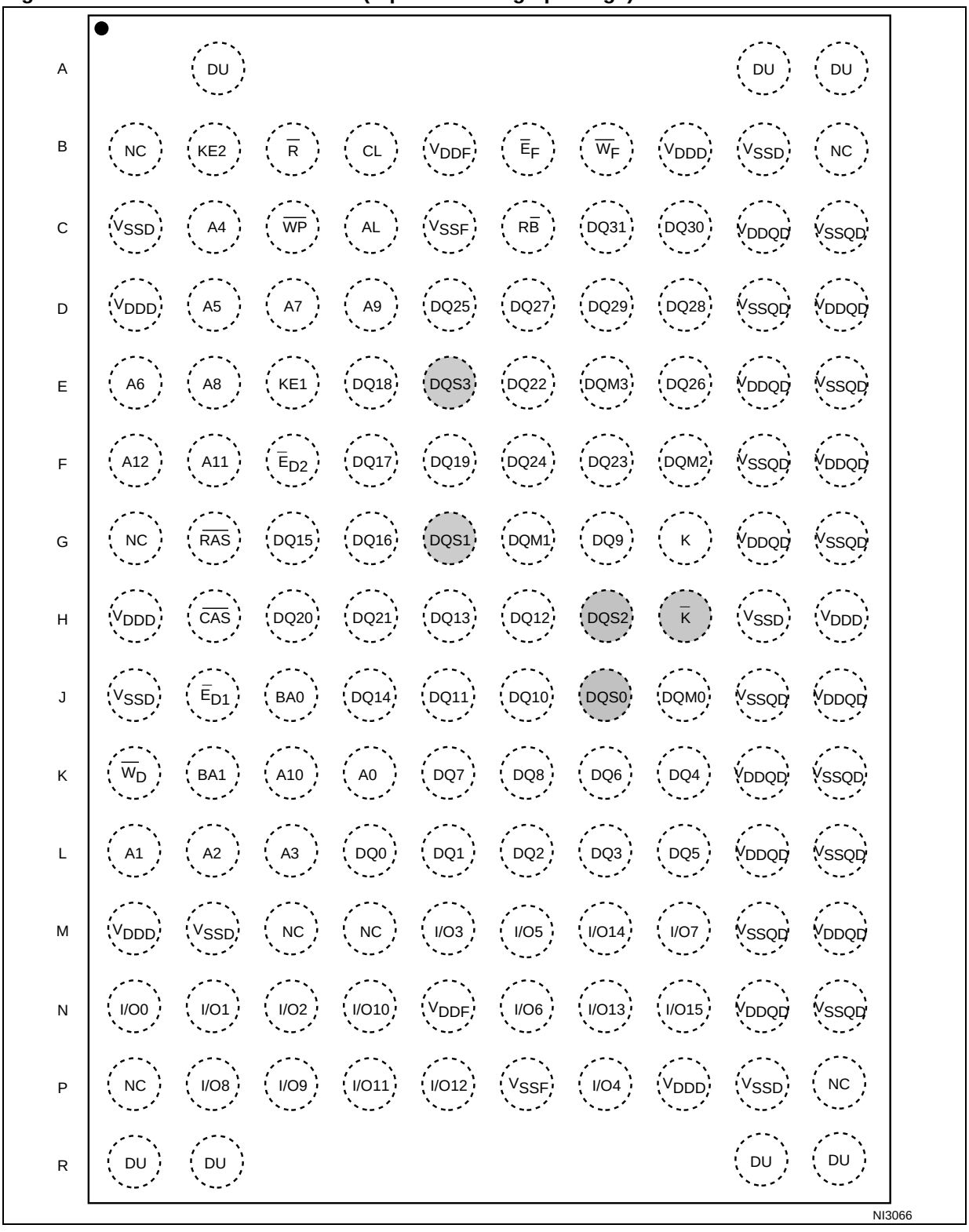
1. Only used for DDR.
2. Only used for the possible second LPSDRAM (NANDBAR3N6).
3. Ball U16 is the LPSDRAM temperature flag.
4. All voltage balls must be connected to the power supply (the internal connection is not guaranteed). All ground balls must be connected to the ground.

Figure 7. TFBGA137 connections (top view through package)



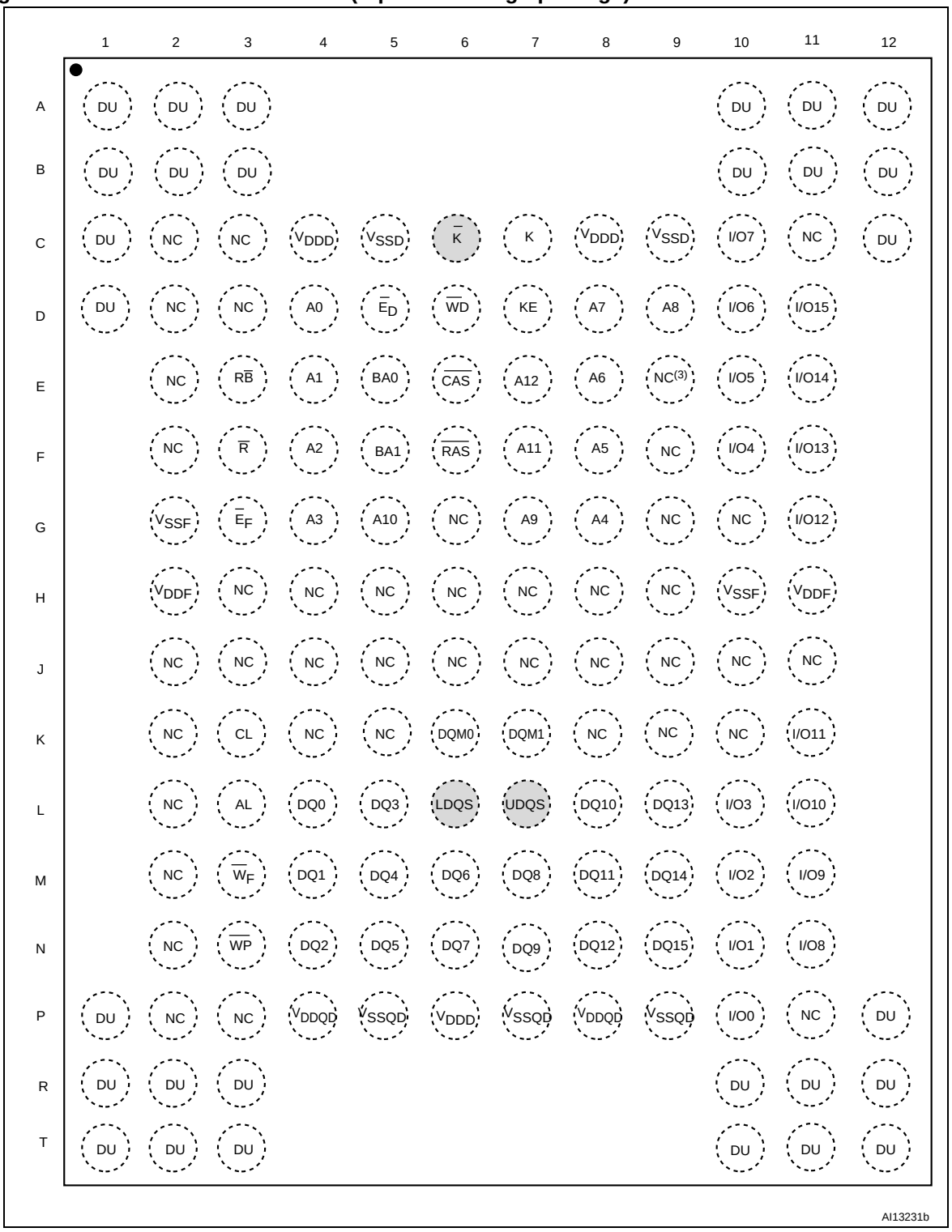
1. Balls shaded in gray are only used for NAND and DDR devices.
2. All voltage balls must be connected to the power supply (the internal connection is not guaranteed). All ground balls must be connected to the ground.

Figure 8. LFBGA137 connections (top view through package)



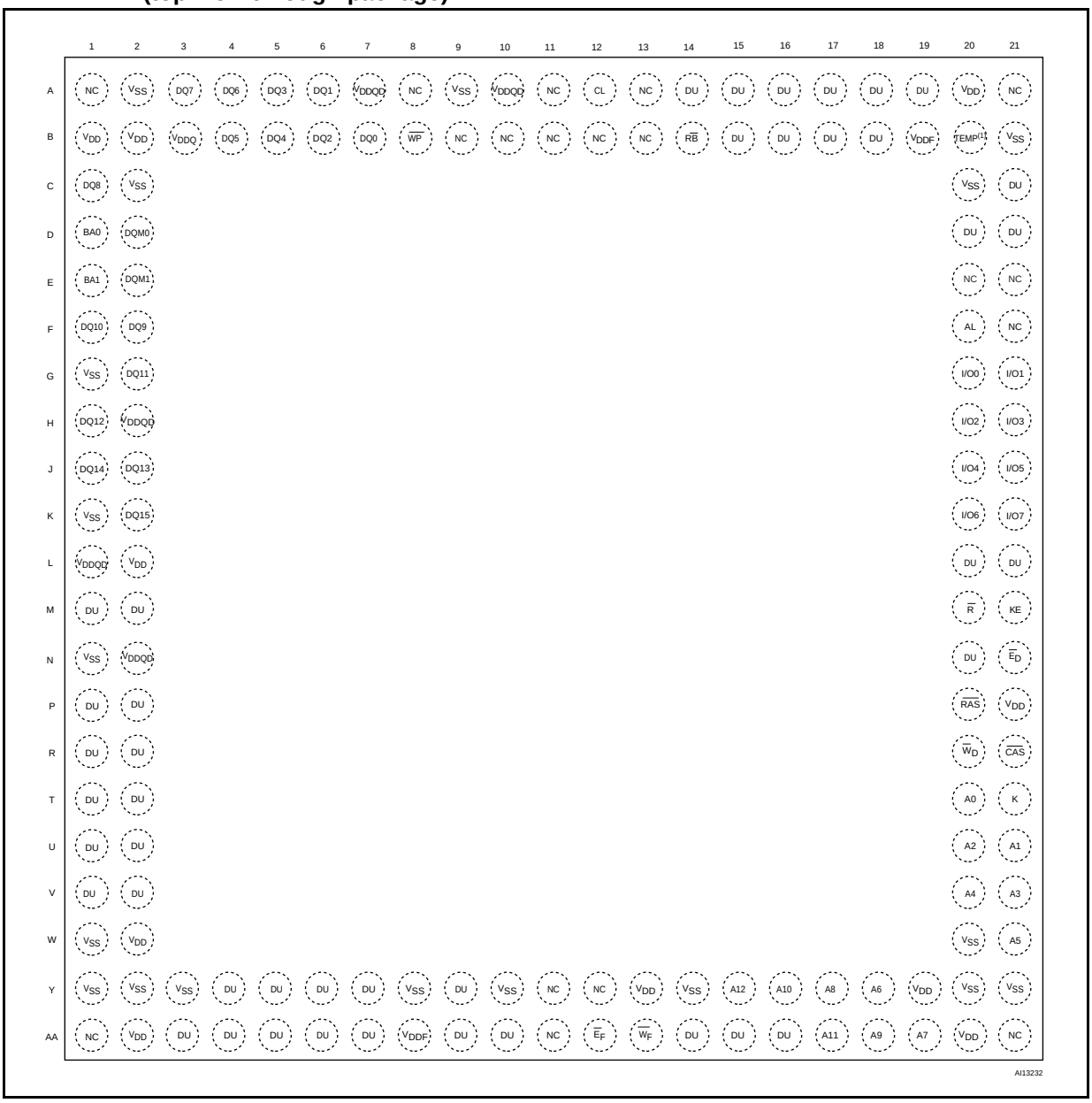
1. Balls shaded in gray are only used for NAND and DDR devices.
2. All voltage balls must be connected to the power supply (the internal connection is not guaranteed). All ground balls must be connected to the ground.

Figure 9. TFBGA149 connections (top view through package)



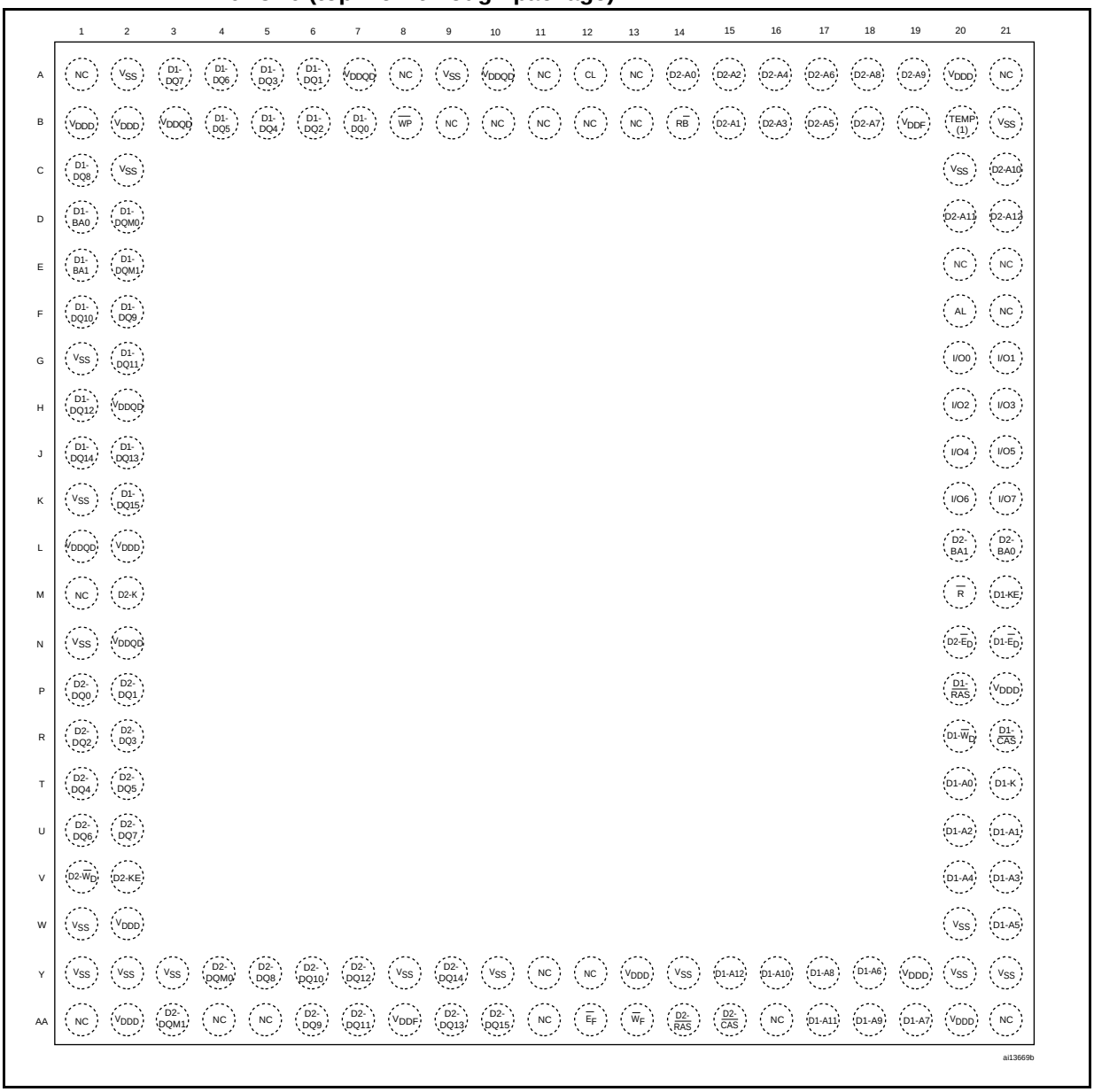
1. Balls shaded in gray are only used for NAND and DDR devices.
2. All voltage balls must be connected to the power supply (the internal connection is not guaranteed). All ground balls must be connected to the ground.
3. For NANDBAR4N0 and NANDBAR4N2, the ball E9 is the address A13.

Figure 10. TFBGA152 connections - NANDA8R3N0, NANDA9R3N0, NANDB9R3N0 (top view through package)



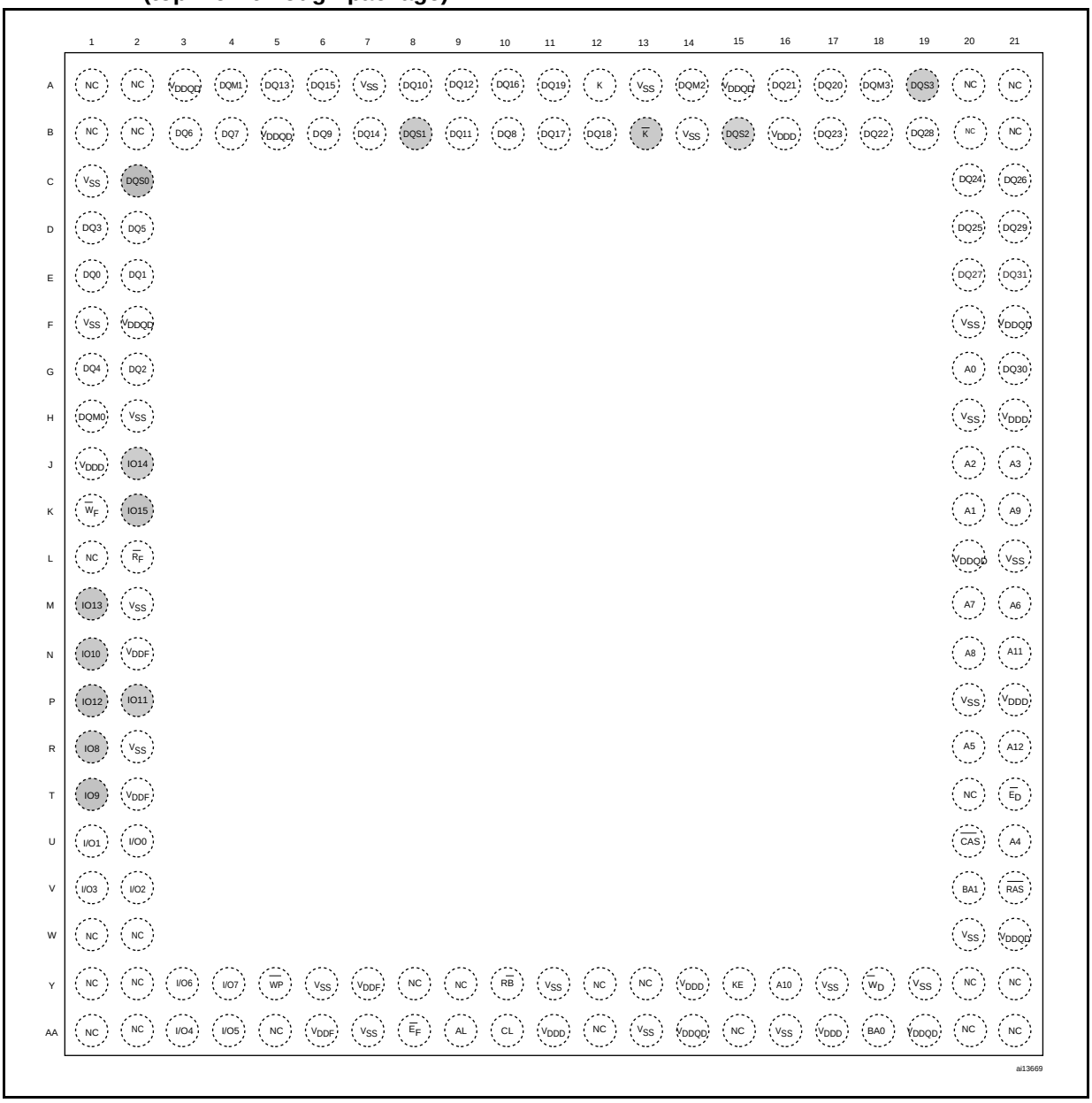
1. Ball B20 is the LPSDRAM temperature flag.
2. All voltage balls must be connected to the power supply (the internal connection is not guaranteed). All ground balls must be connected to the ground.

Figure 11. TFBGA152 connections - NANDBAR3N0, NANDB0R3N0, NANDB1R3N0, NANDA0R3N0 (top view through package)



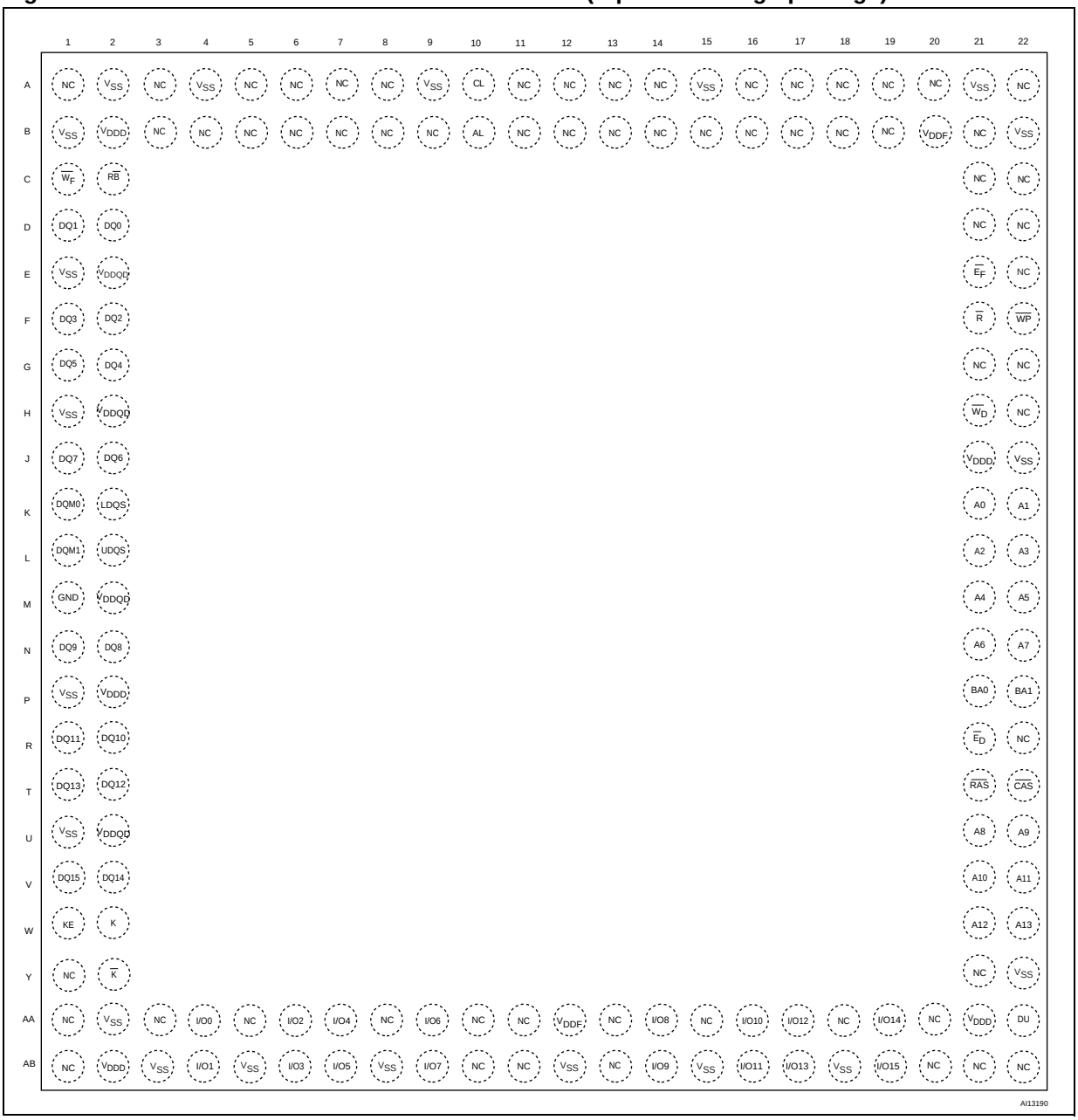
1. Ball B20 is the LPSDRAM temperature flag.
2. D1-X signals are related to the 128-Mbit SDR, while D2-X signals are related to the 512- or 256-Mbit SDR.
3. All voltage balls must be connected to the power supply (the internal connection is not guaranteed). All ground balls must be connected to the ground.

Figure 12. TFBGA152 (NANDBAR3N1) and VFBGA152 (NANDBAR4N5) connections - (top view through package)



1. All voltage balls must be connected to the power supply (the internal connection is not guaranteed). All ground balls must be connected to the ground.
2. Balls shaded in gray are only used for NANDBAR4N5.

Figure 13. VFBGA160 connections - NANDBAR4N2 (top view through package)



1. All voltage balls must be connected to the power supply (the internal connection is not guaranteed). All ground balls must be connected to the ground.

2 Signal descriptions

See *Figure 1*, *Figure 2*, *Figure 3*, *Figure 4*, and *Table 3* for a brief overview of the signals connected to this device. The following sections further describe the signals.

For additional details on the signals, refer to the NAND flash memory and the LPSDRAM datasheets.

2.1 Flash memory inputs/outputs (I/O0-I/O7)

Input/outputs 0 to 7 are used by the NAND flash memory to input the selected address, output the data during a read operation, or input a command or data during a write operation. The inputs are latched on the rising edge of Write Enable. I/O0-I/O7 are left floating when the NAND flash memory is deselected or the outputs are disabled.

2.2 Flash memory inputs/outputs (I/O8-I/O15)

Input/outputs 8 to 15 are only available in x16 NAND flash devices. They are used to output the data during a read operation or input data during a write operation. Command and address inputs only require I/O0 to I/O7.

The inputs are latched on the rising edge of Write Enable. I/O8-I/O15 are left floating when the device is deselected or the outputs are disabled.

2.3 Flash memory Address Latch Enable (AL)

The Address Latch Enable activates the latching of the address inputs in the command interface of the NAND flash memory. When AL is High, the inputs are latched on the rising edge of Write Enable.

2.4 Flash memory Command Latch Enable (CL)

The Command Latch Enable activates the latching of the command inputs in the command Interface of the NAND flash memory. When CL is high, the inputs are latched on the rising edge of Write Enable.

2.5 Flash memory Chip Enable ($\overline{E}_F$)

The NAND flash memory Chip Enable input activates the memory control logic, input buffers, decoders, and sense amplifiers. When Chip Enable is Low, V_{IL}, the NAND flash memory device is selected. If Chip Enable goes High, v_{IH}, while the NAND flash memory is busy, the device remains selected and does not go into standby mode.

2.6 Flash memory Read Enable ($\overline{R}$)

The NAND flash memory Read Enable pin, $\overline{R}$, controls the sequential data output during read operations. The falling edge of $\overline{R}$ also increments the internal column address counter by one.

2.7 Flash memory Write Enable ($\overline{W}_F$)

The NAND flash memory Write Enable input, $\overline{W}_F$, controls writing to the command interface, input address, and data latches. Both addresses and data are latched on the rising edge of Write Enable.

2.8 Flash memory Write Protect ($\overline{WP}$)

The Write Protect pin is a NAND flash memory input that gives a hardware protection against unwanted program or erase operations. When Write Protect is Low, V_{IL}, the NAND flash memory device does not accept any program or erase operations.

It is recommended to keep the Write Protect pin Low, V_{IL}, during power-up and power-down.

2.9 Flash memory Ready/Busy ($\overline{RB}$)

The Ready/Busy output, $\overline{RB}$, is an open-drain NAND flash memory output that can be used to identify if the P/E/R controller is currently active.

When Ready/Busy is Low, V_{OL}, a read, program or erase operation is in progress. When the operation completes Ready/Busy goes High, V_{OH}.

The use of an open-drain output allows the Ready/Busy pins from several memories to be connected to a single pull-up resistor. A Low then indicates that one or more of the memories is busy.

2.10 Flash memory V_{DDF} supply voltage

V_{DDF} provides the power supply to the internal core of the NAND flash memory device. It is the main power supply for all operations (read, program and erase).

2.11 LPSDRAM Address inputs (A0-Ax)

The A0-Ax address inputs are used by the LPSDRAM to select the row or column to be made active. If A10 is High (set to ‘1’) during read or write, the read or write cycle operation includes an auto precharge cycle. If A10 is Low (set to ‘0’) during read or write, the read or write cycle does not include an auto precharge cycle.

2.12 LPSDRAM Bank Select Address inputs (BA0-BA1)

The BA0 and BA1 banks select address inputs are used by the LPSDRAM to select the bank to be made active.

When selecting the addresses the LPSDRAM must be enabled, the Row Address Strobe, $\overline{RAS}$, must be Low, V_{IL}, the Column Address Strobe, $\overline{CAS}$, and $\overline{W}$ must be High, V_{IH}.

2.13 LPSDRAM Data inputs/outputs (DQ0-DQ31)

On the LPSDRAM, DQ0-DQ31 output the data stored at the selected address during a read operation, or are used to input the data during a write operation.

DQ16-DQ31 data inputs/outputs are only available in 32-bit bus width mode.

2.14 LPSDRAM Chip Select ($\overline{E}_D$)

The Chip Select input $\overline{E}_D$ activates the LPSDRAM state machine, address buffers, and decoders when driven Low, V_{IL}. When High, V_{IH}, the device is not selected.

2.15 LPSDRAM Column Address Strobe ($\overline{CAS}$)

The Column Address Strobe, $\overline{CAS}$, is used in conjunction with Address Inputs A8-A0 and BA1-BA0, to select the starting column location prior to a read or write operation.

2.16 LPSDRAM Row Address Strobe ($\overline{RAS}$)

The Row Address Strobe, $\overline{RAS}$, is used in conjunction with Address Inputs A11-A0 and BA1-BA0 to select the starting address location prior to a read or write operation.

2.17 LPSDRAM Write Enable ($\overline{W}_D$)

The LPSDRAM Write Enable input, $\overline{W}_D$, controls writing to the LPSDRAM.

2.18 LPSDRAM Clock Input (K)

The Clock signal, K, is used to clock the read and write cycles on the LPSDRAM. During normal operation, the Clock Enable pin, KE, is High, V_{IH}. The Clock signal K can be suspended to switch the device to the self-refresh, power-down or deep power-down mode by driving KE Low, V_{IL}.

2.19 LPSDRAM Clock Input ($\overline{K}$)

The Clock signal, $\overline{K}$, is only available on the DDR LPSDRAM. It is used in conjunction with the Clock signal, K.

All LPSDRAM input signals except DQM0/DQM1/DQM2/DQM3, UDQS/LDQS and DQ0-DQ31 are referred to the cross point of $\overline{K}$ rising edge and K falling edge.

2.20 LPSDRAM Clock Enable (KE)

The Clock Enable, KE, pin is used by the LPSDRAM to control the synchronizing of the signals with Clock signal K. If KE is High, V_{IH}, the next Clock rising edge is valid. When KE is Low, V_{IL}, the signals are no longer clocked and data read and write cycles are extended. KE is also involved in switching the device to the self-refresh, power-down and deep power-down modes.

2.21 LPSDRAM lower/upper data input/output mask (DQM0 to DQM3)

Data Mask Enable inputs, DQM0, DQM1, DQM2, and DQM3 are used to mask the read or write data. DQM2 and DQM3 are only available in 32-bit bus width mode.

2.22 DQS0 to DQS3 input/outputs

DQS0 to DQS3 can be either input or output signals and act as Write Data Strobe and Read Data Strobe, respectively. Each DQS signal corresponds to eight DQ pins.

2.23 Lower/Upper Data Read/Write Strobe input/output (LDQS, UDQS)

LDQS and UDQS can be either input or output signals, and act as Write Data Strobe and Read Data Strobe respectively. LDQS and UDQS are the strobe signals for DQ0 to DQ7 and DQ8 to DQ15, respectively.

2.24 LPSDRAM V_{DDD} supply voltage

V_{DDD} provides the power supply to the internal core of the LPSDRAM. It is the main power supply for all operations (read and write).

2.25 LPSDRAM V_{DDQD} supply voltage

V_{DDQD} provides the power supply to the I/O pins of the LPSDRAM and enables all outputs to be powered independently of V_{DDD}. V_{DDQD} can be tied to V_{DDD} or can use a separate supply.

It is recommended to power-up and power-down V_{DDD} and V_{DDQD} together to avoid certain conditions that would result in data corruption.

2.26 Ground

2.26.1 NANDxxxxNx devices delivered in TFBGA107/137/149 packages

The NAND flash memory and LPSDRAM components have separate grounds, as described below.

NAND flash V_{SSF} ground

V_{SSF} is the reference for the NAND flash power supply. It must be connected to the system ground.

LPSDRAM V_{SSD} ground

V_{SSD} is the reference for the NAND flash power supply. It must be connected to the system ground.

LPSDRAM V_{SSQD} ground

V_{SSQD} ground is the reference for the LPSDRAM input/output circuitry driven by V_{DDQD}. V_{SSQD} must be connected to V_{SSD}.

2.26.2 NANDxxxxNx delivered in TFBGA128/152 and VFBGA160 packages

The NAND flash memory and LPSDRAM components share the same ground V_{SS}, as described below.

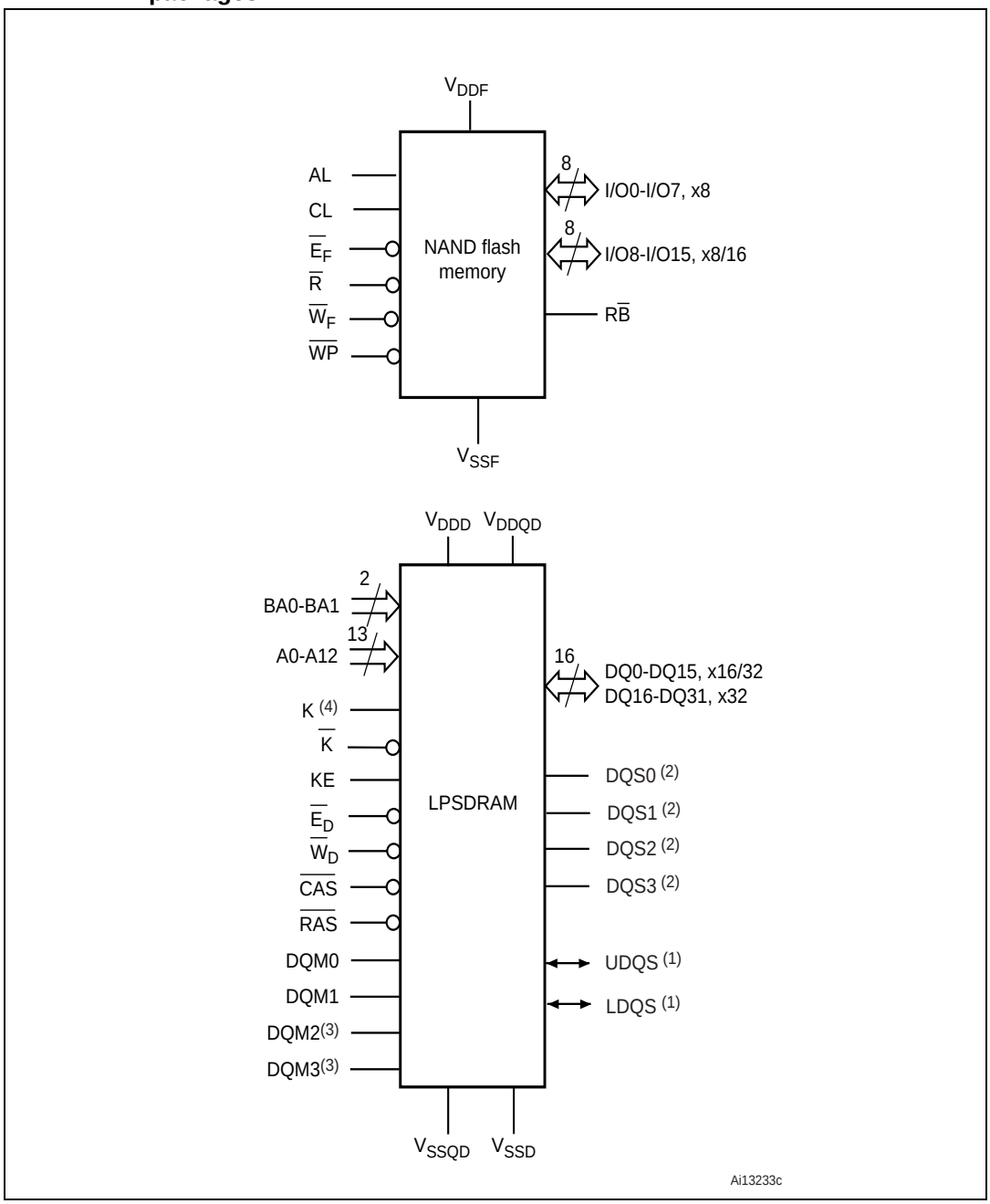
V_{SS} ground

V_{SS} ground is the reference for the power supply for the NAND flash and LPSDRAM components. It must be connected to the system ground.

3 Functional description

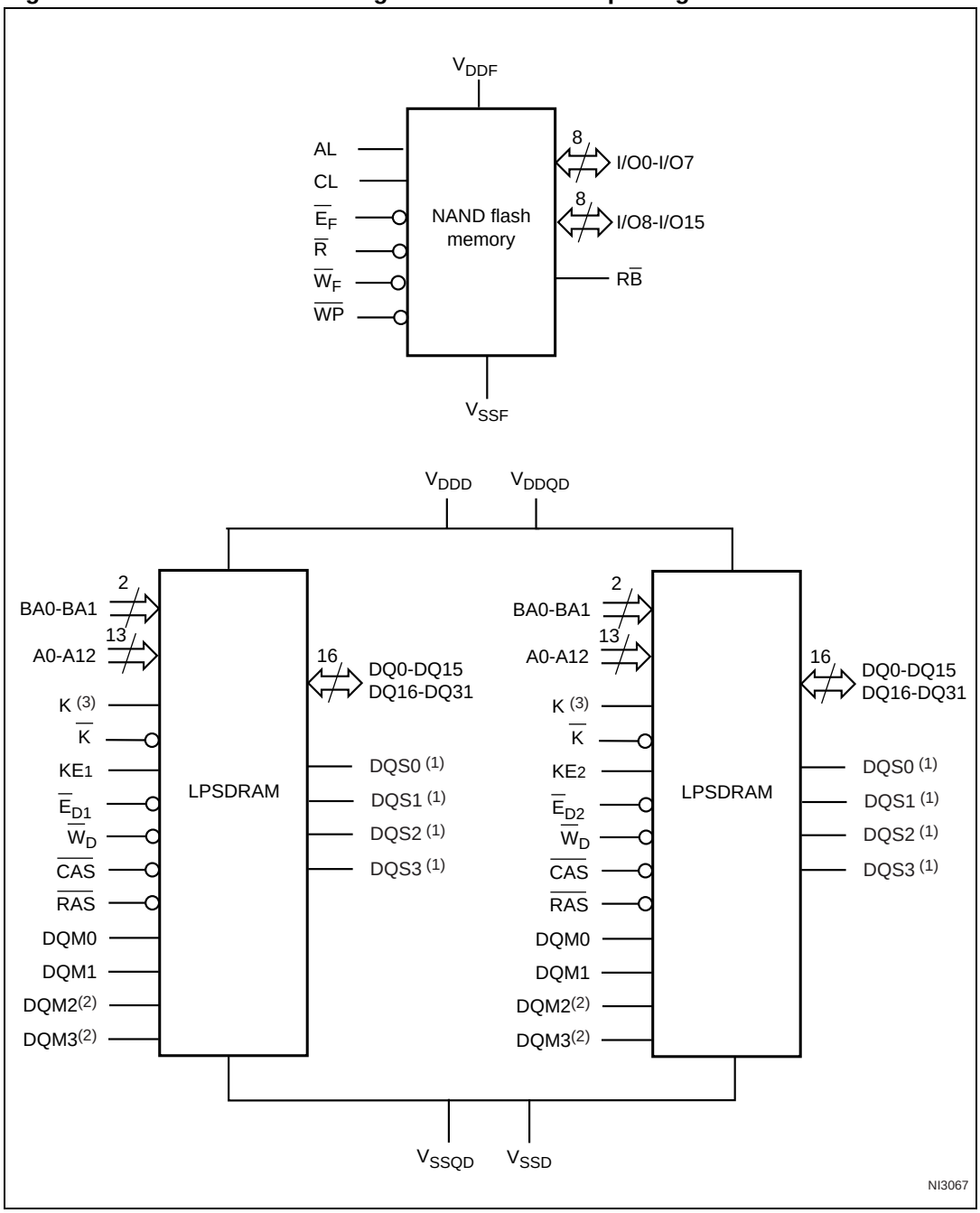
The NAND flash memory and LPSDRAM components have separate power supplies and, according to in which package they are delivered, they either share the same grounds or have separate grounds. They also have separate control signals, addresses, and data input/outputs, which allows simultaneous access to both devices at any time. *Figure 14*, *Figure 15*, *Figure 16*, *Figure 17* and *Figure 18* show the functional block diagrams.

Figure 14. Functional block diagram for TFBGA107, TFBGA137, TFBGA149 packages



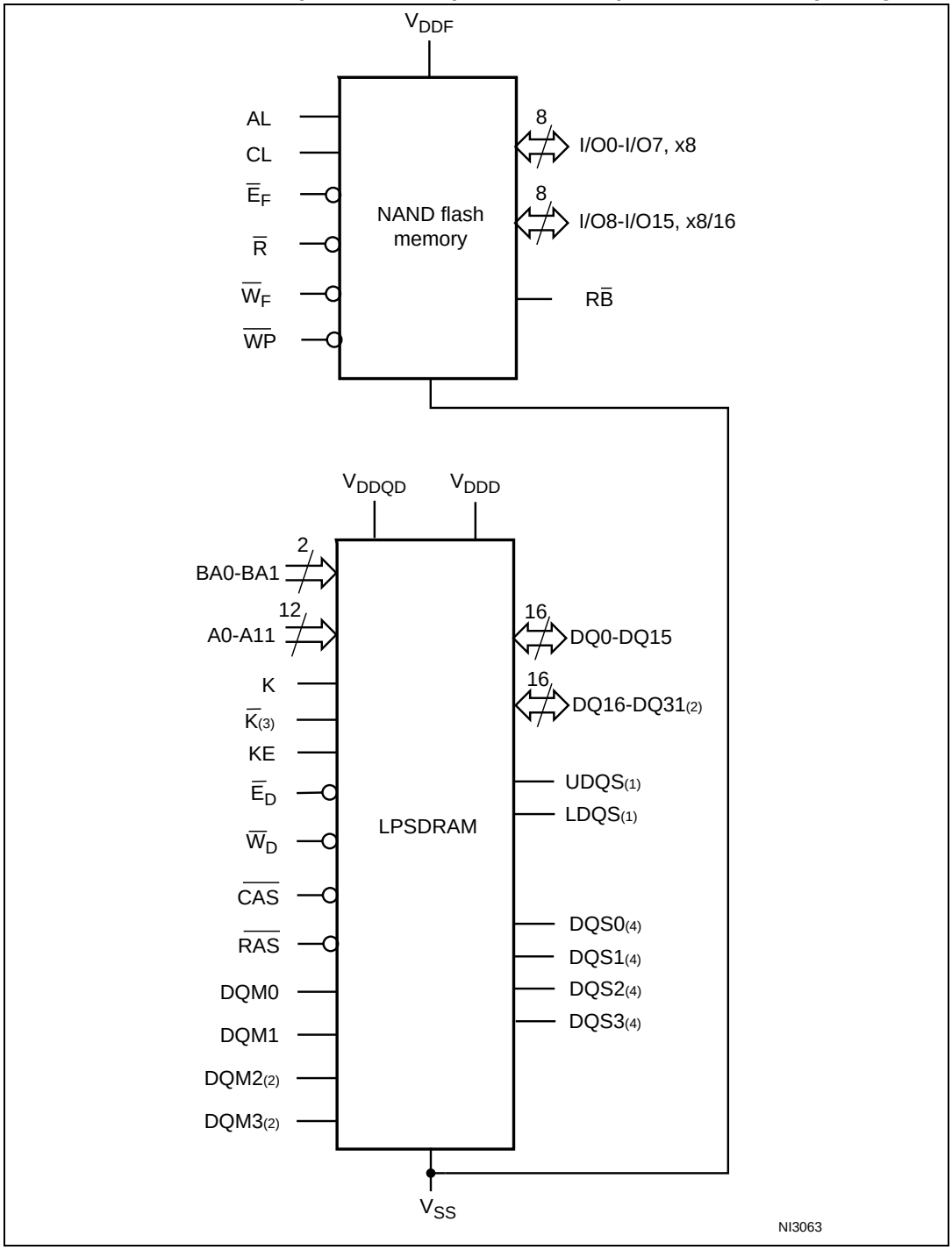
1. Only available in MCP with DDR x16.
2. Only available in MCP with DDR x32.
3. Only available in MCP with SDR/DDR x32.
4. Only available in MCP with DDR LPSDRAM.

Figure 15. Functional block diagram for LFBGA137 package



1. Only available in MCP with DDR x32.
2. Only available in MCP with SDR/DDR x32.
3. Only available in MCP with DDR LPSDRAM.

Figure 16. Functional block diagram for TFBGA128 (NANDA9R3N0, NANDB9R3N0), TFBGA152 (NANDA8R3N0, NANDA9R3N0, NANDBAR3N1, NANDB9R3N0), VFBGA152 (NANDBAR4N5), and VFBGA160 packages



1. Only available in PoP with DDR x16.
2. Only available in PoP with DDR/SDR x32.
3. Only available in PoP with DDR LPSDRAM.
4. Only available in MCP with DDR x32.

Figure 17. Functional block diagram for TFBGA152 (NANDBAR3N0, NANDB0R3N0, NANDB1R3N0, NANDA0R3N0) package

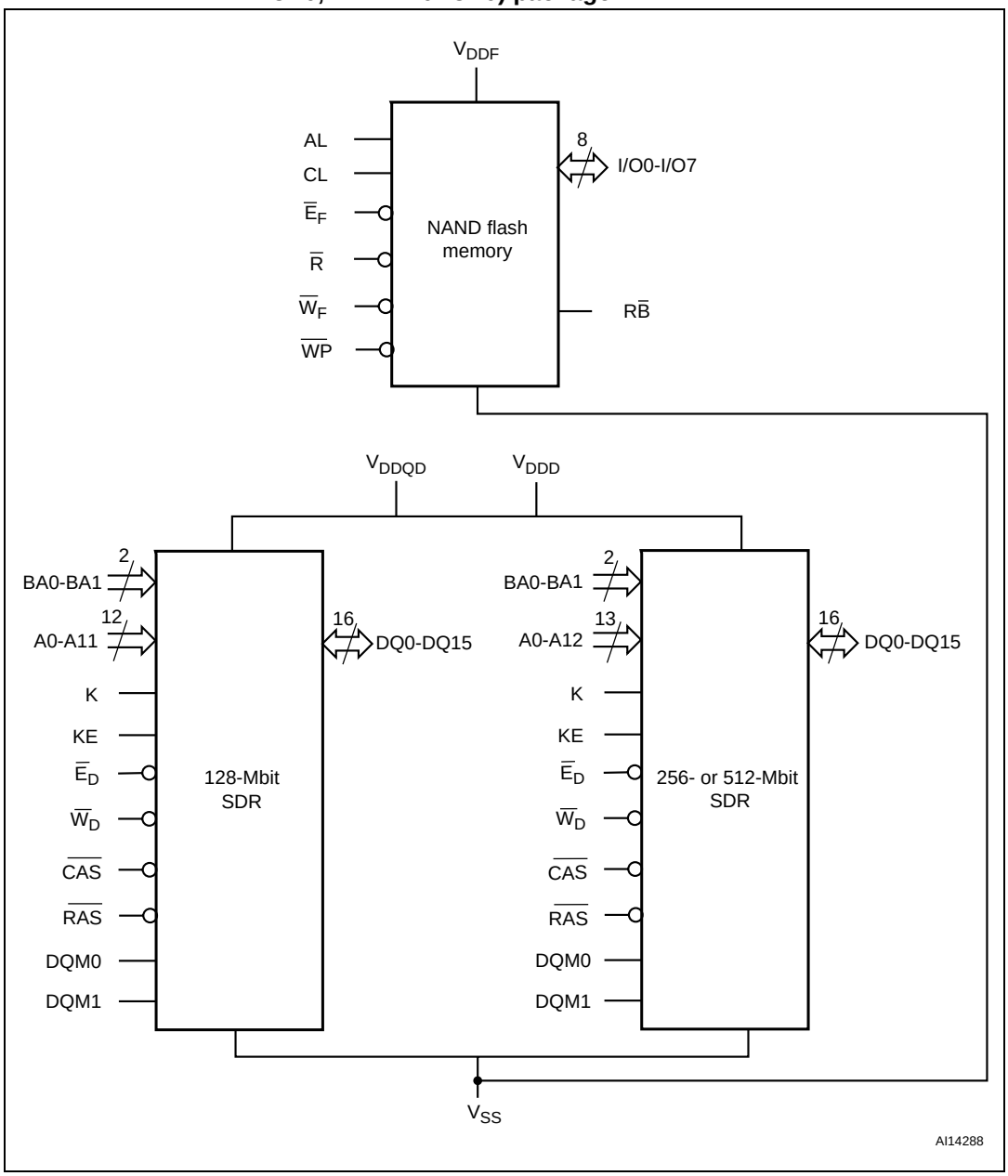
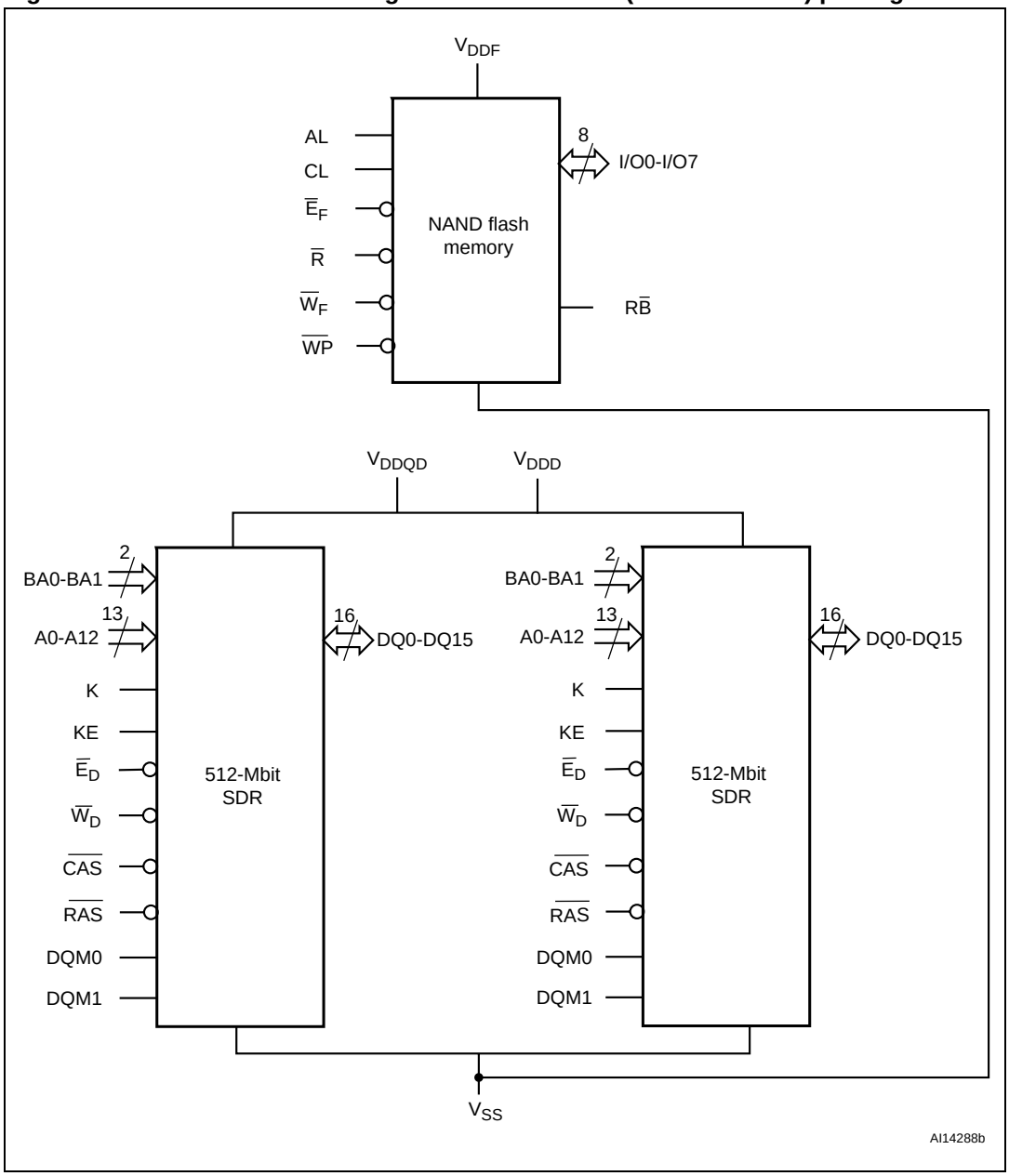


Figure 18. Functional block diagram for TFBGA128 (NANDBAR3N6) package



4 Maximum ratings

Stressing the device above the rating listed in *Table 4: Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Absolute maximum ratings(1)

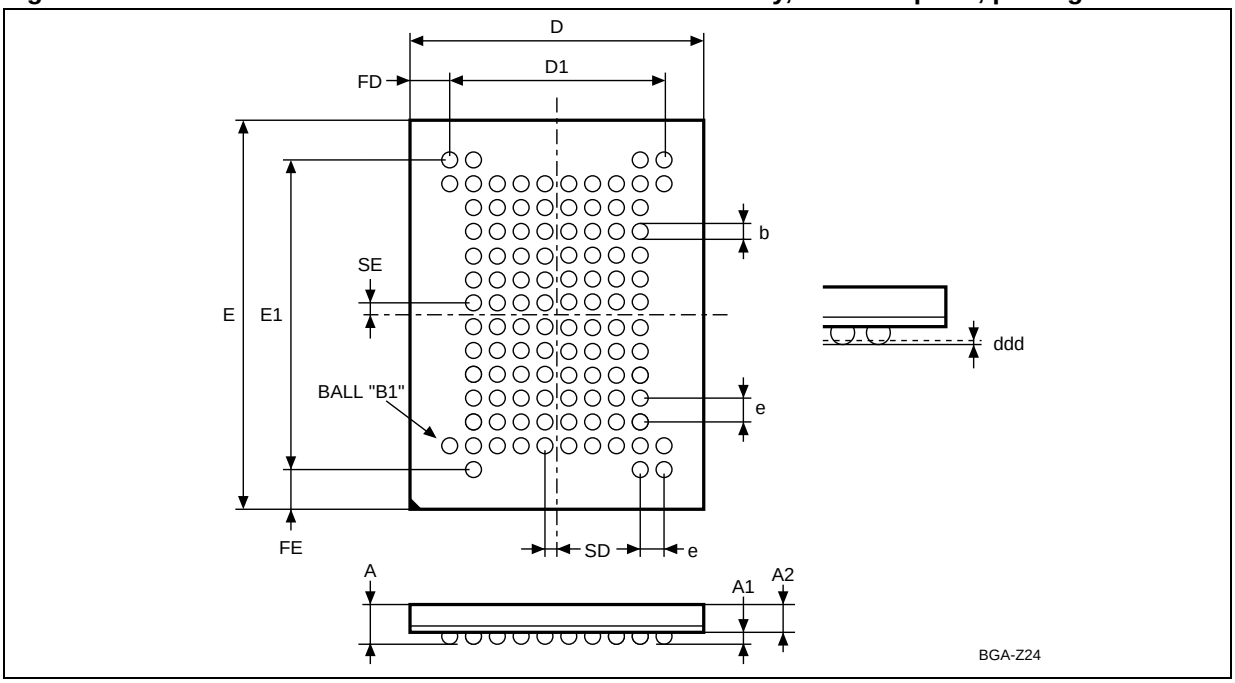
Symbol	Parameter		Value		Unit
			Min	Max	
T_A	Ambient operating temperature		–30	85	°C
T_{STG}	Storage temperature		–55	125	°C
V_{IO}	NAND flash input or output voltage	1.8 V	–0.6	2.7	V
		2.6 V	–0.6	4.6	V
V_{DDDQ},	LPSDRAM input or output voltage	1.8 V	–0.5	2.3	V
V_{DDF}	NAND flash supply voltage	1.8 V	–0.6	2.7	V
		2.6 V	–0.6	4.6	V
V_{DDD}	LPSDRAM supply voltage	1.8 V	–0.5	2.3	V
I_{OS}	LPSDRAM short circuit output current		50		mA

1. For detailed information on the LPSDRAM parameters, refer to the M65KA512AB, M65KA512AC, M65KG512AB, M65KA256AG, M65KC512AB, M65KC512AC, M65KD512AC, M65KAxxxAJ, M65KA512AH, M65KG512AH, M65KG512AC, M65KGxxxAJ, M65KAxxxAM, M65KCxxxAJ, M65KDxxxAJ, and M65KGxxxAM datasheets available from your local Numonyx sales office.

5 Package mechanical

To meet environmental requirements, Numonyx offers these devices in ECOPACK® packages. ECOPACK® packages are lead-free. The category of second-level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

Figure 19. TFBGA107 10.5 × 13 mm - 10 × 14 active ball array, 0.80 mm pitch, package outline

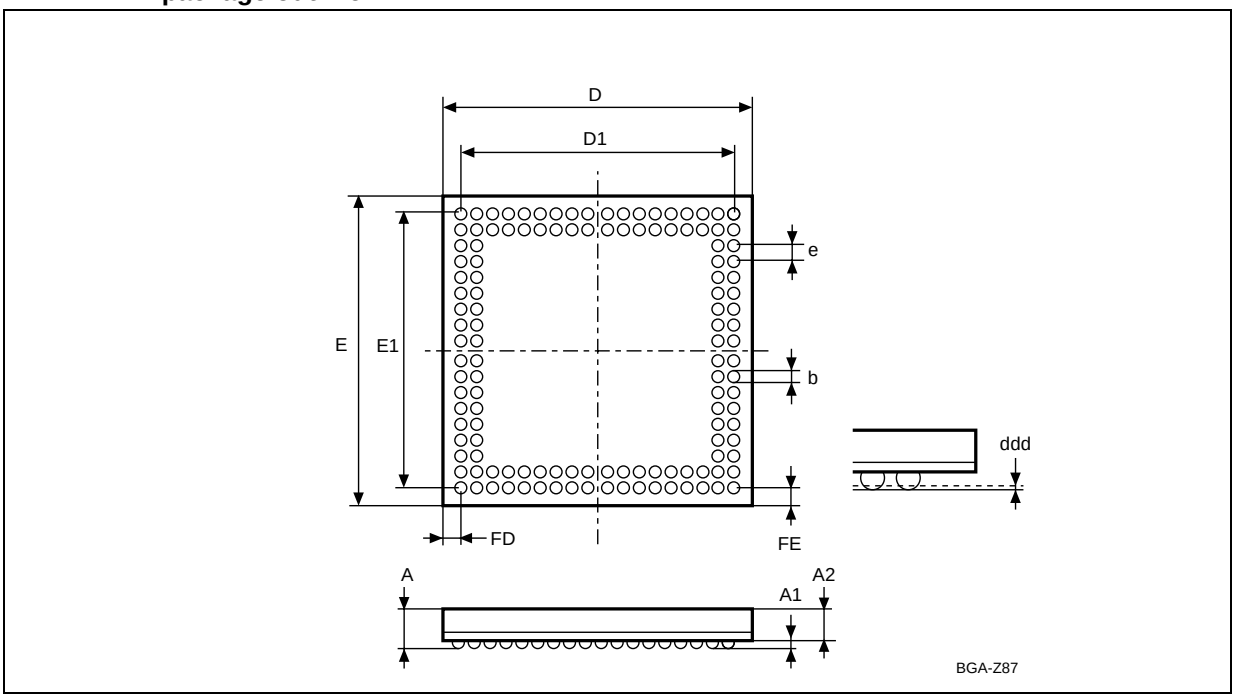


1. Drawing is not to scale.

Table 5. TFBGA107 10.5 × 13 mm - 10 × 14 active ball array, 0.80 mm pitch, mechanical data

Symbol	Millimeters			Inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.25			0.010	
A2	0.80			0.031		
b	0.45	0.40	0.50	0.018	0.016	0.020
D	10.50	10.40	10.60	0.413	0.409	0.417
D1	7.20			0.283		
ddd			0.10			0.004
E	13.00	12.90	13.10	0.512	0.508	0.516
E1	10.40			0.409		
e	0.80	–	–	0.031	–	–
FD	1.65			0.065		
FE	1.30			0.051		
SD	0.40			0.016		
SE	0.40			0.016		

Figure 20. TFBGA128 - 2-row perimeter matrix 2R18 × 18, 12 × 12 mm, 0.65 mm pitch, package outline

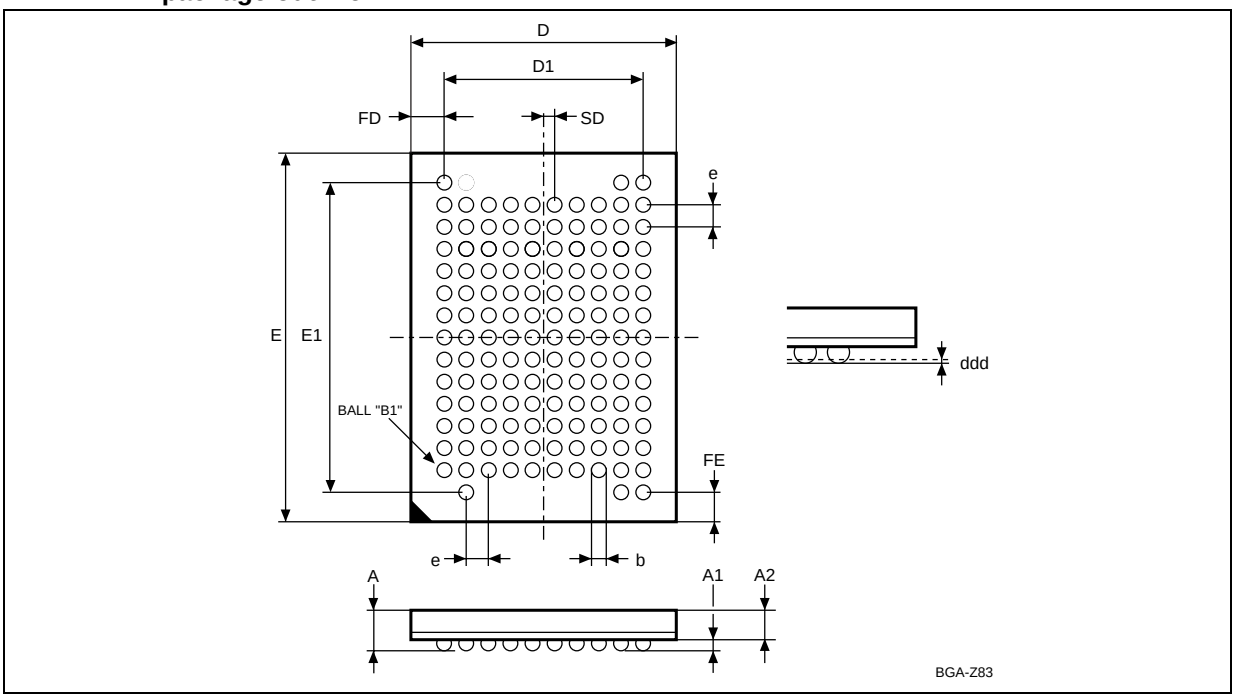


1. Drawing is not to scale.

Table 6. TFBGA128 - 2-row perimeter matrix 2R18 × 18, 12 × 12 mm, 0.65 mm pitch, mechanical data

Symbol	Millimeters			Inches		
	Typ	Min	Max	Typ	Min	Max
A			1.10			0.043
A1		0.32			0.013	
A2	0.63			0.025		
b	0.42	0.37	0.47	0.016	0.015	0.018
D	12.00	11.90	12.10	0.472	0.468	0.476
D1	11.05			0.435		
ddd			0.10			0.004
E	12.00	11.90	12.10	0.472	0.468	0.476
E1	11.05			0.435		
e	0.65			0.026		
FD	0.47			0.019		
FE	0.47			0.019		

Figure 21. TFBGA137 10.5 x 13 x 1.2 mm - 10 x 15-13 active ball array, 0.80 mm pitch, package outline

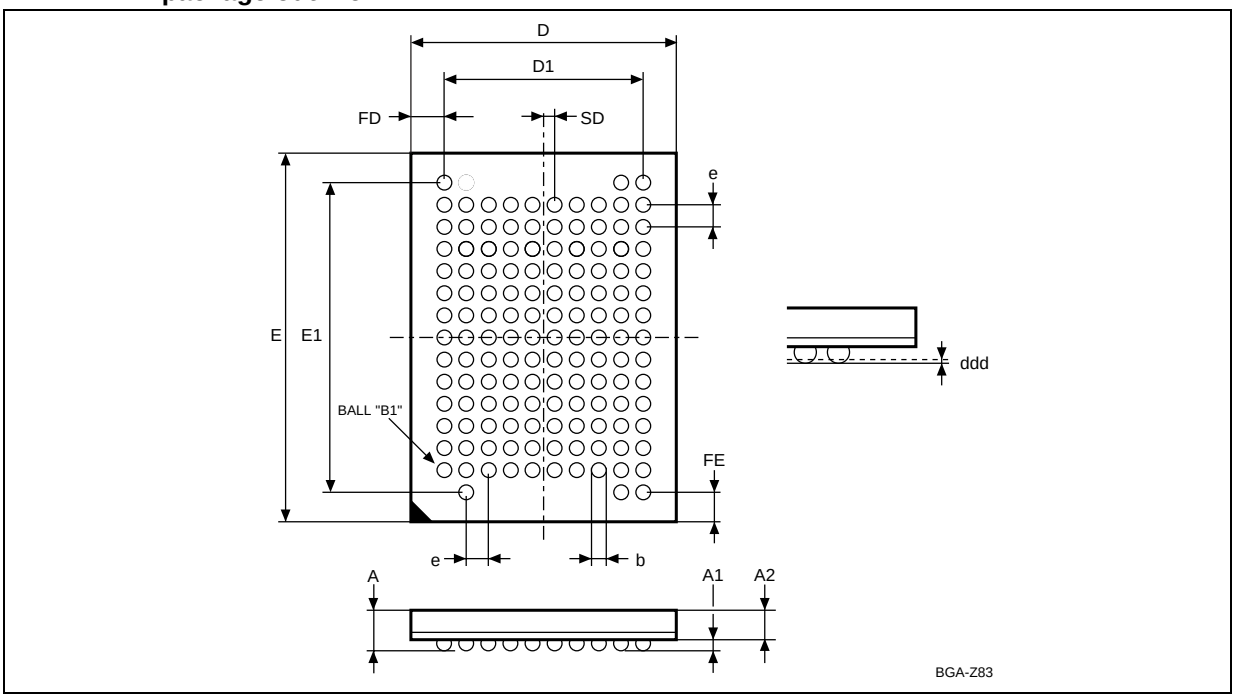


1. Drawing is not to scale.

Table 7. TFBGA137 10.5 x 13 mm - 10 x 15-13 active ball array, 0.80 mm pitch, mechanical data

Symbol	Millimeters			Inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.25			0.010	
A2	0.80			0.031		
b	0.45	0.40	0.50	0.018	0.016	0.020
D	10.50	10.40	10.60	0.413	0.409	0.417
D1	7.20			0.283		
E	13.00	12.90	13.10	0.512	0.508	0.516
E1	11.20			0.441		
e	0.80	–	–	0.031	–	–
FD	1.65			0.065		
FE	0.90			0.035		
SD	0.40	–	–	0.016	–	–

Figure 22. LFBGA137 10.5 x 13 x 1.4 mm - 10 x 15-13 active ball array, 0.80 mm pitch, package outline

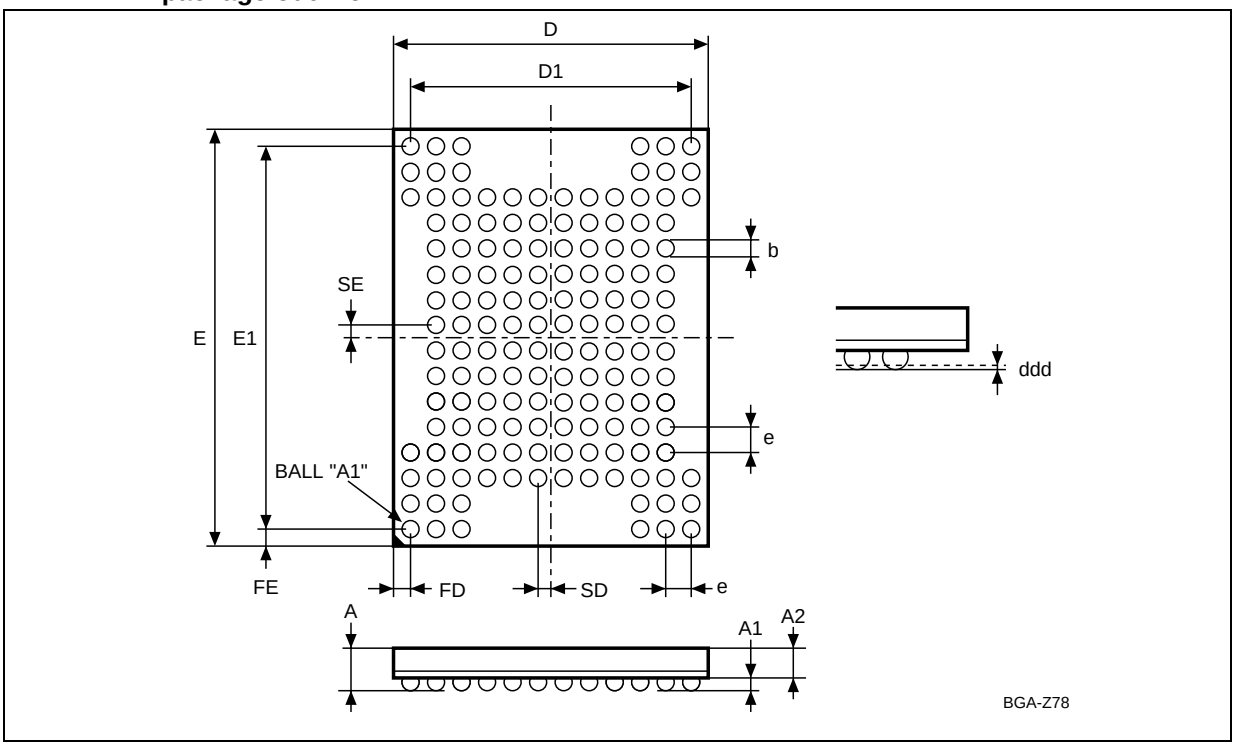


1. Drawing is not to scale.

Table 8. LFBGA137 10.5 x 13 x 1.4 mm - 10 x 15-13 active ball array, 0.80 mm pitch, mechanical data

Symbol	Millimeters			Inches		
	Typ	Min	Max	Typ	Min	Max
A			1.40			0.055
A1		0.25			0.010	
A2	1.00			0.039		
b	0.45	0.40	0.50	0.018	0.016	0.020
D	10.50	10.40	10.60	0.413	0.409	0.417
D1	7.20			0.283		
ddd			0.10			0.004
E	13.00	12.90	13.10	0.512	0.508	0.516
E1	11.20			0.441		
e	0.80	–	–	0.031	–	–
FD	1.65			0.065		
FE	0.90			0.035		
SD	0.40	–	–	0.016	–	–

Figure 23. TFBGA149 10 × 13.5 mm - 12 × 16 active ball array, 0.80 mm pitch, package outline

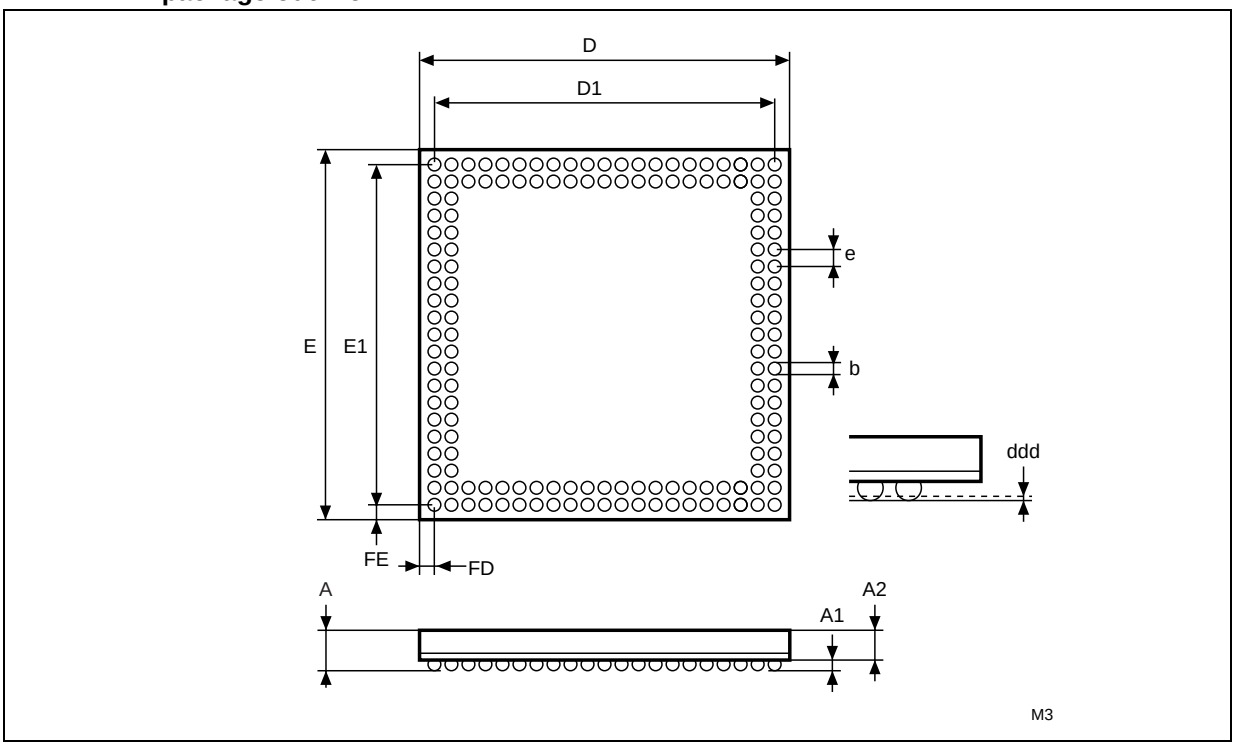


1. Drawing not to scale.

Table 9. TFBGA149 10 × 13.5 mm - 12 × 16 active ball array, 0.80 mm pitch, mechanical data

Symbol	Millimeters			Inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.25			0.010	
A2	0.80			0.031		
b	0.45	0.40	0.50	0.018	0.016	0.020
D	10.00	9.90	10.10	0.394	0.390	0.398
D1	8.80			0.346		
ddd			0.10			0.004
E	13.50	13.40	13.60	0.531	0.528	0.535
E1	12.00			0.472		
e	0.80	–	–	0.031	–	–
FD	0.60			0.024		
FE	0.75			0.029		
SD	0.40	–	–	0.016	–	–
SE	0.40	–	–	0.016	–	–

Figure 24. TFBGA152, 2-row perimeter matrix 2R21 x 21, 14 x 14 x 1.1 mm, 0.65 mm pitch, package outline

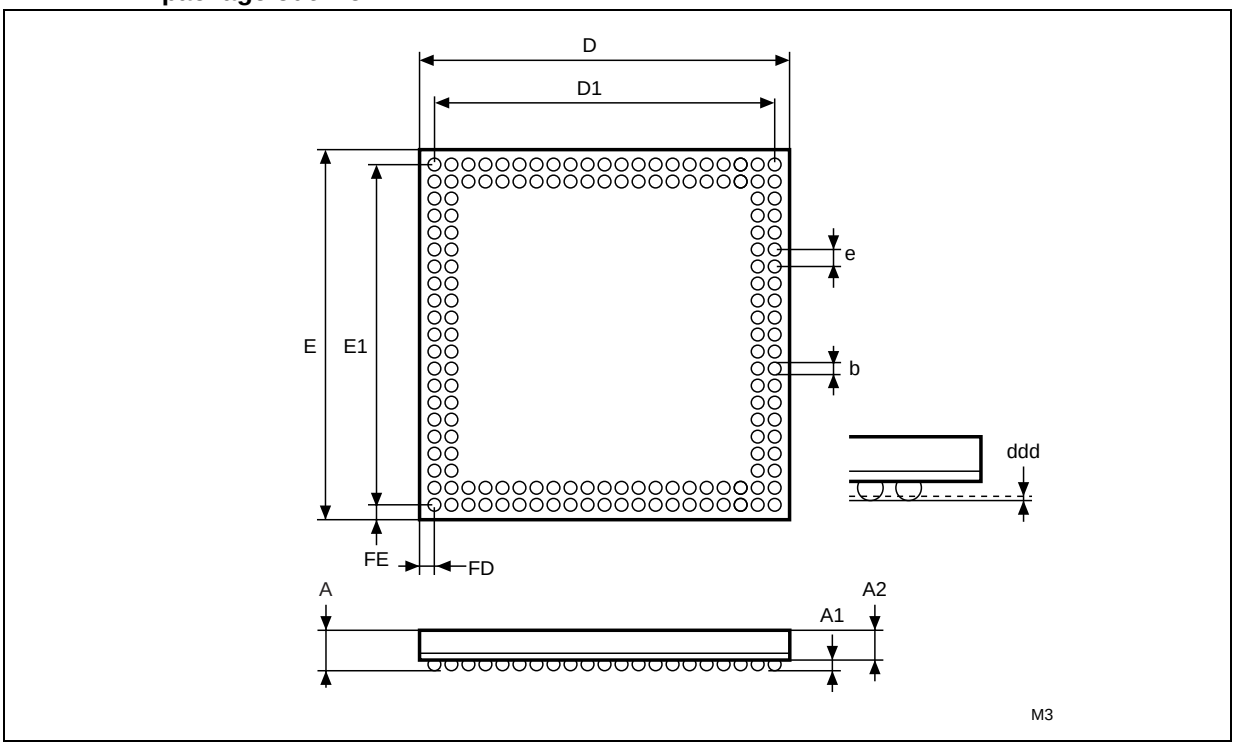


1. Drawing is not to scale.

Table 10. TFBGA152, 2-row perimeter matrix 2R21 x 21, 14 x 14 x 1.1 mm, 0.65 mm pitch, mechanical data

Symbol	Millimeters			Inches		
	Typ	Min	Max	Typ	Min	Max
A			1.10			0.043
A1		0.32			0.013	
A2	0.63			0.025		
b	0.42	0.37	0.47	0.016	0.015	0.018
ddd			0.10			0.004
D	14.00	13.90	14.10	0.551	0.547	0.555
D1	13.00			0.512		
E	14.00	13.90	14.10	0.551	0.547	0.555
E1	13.00			0.512		
e	0.65	–	–	0.026	–	–
FD	0.50			0.020		
FE	0.50			0.020		

Figure 25. VFBGA152, 2-row perimeter matrix 2R21 x 21, 14 x 14 x 0.9 mm, 0.65 mm pitch, package outline

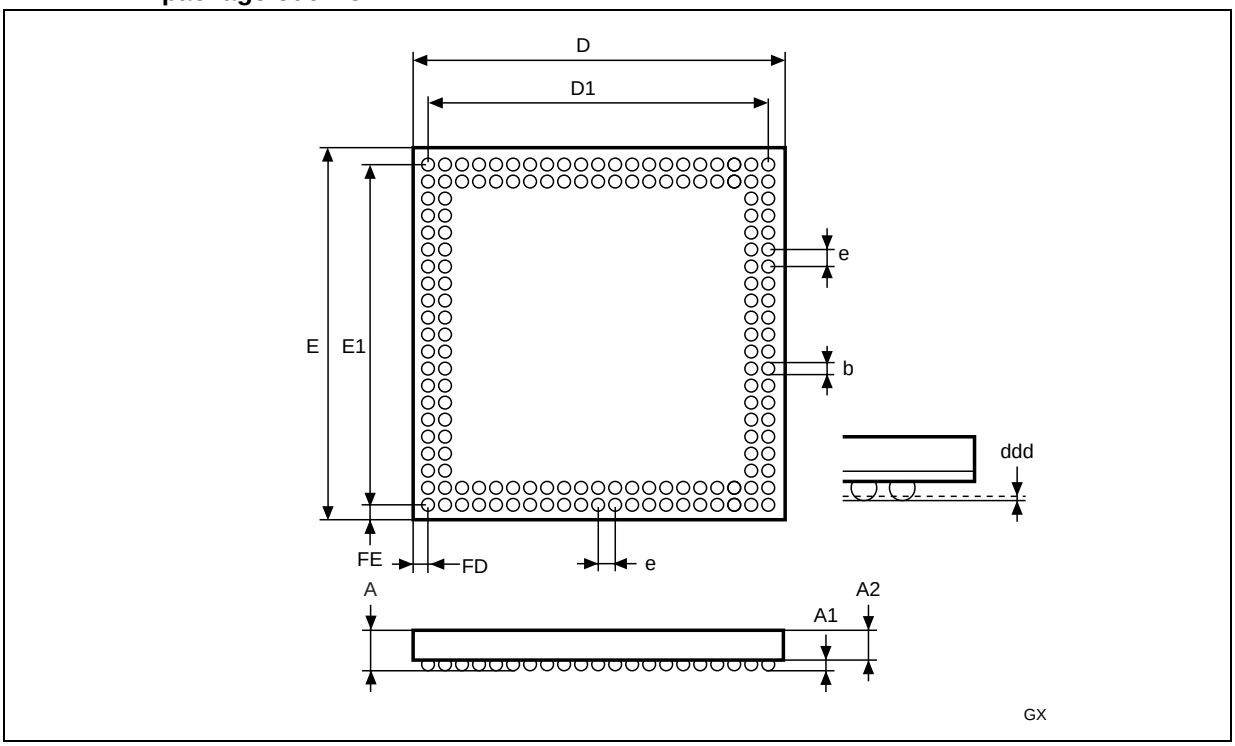


1. Drawing is not to scale.

Table 11. TFBGA152, 2-row perimeter matrix 2R21 x 21, 14 x 14 x 0.9 mm, 0.65 mm pitch, mechanical data

Symbol	Millimeters			Inches		
	Typ	Min	Max	Typ	Min	Max
A			0.90			0.035
A1		0.35			0.014	
A2	0.45			0.018		
b	0.45	0.40	0.50	0.018	0.016	0.020
ddd			0.10			0.004
D	14.00	13.90	14.10	0.551	0.547	0.555
D1	13.00			0.512		
E	14.00	13.90	14.10	0.551	0.547	0.555
E1	13.00			0.512		
e	0.65	–	–	0.026	–	–
FD	0.50			0.020		
FE	0.50			0.020		

Figure 26. TFBGA152, 2-row perimeter matrix 2R21 x 21, 14 × 14 x 1.2 mm, 0.65 mm pitch, package outline

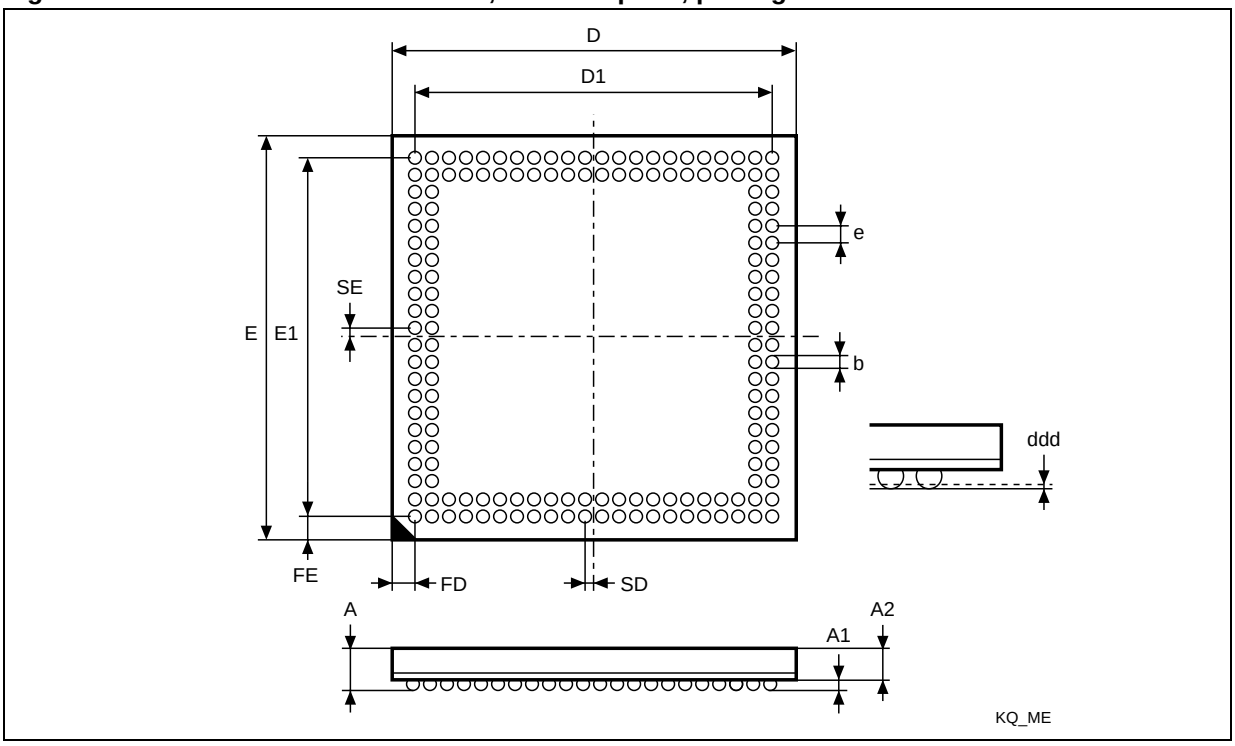


1. Drawing is not to scale.

Table 12. TFBGA152, 2-row perimeter matrix 2R21 x 21, 14 × 14 x 1.2 mm, 0.65 mm pitch, mechanical data

Symbol	Millimeters			Inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.32			0.013	
A2	0.78				0.031	
b	0.42	0.37	0.47	0.016	0.015	0.018
D	14.00	13.90	14.10	0.551	0.547	0.555
D1	13.00			0.512		
E	14.00	13.90	14.10	0.551	0.547	0.555
E1	13.00			0.512		
e	0.65			0.026		
FD	0.50			0.020		
FE	0.50			0.020		
ddd	0.10			0.004		

Figure 27. VFBGA160 15 × 15 x 1 mm, 0.65 mm pitch, package outline



1. Drawing not to scale.

Table 13. VFBGA160 15 × 15 x 1 mm, 0.65 mm pitch, mechanical data

Symbol	Millimeters			Inches		
	Typ	Min	Max	Typ	Min	Max
A			1.00			0.039
A1		0.38			0.015	
A2	0.51			0.020		
b	0.48	0.43	0.53	0.019	0.017	0.021
D	15.00	14.90	15.10	0.591	0.587	0.594
D1	13.65			0.537		
ddd			0.10			0.004
E	15.00	14.90	15.10	0.591	0.587	0.594
E1	13.65			0.537		
e	0.65	–	–	0.026	–	–
FD	0.67			0.027		
FE	0.67			0.027		
SD	0.32	–	–	0.013	–	–
SE	0.32	–	–	0.013	–	–

6 Ordering information

Table 14. Ordering information scheme

Example: NANDA 9 R 3 N 0 A ZPA 5 E

Device type

NAND flash memory

NAND flash density

A = 1 Gbit
B = 2 Gbits
C = 4 Gbits

DRAM density

9 = 512 Mbits
8 = 256 Mbits
A = 1 Gbit
B = 2 Gbits
0 = 128 Mbits + 512 Mbits
1 = 128 Mbits + 256 Mbits

NAND flash operating voltage

R = 1.7 V to 1.95 V
W = 2.5 V to 3.6 V

NAND bus width

3 = x8
4 = x16

Family identifier

N = 2112-byte page NAND flash

DRAM options

0 = SDR, x16, 133 MHz
1 = SDR, x32, 133 MHz
2 = DDR, x16, 133 MHz
3 = DDR, x32, 133 MHz
4 = DDR, x16, 166 MHz
5 = DDR, x32, 166 MHz
6 = SDR, x16, 166 MHz
7 = SDR, x32, 166 MHz

Product version

A or B or C or D

Package

ZBB = TFBGA107 10.5 × 13 mm x 1.2 mm
ZPC = TFBGA128 12 x 12 x 1.1 mm
ZBC = TFBGA137 10.5 x 13 mm x 1.2 mm
ZCC = LFBGA137 10.5 x 13 mm x 1.4 mm
ZBA = TFBGA149, 10 × 13.5 x 1.2 mm
ZPA = TFBGA152, 14 × 14 x 1.1 mm
ZQA = TFBGA152 14 x 14 x 1.2 mm
ZPB = VFBGA160 15 x 15 x 1 mm
ZOB = VFBGA152 14 x 14 x 0.9 mm

Temperature

5 = –30 °C to 85 °C

Option

E = ECOPACK® package, standard packing
F = ECOPACK® package, tape and reel packing

Note: Devices are shipped from the factory with the flash memory content bits, in valid blocks, erased to '1'. For further information on any aspect of this device, please contact your nearest Numonyx sales office.

7 Revision history

Table 15. Document revision history

Date	Version	Changes
04-Jul-2006	1	Initial release.
18-Sep-2006	2	NANDC9R4N0, NANDA8R3N0 and NANDA9R4N2 added. Updated signal names in *Figure 1: Block diagram for TFBGA107, TFBGA137, and TFBGA149 packages*, *Table 3: Signal names*, *Figure 9: TFBGA149 connections (top view through package)* and *Figure 14: Functional block diagram for TFBGA107, TFBGA137, TFBGA149 packages*
02-Nov-2006	3	NANDA9R4N2, NANDA9W3N1, NANDA9R3N1 root part number added. TFBGA137 10.5 x 13 mm and TFBGA160 15 x 15 mm added. *Section 1: Description*, *Section 2: Signal descriptions*, and *Section 3: Functional description* updated accordingly. *Table 4: Absolute maximum ratings* updated to add 3V NAND Flash memory. *Table 7: TFBGA137 10.5 x 13 mm - 10 x 15-13 active ball array, 0.80 mm pitch, mechanical data*, *Figure 7: TFBGA137 connections (top view through package)*, and *Figure 13: VFBGA160 connections - NANDBAR4N2 (top view through package)* added. *Table 14: Ordering information scheme* updated.
06-Mar-2007	4	NANDBAR3N1 root part number added. NANDB9R4N2 removed. TFBGA152 (14 × 14 × 1.2 mm) and TFBGA128 (12 x 12 x 1.1 mm) added. *Section 1: Description*, *Section 2: Signal descriptions*, and *Section 3: Functional description* updated accordingly. TBIAS removed from *Table 4: Absolute maximum ratings*.
24-July-2007	5	Added root part numbers NANDA9W4N1, NANDA9R4N1, NANDB9R4N5, and NANDA9R3N2, and references to their respective datasheets. This updated the reference that represents the family as NANDxxxxNx throughout the document. Updated *Table 2: Product list* with new root part number information. Modified *Figure 7: TFBGA137 connections (top view through package)*. Changed the LPSDRAM Input or Output voltage and supply voltage symbols in *Table 4: Absolute maximum ratings*, and updated the information in *Chapter 6: Ordering information*. Changed NAND Flash voltage range from 1.8/3 V to 1.8/2.6 V throughout the document. Modified *Figure 5: TFBGA107 connections (top view through package)* to add three signals. Updated *Figure 14* to add 4-Gbit option and notes. Also added notes to *Figure 16*.
16-Apr-2008	6	Applied Numonyx branding.
04-Jun-2008	7	Added root part numbers NANDB0R3N0 and NANDB1R3N0 throughout the document. Minor text changes.
04-Jul-2008	8	Added root part numbers NANDBAR4N0, NANDBAR4N1 and NANDBAR4N2 throughout the document.

Table 15. Document revision history (continued)

Date	Version	Changes
06-Aug-2008	9	Modified datasheet's title. Added root part numbers NANDBAR4N5, NANDA0R3N0, NANDA9R3N6, and NANDBAR4N7 throughout the document. Removed TFBGA160 15 x 15 x 1.2 mm and added VFBGA160 15 x 15 x 1 mm packages.
14-Aug-2008	10	Added NANDA9R3N3, NANDA9R4N3, NANDA9R4N4, NANDA9R4N6, and NANDBAR3N6 root part numbers throughout the document.
23-Sep-2008	11	Modifed the datasheet's name in NANDxxxxNx. Added NANDBAW4N1, NANDCAW4N1, NANDCBR4N3, and NANDB9R4N2 root part numbers throughout the document.
01-Oct_2008	12	Added NANDD3R4N5, NANDDBR3N5, NANDC3R4N5

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