

# PH5525L

## N-channel TrenchMOS logic level FET

Rev. 02 — 5 December 2006

Product data sheet

### 1. Product profile

#### 1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology.

#### 1.2 Features

- Logic level threshold
- Optimized for use in DC-to-DC converters
- 100 % R<sub>G</sub> tested
- Lead-free package
- Very low switching and conduction losses

#### 1.3 Applications

- DC-to-DC converters
- Voltage regulators
- Switched-mode power supplies
- PC Motherboards

#### 1.4 Quick reference data

- V<sub>DS</sub> ≤ 25 V
- R<sub>DSon</sub> ≤ 5.5 mΩ
- I<sub>D</sub> ≤ 81.7 A
- Q<sub>GD</sub> = 3.3 nC (typ)

### 2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Symbol
1, 2, 3	source (S)	<p>SOT669 (LFAK)</p>	<p>mbb076</p>
4	gate (G)		
mb	mounting base; connected to drain (D)		

### 3. Ordering information

**Table 2. Ordering information**

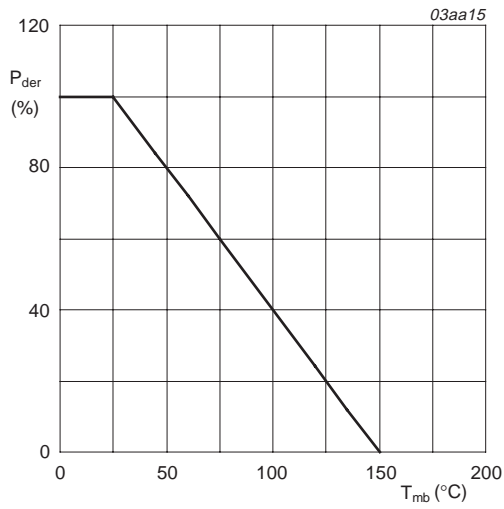
Type number	Package		Version
	Name	Description	
PH5525L	LFPK	plastic single-ended surface-mounted package; 4 leads	SOT669

### 4. Limiting values

**Table 3. Limiting values**

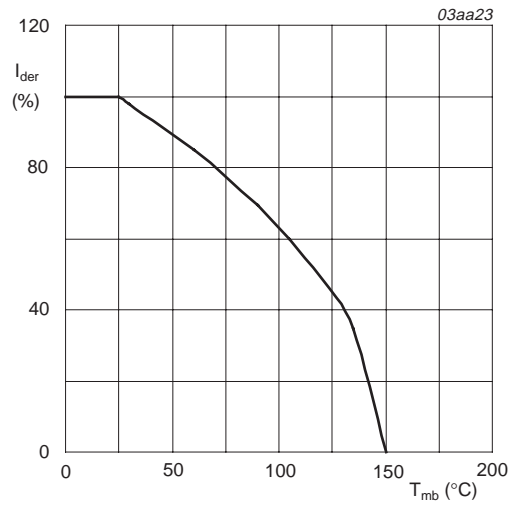
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	25	V
$V_{DGR}$	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	25	V
$V_{GS}$	gate-source voltage		-	$\pm 20$	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 2</a> and <a href="#">3</a>	-	81.7	A
		$T_{mb} = 100\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 2</a>	-	51.7	A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; see <a href="#">Figure 3</a>	-	300	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 1</a>	-	62.5	W
$T_{stg}$	storage temperature		-55	+150	°C
$T_j$	junction temperature		-55	+150	°C
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25\text{ °C}$	-	52	A
$I_{SM}$	peak source current	$T_{mb} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	208	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 45\text{ A}$ ; $t_p = 0.1\text{ ms}$ ; $V_{DS} \leq 25\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; $V_{GS} = 10\text{ V}$ ; starting at $T_j = 25\text{ °C}$	-	100	mJ



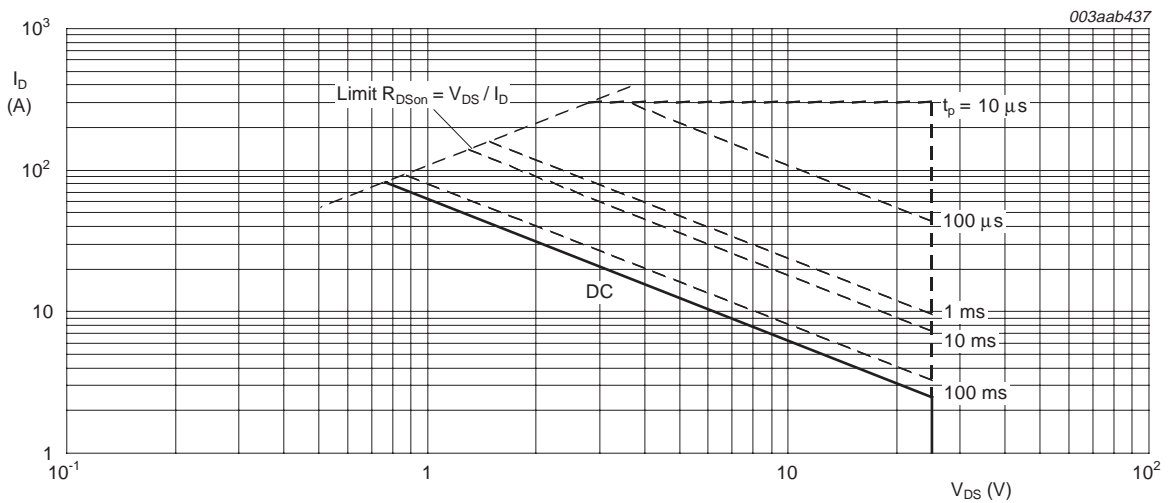
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100 \%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature



T<sub>mb</sub> = 25 °C; I<sub>DM</sub> is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

### 5. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 4</a>	-	-	2	K/W

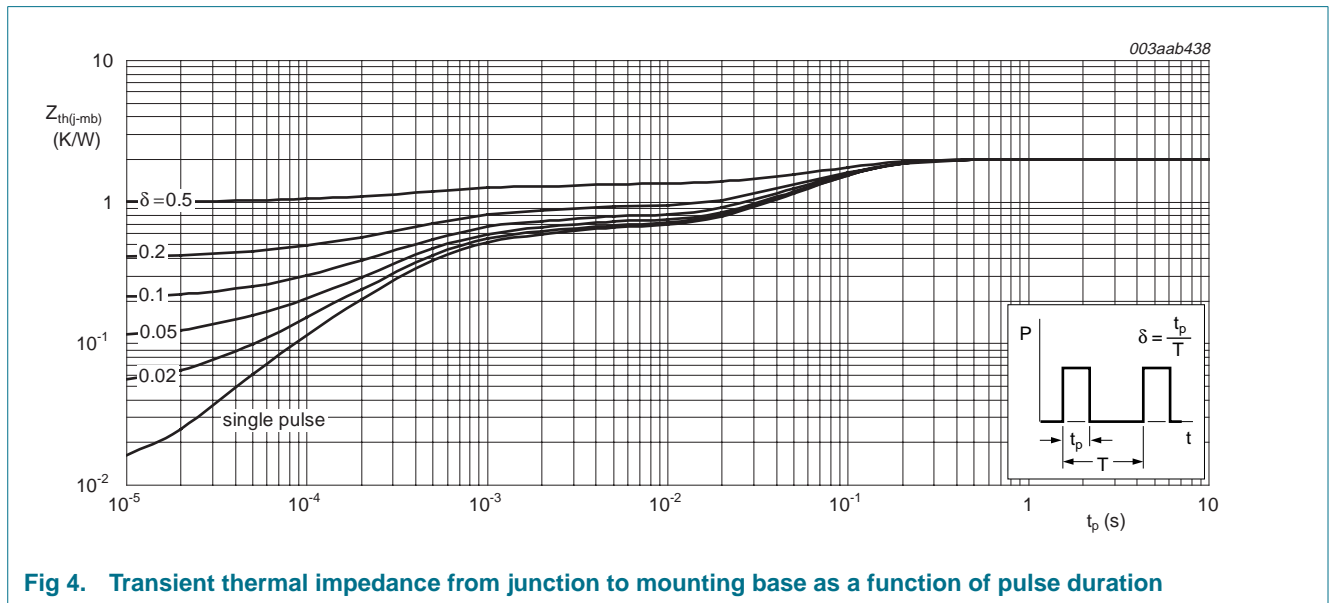


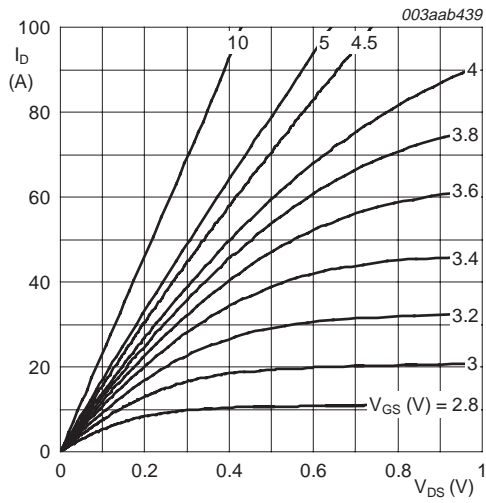
Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 6. Characteristics

**Table 5. Characteristics**

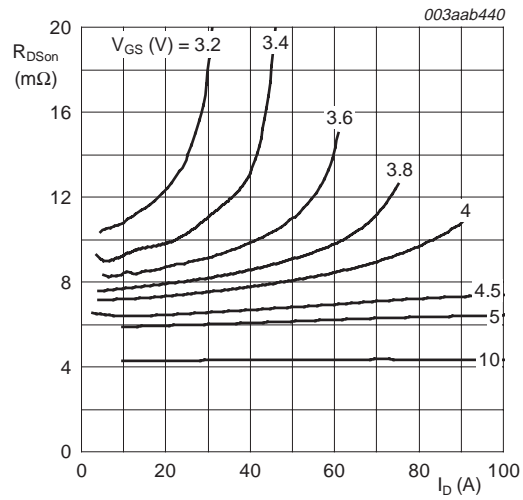
$T_j = 25\text{ °C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu\text{A}; V_{GS} = 0\ \text{V}$				
		$T_j = 25\text{ °C}$	25	-	-	V
		$T_j = -55\text{ °C}$	22.5	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ \text{mA}; V_{DS} = V_{GS}$ ; see <a href="#">Figure 9</a> and <a href="#">10</a>				
		$T_j = 25\text{ °C}$	1.3	1.7	2.15	V
		$T_j = 150\text{ °C}$	0.8	-	-	V
		$T_j = -55\text{ °C}$	-	-	2.6	V
$I_{DSS}$	drain leakage current	$V_{DS} = 25\ \text{V}; V_{GS} = 0\ \text{V}$				
		$T_j = 25\text{ °C}$	-	-	1	$\mu\text{A}$
		$T_j = 150\text{ °C}$	-	-	100	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = \pm 16\ \text{V}; V_{DS} = 0\ \text{V}$	-	-	100	nA
$R_G$	gate resistance	$f = 1\ \text{MHz}$	-	1.8	-	$\Omega$
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\ \text{V}; I_D = 25\ \text{A}$ ; see <a href="#">Figure 6</a> and <a href="#">8</a>				
		$T_j = 25\text{ °C}$	-	4	5.5	m $\Omega$
		$T_j = 150\text{ °C}$	-	6.8	9.35	m $\Omega$
		$V_{GS} = 4.5\ \text{V}; I_D = 25\ \text{A}$ ; see <a href="#">Figure 6</a> and <a href="#">8</a>	-	5.9	8.2	m $\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25\ \text{A}; V_{DS} = 12\ \text{V}; V_{GS} = 4.5\ \text{V}$ ; see <a href="#">Figure 11</a> and <a href="#">12</a>	-	16.6	-	nC
$Q_{GS}$	gate-source charge		-	8	-	nC
$Q_{GS1}$	pre- $V_{GS(th)}$ gate-source charge		-	3.4	-	nC
$Q_{GS2}$	post- $V_{GS(th)}$ gate-source charge		-	4.6	-	nC
$Q_{GD}$	gate-drain charge		-	3.3	-	nC
$V_{GS(pl)}$	gate-source plateau voltage		-	3.1	-	V
$C_{iss}$	input capacitance	$V_{GS} = 0\ \text{V}; V_{DS} = 12\ \text{V}; f = 1\ \text{MHz}$ ; see <a href="#">Figure 14</a>	-	2150	-	pF
$C_{oss}$	output capacitance		-	500	-	pF
$C_{rss}$	reverse transfer capacitance		-	225	-	pF
$C_{iss}$	input capacitance	$V_{GS} = 0\ \text{V}; V_{DS} = 0\ \text{V}; f = 1\ \text{MHz}$	-	2460	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 12\ \text{V}; R_L = 0.5\ \Omega; V_{GS} = 4.5\ \text{V}$ ; $R_G = 5.6\ \Omega$	-	25	-	ns
$t_r$	rise time		-	55	-	ns
$t_{d(off)}$	turn-off delay time		-	28	-	ns
$t_f$	fall time		-	17	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25\ \text{A}; V_{GS} = 0\ \text{V}$ ; see <a href="#">Figure 13</a>	-	0.83	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 20\ \text{A}; dI_S/dt = -100\ \text{A}/\mu\text{s}; V_{GS} = 0\ \text{V}$	-	33.2	-	ns
$Q_r$	recovered charge		-	10.8	-	nC



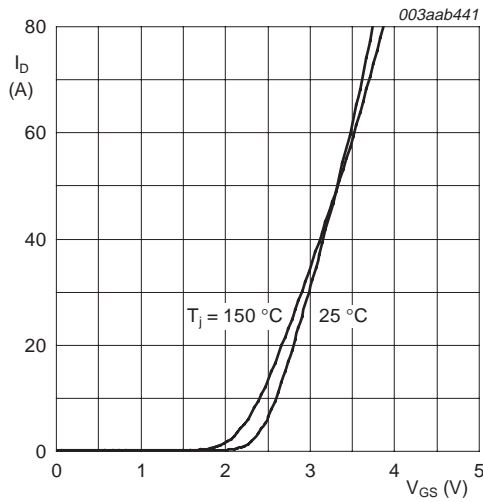
$T_j = 25\text{ }^\circ\text{C}$

**Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values**



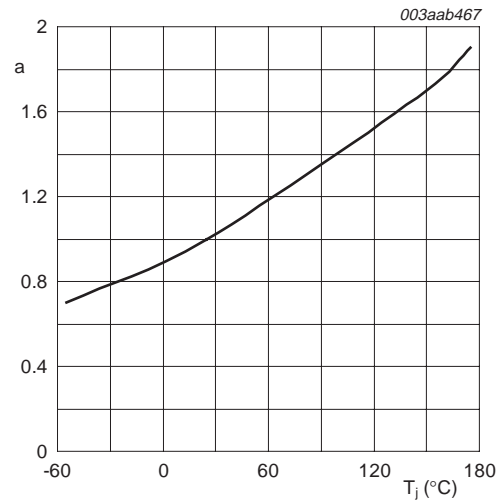
$T_j = 25\text{ }^\circ\text{C}$

**Fig 6. Drain-source on-state resistance as a function of drain current; typical values**



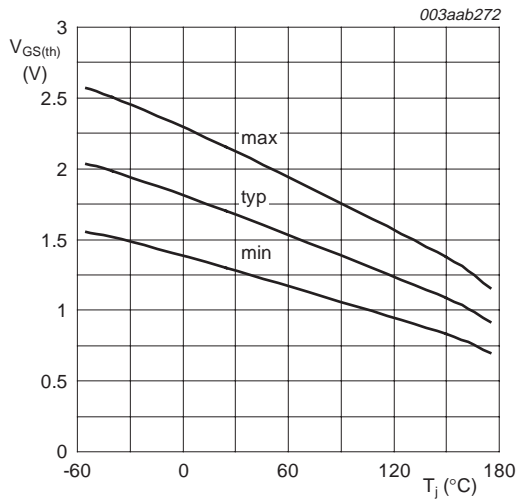
$T_j = 25\text{ }^\circ\text{C}$  and  $150\text{ }^\circ\text{C}$ ;  $V_{DS} > I_D \times R_{DS(on)}$

**Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



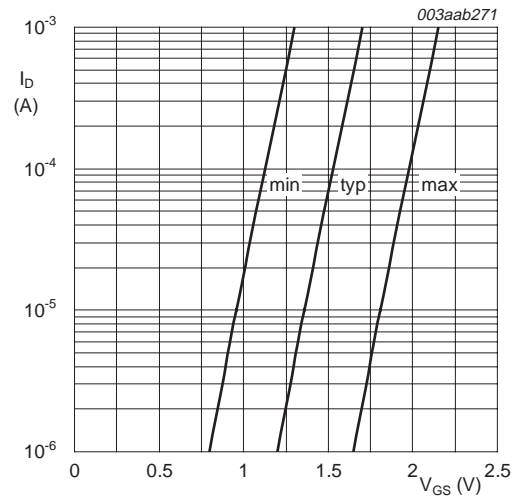
$$a = \frac{R_{DS(on)}}{R_{DS(on)(25^\circ\text{C})}}$$

**Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature**



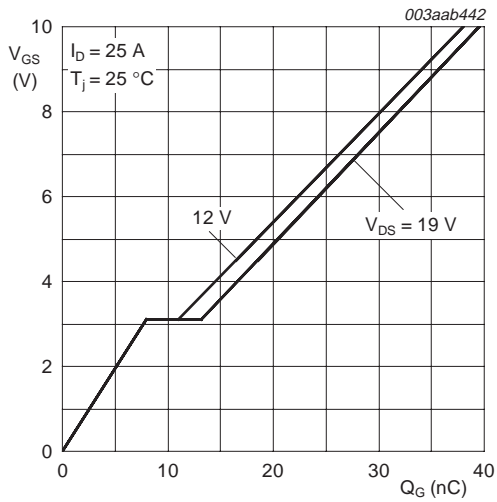
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature



$T_j = 25 \text{ }^\circ\text{C}; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



$I_D = 25 \text{ A}; V_{DS} = 12 \text{ V and } 19 \text{ V}$

Fig 11. Gate-source voltage as a function of gate charge; typical values

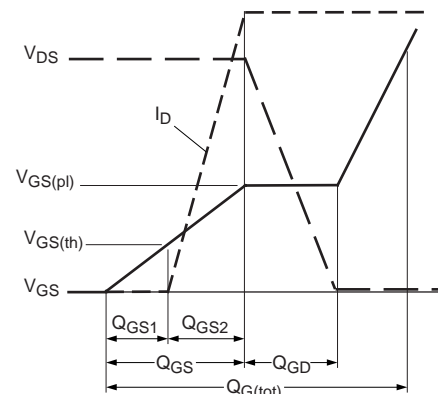
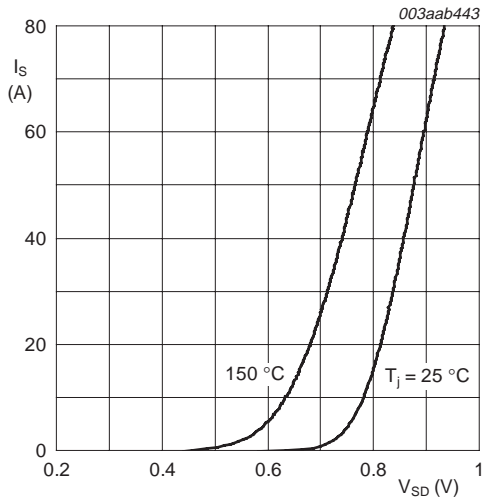
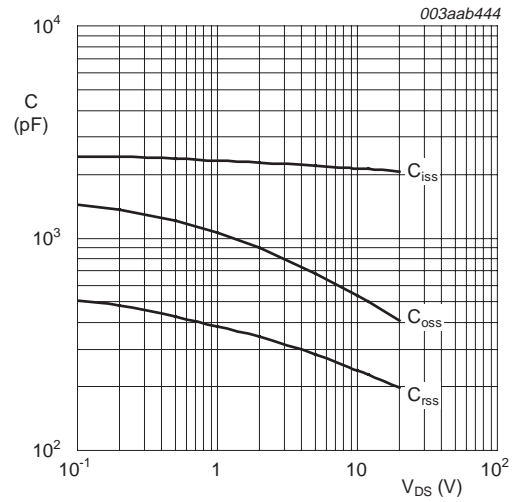


Fig 12. Gate charge waveform definitions



$T_j = 25\text{ }^\circ\text{C}$  and  $150\text{ }^\circ\text{C}$ ;  $V_{GS} = 0\text{ V}$

**Fig 13. Source current as a function of source-drain voltage; typical values**



$V_{GS} = 0\text{ V}$ ;  $f = 1\text{ MHz}$

**Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



7. Package outline

Plastic single-ended surface-mounted package (LPAK); 4 leads

SOT669

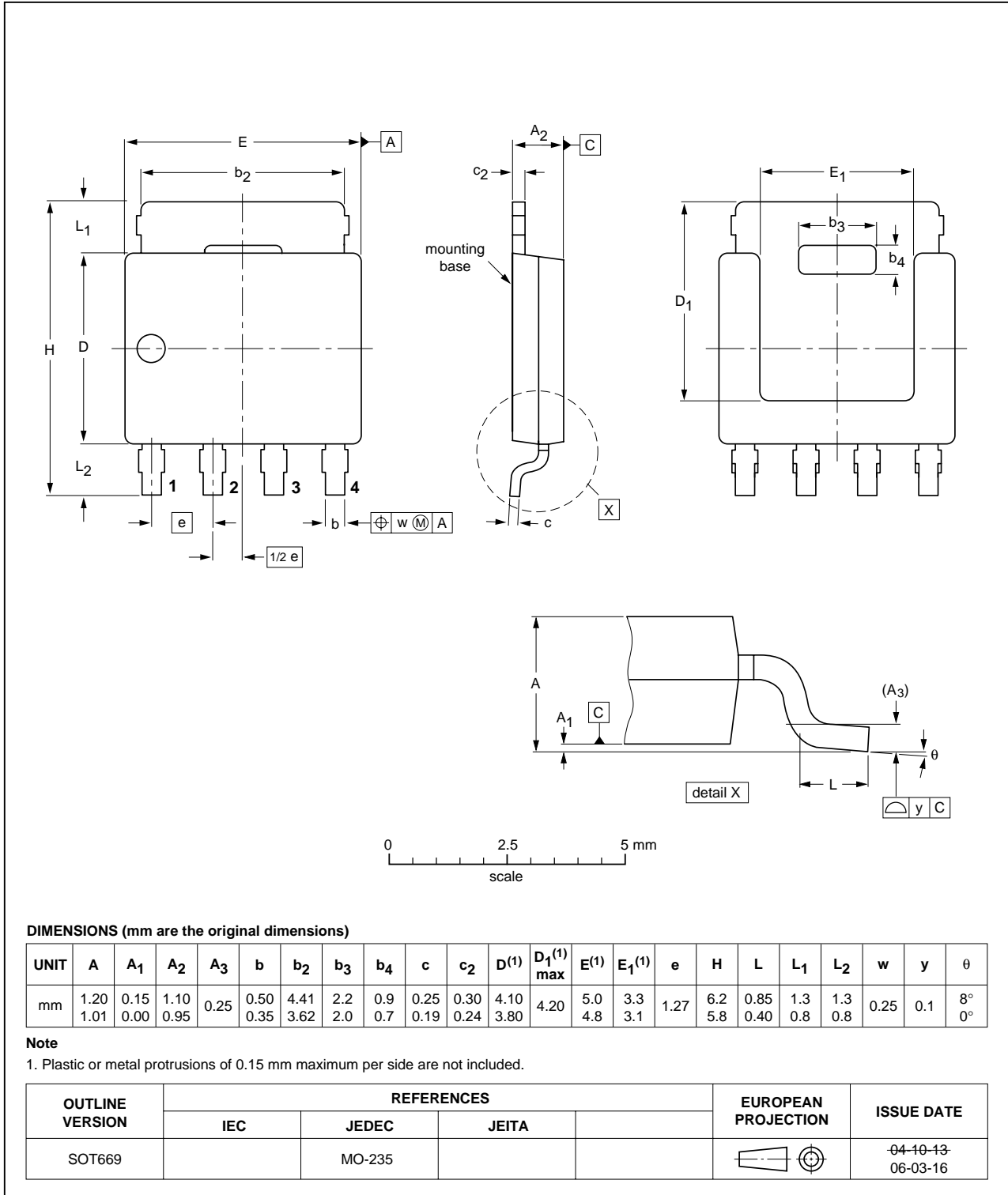


Fig 15. Package outline SOT669 (LPAK)

## 8. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PH5525L_2	20061205	Product data sheet	-	PH5525L_1
Modifications:	• <a href="#">Section 1.2</a> : updated the list			
PH5525L_1	20061010	Product data sheet	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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