Integrated Device Technology, Inc.

16-BIT CMOS ERROR DETECTION AND CORRECTION UNIT

IDT39C60
IDT39C60–1
IDT39C60A
IDT39C60B

FEATURES

- Low-power CEMOS™
  - — Military: 100mA (max.)
  - — Commercial: 85mA (max.)
- Fast
  - — Data in to Error Detect
    IDT39C60B: 16ns (max.), IDT39C60A: 20ns (max.)
    IDT39C60–1: 25ns (max.), IDT39C60: 32ns (max.)
  - — Data in to Corrected Data out
    IDT39C60B: 25ns (max.), IDT39C60A: 30ns (max.)
    IDT39C60–1: 52ns (max.), IDT39C60: 65ns (max.)
- Improves system memory reliability
  - — Corrects all single-bit errors, detects all double and some triple-bit errors
- Cascadable
  - — Data words up to 64 bits
- Built-in diagnostics
  - — Capable of verifying proper EDC operation via software control
- Simplified byte operations
  - — Fast byte writes possible with separate byte enables
- Available in 48-pin DIP, 52-pin PLCC and LCC
- Pin-compatible to all versions of the AMD2960
- Military product available compliant to MIL-STD-883, Class B
- Standard Military Drawing #5962-88613 available for this function

DESCRIPTIONS

The IDT39C60 family are high-speed, low-power, 16-bit Error Detection and Correction Units which generate check-bits on a 16-bit data field according to a modified Hamming Code and correct the data word when checkbits are supplied. When performing a read operation from memory, the IDT39C60s will correct 100% of all single bit errors, will detect all double bit errors and some triple bit errors.

The IDT39C60s are easily cascadable from 16 bits up to 64 bits. Sixteen-bit systems use 6 check bits, 32-bit systems use 7 check bits and 64-bit systems use 8 check bits. For all three configurations, the error syndrome is made available.

All parts incorporate 2 built-in diagnostic modes. Both simplify testing by allowing for diagnostic data to be entered into the device and to execute system diagnostic functions.

The IDT39C60s are pin-compatible, performance-enhanced functional replacements for all versions of the 2960. They are fabricated using CEMOS, a CMOS technology designed for high-performance and high-reliability. The devices are packaged in either 48-pin DIPs and 52-pin PLCC and LCCs.

Military grade product is manufactured in compliance to the latest revision of MIL-STD-883, Class B.

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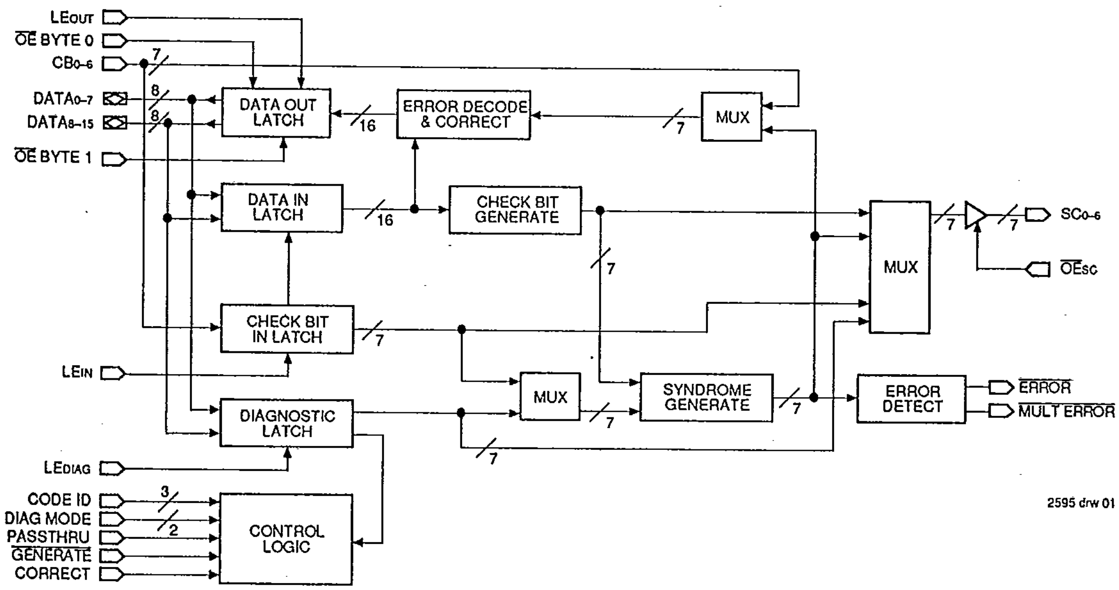
FUNCTIONAL BLOCK DIAGRAM



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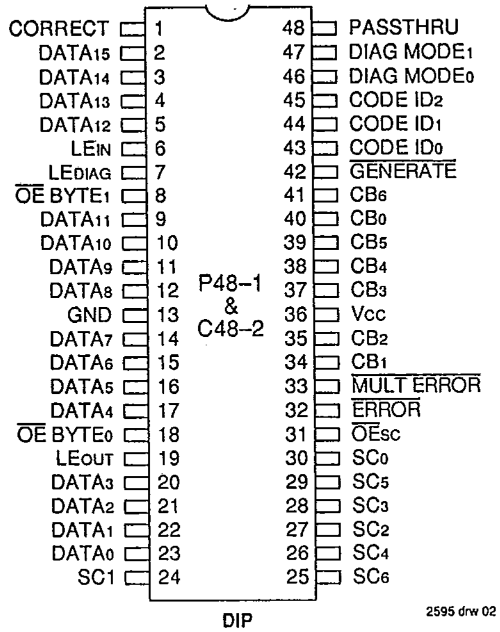
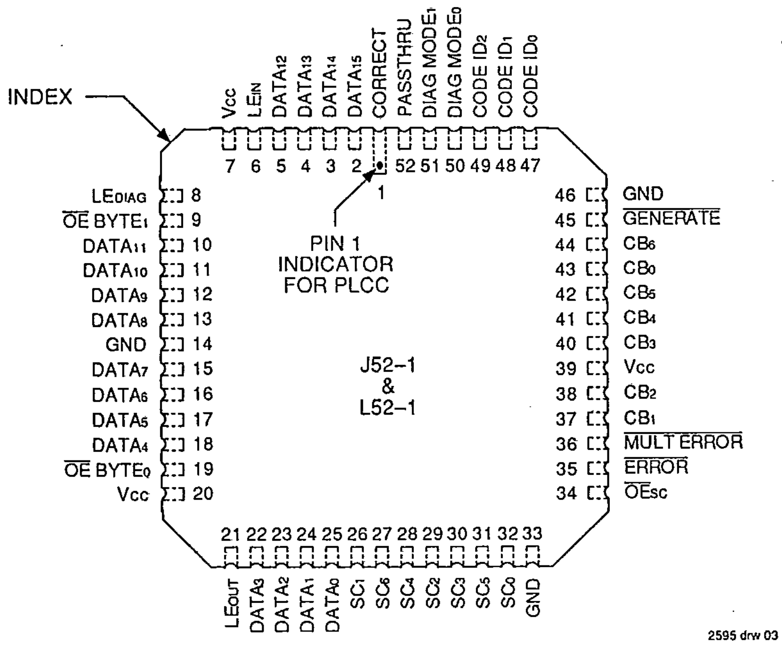
PIN CONFIGURATION

T-45-17



DIP
TOP VIEW
(600 mil x 100 mil Centers)



PLCC/LCC
TOP VIEW
(750 mil x 750 mil Centers)

T-45-17

PIN DESCRIPTIONS

Pin Name	I/O	Description
DATA$_{0-15}$	I/O	16 bidirectional data lines provide input to the Data Input Latch and receive output from the Data Output Latch. DATA$_0$ is the least significant bit; DATA$_{15}$ the most significant.
CB$_{0-6}$	I	Seven check bit input lines are used to input check bits for error detection. Also used to input syndrome bits for error correction in 32- and 64-bit configurations.
LE$_{IN}$	I	Latch Enable — Data Input Latch. Controls latching of the input data. When HIGH, the Data Input Latch and Check Bit Input Latch follow the input data and input check bits. When LOW, the Data Input Latch and Check Bit Input Latch are latched to their previous state.
$\overline{\text{GENERATE}}$	I	Generate Check Bits input. When this input is LOW, the EDC is in the Check Bit Generate mode. When HIGH, the EDC is in the Detect mode or Correct mode. In the Generate mode, the circuit generates the check bits or partial check bits specific to the data in the Data Input Latch. The generated check bits are placed on the SC outputs. In the Detect or Correct modes the EDC detects single and multiple errors and generates syndrome bits based upon the contents of the Data Input Latch and Check Bit Input Latch. In Correct mode, single-bit errors are also automatically corrected — corrected data is placed at the input of the Data Output Latch. The syndrome result is placed on the SC outputs and indicates, in a coded form, the number of errors and the bit-in-error.
SC$_{0-6}$	O	Syndrome/Check Bit outputs hold the check/partial check bits when the EDC is in Generate mode and will hold the syndrome/partial syndrome bits when the device is in Detect or Correct modes. These are 3-state outputs.
$\overline{\text{OE}}$SC	I	Output Enable — Syndrome/Check Bits. When LOW, the 3-state output lines SC$_{0-6}$ are enabled. When HIGH, the SC outputs are in the high impedance state.
$\overline{\text{ERROR}}$	O	Error Detected output. When the EDC is in Detect or Correct mode, this output will go LOW if one or more syndrome bits are asserted, meaning there are one or more bit errors in the data or check bits. If no syndrome bits are asserted, there are no errors detected and the output will be HIGH. In Generate mode, $\overline{\text{ERROR}}$ is forced HIGH. (In a 64-bit configuration, $\overline{\text{ERROR}}$ must be implemented externally.)
$\overline{\text{MULT ERROR}}$	O	Multiple Errors Detected output. When the EDC is in Detect or Correct mode this output, if LOW, indicates that there are two or more bit errors that have been detected. If HIGH, this indicates that either one or no errors have been detected. In Generate mode, $\overline{\text{MULT ERROR}}$ is forced HIGH. (In a 64-bit configuration, $\overline{\text{MULT ERROR}}$ must be implemented externally.)
CORRECT	I	Correct input. When HIGH, this signal allows the correction network to correct any single-bit error in the Data Input Latch (by complementing the bit-in-error) before putting it into the Data Output Latch. When LOW, the EDC will drive data directly from the Data Input Latch to the Data Output Latch without correction.
LE$_{OUT}$	I	Latch Enable — Data Output Latch. Controls the latching of the Data Output Latch. When LOW, the Data Output Latch is latched to its previous state. When HIGH, the Data Output Latch follows the output of the Data Input Latch as modified by the correction logic network. In Correct mode, single-bit errors are corrected by the network before loading into the Data Output Latch. In Detect mode, the contents of the Data Input Latch are passed through the correction network unchanged into the Data Output Latch. The inputs to the Data Output Latch are disabled with its contents unchanged if the EDC is in Generate mode.
$\overline{\text{OE}}$ BYTE$_0$ $\overline{\text{OE}}$ BYTE$_1$	I	Output Enable — Bytes 0 and 1, Data Output Latch controls the 3-state outputs for each of the two bytes of the Data Output Latch. When LOW, these lines enable the Data Output Latch and, when HIGH, these lines force the Data Output Latch into the high impedance state. The two enable lines can be separately activated to enable only one byte of the Data Output at a time.
PASSTHRU	I	PASSTHRU input, when HIGH, forces the contents of the Check Bit Input Latch onto the Syndrome/Check Bit outputs (SC$_{0-6}$) and the unmodified contents of the Data Input Latch onto the inputs of the Data Output Latch.
DIAG MODE$_{0-1}$	I	Diagnostic Mode Select controls the initialization and diagnostic operation of the EDC.
CODE ID$_{0-2}$	I	Code Identification inputs identify the size of the total data word to be processed and which 16-bit slice of larger data words a particular EDC is processing. The three allowable data word sizes are 16, 32, and 64 bits and their respective modified Hamming Codes are designated 16/22, 32/39 and 64/72. Special CODE ID input 001 (ID$_2$, ID$_1$, ID$_0$) is also used to instruct the EDC that the signals CODE ID$_{0-2}$, DIAG MODE$_{0-1}$, CORRECT and PASSTHRU are to be taken from the diagnostic latch rather than the control lines.
LE$_{DIAG}$	I	Latch Enable — Diagnostic Latch. The Diagnostic Latch follows the 16-bit data on the input lines when HIGH. When LOW, the outputs of the Diagnostic Latch are latched to their previous states. The Diagnostic Latch holds diagnostic check bits and internal control signals for CODE ID$_{0-2}$, DIAG MODE$_{0-1}$, CORRECT and PASSTHRU.

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PRODUCT DESCRIPTION

The IDT39C60 EDC Unit is a powerful 16-bit cascadable slice used for check bit generation, error detection, error correction and diagnostics. As shown in the Functional Block Diagram, the device consists of the following:

- — Data Input Latch
- — Data Output Latch
- — Diagnostic Latch
- — Check Bit Input Latch
- — Check Bit Generation Logic
- — Syndrome Generation Logic
- — Error Detection Logic
- — Error Correction Logic
- — Control Logic

DATA INPUT/OUTPUT/DIAGNOSTIC LATCHES

The LE_{IN}, Latch Enable input, controls the Data Input which can load 16 bits of data from the bidirectional DATA lines. The input data is used for either check bit generation or error detection/correction.

The 16 bits of data from the DATA lines can be loaded into the Diagnostic Latch under control of the Diagnostic Latch Enable, LE_{DIAG}, giving check bit information in one byte and control information in the other byte. The Diagnostic Latch is used when in Internal Control mode or in one of the Diagnostics modes.

The Data Output Latch is split into two bytes and enabled onto the DATA lines through separate byte control lines. The Data Output Latch stores the result of an error correction operation or is loaded directly from the Data Input Latch under control of the Latch Enable Out (LE_{OUT}). The PASSTHRU control input determines which data is loaded.

CHECK BIT GENERATION LOGIC

This block of combinational logic generates 7 check bits using a modified Hamming Code from the 16 bits of data input from the Data Input Latch.

SYNDROME GENERATION LOGIC

This logic compares the check bits generated through the Check Bit Generator with either the check bits in the Check Bit Input Latch or 7 bits assigned in the Diagnostic Latch.

Syndrome bits are produced by an exclusive-OR of the two sets of bits. A match indicates no errors. If errors occur, the syndrome bits can be decoded to indicate the bit in error, whether 2 errors were detected or 3 or more errors.

ERROR DETECTION/CORRECTION LOGIC

The syndrome bits generated by the Syndrome Logic are decoded and used to control the $\overline{ERROR}$ and $\overline{MULTERROR}$ outputs. If one or more errors are detected, $\overline{ERROR}$ goes low. If two or more errors are detected, both $\overline{ERROR}$ and $\overline{MULT ERROR}$ go low. Both outputs remain high when there are no errors detected.

For single bit errors, the correction logic will complement (correct) the bit in error, which can then be loaded into the Data Out Latches under the LE_{OUT} control. If check bit errors need to be corrected, then the device must be operated in the Generate mode.

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CONTROL LOGIC

The control logic determines the specific mode of operation, usually from external control signals. However, the Internal Control mode allows these signals to be provided from the Diagnostic Latch.

DETAILED PRODUCT DESCRIPTION

The IDT39C60 EDC unit contains the logic necessary to generate check bits on a 16-bit data input according to a modified Hamming Code. The EDC can compare internally generated check bits against those read with the 16-bit data to allow correction of any single bit data error and detection of all double and some triple bit errors. The IDT39C60 can be used for 16-bit data words (6 check bits), 32-bit data words (7 check bits) or 64-bit data words (8 check bits).

CODE AND BYTE SELECTION

The 3 code identification pins, ID_{0-2}, are used to determine the data word size from 16, 32 or 64 bits and the byte position of each 16-bit IDT39C60 EDC device.

Code 16/22 refers to a 16-bit data field with 6 check bits.
Code 32/39 refers to a 32-bit data field with 7 check bits.
Code 64/72 refers to a 64-bit data field with 8 check bits.

The ID_{0-2} of 001 is used to place the device in the Internal Control mode as described later in this section.

Table 1 defines all possible identification codes.

CHECK AND SYNDROME BITS

The IDT39C60 provides either check bits or syndrome bits on the three-state output pins, SC_{0-6}. Check bits are generated from a combination of the Data Input bits, while syndrome bits are an Exclusive-OR of the check bits generated from read data with the read check bits stored with the data. Syndrome bits can be decoded to determine the single bit-in-error or that a double error was detected. Some triple bit errors are also detected. The check bits are labeled:

C_0, C_1, C_2, C_3, C_4	for the 8-bit configuration
$C_0, C_1, C_2, C_3, C_4, C_5$	for the 16-bit configuration
$C_0, C_1, C_2, C_3, C_4, C_5, C_6$	for the 32-bit configuration
$C_0, C_1, C_2, C_3, C_4, C_5, C_6, C_7$	for the 64-bit configuration

Syndrome bits are similarly labeled S_0 through S_7.

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CONTROL MODE SELECTION

Tables 2 and 3 describe the 9 operating modes of the IDT39C60. The Diagnostic mode pins, DIAG MODE$_{0-1}$, define 4 basic areas of operation, with $\overline{\text{GENERATE}}$, CORRECT and PASSTHRU, further dividing operation into 8 functions with the ID$_{0-2}$ defining the ninth mode as the Internal mode.

Generate mode is used to display the check bits on the outputs SC$_{0-6}$. The Diagnostic Generate mode displays check bits as stored in the Diagnostic Latch.

Detect mode provides an indication of errors or multiple errors on the outputs $\overline{\text{ERROR}}$ and $\overline{\text{MULTERROR}}$. Single bit errors are not corrected in this mode. The syndrome bits are provided on the outputs SC$_{0-6}$. For the Diagnostic Detect mode, the syndrome bits are generated by comparing the internally generated check bits from the Data In Latch with check bits stored in the diagnostic latch rather than with the check bit latch contents.

Correct mode is similar to the Detect mode except that single bit errors will be complemented (corrected) and made available as input to the Data Out Latch. Again, the Diagnostic Correct mode will correct single bit errors as determined by syndrome bits generated from the Data Input and contents of the Diagnostic Latch.

The Initialize mode provides check bits for all zero bit data. Data In Latch is set and latched to a logic zero and made available as input to the Data Out Latch.

The Internal mode disables the external control pins DIAG MODE$_{0-1}$, CORRECT, PASSTHRU and CODE ID to be defined by the Diagnostic Latch. When in the internal control mode, the data loaded into the diagnostic latch should have the CODE ID different from 001 as this would represent an invalid operation.

CODE ID$_2$	CODE ID$_1$	CODE ID$_0$	Hamming Code and Slice Selected
0	0	0	Code 16/22
0	0	1	Internal Control Mode
0	1	0	Code 32/39, Byte 0 and 1
0	1	1	Code 32/39, Byte 2 and 3
1	0	0	Code 64/72, Byte 0 and 1
1	0	1	Code 64/72, Byte 2 and 3
1	1	0	Code 64/72, Byte 4 and 5
1	1	1	Code 64/72, Byte 6 and 7

2595 tbl 02

Table 1. Hamming Code and Slice Identification

DIAG MODE$_1$	DIAG MODE$_2$	Diagnostic Mode Selected
0	0	**Non-diagnostic mode.** The EDC functions normally in all modes.
0	1	**Diagnostic Generate.** The contents of the Diagnostic Latch are substituted for the normally generated check bits when in the Generate mode. The EDC functions normally in the Detect or Correct modes.
1	0	**Diagnostic Detect/Correct.** In the Detect or Correct mode, the contents of the Diagnostic Latch are substituted for the check bits normally read from the Check Bit Input Latch. The EDC functions normally in the Generate mode.
1	1	**Initialize.** The outputs of the Data Input Latch are forced to zeroes and the check bits generated correspond to the all zero data. The latch is not reset, a functional difference from the Am2960.

2595 tbl 03

Table 2. Diagnostic Mode Control

Operating Mode	DM1 DM0	GENERATE	CORRECT	PASS-THRU	DATAOUT Latch (LEOUT = High)	SC0–6 (OEsc = Low)	ERROR / MULT ERROR
Generate	0 0 1 0	0	X	0	—	Check Bits Generated from DATAIN Latch	High
Detect	0 0 0 1	1	0	0	DATAIN Latch	Syndrome Bits DATAIN/ Check Bit Latch	Error Dep[1]
Correct	0 0 0 1	1	1	0	DATAIN Latch with Single Bit Correction	Syndrome Bits DATAIN/ Check Bit Latch	Error Dep
PASSTHRU	0 0 0 1 1 0	X	X	1	DATAIN Latch	Check Bit Latch	High
Diagnostic Generate	0 1	0	X	0	—	Check Bits from Diagnostic Latch	High
Diagnostic Detect	1 0	1	0	0	DATAIN Latch	Syndrome Bits DATAIN/ Diagnostic Latch	Error Dep
Diagnostic Correct	1 0	1	1	0	DATAIN Latch with Single Bit Correction	Syndrome Bits DATAIN/ Diagnostic Latch	Error Dep
Initialization Mode	1 1	X	X	X	DATAIN Latch Set to 0000	Check Bits Generated from DATAIN Latch (0000)	—
Internal Mode	ID0–2 = 001 (Control Signals ID0–2, DIAG MODE0–1, CORRECT and PASSTHRU are taken from the Diagnostic Latch)						

2595 tbl 04

NOTE:
1. ERROR DEP (Error Dependent): ERROR will be low for single or multiple errors, with MULT ERROR low for double or multiple errors. Both signals are high for no errors.

Table 3. IDT39C60 Operating Modes

16-BIT DATA WORD CONFIGURATION

Figure 1 indicates the 22-bit data format for two bytes of data and 6 check bits.

A single IDT39C60 EDC unit, connected as shown in Figure 2, provides all the logic needed for single bit error correction and double bit error detection of a 16-bit data field. The identification code 16/22 indicates 6 check bits are required. The CB_6 pin is, therefore, a "Don't Care" and ID_2, ID_1, ID_0 = 000.

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DATA		CHECK BITS					
$BYTE_1$	$BYTE_0$	C_0	C_1	C_2	C_3	C_4	C_5
15 8	7 0						

2595 drw 04

Uses Modified Hamming Code 16/22
16 Data Bits with 6 Check Bits

Figure 1. 16-Bit Data Format

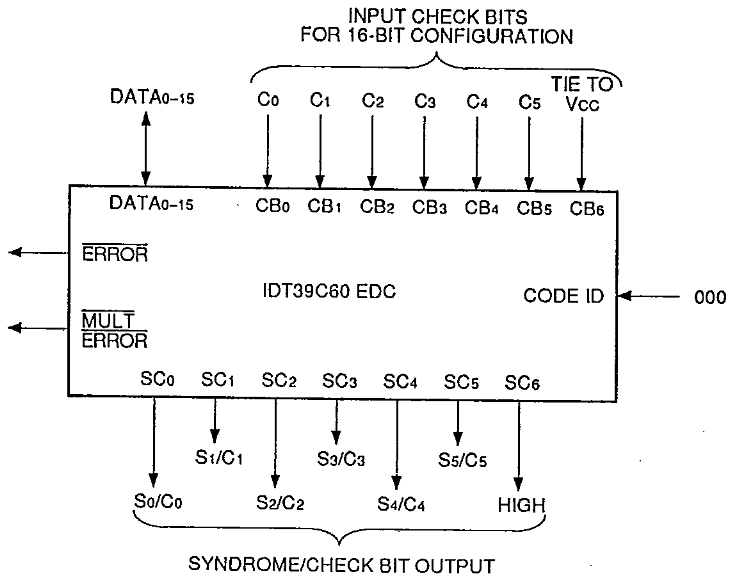

Figure 2. 16-Bit Configuration

Table 3 describes the operating modes available. The output pin SC_6, is forced high for either syndrome or check bits since only 6 check bits are used for the 16/22 code.

Table 4 indicates the data bits participating in the check bit generation. For example, check bit C_0 is the Exclusive-OR function of the 8 data input bits marked with an X. Check bits are generated and output in the Generate and Initialization Mode. Check bits are passed as stored in the PASSTHRU or Diagnostic Generate Mode.

Syndrome bits are generated by an Exclusive-OR of the generated check bits with the read check bits. For example, SX is the XOR of check bits CX from those read with those generated. Table 5 indicates the decoding of the six syndrome bits to indicate the bit-in-error for a single bit error, or whether a double or triple bit error was detected. The all zero case indicates no errors detected.

In the Correct Mode, the syndrome bits are used to complement (correct) single bit errors in the data bits. For double or multiple error detection, the data available as input to the Data Out Latch is not defined.

Table 6 defines the bit definition for the Diagnostic Latch. As defined in Table 3, several modes will use the diagnostic check bits to determine syndrome bits or to pass as check bits to the SC_{0-5} outputs. The Internal Mode substitutes the indicated bit position for the external control signals.

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Generated Check Bits	Parity	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		Participating Data Bits[1]															
C_0	Even (XOR)		X	X	X		X			X	X		X			X	
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X

NOTE:
1. The check bit is generated as either an XOR or XNOR of the eight data bits noted by an "X" in the table.

2595 tbl 05

Table 4. 16-Bit Modified Hamming Code — Check Bit Encode Chart

Hex	S_3	S_2	S_1	S_0	0	1	2	3
Syndrome Bits S_5					0	0	1	1
Syndrome Bits S_4					0	1	0	1
0	0	0	0	0	*	C4	C5	T
1	0	0	0	1	C0	T	T	14
2	0	0	1	0	C1	T	T	M
3	0	0	1	1	T	2	8	T
4	0	1	0	0	C2	T	T	15
5	0	1	0	1	T	3	10	T
6	0	1	1	0	T	4	9	T
7	0	1	1	1	M	T	T	M
8	1	0	0	0	C3	T	T	M
9	1	0	0	1	T	5	11	T
A	1	0	1	0	T	6	12	T
B	1	0	1	1	1	T	T	M
C	1	1	0	0	T	7	13	T
D	1	1	0	1	M	T	T	M
E	1	1	1	0	0	T	T	M
F	1	1	1	1	T	M	M	T

NOTES:
* = No errors detected
Number = The number of the single bit-in-error
T = Two errors detected
M = Three or more errors detected

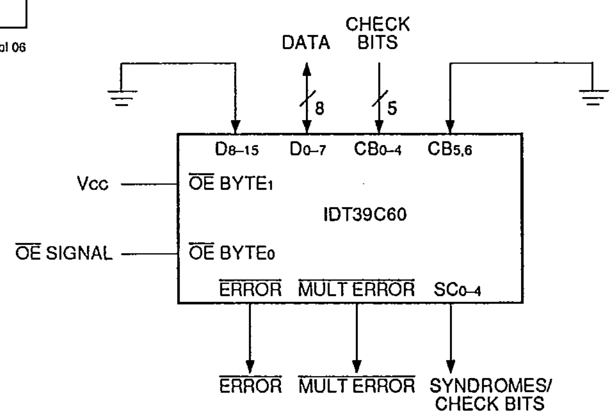
2595 tbl 06

Table 5. Syndrome Decode to Bit-In-Error (16-Bit Configuration)

Data Bit	Internal Function
0	Diagnostic Check Bit_0
1	Diagnostic Check Bit_1
2	Diagnostic Check Bit_2
3	Diagnostic Check Bit_3
4	Diagnostic Check Bit_4
5	Diagnostic Check Bit_5
6, 7	Don't Care
8	CODE ID_0
9	CODE ID_1
10	CODE ID_2
11	DIAG $MODE_0$
12	DIAG $MODE_1$
13	CORRECT
14	PASSTHRU
15	Don't Care

2595 tbl 07

Table 6. Diagnostic Latch Loading — 16-Bit Format



2595 drw 06

Figure 3. 8-Bit Configuration

32-BIT DATA WORD CONFIGURATION

Two IDT39C60 EDC units, connected as shown in Figure 5, provide all the logic needed for single bit error correction and double bit error detection of a 32-bit data field. The identification code 32/39 indicates 7 check bits are required. Table 1 gives the ID_2, ID_1, ID_0 values needed for distinguishing the byte 0/1 from byte 2/3. Valid syndrome, check bits and the $\overline{ERROR}$ and $\overline{MULTERROR}$ signal come from the byte 2/3 unit. Control signals not indicated are connected to both units in parallel. The $\overline{OE}_{SC}$ always enables the SC_{0-6} outputs of byte 0/1, but must be used to select data check bits or syndrome bits fed back from the byte 2/3 for data correction modes.

Data In bits 0 through 15 are connected to the same numbered inputs of the byte 0/1 EDC unit, while Data In bits 16 through 31 are connected to byte 2/3 Data Inputs 0 to 15, respectively.

Figure 4 indicates the 39-bit data format for 4 bytes of data and 7 check bits. Check bits are input to the byte 0/1 unit through a tri-state buffer unit such as the IDT74FCT244. Correction of single bit errors of the 32-bit configuration requires a feedback of sydrome bits from byte 2/3 into the byte 0/1 unit. The MUX shown on the functional block diagram is used to select the CB_{0-6} pins as the syndrome bits rather than internally generated syndrome bits.

Table 3 describes the operating mode available for the 32/39 configuration.

Syndrome bits are generated by an Exclusive-OR of the generated check bits with the read check bits. For example, S_n is the XOR of check bits C_n from those read with those generated. Table 7 indicates the decoding of the seven syndrome bits to determine the bit-in-error for a single bit error, or whether a double or triple bit error was detected. The all zero case indicates no errors detected.

In the Correct Mode, the syndrome bits are used to complement (correct) single bit errors in the data bits. For double or multiple error detection, the data available as input to the Data Out Latch is not defined.

Performance data is provided in Table 8 in relating a single IDT39C60 EDC with the two cascaded units of Figure 5. As indicated, a summation of propagation delays is required from the cascading arrangement of EDC units.

Table 9 defines the bit definition for the Diagnostic Latch. As defined in Table 3, several modes will use the Diagnostic check bits to determine syndrome bits or to pass as check bits to the SC_{0-6} outputs. The Internal Mode substitutes the indicated bit position for the external control signals.

Table 10 indicates the data bits participating in the check bit generation. For example, check bit C_0 is the Exclusive-OR function of the 16 data input bits marked with an X. Check bits are generated and output in the Generate and Initialization Mode. Check bits are passed as stored in the PASSTHRU or Diagnostic Generate Mode.

				Hex	0	1	2	3	4	5	6	7
	Syndrome Bits			S6	0	0	0	0	1	1	1	1
				S5	0	0	1	1	0	0	1	1
				S4	0	1	0	1	0	1	0	1
Hex	S_3	S_2	S_1	S_0								
0	0	0	0	0	*	C4	C5	T	C6	T	T	30
1	0	0	0	1	C0	T	T	14	T	M	M	T
2	0	0	1	0	C1	T	T	M	T	2	24	T
3	0	0	1	1	T	18	8	T	M	T	T	M
4	0	1	0	0	C2	T	T	15	T	3	25	T
5	0	1	0	1	T	19	9	T	M	T	T	31
6	0	1	1	0	T	20	10	T	M	T	T	M
7	0	1	1	1	M	T	T	M	T	4	26	M
8	1	0	0	0	C3	T	T	M	T	5	27	T
9	1	0	0	1	T	21	11	T	M	T	T	M
A	1	0	1	0	T	22	12	T	1	T	T	M
B	1	0	1	1	17	T	T	M	T	6	28	T
C	1	1	0	0	T	23	13	T	M	T	T	M
D	1	1	0	1	M	T	T	M	T	7	29	T
E	1	1	1	0	16	T	T	M	T	M	M	T
F	1	1	1	1	T	M	M	T	0	T	T	M

NOTES:
* = No errors detected
Number = The number of the single bit-in-error
T = Two errors detected
M = Three or more errors detected

2595 tbl 08

Table 7. Syndrome Decode to Bit-In-Error (32-Bit Configuration)

32-Bit Propagation Delay		Component Delay From IDT39C60 AC Specifications
From	To	
DATA	Check Bits Out	(DATA to SC) + (CB to SC, CODE ID 011)
DATA	Corrected $DATA_{OUT}$	(DATA to SC) + (CB to SC, CODE ID 011) + CB to DATA, CODE ID 010)
DATA	Syndromes Out	(DATA to SC) + (CB to SC, CODE ID 011)
DATA	$\overline{ERROR}$ for 32 Bits	(DATA to SC) + (CB to $\overline{ERROR}$, CODE ID011)
DATA	$\overline{MULT ERROR}$ for 32 Bits	(DATA to SC) + (CB to $\overline{MULT ERROR}$, CODE ID 011)

2595 tbl 09

Table 8. Key AC Calculations for the 32-Bit Configuration

T-45-17

DATA				CHECK BITS						
BYTE3	BYTE2	BYTE1	BYTE0	C0	C1	C2	C3	C4	C5	C6
31 24	23 16	15 8	7 0							

Uses Modified Hamming Code 32/39
32 Data Bits with 7 Check Bits

2595 drw 07

Figure 4. 32-Bit Data Format

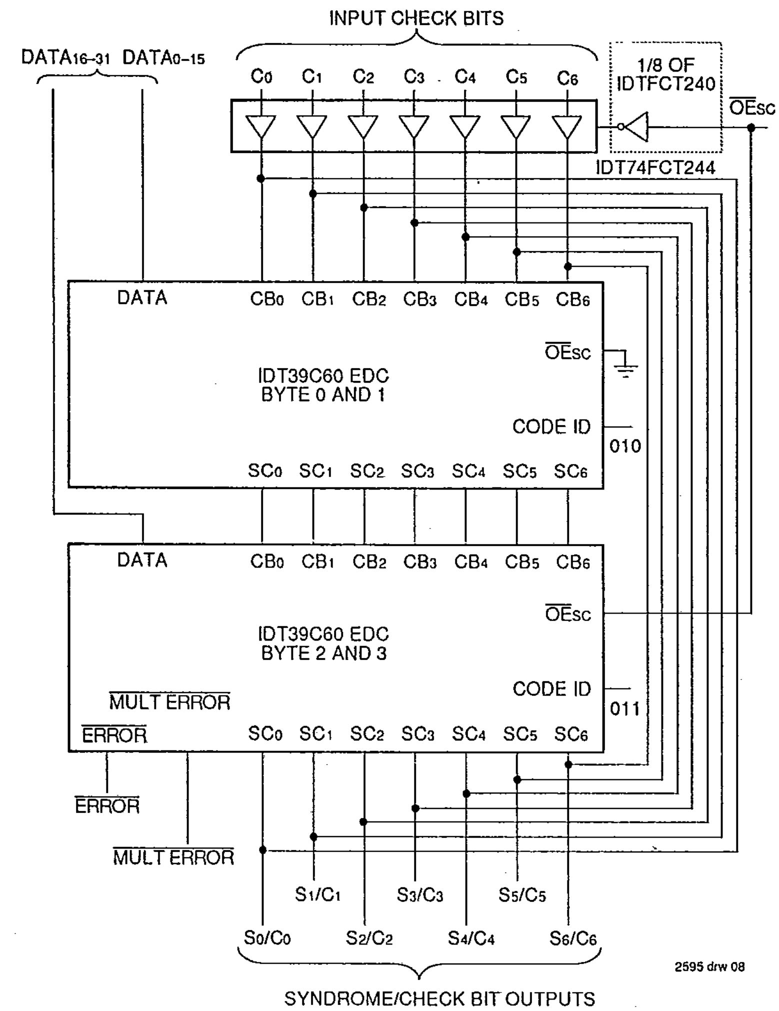


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Figure 5. 32-Bit Configuration

T-45-17

Data Bit	Internal Function
0	Diagnostic Check Bit_0
1	Diagnostic Check Bit_1
2	Diagnostic Check Bit_2
3	Diagnostic Check Bit_3
4	Diagnostic Check Bit_4
5	Diagnostic Check Bit_5
6	Diagnostic Check Bit_6
7	Don't Care
8	Slice 0/1 — CODE ID_0
9	Slice 0/1 — CODE ID_1
10	Slice 0/1 — CODE ID_2
11	Slice 0/1 — DIAG $MODE_0$
12	Slice 0/1 — DIAG $MODE_1$
13	Slice 0/1 — CORRECT
14	Slice 0/1 — PASSTHRU
15	Don't Care
16-23	Don't Care
24	Slice 2/3 — CODE ID_0
25	Slice 2/3 — CODE ID_1
26	Slice 2/3 — CODE ID_2
27	Slice 2/3 — DIAG $MODE_0$
28	Slice 2/3 — DIAG $MODE_1$
29	Slice 2/3 — CORRECT
30	Slice 2/3 — PASSTHRU
31	Don't Care

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Table 9. Diagnostic Latch Loading — 32-Bit Format

Generated Check Bits	Parity	Participating Data Bits															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
C_0	Even (XOR)	X				X		X	X	X	X		X			X	
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)	X	X	X	X	X	X	X	X								

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Generated Check Bits	Parity	Participating Data Bits															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
C_0	Even (XOR)		X	X	X		X					X		X	X		X
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)									X	X	X	X	X	X	X	X

2595 tbl 12

Table 10. 32-Bit Modified Hamming Code — Check Bit Encode Chart

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64-BIT DATA WORD CONFIGURATION

The IDT39C60 EDC units connected with the MSI gates, as shown in Figure 6, provide all the logic needed for single bit error detection and double bit error detection of a 64-bit data field. The Identification code 64/72 is used, indicating 8 check bits are required. Check bits and Syndrome bits are generated external to the IDT39C60 EDC using Exclusive-OR gates. For error correction, the syndrome bits must be fed back to the CB_{0-6} inputs. Thus, external tri-state buffers are used to select between the check bits read in from memory and the syndrome bits being fed back.

The $\overline{\text{ERROR}}$ signal is low for one or more errors detected. From any of the 4 devices, $\overline{\text{MULTERROR}}$ is low for some double bit errors and for all three bit errors. Both are high otherwise. The DOUBLE ERROR signal is high only when a double bit error is detected.

Figure 6 indicates the 72-bit data format of 8 bytes of data and 8 check bits. Check bits are input to the various units through a tri-state buffer such as the IDT74FCT244. Correction of single bit errors of the 64-bit configuration requires a feedback of syndrome bits as generated external to the IDT39C60 EDC. The MUX shown on the functional block diagram is used to select the CB_{0-6} pins as the syndrome bits rather than internally generated syndrome bits.

Table 3 describes the operating modes available for the 64/72 configuration.

Syndrome bits are generated by an Exclusive-OR of the generated check bits with the read check bits. For example, S_n is the XOR of check bits C_n from those read with those generated. Table 11 indicates the decoding of the 8 syndrome bits to determine the bit-in-error for a single bit error or whether a double or triple bit error was detected. The all zero case indicates no errors detected.

In the Correct Mode, the syndrome bits are used to complement (correct) single bit errors in the data bits. For double or multiple error detection, the data available as input to the Data Out Latch is not defined.

Performance data is provided in Table 12 in relating a single IDT39C60 EDC with the four units of Figure 7. Delay through the Exclusive-OR gates and the 3-state buffer must be included.

Table 13 indicates the Data Bits participating in the check bit generation. For example, check bit C_0 is the Exclusive-OR function of the 32 data input bits marked with an X. Check bits are generated and output in the Generate and Initialization mode. In the PASSTHRU mode, the contents of the check bit latch are passed through the external Exclusive-OR gates and appear inverted at the outputs C_0 to C_7.

Table 14 defines the bit definition for the Diagnostic Latch. As defined in Table 3, several modes will use the Diagnostic Check Bits to determine syndrome bits or to pass as check bits to the SC_{0-6} outputs. The Internal Mode substitutes the indicated bit position for the external control signals.

Some multiple errors will cause a data bit to be inverted. For example, in the 16-bit mode where bits 8 and 13 are in error, the syndrome 111100 (S_0, S_1, S_2, S_3, S_4, S_5) is produced. The bit-in-error decoder receives the syndrome 11100 (S_0, S_1, S_2, S_3, S_4) which it decodes as a single error in data bit 0 and inverts that bit. Figure 8 indicates a method for inhibiting correction when a multiple error occurs.

DATA								CHECK BITS							
$BYTE_7$	$BYTE_6$	$BYTE_5$	$BYTE_4$	$BYTE_3$	$BYTE_2$	$BYTE_1$	$BYTE_0$	C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7
63 56	55 48	47 40	39 32	31 24	23 16	15 8	7 0								

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Uses Modified Hamming Code 64/72
32 Data Bits with 8 Check Bits

Figure 6. 64-Bit Data Format

					Hex	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
	Syndrome Bits				S_7	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
					S_6	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
					S_5	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
					S_4	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
Hex	S_3	S_2	S_1	S_0																	
0	0	0	0	0		*	C4	C5	T	C6	T	T	62	C7	T	T	46	T	M	M	T
1	0	0	0	1		C0	T	T	14	T	M	M	T	T	M	M	T	M	T	T	30
2	0	0	1	0		C1	T	T	M	T	34	56	T	T	50	40	T	M	T	T	M
3	0	0	1	1		T	18	8	T	M	T	T	M	M	T	T	M	T	2	24	T
4	0	1	0	0		C2	T	T	15	T	35	57	T	T	51	41	T	M	T	T	31
5	0	1	0	1		T	19	9	T	M	T	T	63	M	T	T	47	T	3	25	T
6	0	1	1	0		T	20	10	T	M	T	T	M	M	T	T	M	T	4	26	T
7	0	1	1	1		M	T	T	M	T	36	58	T	T	52	42	T	M	T	T	M
8	1	0	0	0		C3	T	T	M	T	37	59	T	T	53	43	T	M	T	T	M
9	1	0	0	1		T	21	11	T	M	T	T	M	M	T	T	M	T	5	27	T
A	1	0	1	0		T	22	12	T	33	T	T	M	49	T	T	M	T	6	28	T
B	1	0	1	1		17	T	T	M	T	38	60	T	T	54	44	T	1	T	T	M
C	1	1	0	0		T	23	13	T	M	T	T	M	M	T	T	M	T	7	29	T
D	1	1	0	1		M	T	T	M	T	39	61	T	T	55	45	T	M	T	T	M
E	1	1	1	0		16	T	T	M	T	M	M	T	T	M	M	T	0	T	T	M
F	1	1	1	1		T	M	M	T	32	T	T	M	48	T	T	M	T	M	M	T

NOTES:
* = No errors detected
Number = The number of the single bit-in-error
T = Two errors detected
M = Three or more errors detected

2595 tbl 13

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Table 11. Syndrome Decode to Bit-In-Error (64-Bit Configuration)

64-Bit Propagation Delay		Component Delay From IDT39C60 AC Specifications
From	To	
DATA	Check Bits Out	(DATA to SC) + (XOR Delay)
DATA	Corrected $DATA_{OUT}$	(DATA to SC) + (XOR Delay) + (Buffer Delay) + (CB to DATA, CODE ID 1xx)
DATA	Syndromes	(DATA to SC) + (XOR Delay)
DATA	$\overline{ERROR}$ for 64 Bits	(DATA to SC) + (XOR Delay) + (NOR Delay)
DATA	$\overline{MULT ERROR}$ for 64 Bits	(DATA to SC) + (XOR Delay) + (Buffer Delay) + (CB to $\overline{MULT ERROR}$, CODE ID 1xx)
DATA	DOUBLE ERROR for 64 Bits	(DATA to SC) + (XOR Delay) + (XOR/NOR Delay)

2595 tbl 14

Table 12. Key AC Calculations for the 64-Bit Configuration

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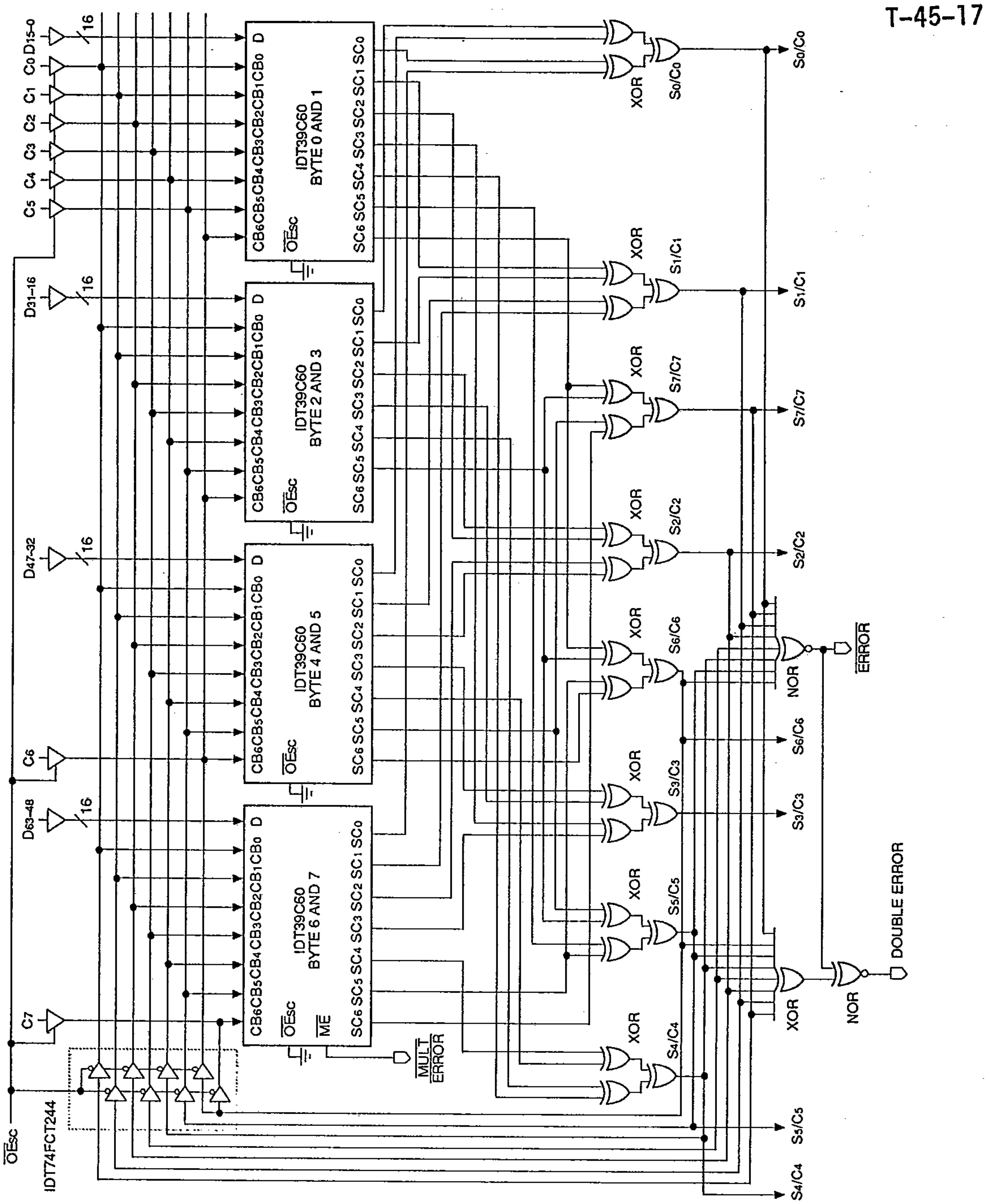

NOTES:
1. In PASSTHRU mode the contents of the Check Latch appears on the XOR outputs inverted.
2. In Diagnostic Generate mode the contents of the Diagnostic Latch appear on the XOR outputs inverted.

Figure 7. 64-Bit Configuration

Generated Check Bits	Parity	Participating Data Bits(1)															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
C_0	Even (XOR)		X	X	X		X			X	X		X			X	
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)	X	X	X	X	X	X	X	X								
C_7	Even (XOR)	X	X	X	X	X	X	X	X								

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Generated Check Bits	Parity	Participating Data Bits(1)															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
C_0	Even (XOR)		X	X	X		X			X	X		X			X	
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)									X	X	X	X	X	X	X	X
C_7	Even (XOR)									X	X	X	X	X	X	X	X

2595 tbl 16

Generated Check Bits	Parity	Participating Data Bits(1)															
		32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
C_0	Even (XOR)	X				X		X	X			X		X	X		X
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)	X	X	X	X	X	X	X	X								
C_7	Even (XOR)									X	X	X	X	X	X	X	X

2595 tbl 17

Generated Check Bits	Parity	Participating Data Bits(1)															
		48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
C_0	Even (XOR)	X				X		X	X			X		X	X		X
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)									X	X	X	X	X	X	X	X
C_7	Even (XOR)	X	X	X	X	X	X	X	X								

2595 tbl 18

NOTE:
1. The check bit is generated as either an XOR or XNOR of the 32 data bits noted by an "X" in the table.

Table 13. 64-Bit Modified Hamming Code — Check Bit Encode Chart

Data Bit	Internal Function
0	Diagnostic Check Bit$_0$
1	Diagnostic Check Bit$_1$
2	Diagnostic Check Bit$_2$
3	Diagnostic Check Bit$_3$
4	Diagnostic Check Bit$_4$
5	Diagnostic Check Bit$_5$
6, 7	Don't Care
8	Slice 0/1 — CODE ID$_0$
9	Slice 0/1 — CODE ID$_1$
10	Slice 0/1 — CODE ID$_2$
11	Slice 0/1 — DIAG MODE$_0$
12	Slice 0/1 — DIAG MODE$_1$
13	Slice 0/1 — CORRECT
14	Slice 0/1 — PASSTHRU
15	Don't Care
16-23	Don't Care
24	Slice 2/3 — CODE ID$_0$
25	Slice 2/3 — CODE ID$_1$
26	Slice 2/3 — CODE ID$_2$
27	Slice 2/3 — DIAG MODE$_0$
28	Slice 2/3 — DIAG MODE$_1$
29	Slice 2/3 — CORRECT
30	Slice 2/3 — PASSTHRU
31	Don't Care
32-37	Don't Care
38	Diagnostic Check Bit$_6$
39	Don't Care
40	Slice 4/5 — CODE ID$_0$
41	Slice 4/5 — CODE ID$_1$
42	Slice 4/5 — CODE ID$_2$
43	Slice 4/5 — DIAG MODE$_0$
44	Slice 4/5 — DIAG MODE$_1$
45	Slice 4/5 — CORRECT
46	Slice 4/5 — PASSTHRU
47	Don't Care
48-54	Don't Care
55	Diagnostic Check Bit$_7$
56	Slice 6/7 — CODE ID$_0$
57	Slice 6/7 — CODE ID$_1$
58	Slice 6/7 — CODE ID$_2$
59	Slice 6/7 — DIAG MODE$_0$
60	Slice 6/7 — DIAG MODE$_1$
61	Slice 6/7 — CORRECT
62	Slice 6/7 — PASSTHRU
63	Don't Care

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2595 tbl 20

Table 14. Diagnostic Latch Loading — 64-Bit Format

Some multiple errors will cause a data bit to be inverted. For example, in the 16-bit mode where bits 8 and 13 are in error, the syndrome 111100 (S_0, S_1, S_2, S_3, S_4, S_5) is produced. The bit-in-error decoder receives the syndrome 11100 (S_0, S_1, S_2, S_3, S_4) which it decodes as a single error in data bit 0 and inverts that bit. Figure 8 indicates a method for inhibiting correction when a multiple error occurs.

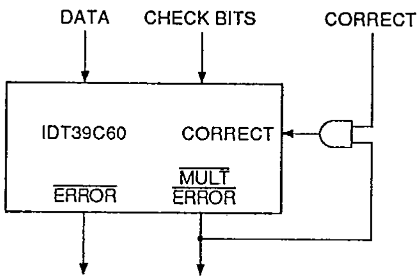

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Figure 8. Inhibition of Data Modification

FUNCTIONAL EQUATIONS

The following equations and tables describe in detail how the output values of the IDT39C60 EDC are determined as a function of the value of the inputs and the internal states. Be sure to carefully read the following definitions of symbols before examining the tables.

T-45-17

DEFINITIONS

$D_I \leftarrow$ DATAI if LE_{IN} is HIGH or the output of bit I of the Data Input Latch if LE_{IN} is LOW
$C_I \leftarrow$ CBI if LE_{IN} is HIGH or the output of bit I of the Check Bit Latch if LE_{IN} is LOW
$DL_I \leftarrow$ Output of bit I of the Diagnostic Latch
$S_I \leftarrow$ Internally generated syndromes (same as outputs of SCI if outputs enabled)

$PA \leftarrow D_0 \oplus D_1 \oplus D_2 \oplus D_4 \oplus D_6 \oplus D_8 \oplus D_{10} \oplus D_{12}$

$PB \leftarrow D_0 \oplus D_1 \oplus D_2 \oplus D_3 \oplus D_4 \oplus D_5 \oplus D_6 \oplus D_7$

$PC \leftarrow D_8 \oplus D_9 \oplus D_{10} \oplus D_{11} \oplus D_{12} \oplus D_{13} \oplus D_{14}$

$PD \leftarrow D_0 \oplus D_3 \oplus D_4 \oplus D_7 \oplus D_9 \oplus D_{10} \oplus D_{13} \oplus D_{15}$

$PE \leftarrow D_0 \oplus D_1 \oplus D_5 \oplus D_6 \oplus D_7 \oplus D_{11} \oplus D_{12} \oplus D_{13}$

$PF \leftarrow D_2 \oplus D_3 \oplus D_4 \oplus D_5 \oplus D_6 \oplus D_{14} \oplus D_{15}$

$PG_1 \leftarrow D_1 \oplus D_4 \oplus D_6 \oplus D_7$

$PG_2 \leftarrow D_1 \oplus D_2 \oplus D_3 \oplus D_5$

$PG_3 \leftarrow D_8 \oplus D_9 \oplus D_{11} \oplus D_{14}$

$PG_4 \leftarrow D_{10} \oplus D_{12} \oplus D_{13} \oplus D_{15}$

Error Signals

$\overline{ERROR}: \leftarrow \overline{(\overline{S6} \cdot \overline{(ID1 + ID2)}) \cdot \overline{S5} \cdot \overline{S4} \cdot \overline{S3} \cdot \overline{S2} \cdot \overline{S1} \cdot \overline{S0}} + GENERATE + INITIALIZE + PASSTHRU$

$\overline{MULT\ ERROR}$:
(16 and 32-Bit Modes) $\leftarrow \overline{((S6 \cdot ID1) \oplus S5 \oplus S4 \oplus S3 \oplus S2 \oplus S1 \oplus S0)\ (ERROR)} + TOME + GENERATE + PASSTHRU + INITIALIZE$

$\overline{MULT\ ERROR}$: (64-Bit Modes) $\leftarrow \overline{TOME} + GENERATE + PASSTHRU + INITIALIZE$

				Hex	0		1		2		3		4		5		6		7	
	Syndrome[1, 2] Bits			S6	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
				S5	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
				S4	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
				S3	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
Hex	S2	S1	S0																	
0 8	0	0	0									1		1	1		1			1
1 9	0	0	1			1			1			1	1	1	1		1		1	1
2 A	0	1	0				1				1	1	1						1	1
3 B	0	1	1		1						1	1	1						1	1
4 C	1	0	0			1						1	1	1						1
5 D	1	0	1		1	1						1	1	1						1
6 E	1	1	0		1			1		1	1	1	1			1		1	1	
7 F	1	1	1		1			1		1	1	1	1			1		1	1	1

NOTES:
1. $S_6, S_5, \ldots S_0$ are internal syndromes except in Modes 010, 100, 101, 110, 111 (CODE ID_2, ID_1, ID_0). In these modes, the syndromes are input over the check bit lines. $S_6 \leftarrow C_6$, $S_5 \leftarrow C_5$, ... $S_1 \leftarrow C_1$, $S_0 \leftarrow C_0$.
2. The S_6 internal syndrome is always forced to 0 in CODE ID 000.

2595 tbl 21

Table 15. TOME (Three or More Errors)

Generate Mode (Check Bits)	CODE ID_{0-2}						
	000	010	011	100	101	110	111
$SC_0 \leftarrow$	$PG_2 \oplus PG_3$	$PG_1 \oplus PG_3$	$PG_2 \oplus PG_4 \oplus CB_0$	$PG_2 \oplus PG_3$	$PG_2 \oplus PG_3$	$PG_1 \oplus PG_4$	$PG_1 \oplus PG_4$
$SC_1 \leftarrow$	PA	PA	$PA \oplus CB_1$	PA	PA	PA	PA
$SC_2 \leftarrow$	$\overline{PD}$	$\overline{PD}$	$PD \oplus CB_2$	$\overline{PD}$	PD	PD	PD
$SC_3 \leftarrow$	$\overline{PE}$	$\overline{PE}$	$PE \oplus CB_3$	$\overline{PE}$	PE	PE	PE
$SC_4 \leftarrow$	PF	PF	$PF \oplus CB_4$	PF	PF	PF	PF
$SC_5 \leftarrow$	PC	PC	$PC \oplus CB_5$	PC	PC	PC	PC
$SC_6 \leftarrow$	1	PB	$PC \oplus CB_6$	PB	PB	PB	PB

2595 tbl 22

Table 16. Generate Mode (Check Bits)

T-45-17

Detect and Correct Modes (Syndromes)	CODE ID_{0-2}						
	000	010	011 [1]	100	101	110	111
$SC_0 \leftarrow$	$PG_2 \oplus PG_3 \oplus C_0$	$PG_1 \oplus PG_3 \oplus C_0$	$PG_2 \oplus PG_4 \oplus CB_0$	$PG_2 \oplus PG_3 \oplus C_0$	$PG_2 \oplus PG_3$	$PG_1 \oplus PG_4$	$PG_1 \oplus PG_4$
$SC_1 \leftarrow$	$PA \oplus C_1$	$PA \oplus C_1$	$PA \oplus CB_1$	$PA \oplus C_1$	PA	PA	PA
$SC_2 \leftarrow$	$\overline{PD} \oplus C_2$	$\overline{PD} \oplus C_2$	$PD \oplus CB_2$	$\overline{PD} \oplus C_2$	PD	PD	PD
$SC_3 \leftarrow$	$\overline{PE} \oplus C_3$	$\overline{PE} \oplus C_3$	$PE \oplus CB_3$	$\overline{PE} \oplus C_3$	PE	PE	PE
$SC_4 \leftarrow$	$PF \oplus C_4$	$PF \oplus C_4$	$PF \oplus CB_4$	$PF \oplus C_4$	PF	PF	PF
$SC_5 \leftarrow$	$PC \oplus C_5$	$PC \oplus C_5$	$PC \oplus CB_5$	$PC \oplus C_5$	PC	PC	PC
$SC_6 \leftarrow$	1	$PB \oplus C_6$	$PC \oplus CB_6$	PB	PB	$PB \oplus C_6$	$PB \oplus C_6$

NOTE:
1. In CODE ID_{2-0} 011 the Check Bit Latch is forced transparent; the Data Latch operates normally.

2595 tbl 23

Table 17. Detect and Correct Modes (Syndromes)

Diagnostic Detect and Correct Mode	CODE ID_{0-2}						
	000	010	011 [1]	100	101	110	111
$SC_0 \leftarrow$	$PG_2 \oplus PG_3 \oplus DL_0$	$PG_1 \oplus PG_3 \oplus DL_0$	$PG_2 \oplus PG_4 \oplus CB_0$	$PG_2 \oplus PG_3 \oplus DL_0$	$PG_2 \oplus PG_3$	$PG_1 \oplus PG_4$	$PG_1 \oplus PG_4$
$SC_1 \leftarrow$	$PA \oplus DL_1$	$PA \oplus DL_1$	$PA \oplus CB_1$	$PA \oplus DL_1$	PA	PA	PA
$SC_2 \leftarrow$	$\overline{PD} \oplus DL_2$	$\overline{PD} \oplus DL_2$	$PD \oplus CB_2$	$\overline{PD} \oplus DL_2$	PD	PD	PD
$SC_3 \leftarrow$	$\overline{PE} \oplus DL_3$	$\overline{PE} \oplus DL_3$	$PE \oplus CB_3$	$\overline{PE} \oplus DL_3$	PE	PE	PE
$SC_4 \leftarrow$	$PF \oplus DL_4$	$PF \oplus DL_4$	$PF \oplus CB_4$	$PF \oplus DL_4$	PF	PF	PF
$SC_5 \leftarrow$	$PDL \oplus DL_5$	$PC \oplus DL_5$	$PC \oplus CB_5$	$PC \oplus DL_5$	PC	PC	PC
$SC_6 \leftarrow$	1	$PB \oplus DL_6$	$PC \oplus CB_6$	PB	PB	$PB \oplus DL_6$	$PB \oplus DL_7$

NOTE:
1. In CODE ID_{2-0} 011 the Check Bit Latch is forced transparent; the Data Latch operates normally.

2595 tbl 24

Table 18. Diagnostic Detect and Correct Mode

Diagnostic Generate Mode	CODE ID_{0-2}						
	000	010	011 [1]	100	101	110	111
$SC_0 \leftarrow$	DL_0	DL_0	CB_0	DL_0	1	1	1
$SC_1 \leftarrow$	DL_1	DL_1	CB_1	DL_1	1	1	1
$SC_2 \leftarrow$	DL_2	DL_2	CB_2	DL_2	1	1	1
$SC_3 \leftarrow$	DL_3	DL_3	CB_3	DL_3	1	1	1
$SC_4 \leftarrow$	DL_4	DL_4	CB_4	DL_4	1	1	1
$SC_5 \leftarrow$	DL_5	DL_5	CB_5	DL_5	1	1	1
$SC_6 \leftarrow$	1	DL_6	CB_6	1	1	DL_6	DL_7

NOTE:
1. In CODE ID_{2-0} 011 the Check Bit Latch is forced transparent; the Data Latch operates normally.

2595 tbl 25

Table 19. Diagnostic Generate Mode

PASSTHRU Mode	CODE ID_{0-2}						
	000	010	011 [1]	100	101	110	111
$SC_0 \leftarrow$	C_0	C_0	CB_0	C_0	1	1	1
$SC_1 \leftarrow$	C_1	C_1	CB_1	C_1	1	1	1
$SC_2 \leftarrow$	C_2	C_2	CB_2	C_2	1	1	1
$SC_3 \leftarrow$	C_3	C_3	CB_3	C_3	1	1	1
$SC_4 \leftarrow$	C_4	C_4	CB_4	C_4	1	1	1
$SC_5 \leftarrow$	C_5	C_5	CB_5	C_5	1	1	1
$SC_6 \leftarrow$	1	C_6	CB_6	1	1	C_6	C_6

NOTE:
1. In CODE ID_{2-0} 011 the Check Bit Latch is forced transparent; the Data Latch operates normally.

2595 tbl 26

Table 20. PASSTHRU Mode

		S5	0	0	0	0	1	1	1	1
		S4	0	0	1	1	0	0	1	1
S2	S1	S3	0	1	0	1	0	1	0	1
0	0		—	—	—	5	—	11	14	—
0	1		—	1	2	6	8	12	—	—
1	0		—	—	3	7	9	13	15	—
1	1		—	0	4	—	10	—	—	—

NOTE:
1. Unlisted S combinations are no correction.

2595 tbl 27

Table 21. CODE ID_{2-0} = 000

		C6	0	0	0	0	1	1	1	1
		C5	1	1	1	1	0	0	0	0
		C4	0	0	1	1	0	0	1	1
C2	C1	C3	0	1	0	1	0	1	0	1
0	0		—	11	14	—	—	—	—	5
0	1		8	12	—	—	—	1	2	6
1	0		9	13	15	—	—	—	3	7
1	1		10	—	—	—	—	0	4	—

NOTE:
1. Unlisted Cn combinations are no correction.

2595 tbl 28

Table 22. CODE ID_{2-0} = 010

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		S6	0	0	0	0	1	1	1	1
		S5	0	0	0	0	1	1	1	1
		S4	0	0	1	1	0	0	1	1
S2	S1	S3	0	1	0	1	0	1	0	1
0	0		—	—	—	5	—	11	14	—
0	1		—	1	2	6	8	12	—	—
1	0		—	—	3	7	9	13	15	—
1	1		—	0	4	—	10	—	—	—

NOTE:
1. Unlisted S combinations are no correction.

2595 tbl 29

Table 23. CODE ID_{2-0} = 011

		C0	0	0	0	0	1	1	1	1
		C6	0	0	0	0	1	1	1	1
		C5	1	1	1	1	0	0	0	0
		C4	0	0	1	1	0	0	1	1
C2	C1	C3	0	1	0	1	0	1	0	1
0	0		—	11	14	—	—	—	—	5
0	1		8	12	—	—	—	1	2	6
1	0		9	13	15	—	—	—	3	7
1	1		10	—	—	—	—	0	4	—

NOTE:
1. Unlisted Cn combinations are no correction.

2595 tbl 30

Table 24. CODE ID_{2-0} = 100

5

		C0	0	0	0	0	1	1	1	1
		C6	0	0	0	0	1	1	1	1
		C5	0	0	0	0	1	1	1	1
		C4	0	0	1	1	0	0	1	1
C2	C1	C3	0	1	0	1	0	1	0	1
0	0		—	—	—	5	—	11	14	—
0	1		—	1	2	6	8	12	—	—
1	0		—	—	3	7	9	13	15	—
1	1		—	0	4	—	10	—	—	—

NOTE:
1. Unlisted Cn combinations are no correction.

2595 tbl 31

Table 25. CODE ID_{2-0} = 101

		C0	0	0	0	0	1	1	1	1
		C6	1	1	1	1	0	0	0	0
		C5	0	0	0	0	1	1	1	1
		C4	0	0	1	1	0	0	1	1
C2	C1	C3	0	1	0	1	0	1	0	1
0	0		—	—	—	5	—	11	14	—
0	1		—	1	2	6	8	12	—	—
1	0		—	—	3	7	9	13	15	—
1	1		—	0	4	—	10	—	—	—

NOTE:
1. Unlisted Cn combinations are no correction.

2595 tbl 32

Table 26. CODE ID_{2-0} = 110

		C0	0	0	0	0	1	1	1	1
		C6	1	1	1	1	0	0	0	0
		C5	1	1	1	1	0	0	0	0
		C4	0	0	1	1	0	0	1	1
C2	C1	C3	0	1	0	1	0	1	0	1
0	0		—	11	14	—	—	—	—	5
0	1		8	12	—	—	—	1	2	6
1	0		9	13	15	—	—	—	3	7
1	1		10	—	—	—	—	0	4	—

NOTE:
1. Unlisted Cn combinations are no correction.

2595 tbl 33

Table 27. CODE ID_{2-0} = 111

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to Ground	−0.5 to V_{CC} + 0.5	−0.5 to V_{CC} + 0.5	V
V_{CC}	Power Supply Voltage	−0.5 to +7.0	−0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	−55 to +125	°C
T_{BIAS}	Temperature Under Bias	−55 to +125	−65 to +135	°C
T_{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
I_{OUT}	DC Output Current	30	30	mA

NOTE: 2595 tbl 34
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE: 2595 tbl 35
1. This parameter is sampled and not 100% tested.

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DC ELECTRICAL CHARACTERISTICS

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10%
V_{LC} = 0.2V; V_{HC} = V_{CC} − 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level[4]		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level[4]		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	0.1	10	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	−0.1	−10	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = −300µA	V_{HC}	V_{CC}	—	V
			I_{OH} = −6mA MIL.	2.4	4.3	—	
			I_{OH} = −6mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 300µA	—	GND	V_{LC}	V
			I_{OL} = 8mA MIL.	—	0.3	0.5	
			I_{OL} = 8mA COM'L.	—	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0V	—	−0.1	−20	µA
			V_O = V_{CC} (Max.)	—	0.1	20	
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0V[3]		−20	—	—	mA

NOTES: 2595 tbl 36
1. For conditions shown as Max. or Min. use appropriate value specified under DC Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These input levels should only be static tested in a noise-free environment. Guaranteed by design.

DC ELECTRICAL CHARACTERISTICS (Cont'd.)

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Commercial: $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$; Military: $T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$
$V_{LC} = 2.0V$; $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CCQ}	Quiescent Power Supply Current (CMOS) Inputs	V_{CC} = Max. $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$ $f_{OP} = 0$		—	3.0	5.0	mA
I_{CCT}	Quiescent Input Power Supply Current (per Input @ TTL High)[3]	V_{CC} = Max., V_{IN} = 3.4V, f_{OP} = 0		—	0.3	0.5	mA/ Input
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$ Outputs Open, $\overline{OE}$ = L	MIL.	—	5.0	8.5	mA/ MHz
			COM'L.	—	5.0	7.0	
I_{CC}	Total Power Supply Current[4]	V_{CC} = Max., f_{OP} = 10MHz Outputs Open, $\overline{OE}$ = L 50% Duty Cycle $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$	MIL.	—	53	90	mA
			COM'L.	—	53	75	
		V_{CC} = Max., f_{OP} = 10MHz Outputs Open, $\overline{OE}$ = L 50% Duty Cycle V_{IN} = 3.4V, V_{IN} = 0.4V	MIL.	—	60	100	
			COM'L.	—	60	85	

2595 tbl 37

NOTES:
1. For conditions shown as Max. or Min. use appropriate value specified under DC Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. I_{CCT} is derived by measuring the total current with all the inputs tied together at 3.4V, subtracting out I_{CCQ}, then dividing by the total number of inputs.
4. Total Supply Current is the sum of the Quiescent Current and the Dynamic Current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:
   $I_{CC} = I_{CCQ} + I_{CCT} (N_T \times D_H) + I_{CCD} (f_{OP})$
   D_H = Data duty cycle TTL high period (V_{IN} = 3.4V)
   N_T = Number of dynamic inputs driven at TTL levels
   f_{OP} = Operating frequency

5

CMOS TESTING CONSIDERATIONS

Special test board considerations must be taken into account when applying high-speed CMOS products to the automatic test environment. Large output currents are being switched in very short periods and proper testing demands that test set-ups have minimized inductance and guaranteed zero voltage grounds. The techniques listed below will assist the user in obtaining accurate testing results:

1) All input pins should be connected to a voltage potential during testing. If left floating, the device may oscillate, causing improper device operation and possible latchup.
2) Placement and value of decoupling capacitors is critical. Each physical set-up has different electrical characteristics and it is recommended that various decoupling capacitor sizes be experimented with. Capacitors should be positioned using the minimum lead lengths. They should also be distributed to decouple power supply lines and be placed as close as possible to the DUT power pins.
3) Device grounding is extremely critical for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is necessary. The ground plane must be sustained from the performance board to the DUT interface board and wiring unused interconnect pins to the ground plane is recommended. Heavy gauge stranded wire should be used for power wiring, with twisted pairs being recommended for minimized inductance.
4) To guarantee data sheet compliance, the input thresholds should be tested per input pin in a static environment. To allow for testing and hardware-induced noise, IDT recommends using $V_{IL} \leq 0V$ and $V_{IH} \geq 3V$ for AC tests.

IDT 39C60B AC ELECTRICAL CHARACTERISTICS

T-45-17

Temperature range: –55°C to +125°C; VCC = 5.0V ± 10%
The inputs switch between 0V to 3V with signal measured at the 1.5V level.

MAXIMUM PROPAGATION DELAYS C_L = 50pF

	From Input		To Output SC$_{0-7}$	DATA$_{0-31}$	ERROR	MULT ERROR	Unit
	DATA$_{0-15}$		22	30 (1)	22	25	ns
	CB$_{0-7}$ (CODE ID$_{1,0}$ = 00, 11)		14	26	20	24	ns
	CB$_{0-7}$ (CODE ID$_{1,0}$ = 10)		14	19	20	24	ns
	GENERATE	↓	15	—	↑ ↓ 14	↑ ↓ 19	ns
	CORRECT Not Internal Control Mode		—	20	—	—	ns
	DIAG MODE and PASSTHRU Not Internal Control Mode		24	26	19	21	ns
	CODE ID$_{1,0}$		24	29	26	29	ns
	LE$_{IN}$ From latched to transparent	↑	24	34	24	26	ns
	LE$_{OUT}$ From latched to transparent	↑	—	13	—	—	ns
	LE$_{DIAG}$ From latched to transparent	↑	24	34	24	26	ns
Internal Control Mode	LE$_{DIAG}$ From latched to transparent	↑	29	40	29	32	ns
Internal Control Mode	DATA$_{0-15}$ Via Diagnostic Latch		29	40	29	32	ns

2595 tbl 38

MINIMUM SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input		To Input (Latching Data)		Set-up Time	Hold Time	Unit
DATA$_{0-15}$		↓	LE$_{IN}$	6	4	ns
CB$_{0-7}$ (not applic. to CODE ID$_{1,0}$ = 11)		↓		6	4	ns
DATA$_{0-15}$		↓	LE$_{OUT}$	29	2	ns
CB$_{0-7}$ (CODE ID 00, 11)		↓		25	0	ns
CB$_{0-7}$ (CODE ID 10)		↓		25	0	ns
CORRECT	↑	↓		26	—	ns
DIAG MODE		↓		26	0	ns
CODE ID$_{1,0}$		↓		30	0	ns
LE$_{IN}$	↑	↓		34	—	ns
DATA$_{0-15}$			LE$_{DIAG}$	6	4	ns

2595 tbl 39

MAXIMUM OUTPUT ENABLE/DISABLE TIMES

Output tests specified with C_L = 5pF and measured to 0.5V change of output voltage level. Test performed with C_L = 50pF and correlated to C_L = 5pF.

From Input	Enable	Disable	To Output	Enable Max.	Disable Max.	Unit
OE Byte$_{0-3}$	↓	↑	DAT$_{0-15}$	15	12	ns
OE$_{SC}$	↓	↑	SC$_{0-7}$	15	12	ns

2595 tbl 40

MINIMUM PULSE WIDTHS

			Min.	
LE$_{IN}$, LE$_{OUT}$, LE$_{DIAG}$	↑↓	(Positive-going pulse)	10	ns

2595 tbl 41

IDT39C60B AC ELECTRICAL CHARACTERISTICS

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(Guaranteed Commercial Range Performance)

The tables below specify the guaranteed performance of the IDT39C60B over the commercial operating range of 0°C to +70°C, with V_{CC} from 4.75V to 5.25V. All data are in nanoseconds, with inputs switching between 0V and 3V at 1V per nanosecond and measurements made at 1.5V.

MAXIMUM COMBINATIONAL PROPAGATION DELAYS $C_L = 50pF$

From Input	To Output: SC_{0-6}	$DATA_{0-15}$	$\overline{ERROR}$	$\overline{MULT\ ERROR}$
$DATA_{0-15}$	18	25 (1)	18	20
CB_{0-6} (CODE ID_{2-0} 000, 011)	12	22	17	20
CB_{0-6} (CODE ID_{2-0} 010, 100, 101, 110, 111)	12	16	17	20
$\overline{GENERATE}$	13	—	—	—
CORRECT (Not Internal Control Mode)	—	17	—	—
DIAG MODE (Not Internal Control Mode)	20	22	16	19
PASSTHRU (Not Internal Control Mode)	20	22	16	19
CODE ID_{1-0}	20	22	22	24
LE_{IN} (From latched to transparent)	20	28	20	22
LE_{OUT} (From latched to transparent)	—	11	—	—
LE_{DIAG} (From latched to transparent; Not Internal Control Mode)	20	28	20	22
Internal Control Mode: LE_{DIAG} (From latched to transparent)	24	33	24	27
Internal Control Mode: $DATA_{0-15}$ (Via Diagnostic Latch)	24	33	24	27

2595 tbl 42

NOTE:
1. $DATA_{IN}$ to corrected $DATA_{OUT}$ measurement requires timing as shown below.

MINIMUM SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input	To (Latching Data)	Set-up Time	Hold Time
$DATA_{0-15}$	LE_{IN}	5	3
CB_{0-6}	LE_{IN}	5	3
$DATA_{0-15}$	LE_{OUT}	24	2
CB_{0-6} (CODE ID 000, 011)	LE_{OUT}	21	0
CB_{0-6} (CODE ID 010, 100, 101, 110, 111)	LE_{OUT}	21	0
CORRECT	LE_{OUT}	22	0
DIAG MODE	LE_{OUT}	22	0
PASSTHRU	LE_{OUT}	22	0
CODE ID_{2-0}	LE_{OUT}	25	0
LE_{IN}	LE_{OUT}	28	0
$DATA_{0-15}$	LE_{DIAG}	5	3

2595 tbl 43

MAXIMUM OUTPUT ENABLE/DISABLE TIMES

Output tests specified with C_L = 5pF and measured to 0.5V change of output voltage level. Test performed with C_L = 50pF and correlated to C_L = 5pF.

Input	Output	Enable Max.	Disable Max.
$\overline{OE}$ $BYTE_0$, $\overline{OE}$ $BYTE_1$	$DATA_{0-15}$	12	10
$\overline{OE}_{SC}$	SC_{0-6}	12	10

2595 tbl 44

MINIMUM PULSE WIDTHS

LE_{IN}, LE_{OUT}, LE_{DIAG}	8

2595 tbl 45

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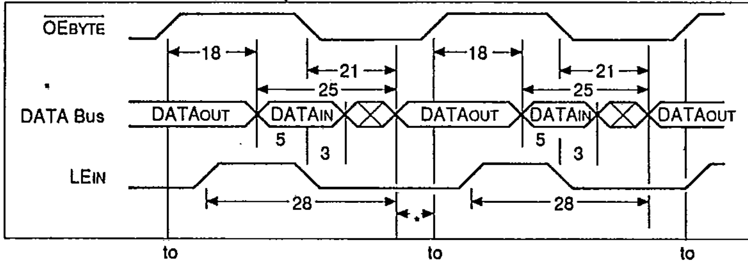
IDT39C60B COMMERCIAL — DATAIN TO CORRECTED DATAOUT TIMING (Two cycles shown)



NOTES:
Device Mode = "Correct"
System Type = "Correct Always"
Min. Period = 51ns (fMAX = 19.6MHz)

Timing Parameter From / To	Min./Max.
OEBYTE = High to DATAOUT Disabled	Max.
OEBYTE = Low to DATAOUT Enabled	Max.
DATAIN to Corrected DATAOUT	Max.
DATAIN Set-up to LEIN = Low	Min.
DATAIN Hold to LEIN = Low	Min.
LEIN = High to DATAOUT	Max.
* = (Memory/System dependent)	

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5

IDT39C60A AC ELECTRICAL CHARACTERISTICS

T-45-17

(Guaranteed Commercial Range Performance)

The tables below specify the guaranteed performance of the IDT39C60A over the commercial operating range of 0°C to +70°C, with Vcc from 4.75V to 5.25V. All data are in nanoseconds, with inputs switching between 0V and 3V at 1V per nanosecond and measurements made at 1.5V.

MAXIMUM COMBINATIONAL PROPAGATION DELAYS CL = 50pF

From Input	To Output			
	SC_{0-6}	$DATA_{0-15}$	$\overline{Error}$	$\overline{MULT\ ERROR}$
$DATA_{0-15}$	20	30(1)	20	23
CB_{0-6} (CODE ID_{2-0} 000, 011)	14	25	20	23
CB_{0-6} (CODE ID_{2-0} 010, 100, 101, 110, 111)	14	18	20	23
$\overline{GENERATE}$	15	—	—	—
CORRECT (Not Internal Control Mode)	—	20	—	—
DIAG MODE (Not Internal Control Mode)	22	25	18	21
PASSTHRU (Not Internal Control Mode)	22	25	18	21
CODE ID_{2-0}	23	28	25	28
LE_{IN} (From latched to transparent)	22	32	22	25
LE_{OUT} (From latched to transparent)	—	13	—	—
LE_{DIAG} (From latched to transparent; Not Internal Control Mode)	22	32	22	25
Internal Control Mode: LE_{DIAG} (From latched to transparent)	28	38	28	31
Internal Control Mode: $DATA_{0-15}$ (Via Diagnostic Latch)	28	38	28	31

2595 tbl 46

NOTE:
1. $DATA_{IN}$ to corrected $DATA_{OUT}$ measurement requires timing as shown below.

MINIMUM SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input	To (Latching Data)	Set-up Time	Hold Time
$DATA_{0-15}$	LE_{IN}	5	3
CB_{0-6}	LE_{IN}	5	3
$DATA_{0-15}$	LE_{OUT}	24	2
CB_{0-6} (CODE ID 000, 011)	LE_{OUT}	21	0
CB_{0-6} (CODE ID 010, 100, 101, 110, 111)	LE_{OUT}	21	0
CORRECT	LE_{OUT}	22	0
DIAG MODE	LE_{OUT}	22	0
PASSTHRU	LE_{OUT}	22	0
CODE ID_{2-0}	LE_{OUT}	25	0
LE_{IN}	LE_{OUT}	28	0
$DATA_{0-15}$	LE_{DIAG}	5	3

2595 tbl 47

MAXIMUM OUTPUT ENABLE/DISABLE TIMES

Output tests specified with CL = 5pF and measured to 0.5V change of output voltage level. Test performed with CL = 50pF and correlated to CL = 5pF.

Input	Output	Enable	Disable
$\overline{OE}$ $BYTE_0$, $\overline{OE}$ $BYTE_1$	$DATA_{0-15}$	24	21
$\overline{OE}_{SC}$	SC_{0-6}	24	21

2595 tbl 48

MINIMUM PULSE WIDTHS

LE_{IN}, LE_{OUT}, LE_{DIAG}	12

2595 tbl 49

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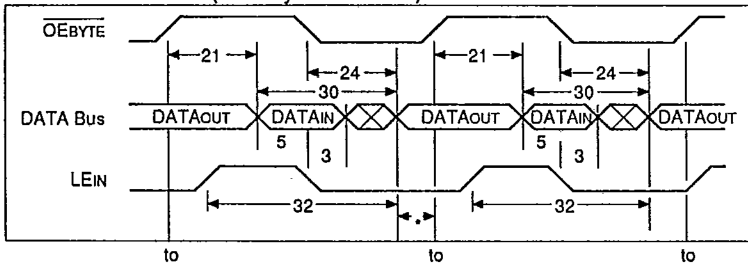
NOTES:
Device Mode = "Correct"
System Type = "Correct Always"
Min. Period = 61ns (f_{MAX} = 16.4MHz)

IDT39C60A COMMERCIAL — DATAIN TO CORRECTED DATAOUT TIMING (Two cycles shown)



Timing Parameter From To	Min./ Max.
OEBYTE = High to DATAOUT Disabled	Max.
OEBYTE = Low to DATAOUT Enabled	Max.
DATAIN to Corrected DATAOUT	Max.
DATAIN Set-up to LEIN = Low	Min.
DATAIN Hold to LEIN = Low	Min.
LEIN = High to DATAOUT	Max.
* = (Memory/System dependent)	

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IDT39C60A AC ELECTRICAL CHARACTERISTICS

T-45-17

(Guaranteed Military Range Performance)

The tables below specify the guaranteed performance of the IDT39C60A over the military operating range of –55°C to +125°C, with Vcc from 4.5V to 5.5V. All data are in nanoseconds, with inputs switching between 0V and 3V at 1V per nanosecond and measurements made at 1.5V.

MAXIMUM COMBINATIONAL PROPAGATION DELAYS $C_L = 50pF$

From Input	To Output: SC_{0-6}	$DATA_{0-15}$	$\overline{ERROR}$	$\overline{MULT\ ERROR}$
$DATA_{0-15}$	22	35(1)	24	27
CB_{0-6} (CODE ID_{2-0} 000, 011)	17	28	24	27
CB_{0-6} (CODE ID_{2-0} 010, 100, 101, 110, 111)	17	20	24	27
$\overline{GENERATE}$	20	—	—	—
CORRECT (Not Internal Control Mode)	—	25	—	—
DIAG MODE (Not Internal Control Mode)	25	28	21	24
PASSTHRU (Not Internal Control Mode)	25	28	21	24
CODE ID_{2-0}	26	31	28	31
LE_{IN} (From latched to transparent)	24	37	26	29
LE_{OUT} (From latched to transparent)	—	16	—	—
LE_{DIAG} (From latched to transparent; Not Internal Control Mode)	24	37	26	29
Internal Control Mode: LE_{DIAG} (From latched to transparent)	30	43	32	35
Internal Control Mode: $DATA_{0-15}$ (Via Diagnostic Latch)	30	43	32	35

2595 tbl 50

NOTE:
1. $DATA_{IN}$ to corrected $DATA_{OUT}$ measurement requires timing as shown below.

MINIMUM SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input	To (Latching Data)	Set-up Time	Hold Time
$DATA_{0-15}$	LE_{IN}	5	3
CB_{0-6}	LE_{IN}	5	3
$DATA_{0-15}$	LE_{OUT}	27	2
CB_{0-6} (CODE ID 000, 011)	LE_{OUT}	24	0
CB_{0-6} (CODE ID 010, 100, 101, 110, 111)	LE_{OUT}	24	0
CORRECT	LE_{OUT}	25	0
DIAG MODE	LE_{OUT}	25	0
PASSTHRU	LE_{OUT}	25	0
CODE ID_{2-0}	LE_{OUT}	28	0
LE_{IN}	LE_{OUT}	30	0
$DATA_{0-15}$	LE_{DIAG}	5	3

2595 tbl 51

MAXIMUM OUTPUT ENABLE/DISABLE TIMES

Output tests specified with C_L = 5pF and measured to 0.5V change of output voltage level. Test performed with C_L = 50pF and correlated to C_L = 5pF.

Input	Output	Enable	Disable
$\overline{OE}$ $BYTE_0$, $\overline{OE}$ $BYTE_1$	$DATA_{0-15}$	28	25
$\overline{OE}_{SC}$	SC_{0-6}	28	25

2595 tbl 52

MINIMUM PULSE WIDTHS

LE_{IN}, LE_{OUT}, LE_{DIAG}	12

2595 tbl 53

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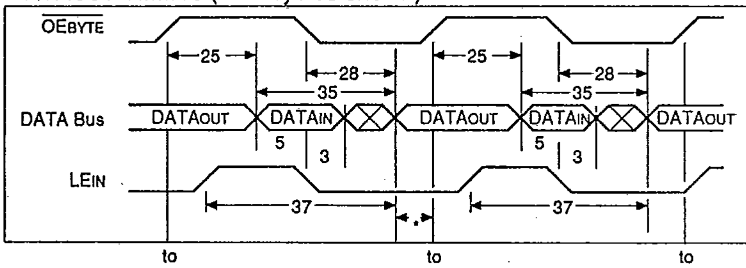
NOTES:
Device Mode = "Correct"
System Type = "Correct Always"
Min. Period = 70ns (f_{MAX} = 14.3MHz)

IDT39C60A MILITARY — DATAIN TO CORRECTED DATAOUT TIMING (Two cycles shown)



Timing Parameter From To	Min./ Max.
OEBYTE = High to DATAOUT Disabled	Max.
OEBYTE = Low to DATAOUT Enabled	Max.
DATAIN to Corrected DATAOUT	Max.
DATAIN Set-up to LEIN = Low	Min.
DATAIN Hold to LEIN = Low	Min.
LEIN = High to DATAOUT	Max.
* = (Memory/System dependent)	

2595 drw 14

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IDT39C60-1 AC ELECTRICAL CHARACTERISTICS

(Guaranteed Commercial Range Performance)

The tables below specify the guaranteed performance of the IDT39C60-1 over the commercial operating range of 0°C to +70°C, with Vcc from 4.75V to 5.25V. All data are in nanoseconds, with inputs switching between 0V and 3V at 1V per nanosecond and measurements made at 1.5V.

MAXIMUM COMBINATIONAL PROPAGATION DELAYS $C_L = 50pF$

From Input	To Output			
	SC_{0-6}	$DATA_{0-15}$	$\overline{ERROR}$	$\overline{MULT\ ERROR}$
$DATA_{0-15}$	28	52(1)	25	50
CB_{0-6} (CODE ID_{2-0} 000, 011)	23	50	23	47
CB_{0-6} (CODE ID_{2-0} 010, 100, 101, 110, 111)	28	34	29	34
$\overline{GENERATE}$	35	—	—	—
CORRECT (Not Internal Control Mode)	—	45	—	—
DIAG MODE (Not Internal Control Mode)	50	78	59	75
PASSTHRU (Not Internal Control Mode)	36	44	29	46
CODE ID_{2-0}	61	90	60	80
LE_{IN} (From latched to transparent)	39	72	39	59
LE_{OUT} (From latched to transparent)	—	31	—	—
LE_{DIAG} (From latched to transparent; Not Internal Control Mode)	45	78	45	65
Internal Control Mode: LE_{DIAG} (From latched to transparent)	67	96	66	86
Internal Control Mode: $DATA_{0-15}$ (Via Diagnostic Latch)	67	96	66	86

2595 tbl 54

NOTE:
1. $DATA_{IN}$ to corrected $DATA_{OUT}$ measurement requires timing as shown below.

MINIMUM SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input	To (Latching Data)	Set-up Time	Hold Time
$DATA_{0-15}$	LE_{IN}	6	7
CB_{0-6}	LE_{IN}	5	6
$DATA_{0-15}$	LE_{OUT}	34	5
CB_{0-6} (CODE ID 000, 011)	LE_{OUT}	35	0
CB_{0-6} (CODE ID 010, 100, 101, 110, 111)	LE_{OUT}	27	0
CORRECT	LE_{OUT}	26	1
DIAG MODE	LE_{OUT}	69	0
PASSTHRU	LE_{OUT}	26	0
CODE ID_{2-0}	LE_{OUT}	81	0
LE_{IN}	LE_{OUT}	51	5
$DATA_{0-15}$	LE_{DIAG}	6	8

2595 tbl 55

MAXIMUM OUTPUT ENABLE/DISABLE TIMES

Output tests specified with C_L = 5pF and measured to 0.5V change of output voltage level. Test performed with C_L = 50pF and correlated to C_L = 5pF.

Input	Output	Enable	Disable
$\overline{OE}$ $BYTE_0$, $\overline{OE}$ $BYTE_1$	$DATA_{0-15}$	30	30
$\overline{OE}_{SC}$	SC_{0-6}	30	30

2595 tbl 56

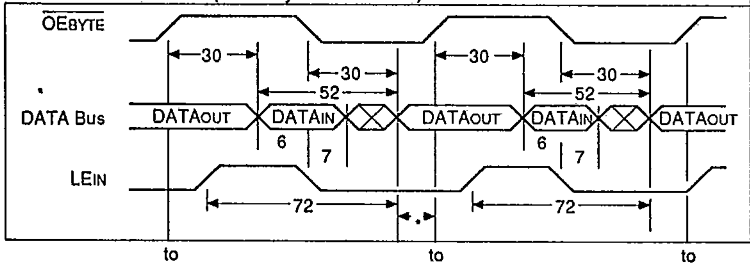
MINIMUM PULSE WIDTHS

LE_{IN}, LE_{OUT}, LE_{DIAG}	15

2595 tbl 57

NOTES:
Device Mode = "Correct"
System Type = "Correct Always"
Min. Period = 92ns (f_{MAX} = 10.9MHz)

IDT39C60–1 COMMERCIAL — DATAIN TO CORRECTED DATAOUT TIMING (Two cycles shown)



Timing Parameter From To	Min./Max.
OEBYTE = High to DATAOUT Disabled	Max.
OEBYTE = Low to DATAOUT Enabled	Max.
DATAIN to Corrected DATAOUT	Max.
DATAIN Set-up to LEIN = Low	Min.
DATAIN Hold to LEIN = Low	Min.
LEIN = High to DATAOUT	Max.
* = (Memory/System dependent)	

2595 drw 15

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IDT39C60-1 AC ELECTRICAL CHARACTERISTICS

(Guaranteed Military Range Performance)

The tables below specify the guaranteed performance of the IDT39C60-1 over the military operating range of –55°C to +125°C, with Vcc from 4.5V to 5.5V. All data are in nanoseconds, with inputs switching between 0V and 3V at 1V per nanosecond and measurements made at 1.5V.

MAXIMUM COMBINATIONAL PROPAGATION DELAYS $C_L = 50pF$

From Input	To Output			
	SC_{0-6}	$DATA_{0-15}$	$\overline{ERROR}$	$\overline{MULT\ ERROR}$
$DATA_{0-15}$	31	59(1)	28	56
CB_{0-6} (CODE ID_{2-0} 000, 011)	25	55	25	50
CB_{0-6} (CODE ID_{2-0} 010, 100, 101, 110, 111)	30	38	31	37
$\overline{GENERATE}$	38	—	—	—
CORRECT (Not Internal Control Mode)	—	49	—	—
DIAG MODE (Not Internal Control Mode)	58	89	65	90
PASSTHRU (Not Internal Control Mode)	39	51	34	54
CODE ID_{2-0}	69	100	68	90
LE_{IN} (From latched to transparent)	39	82	43	66
LE_{OUT} (From latched to transparent)	—	33	—	—
LE_{DIAG} (From latched to transparent; Not Internal Control Mode)	50	88	49	72
Internal Control Mode: LE_{DIAG} (From latched to transparent)	75	106	74	96
Internal Control Mode: $DATA_{0-15}$ (Via Diagnostic Latch)	75	106	74	96

2595 tbl 58

NOTE:
1. $DATA_{IN}$ to corrected $DATA_{OUT}$ measurement requires timing as shown below.

MINIMUM SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input	To (Latching Data)	Set-up Time	Hold Time
$DATA_{0-15}$	LE_{IN}	7	7
CB_{0-6}	LE_{IN}	5	7
$DATA_{0-15}$	LE_{OUT}	39	5
CB_{0-6} (CODE ID 000, 011)	LE_{OUT}	38	0
CB_{0-6} (CODE ID 010, 100, 101, 110, 111)	LE_{OUT}	30	0
CORRECT	LE_{OUT}	28	1
DIAG MODE	LE_{OUT}	84	0
PASSTHRU	LE_{OUT}	30	0
CODE ID_{2-0}	LE_{OUT}	89	0
LE_{IN}	LE_{OUT}	59	5
$DATA_{0-15}$	LE_{DIAG}	7	9

2595 tbl 59

MAXIMUM OUTPUT ENABLE/DISABLE TIMES

Output tests specified with $C_L = 5pF$ and measured to 0.5V change of output voltage level. Test performed with $C_L = 50pF$ and correlated to $C_L = 5pF$.

Input	Output	Enable	Disable
$\overline{OE}$ $BYTE_0$, $\overline{OE}$ $BYTE_1$	$DATA_{0-15}$	35	35
$\overline{OE}_{SC}$	SC_{0-6}	35	35

2595 tbl 60

MINIMUM PULSE WIDTHS

LE_{IN}, LE_{OUT}, LE_{DIAG}	15

2595 tbl 61

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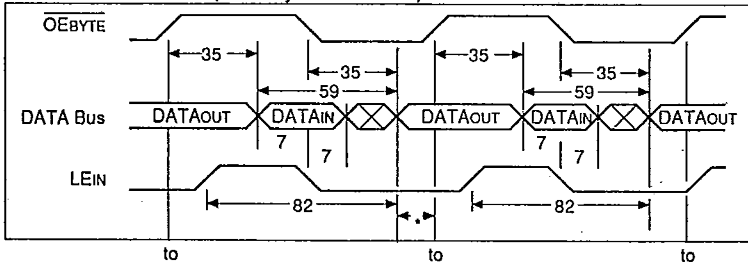
IDT39C60-1 MILITARY — DATAIN TO CORRECTED DATAOUT TIMING (Two cycles shown)



NOTES:
Device Mode = "Correct"
System Type = "Correct Always"
Min. Period = 104ns (fMAX = 9.6MHz)

Timing Parameter From To	Min./ Max.
OEBYTE = High to DATAOUT Disabled	Max.
OEBYTE = Low to DATAOUT Enabled	Max.
DATAIN to Corrected DATAOUT	Max.
DATAIN Set-up to LEIN = Low	Min.
DATAIN Hold to LEIN = Low	Min.
LEIN = High to DATAOUT	Max.

* = (Memory/System dependent)

2595 drw 16

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IDT39C60 AC ELECTRICAL CHARACTERISTICS

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(Guaranteed Commercial Range Performance)

The tables below specify the guaranteed performance of the IDT39C60 over the commercial operating range of 0°C to +70°C, with Vcc from 4.75V to 5.25V. All data are in nanoseconds, with inputs switching between 0V and 3V at 1V per nanosecond and measurements made at 1.5V.

MAXIMUM COMBINATIONAL PROPAGATION DELAYS CL = 50pF

From Input	To Output: SC_{0-6}	$DATA_{0-15}$	$\overline{ERROR}$	$\overline{MULT\ ERROR}$
$DATA_{0-15}$	32	65(1)	32	50
CB_{0-6} (CODE ID_{2-0} 000, 011)	28	56	29	47
CB_{0-6} (CODE ID_{2-0} 010, 100, 101, 110, 111)	28	45	29	34
$\overline{GENERATE}$	35	—	—	—
CORRECT (Not Internal Control Mode)	—	45	—	—
DIAG MODE (Not Internal Control Mode)	50	78	59	75
PASSTHRU (Not Internal Control Mode)	36	44	29	46
CODE ID_{2-0}	61	90	60	80
LE_{IN} (From latched to transparent)	39	72	39	59
LE_{OUT} (From latched to transparent)	—	31	—	—
LE_{DIAG} (From latched to transparent; Not Internal Control Mode)	45	78	45	65
Internal Control Mode: LE_{DIAG} (From latched to transparent)	67	96	66	86
Internal Control Mode: $DATA_{0-15}$ (Via Diagnostic Latch)	67	96	66	86

2595 tbl 62

NOTE:
1. $DATA_{IN}$ to corrected $DATA_{OUT}$ measurement requires timing as shown below.

MINIMUM SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input	To (Latching Data)	Set-up Time	Hold Time
$DATA_{0-15}$	LE_{IN}	6	7
CB_{0-6}	LE_{IN}	5	6
$DATA_{0-15}$	LE_{OUT}	44	5
CB_{0-6} (CODE ID 000, 011)	LE_{OUT}	35	0
CB_{0-6} (CODE ID 010, 100, 101, 110, 111)	LE_{OUT}	27	0
CORRECT	LE_{OUT}	26	1
DIAG MODE	LE_{OUT}	69	0
PASSTHRU	LE_{OUT}	26	0
CODE ID_{2-0}	LE_{OUT}	81	0
LE_{IN}	LE_{OUT}	51	5
$DATA_{0-15}$	LE_{DIAG}	6	8

2595 tbl 63

MAXIMUM OUTPUT ENABLE/DISABLE TIMES

Output tests specified with CL = 5pF and measured to 0.5V change of output voltage level. Test performed with CL = 50pF and correlated to CL = 5pF.

Input	Output	Enable	Disable
$\overline{OE}$ $BYTE_0$, $\overline{OE}$ $BYTE_1$	$DATA_{0-15}$	30	30
$\overline{OE}_{SC}$	SC_{0-6}	30	30

2595 tbl 64

MINIMUM PULSE WIDTHS

LE_{IN}, LE_{OUT}, LE_{DIAG}	15

2595 tbl 65

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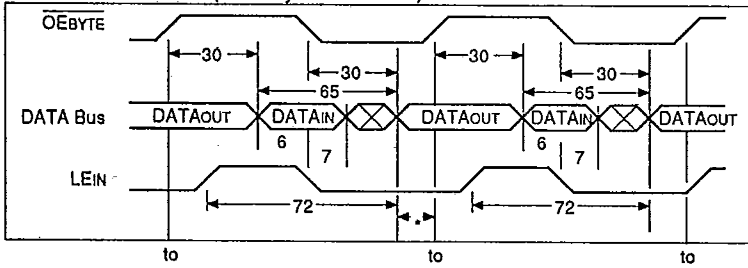
IDT39C60 COMMERCIAL — DATAIN TO CORRECTED DATAOUT TIMING (Two cycles shown)



NOTES:
Device Mode = "Correct"
System Type = "Correct Always"
Min. Period = 105ns (fMAX = 9.5MHz)

Timing Parameter From	To	Min./Max.
OEBYTE = High	to DATAOUT Disabled	Max.
OEBYTE = Low	to DATAOUT Enabled	Max.
DATAIN	to Corrected DATAOUT	Max.
DATAIN Set-up	to LEIN = Low	Min.
DATAIN Hold	to LEIN = Low	Min.
LEIN = High	to DATAOUT	Max.

* = (Memory/System dependent)

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IDT39C60 AC ELECTRICAL CHARACTERISTICS

(Guaranteed Military Range Performance)

The tables below specify the guaranteed performance of the IDT39C60 over the military operating range of –55°C to +125°C, with Vcc from 4.5V to 5.5V. All data are in nanoseconds, with inputs switching between 0V and 3V at 1V per nanosecond and measurements made at 1.5V.

MAXIMUM COMBINATIONAL PROPAGATION DELAYS $C_L = 50pF$

From Input	To Output			
	SC_{0-6}	$DATA_{0-15}$	$\overline{ERROR}$	$\overline{MULT\ ERROR}$
$DATA_{0-15}$	35	73(1)	36	56
CB_{0-6} (CODE ID_{2-0} 000, 011)	30	61	31	50
CB_{0-6} (CODE ID_{2-0} 010, 100, 101, 110, 111)	30	50	31	37
$\overline{GENERATE}$	38	—	—	—
CORRECT (Not Internal Control Mode)	—	49	—	—
DIAG MODE (Not Internal Control Mode)	58	89	65	90
PASSTHRU (Not Internal Control Mode)	39	51	34	54
CODE ID_{2-0}	69	100	68	90
LE_{IN} (From latched to transparent)	44	82	43	66
LE_{OUT} (From latched to transparent)	—	33	—	—
LE_{DIAG} (From latched to transparent; Not Internal Control Mode)	50	88	49	72
Internal Control Mode: LE_{DIAG} (From latched to transparent)	75	106	74	96
Internal Control Mode: $DATA_{0-15}$ (Via Diagnostic Latch)	75	106	74	96

2595 tbl 66

NOTE:
1. $DATA_{IN}$ to corrected $DATA_{OUT}$ measurement requires timing as shown below.

MINIMUM SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input	To (Latching Data)	Set-up Time	Hold Time
$DATA_{0-15}$	LE_{IN}	7	7
CB_{0-6}	LE_{IN}	5	7
$DATA_{0-15}$	LE_{OUT}	50	5
CB_{0-6} (CODE ID 000, 011)	LE_{OUT}	38	0
CB_{0-6} (CODE ID 010, 100, 101, 110, 111)	LE_{OUT}	30	0
CORRECT	LE_{OUT}	28	1
DIAG MODE	LE_{OUT}	84	0
PASSTHRU	LE_{OUT}	30	0
CODE ID_{2-0}	LE_{OUT}	89	0
LE_{IN}	LE_{OUT}	59	5
$DATA_{0-15}$	LE_{DIAG}	7	9

2595 tbl 67

MAXIMUM OUTPUT ENABLE/DISABLE TIMES

Output tests specified with $C_L = 5pF$ and measured to 0.5V change of output voltage level. Test performed with $C_L = 50pF$ and correlated to $C_L = 5pF$.

Input	Output	Enable	Disable
$\overline{OE}$ $BYTE_0$, $\overline{OE}$ $BYTE_1$	$DATA_{0-15}$	35	35
$\overline{OE}_{SC}$	SC_{0-6}	35	35

2595 tbl 68

MINIMUM PULSE WIDTHS

LE_{IN}, LE_{OUT}, LE_{DIAG}	15

2595 tbl 69

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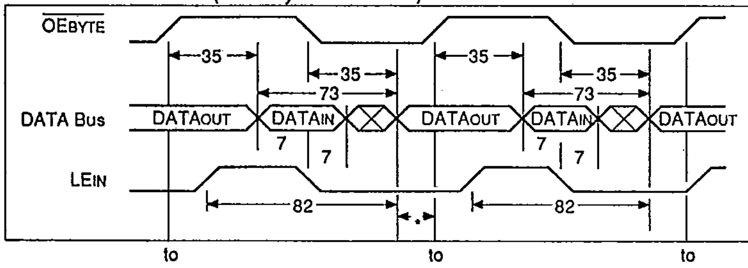
IDT39C60 MILITARY — DATAIN TO CORRECTED DATAOUT TIMING (Two cycles shown)



NOTES:
Device Mode = "Correct"
System Type = "Correct Always"
Min. Period = 118ns (fMAX = 8.5MHz)

Timing Parameter From / To	Min./Max.
OEBYTE = High to DATAOUT Disabled	Max.
OEBYTE = Low to DATAOUT Enabled	Max.
DATAIN to Corrected DATAOUT	Max.
DATAIN Set-up to LEIN = Low	Min.
DATAIN Hold to LEIN = Low	Min.
LEIN = High to DATAOUT	Max.

* = (Memory/System dependent)

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AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 12

2595 tbl 70

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

2595 tbl 71

IDT39C60 INPUT/OUTPUT INTERFACE CIRCUIT

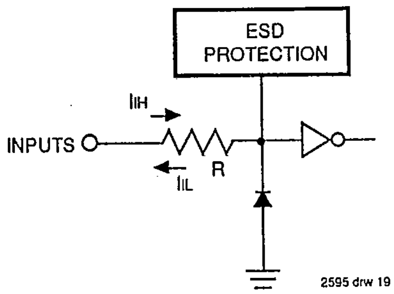


Figure 10. Input Structure (All Inputs)

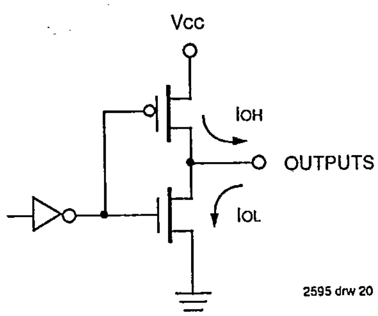
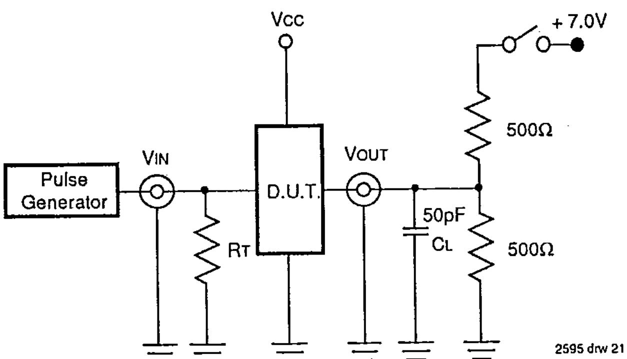


Figure 11. Output Structure

TEST CIRCUIT LOAD



DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance
R_L = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator

Figure 12.

ORDERING INFORMATION

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IDT XXXXX X X

Device Type — Package — Process/Temperature Range

Process/Temperature Range	
BLANK	Commercial (0°C to +70°C)
B	Military (–55°C to +125°C) Compliant to MIL-STD-883, Class B

Package	
P	Plastic DIP
C	Sidebraze DIP
J	Plastic Leaded Chip Carrier
L	Leadless Chip Carrier

Device Type	
39C60	16-Bit EDC Unit
39C60–1	Fast 16-Bit EDC Unit
39C60A	Very-Fast 16-Bit EDC Unit
39C60B	Ultra-Fast 16-Bit EDC Unit

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