



# **PIC18F6393/6493/8393/8493**

## **Data Sheet**

64/80-Pin High Performance,  
Flash Microcontrollers with LCD Driver,  
12-Bit ADC and nanoWatt Technology

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# MICROCHIP PIC18F6393/6493/8393/8493

## 64/80-Pin High-Performance, Flash Microcontrollers with LCD Driver, 12-Bit ADC and nanoWatt Technology

### LCD Driver Module Features:

- Direct Driving of LCD Panel
- Up to 192 Pixels: Software Selectable
- Programmable LCD Timing module:
  - Multiple LCD timing sources available
  - Up to four commons: Static, 1/2, 1/3 or 1/4 multiplex
  - Static, 1/2 or 1/3 bias configuration
- Can Drive LCD Panel while in Sleep mode for Low-Power Operation

### Power-Managed Modes:

- Run: CPU On, Peripherals On
- Idle: CPU Off, Peripherals On
- Sleep: CPU Off, Peripherals Off
- Run mode Current Down to 14  $\mu$ A Typical
- Idle mode Currents Down to 5.8  $\mu$ A Typical
- Sleep mode Currents Down to 0.1  $\mu$ A Typical
- Timer1 Oscillator: 1.8  $\mu$ A, 32 kHz, 2V
- Watchdog Timer: 2.1  $\mu$ A Typical
- Two-Speed Oscillator Start-up

### Flexible Oscillator Structure:

- Four Crystal modes:
  - LP: Up to 200 kHz
  - XT: Up to 4 MHz
  - HS: Up to 40 MHz
  - HSPLL: 4-10 MHz (16-40 MHz internal)
- 4x Phase Lock Loop (available for crystal and internal oscillators)
- Two External RC modes, Up to 4 MHz
- Two External Clock modes, Up to 40 MHz
- Internal Oscillator Block:
  - Eight selectable frequencies, from 31 kHz to 8 MHz
  - Provides a complete range of clock speeds from 31 kHz to 32 MHz when used with PLL
  - User-tunable to compensate for frequency drift
- Secondary Oscillator Using Timer1 at 32 kHz
- Fail-Safe Clock Monitor:
  - Allows for safe shutdown of device if primary or secondary clock fails

### Peripheral Highlights:

- 12-Bit, Up to 12-Channel Analog-to-Digital (A/D) Converter module:
  - Auto-acquisition capability
  - Conversion available during Sleep
- High-Current Sink/Source 25 mA/25 mA
- Four External Interrupts
- Four Input Change Interrupts
- Four 8-Bit/16-Bit Timer/Counter modules
- Real-Time Clock (RTC) Software module:
  - Configurable 24-hour clock, calendar, automatic 100-year or 12,800-year, day-of-week calculator
  - Uses Timer1
- Up to Two Capture/Compare/PWM (CCP) modules
- Master Synchronous Serial Port (MSSP) module Supporting Three-Wire SPI (all four modes) and I<sup>2</sup>C™ Master and Slave modes
- Addressable USART module:
  - Supports RS-485 and RS-232
- Enhanced Addressable USART module:
  - Supports RS-485, RS-232 and LIN 1.2
  - Auto-wake-up on Start bit
  - Auto-Baud Detect
- Dual Analog Comparators with Input Multiplexing

### Special Microcontroller Features:

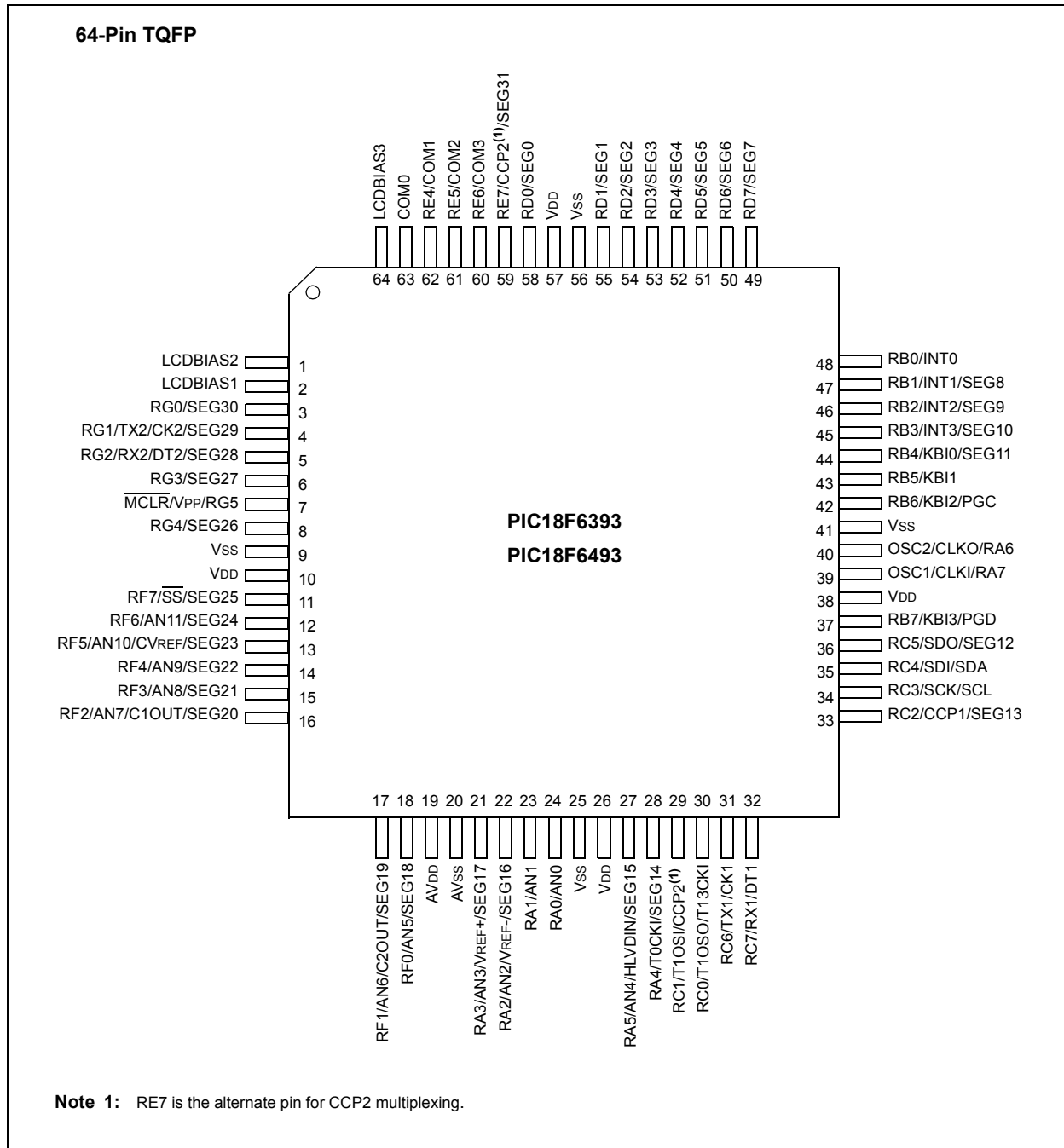
- C Compiler Optimized Architecture:
  - Optional extended instruction set designed to optimize re-entrant code
- 1000 Erase/Write Cycle Flash Program Memory Typical
- Flash Retention: 100 Years Typical
- Priority Levels for Interrupts
- 8 x 8 Single-Cycle Hardware Multiplier
- Extended Watchdog Timer (WDT):
  - Programmable period from 4 ms to 132s
  - 2% stability over VDD and temperature
- In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug (ICD) via Two Pins
- Wide Operating Voltage Range: 2.0V to 5.5V

**Note:** This document is supplemented by the "PIC18F6390/6490/8390/8490 Data Sheet" (DS39629). See **Section 1.0 "Device Overview"**.

# PIC18F6393/6493/8393/8493

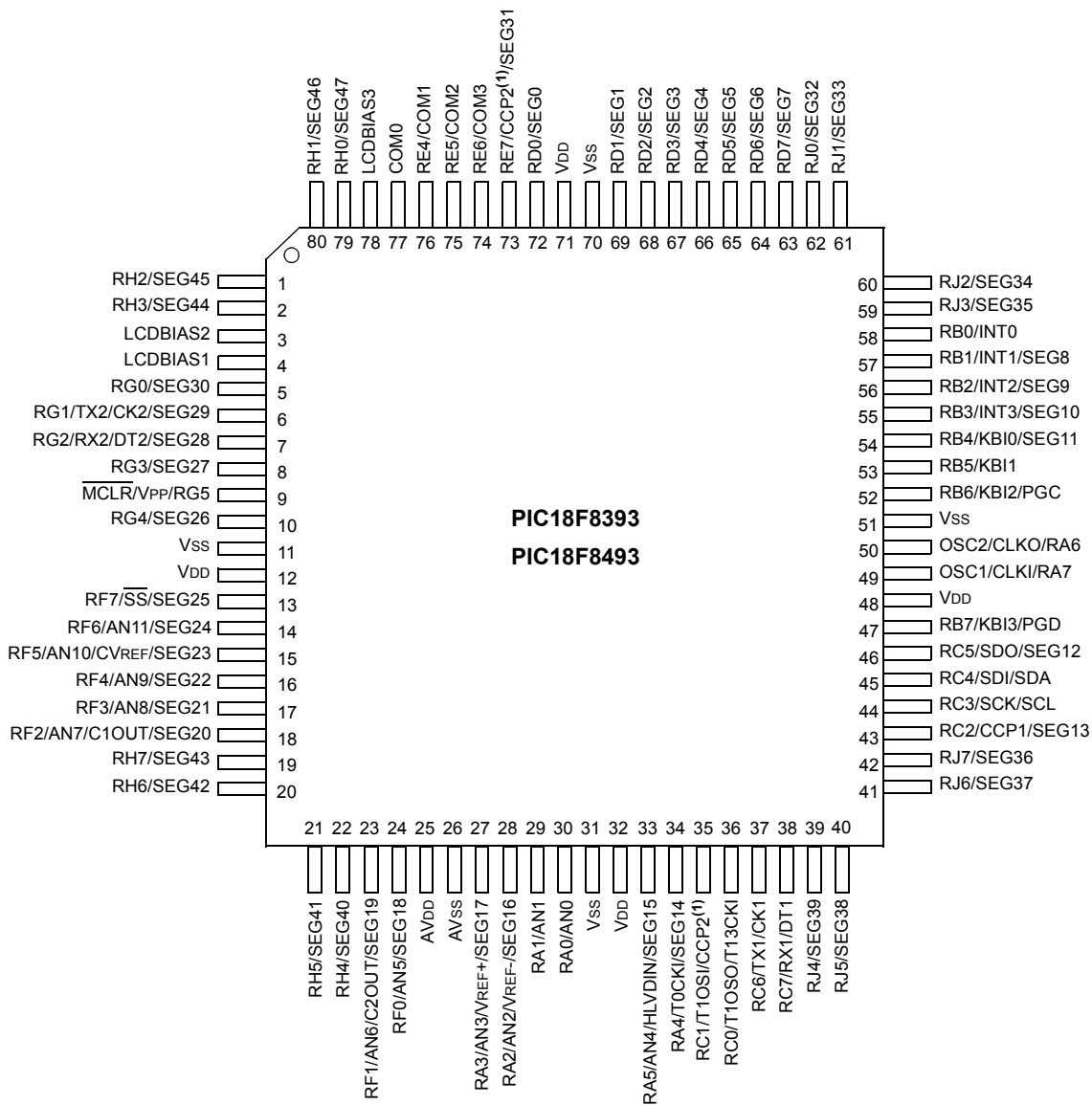
Device	Program Memory		Data Memory	I/O	LCD (pixel)	12-Bit A/D (channels)	CCP (PWM)	MSSP		EUSART/AUSART	Comparators	Timers 8/16-Bit
	Flash (bytes)	# Single-Word Instructions	SRAM (bytes)					SPI	Master I <sup>2</sup> C™			
PIC18F6393	8K	4096	768	50	128	12	2	Y	Y	1/1	2	1/3
PIC18F6493	16K	8192	768	50	128	12	2	Y	Y	1/1	2	1/3
PIC18F8393	8K	4096	768	66	192	12	2	Y	Y	1/1	2	1/3
PIC18F8493	16K	8192	768	66	192	12	2	Y	Y	1/1	2	1/3

## Pin Diagrams



## Pin Diagrams (Continued)

### 80-Pin TQFP



**Note 1:** RE7 is the alternate pin for CCP2 multiplexing.

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NOTES:



## 1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

- PIC18F6393
- PIC18F8393
- PIC18F6493
- PIC18F8493

**Note:** This data sheet documents only the devices' features and specifications that are in addition to the features and specifications of the PIC18F6390/6490/8390/8490 devices. For information on the features and specifications shared by the PIC18F6393/6493/8393/8493 and PIC18F6390/6490/8390/8490 devices, see the "PIC18F6390/6490/8390/8490 Data Sheet" (DS39629).

This family offers the advantages of all PIC18 microcontrollers – namely, high computational performance at an economical price. In addition to these features, the PIC18F6393/6493/8393/8493 family introduces design enhancements that make these microcontrollers a logical choice for many high-performance, power-sensitive applications.

### 1.1 Special Features

- **12-Bit A/D Converter:** This module incorporates programmable acquisition time, allowing for a channel to be selected and a conversion to be initiated without waiting for a sampling period and thus, reduces code overhead.

## 1.2 Details on Individual Family Members

Devices in the PIC18F6393/6493/8393/8493 family are available in 64-pin (PIC18F6X93) and 80-pin (PIC18F8X93) packages. Block diagrams for the two groups are shown in Figure 1-1 and Figure 1-2, respectively.

The devices are differentiated from each other in the following ways:

- I/O Ports:
  - 64-pin devices – 7 bidirectional ports
  - 80-pin devices – 9 bidirectional ports
- LCD Pixels:
  - 64-pin devices – 128 (32 SEGs x 4 COMs) pixels can be driven
  - 80-pin devices – 192 (48 SEGs x 4 COMs) pixels can be driven
- Flash Program Memory:
  - PIC18FX393 devices – 8 Kbytes
  - PIC18FX493 devices – 16 Kbytes

All other features for devices in this family are identical. These are summarized in Table 1-1.

The pinouts for all devices are listed in Table 1-2 and Table 1-3.

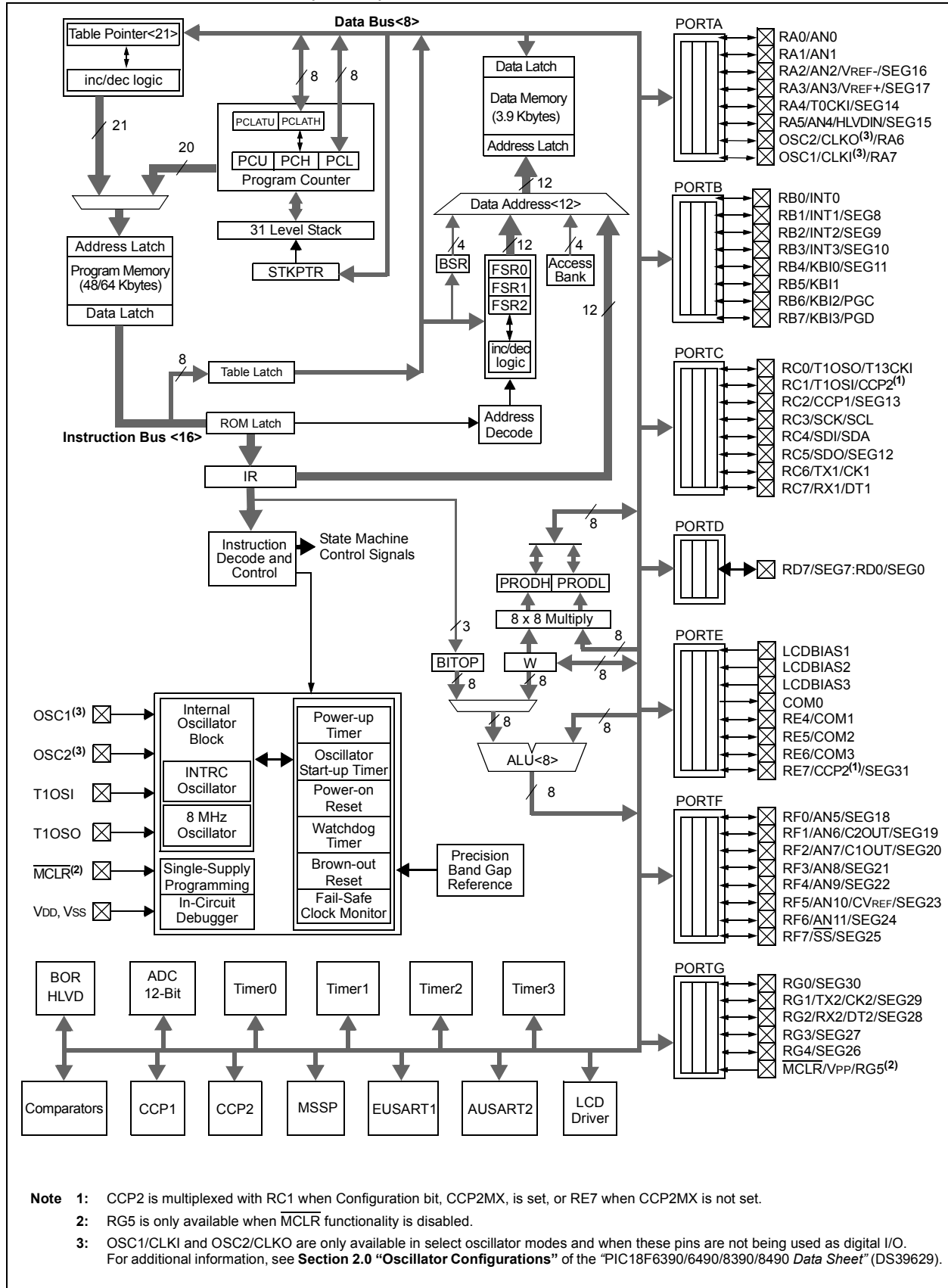
Like all Microchip PIC18 devices, members of the PIC18F6393/6493/8393/8493 family are available as both standard and low-voltage devices. Standard devices with Flash memory, designated with an "F" in the part number (such as PIC18F6393), accommodate an operating VDD range of 4.2V to 5.5V. Low-voltage parts, designated by "LF" (such as PIC18LF6490), function over an extended VDD range of 2.0V to 5.5V.

# PIC18F6393/6493/8393/8493

**TABLE 1-1: DEVICE FEATURES**

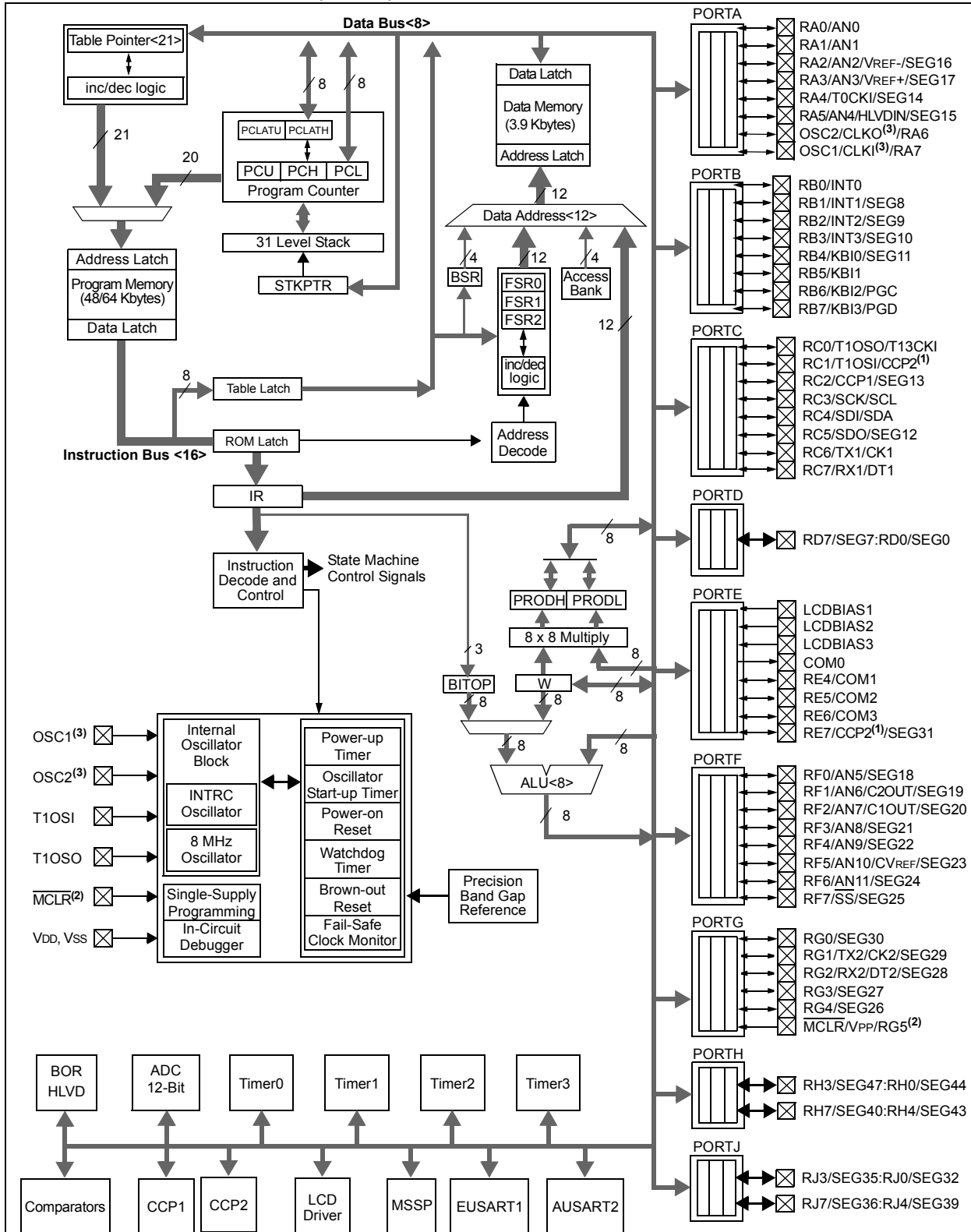
Features	PIC18F6393	PIC18F6493	PIC18F8393	PIC18F8493
Operating Frequency	DC – 40 MHz	DC – 40 MHz	DC – 40 MHz	DC – 40 MHz
Program Memory (Bytes)	8K	16K	8K	16K
Program Memory (Instructions)	4096	8192	4096	8192
Data Memory (Bytes)	768	768	768	768
Interrupt Sources	22	22	22	22
I/O Ports	Ports A, B, C, D, E, F, G	Ports A, B, C, D, E, F, G	Ports A, B, C, D, E, F, G, H, J	Ports A, B, C, D, E, F, G, H, J
Number of Pixels the LCD Driver Can Drive	128 (32 SEGs x 4 COMs)	128 (32 SEGs x 4 COMs)	192 (48 SEGs x 4 COMs)	192 (48 SEGs x 4 COMs)
Timers	4	4	4	4
Capture/Compare/PWM Modules	2	2	2	2
Serial Communications	MSSP, AUSART, Enhanced USART	MSSP, AUSART, Enhanced USART	MSSP, AUSART, Enhanced USART	MSSP, AUSART, Enhanced USART
12-Bit Analog-to-Digital Module	12 Input Channels	12 Input Channels	12 Input Channels	12 Input Channels
Resets (and Delays)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT
Programmable Low-Voltage Detect	Yes	Yes	Yes	Yes
Programmable Brown-out Reset	Yes	Yes	Yes	Yes
Instruction Set	75 Instructions; 83 with Extended Instruction Set Enabled	75 Instructions; 83 with Extended Instruction Set Enabled	75 Instructions; 83 with Extended Instruction Set Enabled	75 Instructions; 83 with Extended Instruction Set Enabled
Packages	64-Pin TQFP	64-Pin TQFP	80-Pin TQFP	80-Pin TQFP

**FIGURE 1-1: PIC18F6X93 (64-PIN) BLOCK DIAGRAM**



# PIC18F6393/6493/8393/8493

**FIGURE 1-2: PIC18F8X93 (80-PIN) BLOCK DIAGRAM**



- Note**
- 1: CCP2 is multiplexed with RC1 when Configuration bit, CCP2MX, is set and RE7 when CCP2MX is not set.
  - 2: RG5 is only available when MCLR functionality is disabled.
  - 3: OSC1/CLKI and OSC2/CLKO are only available in select oscillator modes and when these pins are not being used as digital I/O. For additional information, see Section 2.0 "Oscillator Configurations" of the "PIC18F6390/6490/8390/8490 Data Sheet" (DS39629).

**TABLE 1-2: PIC18F6X93 PINOUT I/O DESCRIPTIONS**

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
MCLR/VPP/RG5 MCLR  VPP RG5	7	I  P I	ST  ST	Master Clear (input) or programming voltage (input). Master Clear (Reset) input. This pin is an active-low Reset to the device. Programming voltage input. Digital input.
OSC1/CLKI/RA7 OSC1  CLKI  RA7	39	I  I I/O	ST  CMOS TTL	Oscillator crystal or external clock input. Oscillator crystal input or external clock source input. ST buffer when configured in RC mode; CMOS otherwise. External clock source input. Always associated with pin function OSC1. (See related OSC1/CLKI, OSC2/CLKO pins.) General purpose I/O pin.
OSC2/CLKO/RA6 OSC2  CLKO  RA6	40	O  O I/O	—  — TTL	Oscillator crystal or clock output. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. In RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate. General purpose I/O pin.

**Legend:** TTL = TTL compatible input  
ST = Schmitt Trigger input with CMOS levels  
I = Input  
P = Power  
CMOS = CMOS compatible input or output  
Analog = Analog input  
O = Output  
OD = Open-Drain (no P diode to VDD)

**Note 1:** Default assignment for CCP2 when Configuration bit, CCP2MX, is set.  
**2:** Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

# PIC18F6393/6493/8393/8493

**TABLE 1-2: PIC18F6X93 PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RA0/AN0	24	I/O I	TTL Analog	PORTA is a bidirectional I/O port.
RA0 AN0				Digital I/O. Analog input 0.
RA1/AN1	23	I/O I	TTL Analog	Digital I/O.
RA1 AN1				Analog input 1.
RA2/AN2/VREF-/SEG16	22	I/O I I O	TTL Analog Analog Analog	Digital I/O.
RA2				Analog input 2.
AN2				A/D reference voltage (Low) input.
VREF- SEG16				SEG16 output for LCD.
RA3/AN3/VREF+/SEG17	21	I/O I I O	TTL Analog Analog Analog	Digital I/O.
RA3				Analog input 3.
AN3				A/D reference voltage (High) input.
VREF+ SEG17				SEG17 output for LCD.
RA4/T0CKI/SEG14	28	I/O I O	ST/OD ST Analog	Digital I/O. Open-drain when configured as output.
RA4				Timer0 external clock input.
T0CKI SEG14				SEG14 output for LCD.
RA5/AN4/HLVDIN/SEG15	27	I/O I I O	TTL Analog Analog Analog	Digital I/O.
RA5				Analog input 4.
AN4				Low-Voltage Detect input.
HLVDIN SEG15				SEG15 output for LCD.
RA6				See the OSC2/CLKO/RA6 pin.
RA7				See the OSC1/CLKI/RA7 pin.

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
 ST = Schmitt Trigger input with CMOS levels      Analog = Analog input  
 I = Input      O = Output  
 P = Power      OD = Open-Drain (no P diode to VDD)

**Note 1:** Default assignment for CCP2 when Configuration bit, CCP2MX, is set.  
**2:** Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

# PIC18F6393/6493/8393/8493

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**TABLE 1-2: PIC18F6X93 PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RB0/INT0 RB0 INT0	48	I/O I	TTL ST	PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs.  Digital I/O. External interrupt 0.
RB1/INT1/SEG8 RB1 INT1 SEG8	47	I/O I O	TTL ST Analog	Digital I/O. External interrupt 1. SEG8 output for LCD.
RB2/INT2/SEG9 RB2 INT2 SEG9	46	I/O I O	TTL ST Analog	Digital I/O. External interrupt 2. SEG9 output for LCD.
RB3/INT3/SEG10 RB3 INT3 SEG10	45	I/O I O	TTL ST Analog	Digital I/O. External interrupt 3. SEG10 output for LCD.
RB4/KBI0/SEG11 RB4 KBI0 SEG11	44	I/O I O	TTL TTL Analog	Digital I/O. Interrupt-on-change pin. SEG11 output for LCD.
RB5/KBI1 RB5 KBI1	43	I/O I	TTL TTL	Digital I/O. Interrupt-on-change pin.
RB6/KBI2/PGC RB6 KBI2 PGC	42	I/O I I/O	TTL TTL ST	Digital I/O. Interrupt-on-change pin. In-Circuit Debugger and ICSP™ programming clock pin.
RB7/KBI3/PGD RB7 KBI3 PGD	37	I/O I I/O	TTL TTL ST	Digital I/O. Interrupt-on-change pin. In-Circuit Debugger and ICSP programming data pin.

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**Note 1:** Default assignment for CCP2 when Configuration bit, CCP2MX, is set.  
**2:** Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

# PIC18F6393/6493/8393/8493

**TABLE 1-2: PIC18F6X93 PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RC0/T1OSO/T13CKI RC0 T1OSO T13CKI	30	I/O	ST	PORTC is a bidirectional I/O port.  Digital I/O. Timer1 oscillator output. Timer1/Timer3 external clock input.
		O	—	
		I	ST	
RC1/T1OSI/CCP2 RC1 T1OSI CCP2 <sup>(1)</sup>	29	I/O	ST	Digital I/O. Timer1 oscillator input. Capture 2 input/Compare 2 output/PWM2 output.
		I	CMOS	
		I/O	ST	
RC2/CCP1/SEG13 RC2 CCP1 SEG13	33	I/O	ST	Digital I/O. Capture 1 input/Compare 1 output/PWM1 output. SEG13 output for LCD.
		I/O	ST	
		O	Analog	
RC3/SCK/SCL RC3 SCK SCL	34	I/O	ST	Digital I/O. Synchronous serial clock input/output for SPI mode. Synchronous serial clock input/output for I <sup>2</sup> C™ mode.
		I/O	ST	
		I/O	ST	
RC4/SDI/SDA RC4 SDI SDA	35	I/O	ST	Digital I/O. SPI data in. I <sup>2</sup> C data I/O.
		I	ST	
		I/O	ST	
RC5/SDO/SEG12 RC5 SDO SEG12	36	I/O	ST	Digital I/O. SPI data out. SEG12 output for LCD.
		O	—	
		O	Analog	
RC6/TX1/CK1 RC6 TX1 CK1	31	I/O	ST	Digital I/O. EUSART1 asynchronous transmit. EUSART1 synchronous clock (see related RX1/DT1).
		O	—	
		I/O	ST	
RC7/RX1/DT1 RC7 RX1 DT1	32	I/O	ST	Digital I/O. EUSART1 asynchronous receive. EUSART1 synchronous data (see related TX1/CK1).
		I	ST	
		I/O	ST	

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
ST = Schmitt Trigger input with CMOS levels      Analog = Analog input  
I = Input      O = Output  
P = Power      OD = Open-Drain (no P diode to VDD)

**Note 1:** Default assignment for CCP2 when Configuration bit, CCP2MX, is set.  
**Note 2:** Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.





# PIC18F6393/6493/8393/8493

**TABLE 1-2: PIC18F6X93 PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
				PORTE is a bidirectional I/O port.
LCDBIAS1 LCDBIAS1	2	I	Analog	BIAS1 input for LCD.
LCDBIAS2 LCDBIAS2	1	I	Analog	BIAS2 input for LCD.
LCDBIAS3 LCDBIAS3	64	I	Analog	BIAS3 input for LCD.
COM0 COM0	63	O	Analog	COM0 output for LCD.
RE4/COM1 RE4 COM1	62	I/O O	ST Analog	Digital I/O. COM1 output for LCD.
RE5/COM2 RE5 COM2	61	I/O O	ST Analog	Digital I/O. COM2 output for LCD.
RE6/COM3 RE6 COM3	60	I/O O	ST Analog	Digital I/O. COM3 output for LCD.
RE7/CCP2/SEG31 RE7 CCP2 <sup>(2)</sup> SEG31	59	I/O I/O O	ST ST Analog	Digital I/O. Capture 2 input/Compare 2 output/PWM2 output. SEG31 output for LCD.

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
 ST = Schmitt Trigger input with CMOS levels      Analog = Analog input  
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**TABLE 1-2: PIC18F6X93 PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RF0/AN5/SEG18	18	I/O	ST	PORTF is a bidirectional I/O port. Digital I/O. Analog input 5. SEG18 output for LCD.
RF0			I	
AN5			O	
RF1/AN6/C2OUT/SEG19	17	I/O	ST	Digital I/O. Analog input 6. Comparator 2 output. SEG19 output for LCD.
RF1			I	
AN6			O	
C2OUT			O	
RF2/AN7/C1OUT/SEG20	16	I/O	ST	Digital I/O. Analog input 7. Comparator 1 output. SEG20 output for LCD.
RF2			I	
AN7			O	
C1OUT			O	
RF3/AN8/SEG21	15	I/O	ST	Digital I/O. Analog input 8. SEG21 output for LCD.
RF3			I	
AN8			O	
RF4/AN9/SEG22	14	I/O	ST	Digital I/O. Analog input 9. SEG22 output for LCD.
RF4			I	
AN9			O	
RF5/AN10/CVREF/SEG23	13	I/O	ST	Digital I/O. Analog input 10. Comparator reference voltage output. SEG23 output for LCD.
RF5			I	
AN10			O	
CVREF			O	
RF6/AN11/SEG24	12	I/O	ST	Digital I/O. Analog input 11. SEG24 output for LCD.
RF6			I	
AN11			O	
RF7/ $\overline{SS}$ /SEG25	11	I/O	ST	Digital I/O. SPI™ slave select input. SEG25 output for LCD.
RF7			I	
$\overline{SS}$			TTL	
SEG25			O	

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
 ST = Schmitt Trigger input with CMOS levels      Analog = Analog input  
 I = Input      O = Output  
 P = Power      OD = Open-Drain (no P diode to VDD)

**Note 1:** Default assignment for CCP2 when Configuration bit, CCP2MX, is set.  
**2:** Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.







**TABLE 1-3: PIC18F8X93 PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RB0/INT0 RB0 INT0	58	I/O I	TTL ST	PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs.  Digital I/O. External interrupt 0.
RB1/INT1/SEG8 RB1 INT1 SEG8	57	I/O I O	TTL ST Analog	Digital I/O. External interrupt 1. SEG8 output for LCD.
RB2/INT2/SEG9 RB2 INT2 SEG9	56	I/O I O	TTL ST Analog	Digital I/O. External interrupt 2. SEG9 output for LCD.
RB3/INT3/SEG10 RB3 INT3 SEG10	55	I/O I O	TTL ST Analog	Digital I/O. External interrupt 3. SEG10 output for LCD.
RB4/KBI0/SEG11 RB4 KBI0 SEG11	54	I/O I O	TTL TTL Analog	Digital I/O. Interrupt-on-change pin. SEG11 output for LCD.
RB5/KBI1 RB5 KBI1	53	I/O I	TTL TTL	Digital I/O. Interrupt-on-change pin.
RB6/KBI2/PGC RB6 KBI2 PGC	52	I/O I I/O	TTL TTL ST	Digital I/O. Interrupt-on-change pin. In-Circuit Debugger and ICSP™ programming clock pin.
RB7/KBI3/PGD RB7 KBI3 PGD	47	I/O I I/O	TTL TTL ST	Digital I/O. Interrupt-on-change pin. In-Circuit Debugger and ICSP programming data pin.

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
 ST = Schmitt Trigger input with CMOS levels      Analog = Analog input  
 I = Input      O = Output  
 P = Power      OD = Open-Drain (no P diode to VDD)

**Note 1:** Default assignment for CCP2 when Configuration bit, CCP2MX, is set.  
**2:** Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.







# PIC18F6393/6493/8393/8493

**TABLE 1-3: PIC18F8X93 PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
LCDBIAS1 LCDBIAS1	4	I	Analog	BIAS1 input for LCD.
LCDBIAS2 LCDBIAS2	3	I	Analog	BIAS2 input for LCD.
LCDBIAS3 LCDBIAS3	78	I	Analog	BIAS3 input for LCD.
COM0 COM0	77	O	Analog	COM0 output for LCD.
RE4/COM1 RE4 COM1	76	I/O O	ST Analog	Digital I/O. COM1 output for LCD.
RE5/COM2 RE5 COM2	75	I/O O	ST Analog	Digital I/O. COM2 output for LCD.
RE6/COM3 RE6 COM3	74	I/O O	ST Analog	Digital I/O. COM3 output for LCD.
RE7/CCP2/SEG31 RE7 CCP2 <sup>(2)</sup> SEG31	73	I/O I/O O	ST ST Analog	Digital I/O. Capture 2 input/Compare 2 output/PWM2 output. SEG31 output for LCD.

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
 ST = Schmitt Trigger input with CMOS levels      Analog = Analog input  
 I = Input      O = Output  
 P = Power      OD = Open-Drain (no P diode to VDD)

**Note 1:** Default assignment for CCP2 when Configuration bit, CCP2MX, is set.  
**2:** Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.









## 2.0 12-BIT ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

The Analog-to-Digital (A/D) Converter module converts an analog input signal to a 12-bit digital number. The module has 12 inputs for both PIC18F6393/6493 (64-pin) and PIC18F8393/8493 (80-pin) devices.

The module has five registers:

- A/D Result High Register (ADRESH)
- A/D Result Low Register (ADRESL)
- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)
- A/D Control Register 2 (ADCON2)

The ADCON0 register, shown in Register 2-1, controls the operation of the A/D module. The ADCON1 register, shown in Register 2-2, configures the functions of the port pins. The ADCON2 register, shown in Register 2-3, configures the A/D clock source, programmed acquisition time and justification.

### REGISTER 2-1: ADCON0: A/D CONTROL REGISTER 0

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CHS3	CHS2	CHS1	CHS0	GO/DONE	ADON
bit 7							bit 0

#### Legend:

R = Readable bit  
-n = Value at POR

W = Writable bit  
'1' = Bit is set

U = Unimplemented bit, read as '0'  
'0' = Bit is cleared

x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-2 **CHS3:CHS0:** Analog Channel Select bits

0000 = Channel 0 (AN0)  
 0001 = Channel 1 (AN1)  
 0010 = Channel 2 (AN2)  
 0011 = Channel 3 (AN3)  
 0100 = Channel 4 (AN4)  
 0101 = Channel 5 (AN5)  
 0110 = Channel 6 (AN6)  
 0111 = Channel 7 (AN7)  
 1000 = Channel 8 (AN8)  
 1001 = Channel 9 (AN9)  
 1010 = Channel 10 (AN10)  
 1011 = Channel 11 (AN11)  
 1100 = Unimplemented<sup>(1)</sup>  
 1101 = Unimplemented<sup>(1)</sup>  
 1110 = Unimplemented<sup>(1)</sup>  
 1111 = Unimplemented<sup>(1)</sup>

bit 1 **GO/DONE:** A/D Conversion Status bit

When ADON = 1:

1 = A/D conversion in progress  
 0 = A/D Idle

bit 0 **ADON:** A/D On bit

1 = A/D Converter module is enabled  
 0 = A/D Converter module is disabled

**Note 1:** Performing a conversion on unimplemented channels will return a floating input measurement.

## REGISTER 2-2: ADCON1: A/D CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

### Legend:

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 7-6                      **Unimplemented:** Read as '0'

bit 5-4                      **VCFG1:VCFG0:** Voltage Reference Configuration bits

	A/D VREF+	A/D VREF-
00	AVDD	AVSS
01	External VREF+	AVSS
10	AVDD	External VREF-
11	External VREF+	External VREF-

bit 3-0                      **PCFG3:PCFG0:** A/D Port Configuration Control bits

PCFG<3:0>	AN11	AN10	AN9	AN8	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0
0000	A	A	A	A	A	A	A	A	A	A	A	A
0001	A	A	A	A	A	A	A	A	A	A	A	A
0010	A	A	A	A	A	A	A	A	A	A	A	A
0011	A	A	A	A	A	A	A	A	A	A	A	A
0100	D	A	A	A	A	A	A	A	A	A	A	A
0101	D	D	A	A	A	A	A	A	A	A	A	A
0110	D	D	D	A	A	A	A	A	A	A	A	A
0111	D	D	D	D	A	A	A	A	A	A	A	A
1000	D	D	D	D	D	A	A	A	A	A	A	A
1001	D	D	D	D	D	D	A	A	A	A	A	A
1010	D	D	D	D	D	D	D	A	A	A	A	A
1011	D	D	D	D	D	D	D	D	A	A	A	A
1100	D	D	D	D	D	D	D	D	D	A	A	A
1101	D	D	D	D	D	D	D	D	D	D	A	A
1110	D	D	D	D	D	D	D	D	D	D	D	A
1111	D	D	D	D	D	D	D	D	D	D	D	D

A = Analog input

D = Digital I/O



## REGISTER 2-3: ADCON2: A/D CONTROL REGISTER 2

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	—	ACQT2	ACQT1	ACQT0	ADCS2	ADCS1	ADCS0
bit 7							bit 0

### Legend:

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

- bit 7                      **ADFM:** A/D Result Format Select bit  
                             1 = Right justified  
                             0 = Left justified
- bit 6                      **Unimplemented:** Read as '0'
- bit 5-3                      **ACQT2:ACQT0:** A/D Acquisition Time Select bits  
                             111 = 20 TAD  
                             110 = 16 TAD  
                             101 = 12 TAD  
                             100 = 8 TAD  
                             011 = 6 TAD  
                             010 = 4 TAD  
                             001 = 2 TAD  
                             000 = 0 TAD<sup>(1)</sup>
- bit 2-0                      **ADCS2:ADCS0:** A/D Conversion Clock Select bits  
                             111 = FRC (clock derived from A/D RC oscillator)<sup>(1)</sup>  
                             110 = FOSC/64  
                             101 = FOSC/16  
                             100 = FOSC/4  
                             011 = FRC (clock derived from A/D RC oscillator)<sup>(1)</sup>  
                             010 = FOSC/32  
                             001 = FOSC/8  
                             000 = FOSC/2

**Note 1:** If the A/D FRC clock source is selected, a delay of one T<sub>CY</sub> (instruction cycle) is added before the A/D clock starts. This allows the SLEEP instruction to be executed before starting a conversion.

The analog reference voltage is software selectable to either the device's positive and negative supply voltage (VDD and VSS), or the voltage level on the RA3/AN3/VREF+/SEG17 and RA2/AN2/VREF-/SEG16 pins.

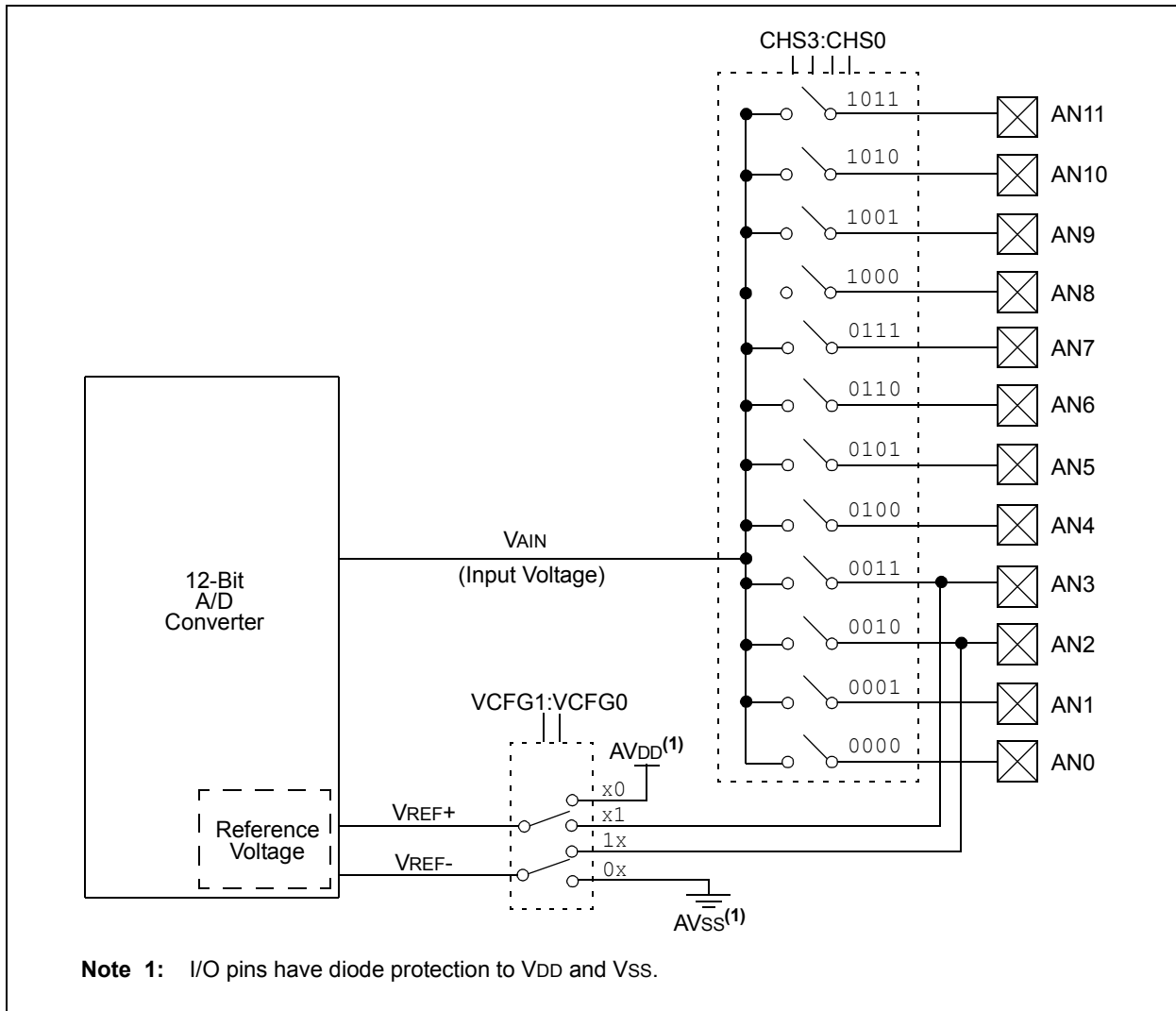
The A/D Converter has a unique feature of being able to operate while the device is in Sleep mode. To operate in Sleep, the A/D conversion clock must be derived from the A/D's internal RC oscillator.

The output of the sample and hold is the input into the converter, which generates the result via successive approximation.

A device Reset forces all registers to their Reset state. This forces the A/D module to be turned off and any conversion in progress is aborted.

Each port pin associated with the A/D Converter can be configured as an analog input or a digital I/O. The ADRESH and ADRESL registers contain the result of the A/D conversion. When the A/D conversion is complete, the result is loaded into the ADRESH:ADRESL register pair, the GO/DONE bit (ADCON0<1>) is cleared and the A/D Interrupt Flag bit, ADIF, is set. The block diagram of the A/D module is shown in Figure 2-1.

**FIGURE 2-1: A/D BLOCK DIAGRAM**



The value in the ADRESH:ADRESL registers is unknown following Power-on and Brown-out Resets and is not affected by any other Reset.

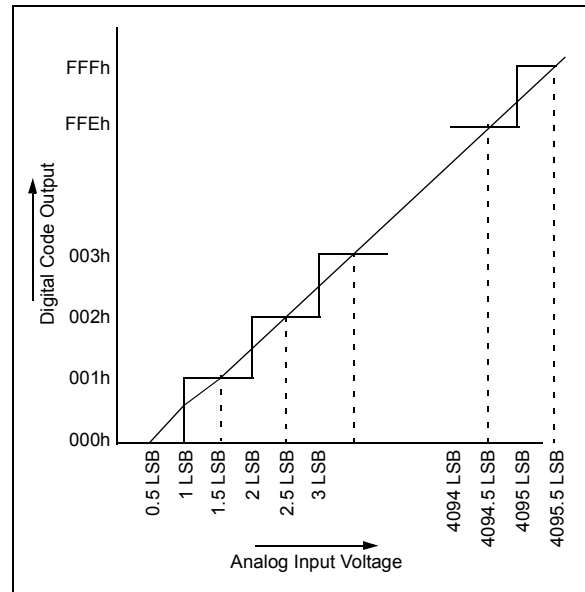
After the A/D module has been configured as desired, the selected channel must be acquired before the conversion is started. The analog input channels must have their corresponding TRIS bits selected as an input. To determine acquisition time, see **Section 2.1 "A/D Acquisition Requirements"**. After this acquisition time has elapsed, the A/D conversion can be started. An acquisition time can be programmed to occur between setting the GO/DONE bit and the actual start of the conversion.

The following steps should be followed to perform an A/D conversion:

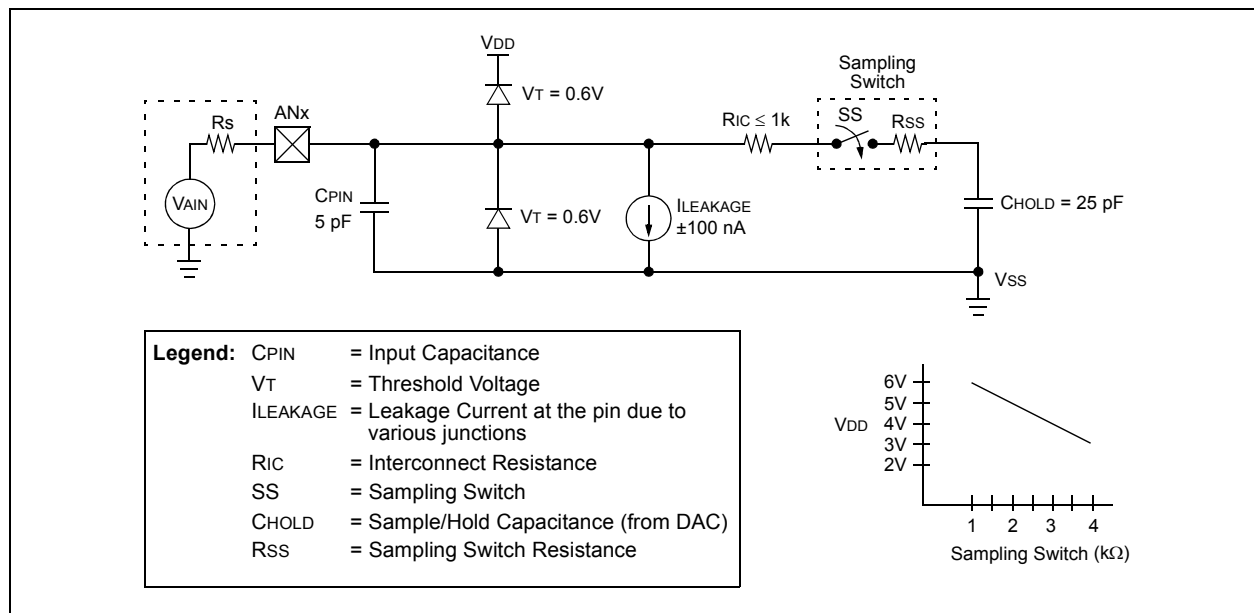
1. Configure the A/D module:
  - Configure analog pins, voltage reference and digital I/O (ADCON1)
  - Select A/D input channel (ADCON0)
  - Select A/D acquisition time (ADCON2)
  - Select A/D conversion clock (ADCON2)
  - Turn on A/D module (ADCON0)
2. Configure A/D interrupt (if desired):
  - Clear ADIF bit
  - Set ADIE bit
  - Set GIE bit
3. Wait the required acquisition time (if required).
4. Start conversion:
  - Set GO/DONE bit (ADCON0<1>)

5. Wait for A/D conversion to complete by either:
  - Polling for the GO/DONE bit to be cleared
  - OR
  - Waiting for the A/D interrupt
6. Read A/D Result registers (ADRESH:ADRESL); clear bit, ADIF, if required.
7. For the next conversion, go to step 1 or step 2, as required. The A/D conversion time per bit is defined as TAD. A minimum wait of 2 TAD is required before the next acquisition starts.

**FIGURE 2-2: A/D TRANSFER FUNCTION**



**FIGURE 2-3: ANALOG INPUT MODEL**



## 2.1 A/D Acquisition Requirements

For the A/D Converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 2-3. The source impedance (Rs) and the internal sampling switch (Rss) impedance directly affect the time required to charge the capacitor, CHOLD. The sampling switch (Rss) impedance varies over the device voltage (VDD). The source impedance affects the offset voltage at the analog input (due to pin leakage current). **The maximum recommended impedance for analog sources is 2.5 kΩ.** After the analog input channel is selected (changed), the channel must be sampled for at least the minimum acquisition time before starting a conversion.

To calculate the minimum acquisition time, Equation 2-1 may be used. This equation assumes that 1/2 LSB error is used (4096 steps for the 12-bit A/D). The 1/2 LSB error is the maximum error allowed for the A/D to meet its specified resolution.

Equation 2-3 shows the calculation of the minimum required acquisition time, TACQ. This calculation is based on the following application system assumptions:

CHOLD	=	25 pF
Rs	=	2.5 kΩ
Conversion Error	≤	1/2 LSB
VDD	=	3V → Rss = 4 kΩ
Temperature	=	85°C (system max.)

**Note:** When the conversion is started, the holding capacitor is disconnected from the input pin.

### EQUATION 2-1: ACQUISITION TIME

$$\begin{aligned} TACQ &= \text{Amplifier Settling Time} + \text{Holding Capacitor Charging Time} + \text{Temperature Coefficient} \\ &= TAMP + TC + TCOFF \end{aligned}$$

### EQUATION 2-2: A/D MINIMUM CHARGING TIME

$$\begin{aligned} V_{HOLD} &= (V_{REF} - (V_{REF}/4096)) \cdot (1 - e^{-(Tc/CHOLD)(RIC + Rss + Rs)}) \\ \text{or} \\ Tc &= -(CHOLD)(RIC + Rss + Rs) \ln(1/4096) \end{aligned}$$

### EQUATION 2-3: CALCULATING THE MINIMUM REQUIRED ACQUISITION TIME

$$\begin{aligned} TACQ &= TAMP + TC + TCOFF \\ TAMP &= 0.2 \mu s \\ TCOFF &= (Temp - 25^\circ C)(0.02 \mu s/^\circ C) \\ &\quad (85^\circ C - 25^\circ C)(0.02 \mu s/^\circ C) \\ &\quad 1.2 \mu s \end{aligned}$$

Temperature coefficient is only required for temperatures > 25°C. Below 25°C, TCOFF = 0 μs.

$$\begin{aligned} TC &= -(CHOLD)(RIC + Rss + Rs) \ln(1/4096) \mu s \\ &\quad -(25 \text{ pF})(1 \text{ k}\Omega + 4 \text{ k}\Omega + 2.5 \text{ k}\Omega) \ln(0.0002441) \mu s \\ &\quad 1.56 \mu s \\ TACQ &= 0.2 \mu s + 1.56 \mu s + 1.2 \mu s \\ &\quad 2.96 \mu s \end{aligned}$$

## 2.2 Selecting and Configuring Acquisition Time

The ADCON2 register allows the user to select an acquisition time that occurs each time the GO/DONE bit is set. It also gives users the option to use an automatically determined acquisition time.

Acquisition time may be set with the ACQT2:ACQT0 bits (ADCON2<5:3>), which provide a range of 2 to 20 TAD. When the GO/DONE bit is set, the A/D module continues to sample the input for the selected acquisition time, then automatically begins a conversion. Since the acquisition time is programmed, there may be no need to wait for an acquisition time between selecting a channel and setting the GO/DONE bit.

Manual acquisition is selected when ACQT2:ACQT0 = 000. When the GO/DONE bit is set, sampling is stopped and a conversion begins. The user is responsible for ensuring the required acquisition time has passed between selecting the desired input channel and setting the GO/DONE bit. This option is also the default Reset state of the ACQT2:ACQT0 bits and is compatible with devices that do not offer programmable acquisition times.

In either case, when the conversion is completed, the GO/DONE bit is cleared, the ADIF flag is set and the A/D begins sampling the currently selected channel again. If an acquisition time is programmed, there is nothing to indicate if the acquisition time has ended or if the conversion has begun.

## 2.3 Selecting the A/D Conversion Clock

The A/D conversion time per bit is defined as TAD. The A/D conversion requires 13 TAD per 12-bit conversion. The source of the A/D conversion clock is software selectable. There are seven possible options for TAD:

- 2 TOSC
- 4 TOSC
- 8 TOSC
- 16 TOSC
- 32 TOSC
- 64 TOSC
- Internal RC Oscillator

For correct A/D conversions, the A/D conversion clock (TAD) must be as short as possible, but greater than the minimum TAD. (See parameter 130 for more information.)

Table 2-1 shows the resultant TAD times derived from the device operating frequencies and the A/D clock source selected.

**TABLE 2-1: TAD vs. DEVICE OPERATING FREQUENCIES**

A/D Clock Source (TAD)		Assumes TAD Min. = 0.8 μs
Operation	ADCS2:ADCS0	Maximum Fosc
2 TOSC	000	2.50 MHz
4 TOSC	100	5.00 MHz
8 TOSC	001	10.00 MHz
16 TOSC	101	20.00 MHz
32 TOSC	010	40.00 MHz
64 TOSC	110	40.00 MHz
RC <sup>(1)</sup>	x11	1.00 MHz <sup>(2)</sup>

**Note 1:** The RC source has a typical TAD time of 2.5 μs.

**2:** For device frequencies above 1 MHz, the device must be in Sleep for the entire conversion or a FOSC divider should be used instead; otherwise, the A/D accuracy specification may not be met.

## 2.4 Operation in Power-Managed Modes

The selection of the automatic acquisition time and A/D conversion clock is determined in part by the clock source and frequency while in a power-managed mode.

If the A/D is expected to operate while the device is in a power-managed mode, the AD<sub>CS</sub>2:AD<sub>CS</sub>0 bits in AD<sub>CON</sub>2 should be updated in accordance with the clock source to be used. The AC<sub>QT</sub>2:AC<sub>QT</sub>0 bits do not need to be adjusted as the AD<sub>CS</sub>2:AD<sub>CS</sub>0 bits adjust the T<sub>AD</sub> time for the new clock speed. After entering the mode, an A/D acquisition or conversion may be started. Once started, the device should continue to be clocked by the same clock source until the conversion has been completed.

If desired, the device may be placed into the corresponding Idle mode during the conversion. If the device clock frequency is less than 1 MHz, the A/D RC clock source should be selected.

Operation in Sleep mode requires the A/D FRC clock to be selected. If the AC<sub>QT</sub>2:AC<sub>QT</sub>0 bits are set to '000' and a conversion is started, the conversion will be delayed one instruction cycle to allow execution of the SLEEP instruction and entry to Sleep mode. The IDLEN bit (OSCCON<7>) must have already been cleared prior to starting the conversion.

## 2.5 Configuring Analog Port Pins

The AD<sub>CON</sub>1, TRISA, TRISF and TRISH registers all configure the A/D port pins. The port pins needed as analog inputs must have their corresponding TRIS bits set (input). If the TRIS bit is cleared (output), the digital output level (V<sub>OH</sub> or V<sub>OL</sub>) will be converted.

The A/D operation is independent of the state of the CH<sub>S</sub>3:CH<sub>S</sub>0 bits and the TRIS bits.

**Note 1:** When reading the PORT register, all pins configured as analog input channels will read as cleared (a low level). Analog conversion on pins configured as digital pins can be performed. The voltage on the pin will be accurately converted.

**2:** Analog levels on any pin defined as a digital input may cause the digital input buffer to consume current out of the device's specification limits.

## 2.6 A/D Conversions

Figure 2-4 shows the operation of the A/D Converter after the  $\overline{\text{GO/DONE}}$  bit has been set and the ACQT2:ACQT0 bits are cleared. A conversion is started after the following instruction to allow entry into Sleep mode before the conversion begins.

Figure 2-5 shows the operation of the A/D Converter after the  $\overline{\text{GO/DONE}}$  bit has been set, the ACQT2:ACQT0 bits are set to '010' and a 4 TAD acquisition time has been selected before the conversion starts.

Clearing the  $\overline{\text{GO/DONE}}$  bit during a conversion will abort the current conversion. The A/D Result register pair will *not* be updated with the partially completed A/D conversion sample. This means the ADRESH:ADRESL registers will continue to contain the value of the last completed conversion (or the last value written to the ADRESH:ADRESL registers).

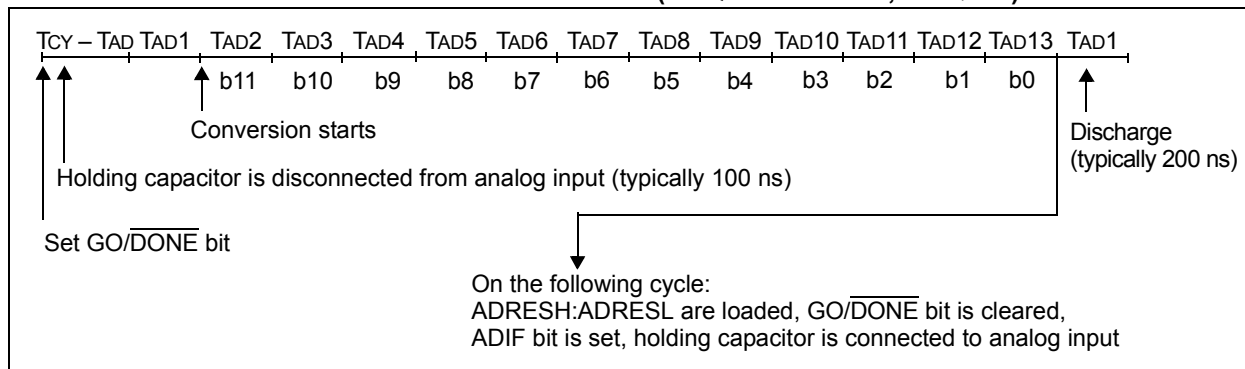
After the A/D conversion is completed or aborted, a 2 TAD wait is required before the next acquisition can be started. After this wait, acquisition on the selected channel is automatically started.

**Note:** The  $\overline{\text{GO/DONE}}$  bit should **NOT** be set in the same instruction that turns on the A/D. Code should wait at least 2  $\mu\text{s}$  after enabling the A/D before beginning an acquisition and conversion cycle.

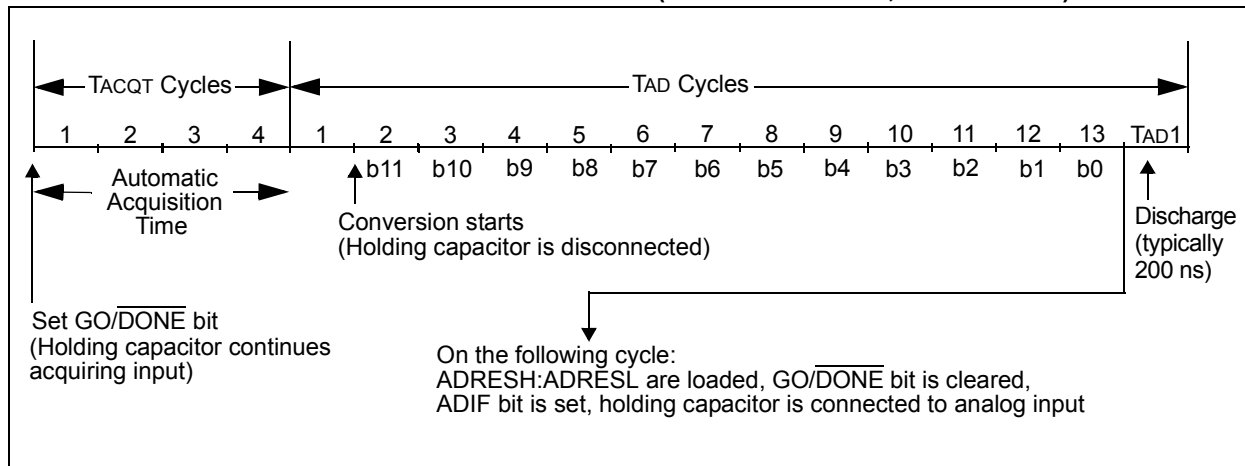
## 2.7 Discharge

The discharge phase is used to initialize the value of the holding capacitor. The array is discharged before every sample. This feature helps to optimize the unity gain amplifier, as the circuit always needs to charge the capacitor array, rather than charge/discharge based on previous-measure values.

**FIGURE 2-4: A/D CONVERSION TAD CYCLES (ACQT<2:0> = 000, TACQ = 0)**



**FIGURE 2-5: A/D CONVERSION TAD CYCLES (ACQT<2:0> = 010, TACQ = 4 TAD)**



## 2.8 Use of the ECCP2 Trigger

An A/D conversion can be started by the Special Event Trigger of the ECCP2 module. This requires that the CCP2M3:CCP2M0 bits (CCP2CON<3:0>) be programmed as '1011' and that the A/D module is enabled (ADON bit is set). When the trigger occurs, the GO/DONE bit will be set, starting the A/D acquisition and conversion, and the Timer1 (or Timer3) counter will be reset to zero. Timer1 (or Timer3) is reset to automatically repeat the A/D acquisition period with minimal software overhead (moving ADRESH:ADRESL to the

desired location). The appropriate analog input channel must be selected and the minimum acquisition period is either timed by the user, or an appropriate TACQ time selected before the Special Event Trigger sets the GO/DONE bit (starts a conversion).

If the A/D module is not enabled (ADON is cleared), the Special Event Trigger will be ignored by the A/D module but will still reset the Timer1 (or Timer3) counter.

**TABLE 2-2: REGISTERS ASSOCIATED WITH A/D OPERATION**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	(3)
PIR1	—	ADIF	RC1IF	TX1IF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	(3)
PIE1	—	ADIE	RC1IE	TX1IE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	(3)
IPR1	—	ADIP	RC1IP	TX1IP	SSP1IP	CCP1IP	TMR2IP	TMR1IP	(3)
PIR2	OSCFIF	CMIF	—	—	BCL1IF	HLVDIF	TMR3IF	CCP2IF	(3)
PIE2	OSCFIE	CMIE	—	—	BCL1IE	HLVDIE	TMR3IE	CCP2IE	(3)
IPR2	OSCFIP	CMIP	—	—	BCL1IP	HLVDIP	TMR3IP	CCP2IP	(3)
ADRESH	A/D Result Register High Byte								(3)
ADRESL	A/D Result Register Low Byte								(3)
ADCON0	—	—	CHS3	CHS2	CHS1	CHS0	GO/DONE	ADON	(3)
ADCON1	—	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0	(3)
ADCON2	ADFM	—	ACQT2	ACQT1	ACQT0	ADCS2	ADCS1	ADCS0	(3)
TRISA	TRISA7 <sup>(1)</sup>	TRISA6 <sup>(1)</sup>	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	(3)
TRISF	TRISF7	TRISF6	TRISF5	TRISF4	TRISF3	TRISF2	TRISF1	TRISF0	(3)
TRISH <sup>(2)</sup>	TRISH7	TRISH6	TRISH5	TRISH4	TRISH3	TRISH2	TRISH1	TRISH0	(3)

**Legend:** — = unimplemented, read as '0'. Shaded cells are not used for A/D conversion.

**Note 1:** PORTA<7:6> and their direction bits are individually configured as port pins based on various primary oscillator modes. When disabled, these bits read as '0'.

**2:** These registers are not implemented on 64-pin devices.

**3:** For these Reset values, see the "PIC18F6390/6490/8390/8490 Data Sheet" (DS39629).



## 3.0 SPECIAL FEATURES OF THE CPU

**Note:** For additional details on the Configuration bits, refer to **Section 23.1 “Configuration Bits”** in the “PIC18F6390/6490/8390/8490 Data Sheet” (DS39629). Device ID information presented in this section is for the PIC18F6393/6493/8393/8493 devices only.

PIC18F6393/6493/8393/8493 devices include several features intended to maximize reliability and minimize cost through elimination of external components. These include:

- Device ID Registers

## 3.1 Device ID Registers

The Device ID registers are “read-only” registers. They identify the device type and revision to device programmers and can be read by firmware using table reads.

**TABLE 3-1: DEVICE IDs**

File Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default/ Unprogrammed Value
3FFFEh	DEVID1	DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0	xxxx xxxx <sup>(1)</sup>
3FFFFh	DEVID2	DEV10	DEV9	DEV8	DEV7	DEV6	DEV5	DEV4	DEV3	xxxx xxxx <sup>(1)</sup>

**Legend:** x = unknown

**Note 1:** See Register 3-1 and Register 3-2 for DEVID values. DEVID registers are read-only and cannot be programmed by the user.

# PIC18F6393/6493/8393/8493

## REGISTER 3-1: DEVID1: DEVICE ID REGISTER 1 FOR PIC18F6393/6493/8393/8493 DEVICES

R	R	R	R	R	R	R	R
DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0
bit 7							bit 0

**Legend:**

R = Read-only bit                      P = Programmable bit                      U = Unimplemented bit, read as '0'  
 -n = Value when device is unprogrammed                      u = Unchanged from programmed state

bit 7-5                      **DEV2:DEV0:** Device ID bits  
 See Register 3-2 for a complete listing.

bit 4-0                      **REV4:REV0:** Revision ID bits  
 These bits are used to indicate the device revision.

## REGISTER 3-2: DEVID2: DEVICE ID REGISTER 2 FOR PIC18F6393/6493/8393/8493 DEVICES

R	R	R	R	R	R	R	R
DEV10	DEV9	DEV8	DEV7	DEV6	DEV5	DEV4	DEV3
bit 7							bit 0

**Legend:**

R = Read-only bit                      P = Programmable bit                      U = Unimplemented bit, read as '0'  
 -n = Value when device is unprogrammed                      u = Unchanged from programmed state

bit 7-0                      **DEV10:DEV3:** Device ID bits

Device	DEV10:DEV3 (DEVID2<7:0>)	DEV2:DEV0 (DEVID1<7:5>)
PIC18F6393	0001 1010	000
PIC18F6493	0000 1110	000
PIC18F8393	0001 1010	001
PIC18F8493	0000 1110	001

## 4.0 ELECTRICAL CHARACTERISTICS

**Note:** Other than some basic data, this section documents only the PIC18F6393/6493/8393/8493 devices' specifications that differ from those of the PIC18F6390/6490/8390/8490 devices. For detailed information on the electrical specifications shared by the PIC18F6393/6493/8393/8493 and PIC18F6390/6490/8390/8490 devices, see the "PIC18F6390/6490/8390/8490 Data Sheet" (DS39629).

### Absolute Maximum Ratings<sup>(†)</sup>

Ambient temperature under bias .....	-40°C to +125°C
Storage temperature .....	-65°C to +150°C
Voltage on any pin with respect to V <sub>SS</sub> (except V <sub>DD</sub> and $\overline{\text{MCLR}}$ ) .....	-0.3V to (V <sub>DD</sub> + 0.3V)
Voltage on V <sub>DD</sub> with respect to V <sub>SS</sub> .....	-0.3V to +7.5V
Voltage on $\overline{\text{MCLR}}$ with respect to V <sub>SS</sub> ( <b>Note 2</b> ) .....	0V to +13.25V
Total power dissipation ( <b>Note 1</b> ) .....	1.0W
Maximum current out of V <sub>SS</sub> pin .....	300 mA
Maximum current into V <sub>DD</sub> pin .....	250 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>DD</sub> ) .....	±20 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>DD</sub> ) .....	±20 mA
Maximum output current sunk by any I/O pin .....	25 mA
Maximum output current sourced by any I/O pin .....	25 mA
Maximum current sunk by all ports .....	200 mA
Maximum current sourced by all ports .....	200 mA

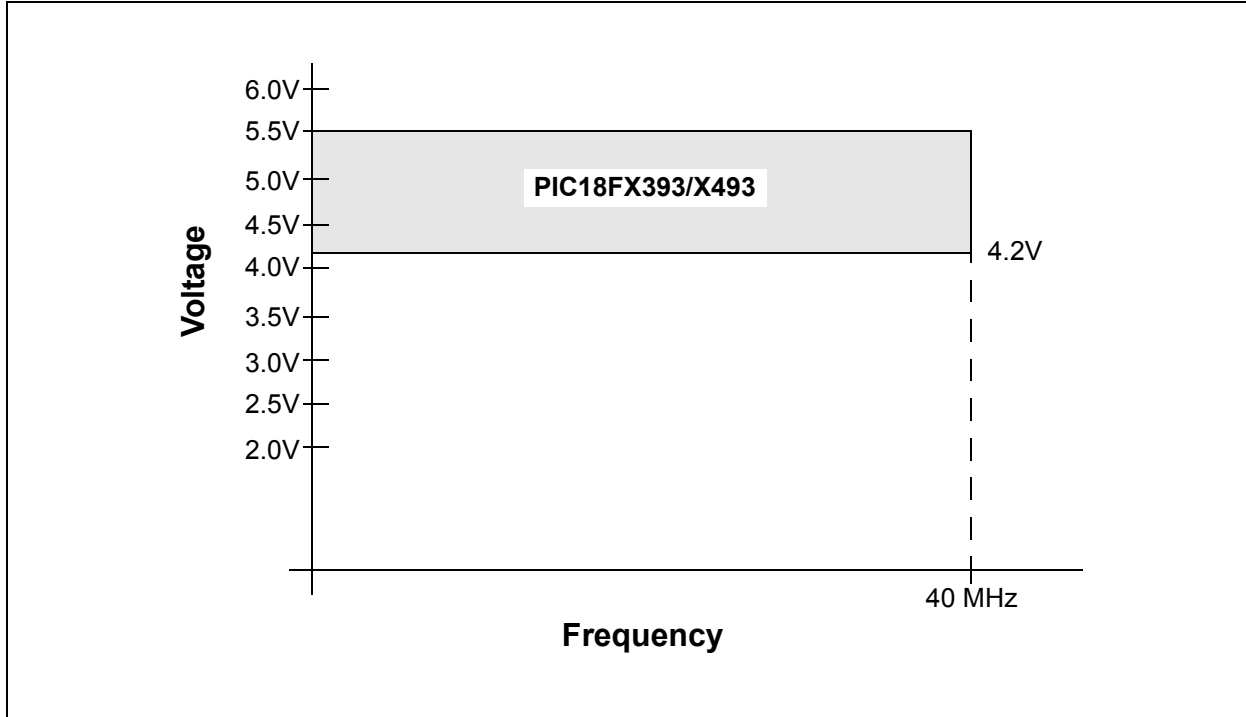
**Note 1:** Power dissipation is calculated as follows:

$$P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$$

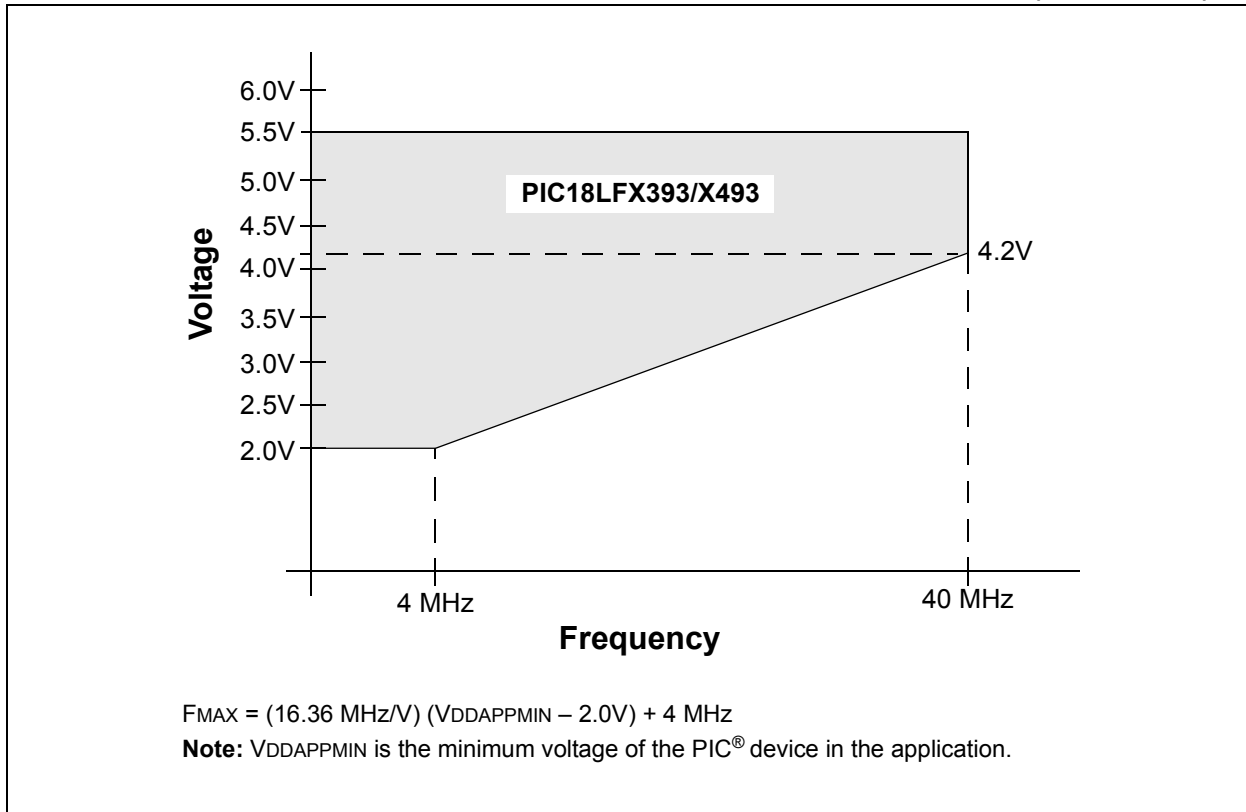
**2:** Voltage spikes below V<sub>SS</sub> at the  $\overline{\text{MCLR}}/\text{VPP}/\text{RG5}$  pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the  $\overline{\text{MCLR}}/\text{VPP}/\text{RG5}$  pin, rather than pulling this pin directly to V<sub>SS</sub>.

† **NOTICE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**FIGURE 4-1: PIC18F6393/6493/8393/8493 VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)**



**FIGURE 4-2: PIC18LF6393/6493/8393/8493 VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)**



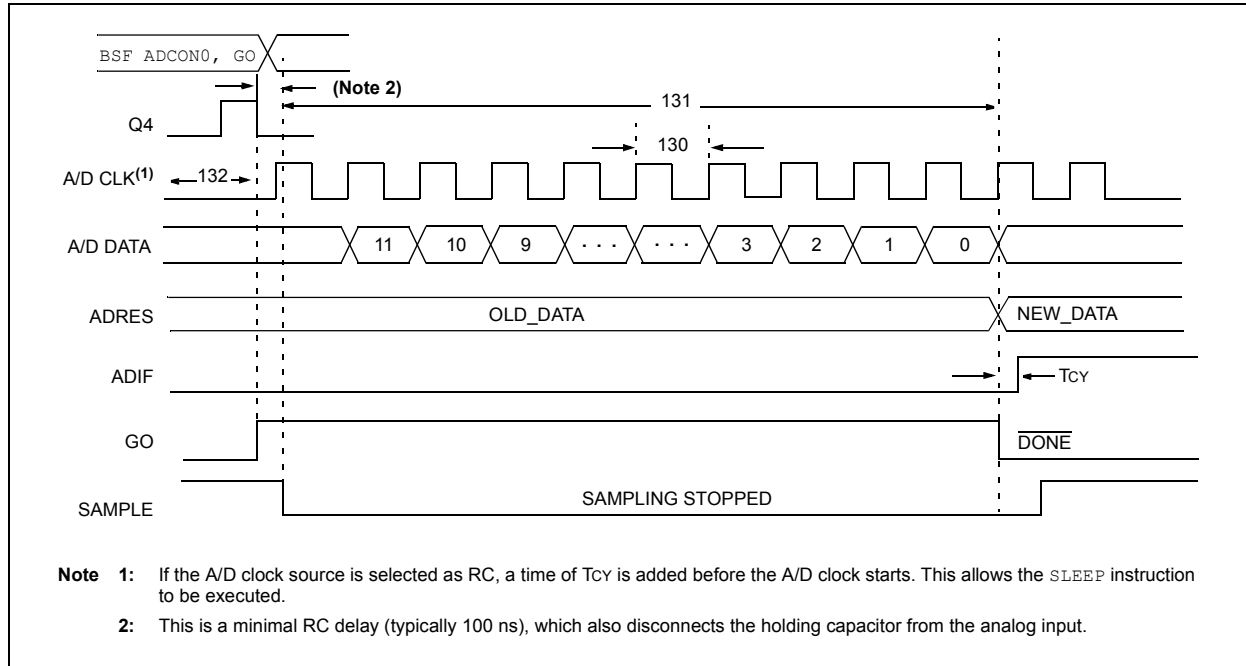
**TABLE 4-1: A/D CONVERTER CHARACTERISTICS: PIC18F6393/6493/8393/8493 (INDUSTRIAL)**

Param No.	Sym	Characteristic	Min	Typ	Max	Units	Conditions	
A01	NR	Resolution	—	—	12	bit	$\Delta V_{REF} \geq 3.0V$	
A03	EIL	Integral Linearity Error	—	$<\pm 1$	$\pm 2.0$	LSB	$V_{DD} = 3.0V$	$\Delta V_{REF} \geq 3.0V$
			—	—	$\pm 2.0$	LSB	$V_{DD} = 5.0V$	
A04	EDL	Differential Linearity Error	—	$<\pm 1$	+1.5/-1.0	LSB	$V_{DD} = 3.0V$	$\Delta V_{REF} \geq 3.0V$
			—	—	+1.5/-1.0	LSB	$V_{DD} = 5.0V$	
A06	EOFF	Offset Error	—	$<\pm 1$	$\pm 5$	LSB	$V_{DD} = 3.0V$	$\Delta V_{REF} \geq 3.0V$
			—	—	$\pm 3$	LSB	$V_{DD} = 5.0V$	
A07	EGN	Gain Error	—	$<\pm 1$	$\pm 2.00$	LSB	$V_{DD} = 3.0V$	$\Delta V_{REF} \geq 3.0V$
			—	—	$\pm 2.00$	LSB	$V_{DD} = 5.0V$	
A10	—	Monotonicity	Guaranteed <sup>(1)</sup>			—	$V_{SS} \leq V_{AIN} \leq V_{REF}$	
A20	$\Delta V_{REF}$	Reference Voltage Range ( $V_{REFH} - V_{REFL}$ )	3	—	$V_{DD} - V_{SS}$	V	For 12-bit resolution	
A21	$V_{REFH}$	Reference Voltage High	$V_{SS} + 3.0V$	—	$V_{DD} + 0.3V$	V	For 12-bit resolution	
A22	$V_{REFL}$	Reference Voltage Low	$V_{SS} - 0.3V$	—	$V_{DD} - 3.0V$	V	For 12-bit resolution	
A25	$V_{AIN}$	Analog Input Voltage	$V_{REFL}$	—	$V_{REFH}$	V		
A30	$Z_{AIN}$	Recommended Impedance of Analog Voltage Source	—	—	2.5	k $\Omega$		
A50	IREF	$V_{REF}$ Input Current <sup>(2)</sup>	—	—	5	$\mu A$	During $V_{AIN}$ acquisition. During A/D conversion cycle.	
			—	—	150	$\mu A$		

**Note 1:** The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

**Note 2:**  $V_{REFH}$  current is from the RA3/AN3/ $V_{REF+}$ /SEG17 pin or  $V_{DD}$ , whichever is selected as the  $V_{REFH}$  source.  $V_{REFL}$  current is from the RA2/AN2/ $V_{REF-}$ /SEG16 pin or  $V_{SS}$ , whichever is selected as the  $V_{REFL}$  source.

**FIGURE 4-3: A/D CONVERSION TIMING**



**TABLE 4-2: A/D CONVERSION REQUIREMENTS**

Param No.	Symbol	Characteristic	Min	Max	Units	Conditions	
130	TAD	A/D Clock Period	PIC18FXXXX	0.8	12.5 <sup>(1)</sup>	$\mu$ S	TOSC based, VREF $\geq$ 3.0V
			PIC18LFXXXX	1.4	25.0 <sup>(1)</sup>	$\mu$ S	VDD = 3.0V; TOSC based, VREF full range
			PIC18FXXXX	—	1	$\mu$ S	A/D RC mode
			PIC18LFXXXX	—	3	$\mu$ S	VDD = 3.0V; A/D RC mode
131	T <sub>cnv</sub>	Conversion Time (not including acquisition time) <sup>(2)</sup>	13	14	TAD		
132	T <sub>Acq</sub>	Acquisition Time <sup>(3)</sup>	1.4	—	$\mu$ S		
135	T <sub>swc</sub>	Switching Time from Convert $\rightarrow$ Sample	—	(Note 4)			
137	T <sub>dis</sub>	Discharge Time	0.2	—	$\mu$ S		

- Note 1:** The time of the A/D clock period is dependent on the device frequency and the TAD clock divider.
- Note 2:** ADRES registers may be read on the following  $T_{CY}$  cycle.
- Note 3:** The time for the holding capacitor to acquire the “New” input voltage when the voltage changes full scale after the conversion (VDD to VSS or VSS to VDD). The source impedance ( $R_S$ ) on the input channels is 50 $\Omega$ .
- Note 4:** On the following cycle of the device clock.

## 5.0 PACKAGING INFORMATION

For packaging information, see the "PIC18F6390/6490/8390/8490 *Data Sheet*" (DS39629).

NOTES:



## APPENDIX A: REVISION HISTORY

### Revision A (September 2007)

Original data sheet for the PIC18F6393/6493/8393/8493 devices.

### Revision B (October 2009)

Removed "Preliminary" marking.

## APPENDIX B: DEVICE DIFFERENCES

The differences between the devices listed in this data sheet are shown in Table B-1.

**TABLE B-1: DEVICE DIFFERENCES**

Features	PIC18F6393	PIC18F6493	PIC18F8393	PIC18F8493
Number of Pixels the LCD Driver Can Drive	128 (4 x 32)	128 (4 x 32)	192 (4 x 48)	192 (4 x 48)
I/O Ports	Ports A, B, C, D, E, F, G	Ports A, B, C, D, E, F, G	Ports A, B, C, D, E, F, G, H, J	Ports A, B, C, D, E, F, G, H, J
Flash Program Memory	8 Kbytes	16 Kbytes	8 Kbytes	16 Kbytes
Packages	64-Pin TQFP	64-Pin TQFP	80-Pin TQFP	80-Pin TQFP

## APPENDIX C: CONVERSION CONSIDERATIONS

This appendix discusses the considerations for converting from previous versions of a device to the ones listed in this data sheet. Typically, these changes are due to the differences in the process technology used. An example of this type of conversion is from a PIC16C74A to a PIC16C74B.

**Not Applicable**

## APPENDIX D: MIGRATION FROM BASELINE TO ENHANCED DEVICES

This section discusses how to migrate from a Baseline device (i.e., PIC16C5X) to an Enhanced MCU device (i.e., PIC18FXXX).

The following are the list of modifications over the PIC16C5X microcontroller family:

**Not Currently Available**

---

## APPENDIX E: MIGRATION FROM MID-RANGE TO ENHANCED DEVICES

A detailed discussion of the differences between the mid-range MCU devices (i.e., PIC16CXXX) and the enhanced devices (i.e., PIC18FXXX) is provided in AN716, "*Migrating Designs from PIC16C74A/74B to PIC18C442*". The changes discussed, while device-specific, are generally applicable to all mid-range to enhanced device migrations.

This Application Note is available as Literature Number DS00716.

## APPENDIX F: MIGRATION FROM HIGH-END TO ENHANCED DEVICES

A detailed discussion of the migration pathway and differences between the high-end MCU devices (i.e., PIC17CXXX) and the enhanced devices (i.e., PIC18FXXX) is provided in AN726, "*PIC17CXXX to PIC18CXXX Migration*". This Application Note is available as Literature Number DS00726.

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## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>X</u>	<u>/XX</u>	<u>XXX</u>
Device	Temperature Range	Package	Pattern
Device <sup>(1), (2)</sup>	PIC18F6393, PIC18F6493, PIC18F8393, PIC18F8493 – VDD range: 4.2V to 5.5V PIC18LF6393, PIC18LF6493, PIC18LF8393, PIC18LF8493 – VDD range: 2.0V to 5.5V		
Temperature Range	I = -40°C to +85°C (Industrial) E = -40°C to +125°C (Extended)		
Package	PT = TQFP (Thin Quad Flatpack)		
Pattern	QTP, SQTP, Code or Special Requirements (blank otherwise)		

**Examples:**

- a) PIC18LF6393-I/PT 301 = Industrial temp., TQFP package, Extended VDD limits, QTP pattern #301.
- b) PIC18LF6393-I/PT = Industrial temp., TQFP package, Extended VDD limits.
- c) PIC18F6393-E/PT = Extended temp., TQFP package, normal VDD limits.

**Note 1:** F = Standard Voltage Range  
 LF = Wide Voltage Range  
**2:** T = in tape and reel TQFP packages only.

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