RENESAS

R1LV0816ASB – 5SI, 7SI

8Mb Advanced LPSRAM (512k word x 16bit)

REJ03C0387-0100 Rev.1.00 2009.12.07

Description

The R1LV0816ASB is a family of low voltage 8-Mbit static RAMs organized as 524,288-words by 16-bit, fabricated by Renesas's high-performance 0.15um CMOS and TFT technologies.

The R1LV0816ASB is suitable for memory applications where a simple interfacing, battery operating and battery backup are the important design objectives.

The R1LV0816ASB is packaged in a 44pin thin small outline mount device [11.76mm×18.41mm 44-pin plastic TSOP (II)]. It gives the best solution for a compaction of mounting area as well as flexibility of wiring pattern of printed circuit boards.

Features

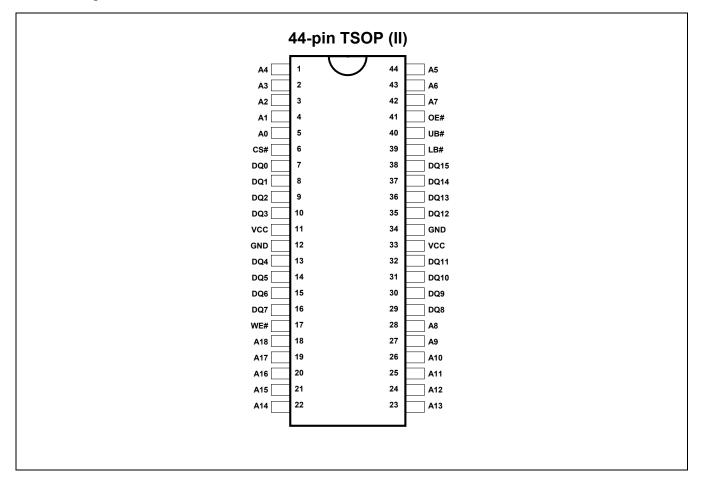
- Single 2.4-3.6V power supply
- Small stand-by current: 1.2µA (Vcc=3.0V, typ.)
- No clocks, No refresh
- All inputs and outputs are TTL compatible
- Easy memory expansion by CS#, LB# and UB#
- Common Data I/O
- Three-state outputs: OR-tie capability
- OE# prevents data contention in the I/O bus
- Operation temperature: -40 ~ +85°C

Type No.	Power supply	Access time	Temperature Range	Package
R1LV0816ASB-5SI	2.7V to 3.6V	55 ns		11 76mmy 19 41mm 14 pip plastic TSOD (II)
R1LV0010A3D-031	2.4V to 2.7V	70 ns	-40 ~ +85°C	11.76mm×18.41mm 44-pin plastic TSOP (II) (normal-bend type) (44P3F)
R1LV0816ASB-7SI	2.4V to 3.6V	70 ns		

Ordering information



Pin Arrangement



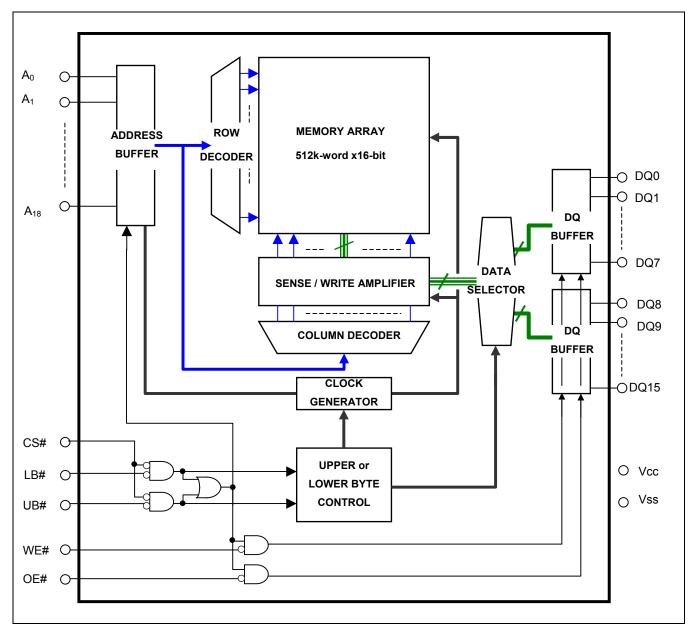


Pin Description

Pin name	Function
Vcc	Power supply
Vss	Ground
A0 to A18	Address input (word mode)
DQ0 to DQ15	Data input/output
CS#	Chip select
WE#	Write enable
OE#	Output enable
LB#	Lower byte enable
UB#	Upper byte enable



Block Diagram



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Operation Table

CS#	WE#	OE#	UB#	LB#	DQ0~7	DQ8~15	Operation
Н	Х	Х	Х	Х	High-Z	High-Z	Stand-by
Х	Х	Х	Н	Н	High-Z	High-Z	Stand-by
L	L	Х	Н	L	Din	High-Z	Write in lower byte
L	Н	L	Н	L	Dout	High-Z	Read in lower byte
L	L	Х	L	Н	High-Z	Din	Write in upper byte
L	Н	L	L	Н	High-Z	Dout	Read in upper byte
L	L	Х	L	L	Din	Din	Word write
L	Н	L	L	L	Dout	Dout	Word read
L	Н	Н	L	L	High-Z	High-Z	Output disable
L	Н	Н	L	Н	High-Z	High-Z	Output disable
L	Н	Н	Н	L	High-Z	High-Z	Output disable

Note 1. H: V_{IH} L: V_{IL} X: V_{IH} or V_{IL}

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage relative to Vss	Vcc	-0.5 to +4.6	V
Terminal voltage on any pin relative to Vss	VT	-0.5 ^{*1} to Vcc+0.3 ^{*2}	V
Power dissipation	PT	0.7	W
Operation temperature	Topr	-40 to +85	°C
Storage temperature range	Tstg	-65 to 150	°C
Storage temperature range under bias	Tbias	-40 to +85	°C

Note 1. -3.0V in case of AC (Pulse width ≤30ns)

2. Maximum voltage is +4.6V



Recommend Operating Conditions

Parameter	Symbol	Min.	Тур.	Max.	Unit	Test conditions	Note
Supply voltage	Vcc	2.4	3.0	3.6	V	-	
	Vss	0	0	0	V	-	
Input high voltage	V	2.0	-	Vcc+0.2	V	Vcc=2.4V to 2.7V	
	V _{IH}	2.2	-	Vcc+0.2	V	Vcc=2.7V to 3.6V	
Input low voltage	V	-0.2	-	0.4	V	Vcc=2.4V to 2.7V	1
	VIL	-0.2	-	0.6	V	Vcc=2.7V to 3.6V	1
Ambient temperature range	Та	-40	-	+85	°C	-	

Note 1. -3.0V in case of AC (Pulse width ≤30ns)

DC Characteristics

Parameter	Symbol	Min.	Тур.	Max.	Unit	Test conditions			
Input leakage current	I _{LI}	-	-	1	μA	Vin = Vss to Vcc			
Output leakage current	I _{LO}	-	-	1	μA	CS# =V _{IH} or OE# =V _{IH} or WE# =V _{IL} or LB# = UB# =V _{IH} , VI/O =Vss to Vcc			
Average operating current	I _{CC1}	-	20 ^{*1}	35	mA	Min. cycle, duty =100%, II/O = 0mA CS# =V _{IL} , Others = V_{IH}/V_{IL}			
	I _{CC2}	-	2 ^{*1}	5	mA	Cycle =1 s, duty =100%, II/O = 0mA CS# \leq 0.2V, V _{IH} \geq V _{CC} -0.2V, V _{IL} \leq 0.2			
Standby current	I _{SB}	-	-	1	mA	CS# =V _{IH}			
Standby current		-	1.2 ^{*1}	4	μA	~+25°C	Vin ≥ 0V		
	I _{SB1}	-	3 ^{*2}	6	μA	~+40°C	(1) CS# \geq V _{CC} -0.2V or (2) LB# = UB# \geq V _{CC} -0.2V,		
		-	-	15	μA	~+70°C	CS# ≤ 0.2V,		
		-	-	20	μA	~+85°C			
Output high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -1mA Vcc≥2.7V			
	V _{OH2}	2.0	-	-	V	I _{OH} = -0.1mA			
Output low voltage	V _{OL}	-	-	0.4	v	$V = \begin{cases} I_{OL} = 2mA \\ Vcc \ge 2.7V \end{cases}$			
	V _{OL2}	-	-	0.4	V	I _{OL} = 0.1mA			

Note 1.Typical parameter indicates the value for the center of distribution at 3.0V(Ta=+25°C), and not 100% tested. 2.Typical parameter indicates the value for the center of distribution at 3.0V(Ta=+40°C), and not 100% tested.

Capacitance

(Ta =25°C, f =1MHz)

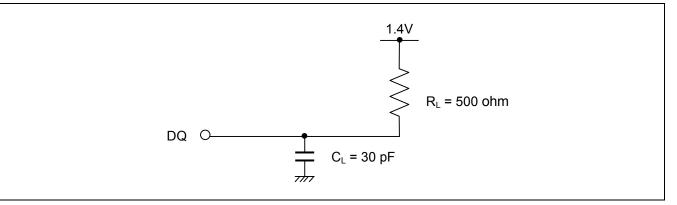
Input capacitance C in 10 pF Vin =0V 1								
Input capacitance C in 10 pF Vin = 0V 1	Parameter	Symbol	Min.	Тур.	Max.	Unit	Test conditions	Note
Input / output capacitance C up 10 pE V/up =0// 1	Input capacitance	C in	-	-	10	pF	Vin =0V	1
	Input / output capacitance	C I/O	-	-	10	pF	V _{I/O} =0V	1

Note 1.Typical parameter is sampled and not 100% tested.

AC Characteristics

Test Conditions (Vcc = $2.4V \sim 3.6V$, Ta = $-40 \sim +85^{\circ}C$)

- Input pulse levels: VIL = 0.4V, VIH = 2.4V (Vcc = 2.7V ~ 3.6 V)
 VIL = 0.4V, VIH = 2.2V (Vcc = 2.4V ~ 2.7 V)
- Input rise and fall times: 5ns
- Input and output timing reference level: 1.4V
- Output load: See figures (Including scope and jig)





Read cycle

Parameter	Symbol		6ASB-5SI te 0)	R1LV081	6ASB-7SI	Unit	Note
		Min.	Max.	Min.	Max.		
Read cycle time	t _{RC}	55	-	70	-	ns	
Address access time	t _{AA}	-	55	-	70	ns	
Chip select access time	t _{ACS}	-	55	-	70	ns	
Output enable to output valid	t _{OE}	-	30	-	35	ns	
Output hold from address change	t _{он}	10	-	10	-	ns	
LB#, UB# access time	t _{BA}	-	55	-	70	ns	
Chip select to output in low-Z	t _{CLZ}	10	-	10	-	ns	2,3
LB#, UB# enable to low-Z	t _{BLZ}	5	-	5	-	ns	2,3
Output enable to output in low-Z	t _{oLZ}	5	-	5	-	ns	2,3
Chip deselect to output in high-Z	t _{CHZ}	0	20	0	25	ns	1,2,3
LB#, UB# disable to high-Z	t _{BHZ}	0	20	0	25	ns	1,2,3
Output disable to output in high-Z	t _{OHZ}	0	20	0	25	ns	1,2,3





Write Cycle

Parameter	Symbol		6ASB-5SI ote 0)	R1LV0816ASB-7SI		Unit	Note
		Min.	Max.	Min.	Max.		
Write cycle time	t _{wc}	55	-	70	-	ns	
Address valid to end of write	t _{AW}	50	-	65	-	ns	
Chip select to end of write	t _{CW}	50	-	65	-	ns	5
Write pulse width	t _{WP}	40	-	55	-	ns	4
LB#, UB# valid to end of write	t _{BW}	50	-	65	-	ns	
Address setup time	t _{AS}	0	-	0	-	ns	6
Write recovery time	t _{WR}	0	-	0	-	ns	7
Data to write time overlap	t _{DW}	25	-	35	-	ns	
Data hold from write time	t _{DH}	0	-	0	-	ns	
Output enable from end of write	t _{ow}	5	-	5	-	ns	2
Output disable to output in high-Z	t _{OHZ}	0	20	0	25	ns	1,2
Write to output in high-Z	t _{WHZ}	0	20	0	25	ns	1,2

Note 0. If Vcc is 2.4-2.7V, parameters of R1LV0816ASB-7SI (70ns) are applied.

- 1. t_{CHZ}, t_{OHZ}, t_{WHZ} and t_{BHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
- 2. Typical parameter is sampled and not 100% tested.
- 3. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for given device and from device to device.
- 4. A write occurs during the overlap of a low CS#, a low WE# and a low LB# or low UB#.

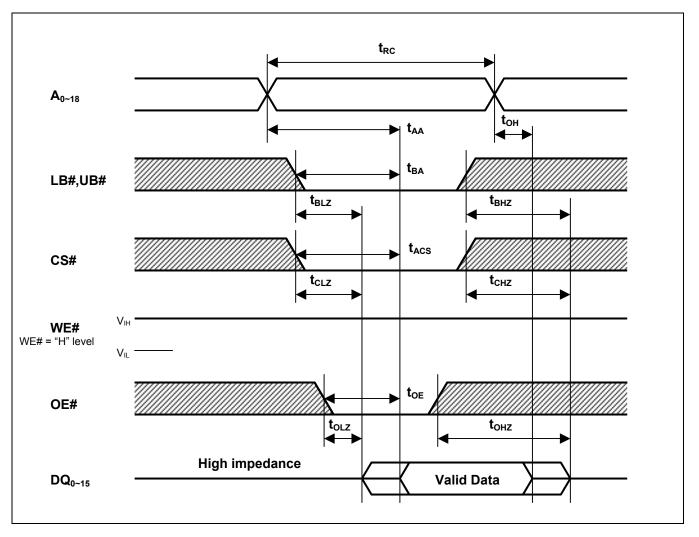
A write begins at the latest transitions among CS# going low, WE# going low and LB# going low or UB# going low. A write ends at the earliest transitions among CS# going high, WE# going high and LB# going high or UB# going high. t_{WP} is measured from the beginning of write to the end of write.

- 5. t_{CW} is measured from the later of CS# going low to the end of write.
- 6. t_{AS} is measured the address valid to the beginning of write.
- 7. t_{WR} is measured from the earliest of CS# or WE# going high to the end of write cycle.



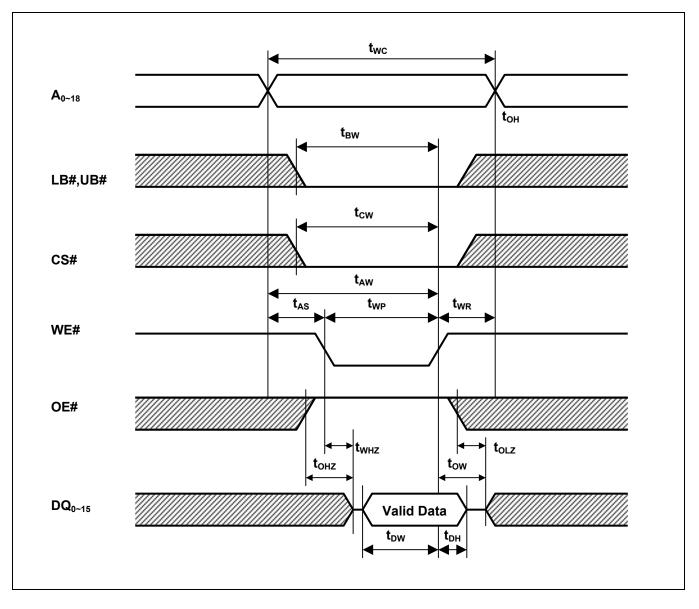
Timing Waveforms

Read Cycle



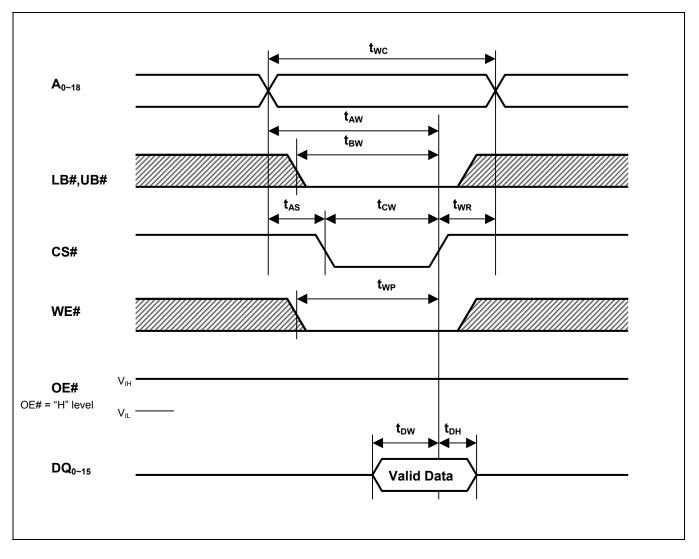


Write Cycle (1) (WE# CLOCK)



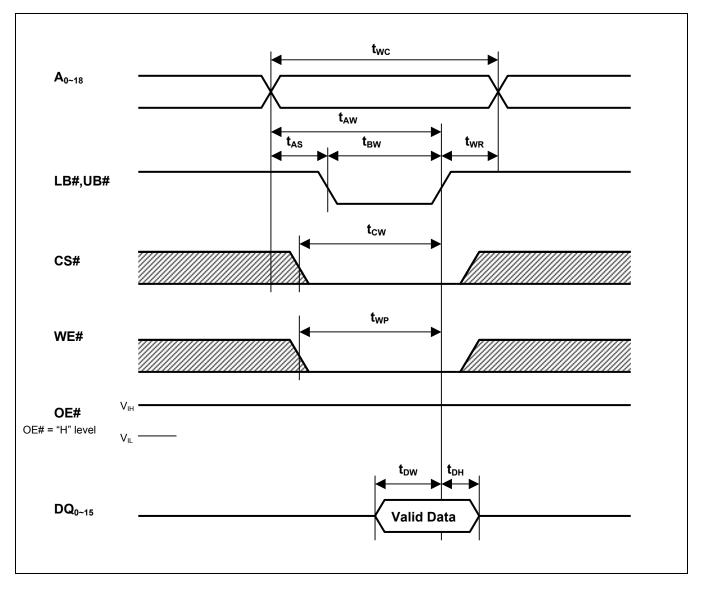


Write Cycle (2) (CS# CLOCK)





Write Cycle (3) (LB#, UB# CLOCK)





Data Retention Characteristics

Parameter	Symbol	Min.	Тур.	Max.	Unit	Test conditions ^{*3}		
V_{CC} for data retention	V _{DR}	1.5	-	3.6	V	Vin ≥ 0V (1) CS# ≥ V _{CC} -0.2V, (2) LB# = UB# ≥ V _{CC} -0.2V, CS# ≤ 0.2V,		
	Iccdr	-	1.2 ^{*1}	4	μA	~+25°C	Vcc=3.0V, Vin ≥ 0V	
Data retention current		-	3 ^{*2}	6	μA	~+40°C	(1) CS# ≥ V _{cc} -0.2V or	
		-	-	15	μA	~+70°C	(2) LB# = UB# ≥ V_{CC} -0.2V, CS# ≤ 0.2V,	
		-	-	20	μA	~+85°C		
Chip select to data retention time	t _{CDR}	0	-	-	ns	See reter	tion waveform	
Operation recovery time	t _R	5	-	-	ms	- See retention waveform.		

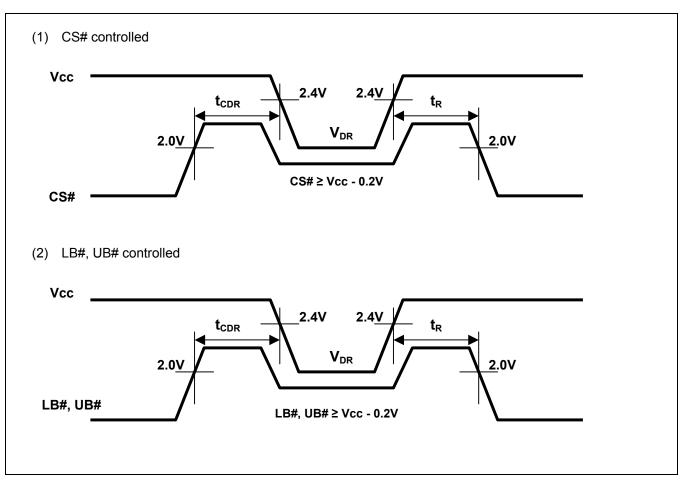
Note 1.Typical parameter indicates the value for the center of distribution at 3.0V(Ta=+25°C), and not 100% tested.

2. Typical parameter indicates the value for the center of distribution at 3.0V(Ta=+40°C), and not 100% tested.

3.CS# controls address buffer, WE# buffer, OE# buffer, LB#, UB# buffer and Din buffer. If CS# controls data retention mode, Vin levels (address, WE#, OE#, LB#, UB#, DQ) can be in the high impedance state.



Data Retention Timing Waveforms





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April 1st, 2010 Renesas Electronics Corporation

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