AKD4686-B

AK4686 Evaluation Board Rev.0

FEATURE

AKD4686-B is an evaluation board for AK4686, a single chip 24bit CODEC that has one stereo ADC and two stereo DAC. This board has interfaces with AKM's evaluation boards for A/D converter and D/A converter and makes easy to evaluate AK4686. Also this board has the digital audio interface and then achieves the interface with digital audio systems via RCA connector.

■ **Ordering guide**

AKD4686-B --- Evaluation Board for AK4686
(Cable for connecting with printer port of IBM-AT compatible PC and control software are packed with this. This control software does not operate on Windows NT.)

FUNCTION

- ☐ **On-board clock generators (AK4118 x 2)**
- ☐ **Compatible with 2 types of digital audio interface**
  - **RCA (S/PDIF) input/output**
  - **10pin headers for interfacing with external data source (x2)**
- ☐ **RCA connectors for clock input with external clock source**
- ☐ **10pin header for register control**

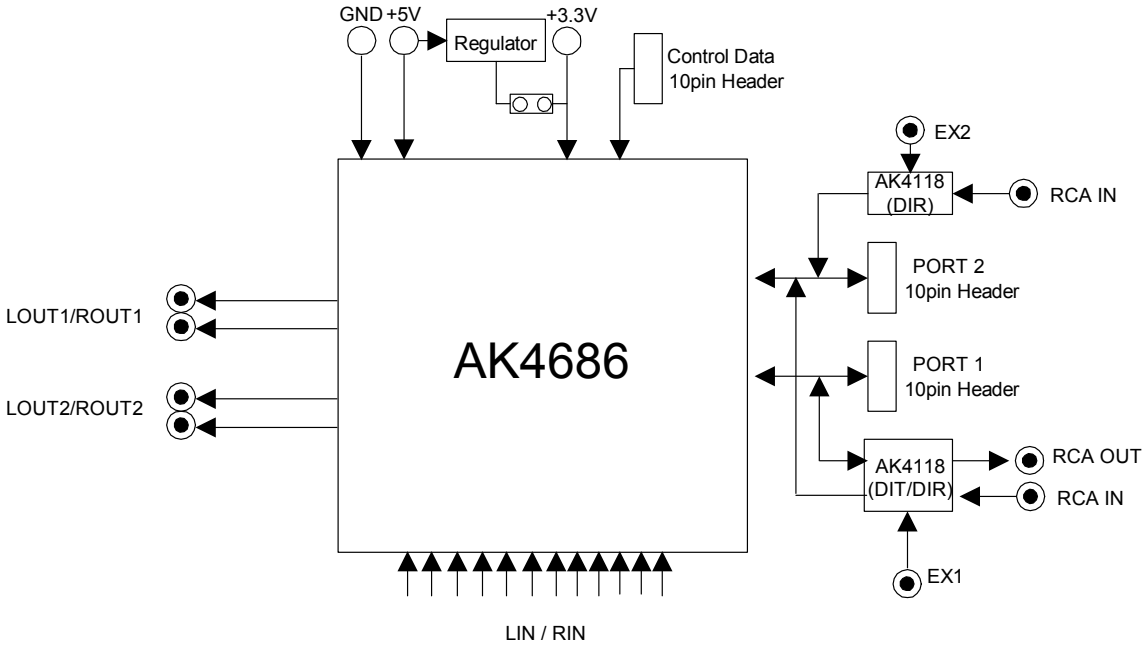


Figure 1. AKD4686-B Block Diagram
(* Circuit diagram and PCB layout are attached at the end of this manual.)

EVALUATION BOARD MANUAL

■ Operating sequence

1. Set up power supply lines.

Name of Jack	Color of Jack	Voltage	Used for	Comment and attention	Default
+5V	Red	+4.5~+5.5V	Regulator T2, T5	Should be always connected	+5V
AVDD1	Orange	+3.0~+3.6V	AVDD1 of AK4686	Should be open when JP40 (AVDD1_SEL) is set to REG side. Should be connected when JP40 (AVDD1_SEL) is set to AVDD1 side.	Open
AVDD2	Orange	+3.0~+3.6V	AVDD2 of AK4686	Should be open when JP41 (AVDD2_SEL) is set to REG side. Should be connected when JP41 (AVDD2_SEL) is set to AVDD2 side.	Open
DVDD	Orange	+3.0~+3.6V	DVDD of AK4686	Should be open when JP42 (DVDD_SEL) is set to REG side. Should be connected when JP42 (DVDD_SEL) is set to DVDD side.	Open
CVDD	Orange	+3.0~+3.6V	CVDD of AK4686	Should be connected when default. Should be open in case of using regulator T2 when R85 is short and L7 is open.	+3.3V
D3.3V	Orange	+3.0~+3.6V	Power supply of logic	Should be open when JP45 (D3.3V_SEL) is set to REG side. Should be connected when JP45 (D3.3V_SEL) is set to D3.3V side.	Open
VSS1	Black	0V	Analog Ground	Should be always connected	0V
VSS2	Black	0V	Analog Ground	Should be always connected	0V
VSS3	Black	0V	Analog Ground	Should be always connected	0V
VSS4	Black	0V	Analog Ground	Should be always connected	0V
DGND	Black	0V	Digital Ground	Should be always connected	0V

Table 1. Power supply lines

Each supply line should be distributed from the power supply unit.

2. Set up evaluation mode and jumper pins. (Refer to the following item.)

3. Connect cables. (Refer to the following item.)

4. Power on.
The AK4686 (U1) should be reset once bringing SW1 (PDN) “L” upon power-up.
Keep “H” during normal operaion.

5. Set up control software registers. (Refer to the following item.)

■ Evaluation modes

(1) DAC with external DIR (Synchronous mode)

1. Connection of connector
   For digital (S/PDIF) input, RCA connectors J12 (PORT1 RX0) and J15 (PORT2 RX0) are available.
   For analog output, RCA connectors J5 (LOUT1)/JP6 (ROUT1), J7 (LOUT2)/J8 (ROUT2) are available.

2. Setting of jumper pin
   Setting of interface signal of PORT1: AK4118 (U4) is as follows.

Jumper	JP19	JP20	JP21	JP22	JP23	JP50	
	XTI1	MCKO_SEL1	MCLK1_SEL	BICK1_SEL	LRCK1_SEL	SDTI1	
Setting	Open	MCKO1	Short	Short	Short	Short	(Default)

Table 2. Setting of interface signal of PORT1: AK4118 (U4) (1/3)

Setting of interface signal of PORT2: AK4118 (U7) is as follows.

Jumper	JP26	JP27	JP28	JP29	JP30	JP31
	XTI2	MCKO_SEL2	MCLK2_SEL	BICK2_SEL	LRCK2_SEL	SDTI2_SEL
Setting	Open	Don't care	MCDIR1	BIDIR1	LRDIR1	SDDIR1

Table 3. Setting of interface signal of PORT2: AK4118 (U7) (1/3)

3. Setting of toggle switch

Switch	SW2	SW5	SW6	SW7
Setting	H	L	H	H

Table 4. Setting of interface signal of PORT1, PORT2: AK4118 (U4,U7) (2/3)

4. Setting of DIP switch

Switch	SW3					
	DIF0	DIF1	DIF2	CM0	OCKS0	OCKS1
Setting	H	L	H	L	L	H

Table 5. Setting of interface signal of PORT1: AK4118 (U4) (3/3)

Switch	SW4					
	DIF0	DIF1	DIF2	CM0	OCKS0	OCKS1
Setting	Don't care	Don't care	Don't care	Don't care	Don't care	Don't care

Table 6. Setting of interface signal of PORT2: AK4118 (U7) (3/3)

(2) DAC with external DIR (Asynchronous mode)

1. Connection of connector
   For digital (S/PDIF) input, RCA connectors J12 (PORT1 RX0) and J15 (PORT2 RX0) are available.
   For analog output, RCA connectors J5 (LOUT1)/JP6 (ROUT1), J7 (LOUT2)/J8 (ROUT2) are available.

2. Setting of jumper pin
   Setting of interface signal of PORT1: AK4118 (U4) is as follows.

Jumper	JP19	JP20	JP21	JP22	JP23	JP50	
	XTI1	MCKO_SEL1	MCLK1_SEL	BICK1_SEL	LRCK1_SEL	SDTI1	
Setting	Open	MCKO1	Short	Short	Short	Short	(Default)

Table 7. Setting of interface signal of PORT1: AK4118 (U4) (1/3)

Setting of interface signal of PORT2: AK4118 (U7) is as follows.

Jumper	JP26	JP27	JP28	JP29	JP30	JP31	
	XTI2	MCKO_SEL2	MCLK2_SEL	BICK2_SEL	LRCK2_SEL	SDTI2_SEL	
Setting	Open	MCKO1	MCDIR2	BIDIR2	LRDIR2	SDDIR2	(Default)

Table 8. Setting of interface signal of PORT2: AK4118 (U7) (1/3)

3. Setting of toggle switch

Switch	SW2	SW5	SW6	SW7
Setting	H	H	H	H

Table 9. Setting of interface signal of PORT1, PORT2: AK4118 (U4, U7) (2/3)

4. Setting of DIP switch

Switch	SW3						
	DIF0	DIF1	DIF2	CM0	OCKS0	OCKS1	
Setting	H	L	H	L	L	H	(Default)

Table 10. Setting of interface signal of PORT1: AK4118 (U4) (3/3)

Switch	SW4						
	DIF0	DIF1	DIF2	CM0	OCKS0	OCKS1	
Setting	H	L	H	L	L	H	(Default)

Table 11. Setting of interface signal of PORT2: AK4118 (U7) (3/3)

(3) ADC with external DIT

1. Connection of connector
   For analog input, RCA connector JL1(LIN1), JL2(LIN2), JL3(LIN3), JL4(LIN4), JL5(LIN5), JL6(LIN6) and JR1(RIN1), JR2(RIN2), JR3(RIN3), JR4(RIN4), JR5(RIN5), JR6(RIN6) are available.
   For digital (S/PDIF) output, RCA connector J13 (PORT1 TX1) is available.

2. Setting of jumper pin
   Setting of interface signal of PORT1: AK4118 (U4) is as follows.
   X1 (24.576MHz) is used as Clock (512fs) .

Jumper	JP19	JP20	JP21	JP22	JP23	JP24	
	XTI1	MCKO1_SEL	MCLK1_SEL	BICK1_SEL	LRCK1_SEL	SDTO1_SEL	
Setting	Open	MCKO1	Short	Short	Short	Short	(Default)

Table 12. Setting of interface signal of PORT1: AK4118 (U4) (1/3)

3. Setting of toggle switch

Switch	SW2	SW5
Setting	H	L

Table 13. Setting of reset of PORT1 AK4118 (U4) (2/3)

4. Setting of DIP switch

Switch	SW3						
	DIF0	DIF1	DIF2	CM0	OCKS0	OCKS1	MS1
Setting	H	L	H	H	L	H	L

Table 14. Setting of interface signal of PORT1: AK4118 (U4) (3/3)

■ Register control

AKD4686-B can be controlled via the printer port (parallel port) of IBM-AT compatible PC. Connect PORT3 (uP-I/F) to PC by 10-line flat cable packed with this. Take care of the direction of connector.

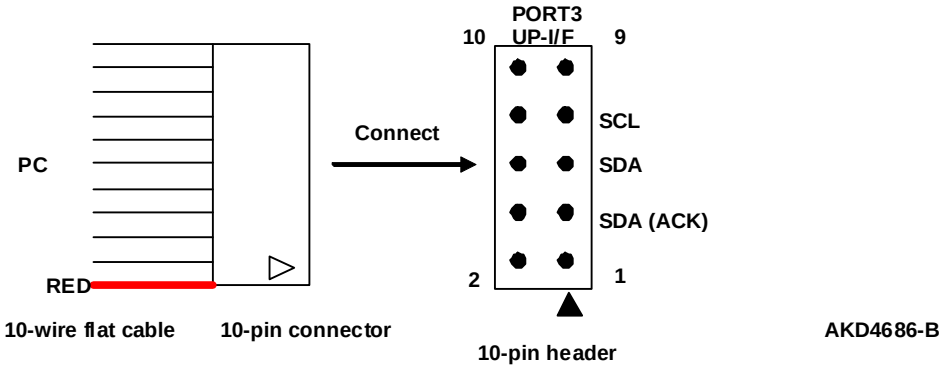


Figure 2. PORT1 pin layout

■ Set-up DIP switch (SW3, 4)

No.	Name	Content	Default
SW3-1	DIF0	Setting of AK4118 Audio Interface Format (Refer Table 16.)	ON
SW3-2	DIF1		OFF
SW3-3	DIF2		ON
SW3-4	CM0	Selection of AK4118 Clock Mode (Clock Source) (Refer Table 17.)	OFF
SW3-6	OCKS0	Selection of AK4118 Master Clock Output frequency (Refer Table 18.)	OFF
SW3-7	OCKS1		ON
SW3-8	MS1	PORT1 Master Mode/Slave Mode Switch (Refer to the AK4686's datasheet)	OFF
SW4-1	DIF0	Setting of AK4118 Audio Interface Format (Refer Table 16.)	ON
SW4-2	DIF1		OFF
SW4-3	DIF2		ON
SW4-4	CM0	Selection of AK4118 Clock Mode (Clock Source) (Refer Table 17.)	OFF
SW4-6	OCKS0	Selection of AK4118 Master Clock Output frequency (Refer Table 18.)	OFF
SW4-7	OCKS1		ON

Table 15. Set up modes of AK4118 (U4, U7) and AK4686 (U1)

Mode	DIF2	DIF1	DIF0	DAUX	SDTO	LRCK		BICK		
							I/O		I/O	
0	0	0	0	24bit, Left justified	16bit, Right justified	H/L	O	64fs	O	
1	0	0	1	24bit, Left justified	18bit, Right justified	H/L	O	64fs	O	
2	0	1	0	24bit, Left justified	20bit, Right justified	H/L	O	64fs	O	
3	0	1	1	24bit, Left justified	24bit, Right justified	H/L	O	64fs	O	
4	1	0	0	24bit, Left justified	24bit, Left justified	H/L	O	64fs	O	
5	1	0	1	24bit, I^2S	24bit, I^2S	L/H	O	64fs	O	<Default>
6	1	1	0	24bit, Left justified	24bit, Left justified	H/L	I	64-128fs	I	
7	1	1	1	24bit, I^2S	24bit, I^2S	L/H	I	64-128fs	I	

Table 16. AK4118 Audio Interface Format

Mode	CM0	PLL	X'tal	Clock source	SDTO	
0	0	ON	ON	PLL	RX	<Default>
1	1	OFF	ON	X'tal	DAUX	

Table 17. AK4118 Clock Mode (Clock Source)

No.	OCKS1	OCKS0	MCKO1	MCKO2	X'tal	fs (max)	
0	0	0	256fs	256fs	256fs	96 kHz	
1	0	1	256fs	128fs	256fs	96 kHz	
2	1	0	512fs	256fs	512fs	48 kHz	<Default>
3	1	1	128fs	64fs	128fs	192 kHz	

Table 18. AK4118 Master Clock Output Frequency

■ Toggle switch

[SW1] PDN:
A switch for power down reset of AK4686 (U1). Keep "H" during operation of AK4686 (U1).
Power down reset of AK4686 will be done by setting SW1 to "L" once, after power on.

[SW2] AK4118 (U4)-PDN:
A switch for power down reset of AK4118 (U4). Keep "H" during operation of AK4118 (U4).
Power down reset of AK4118 (U4) will be done by setting SW2 to "L" once, after power on.

[SW5] AK4118 (U7)-PDN:
A switch for power down reset of AK4118 (U7). Keep "H" during operation of AK4118 (U7).
Power down reset of AK4118 (U7) will be done by setting SW5 to "L" once, after power on.

[SW6] MT1N:
A switch for LOUT1/ROUT1 mute control. Keep SW6 "H" during normal operation of AK4686 (U1)'s DAC1.
Analog output will be muted by setting SW6 to "L".
Refer to Page 20 of AK4686's datasheet for analog soft mute function of AK4686.

[SW7] MT2N:
A switch for LOUT2/ROUT2 mute control. Keep SW7 "H" during normal operation of AK4686 (U1)'s DAC2.
Analog output will be muted by setting SW7 to "L".
Refer to Page 20 of AK4686's datasheet for analog soft mute function of AK4686.

■ LED indication

[LED1] ERF:
An error detection for AK4118(U4). It turns on when output of AK4118 (U4): INT0 is "H".

[LED2] ERF:
An error detection for AK4118(U7). It turns on when output of AK4118 (U7): INT0 is "H".

■ Analog Input Circuit

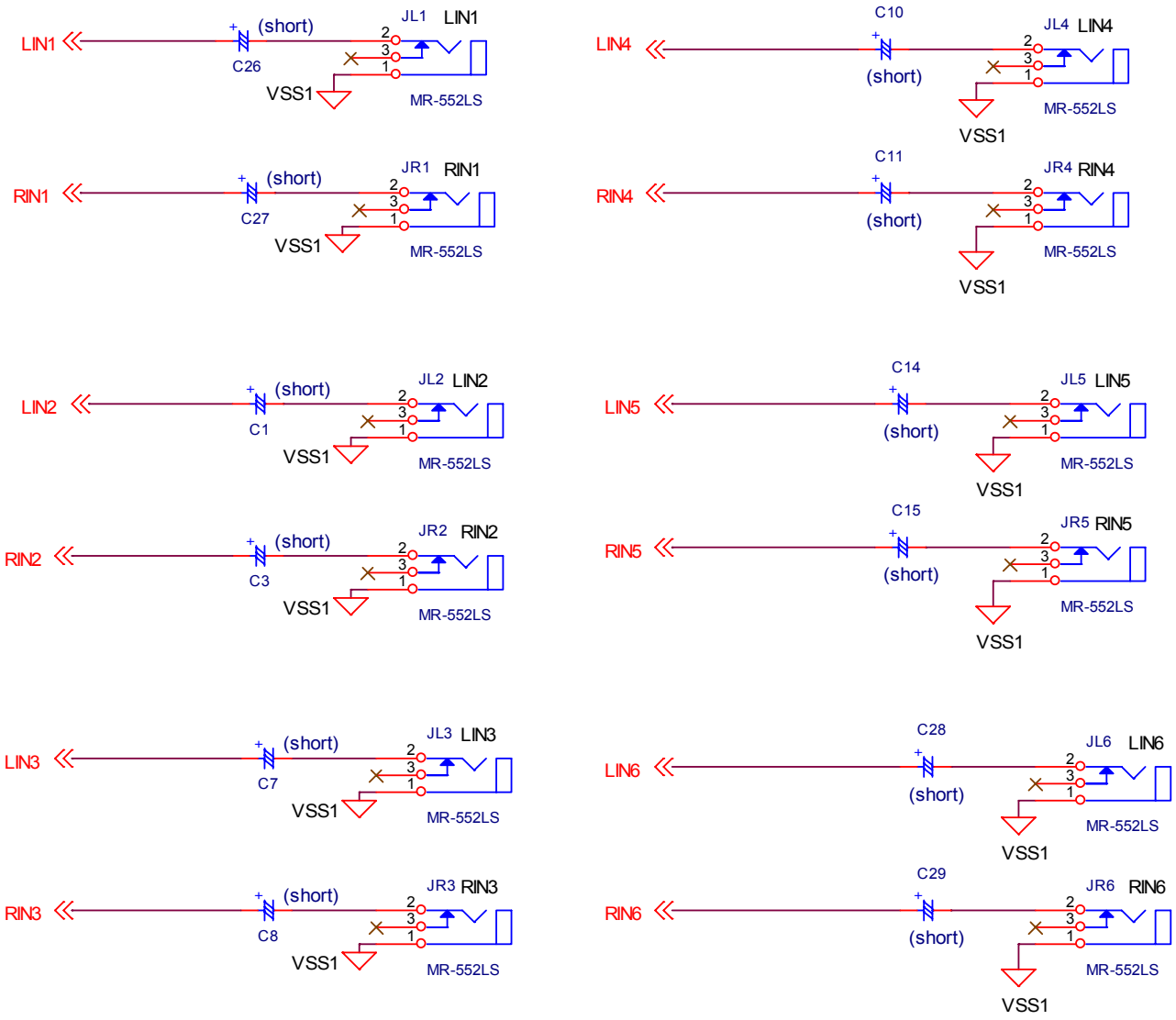


Figure 3. Analog Input Circuit

For analog input, RCA connector: JL1(LIN1), JL2(LIN2), JL3(LIN3), JL4(LIN4), JL5(LIN5), JL6(LIN6) and JR1(RIN1), JR2(RIN2), JR3(RIN3), JR4(RIN4), JR5(RIN5), JR6(RIN6) are available to use.
Analog inputs are single-ended and input range of each channel is 2.2Vrms (typ) when AVDD1=3.3Vrms.

■ Analog Output Circuit

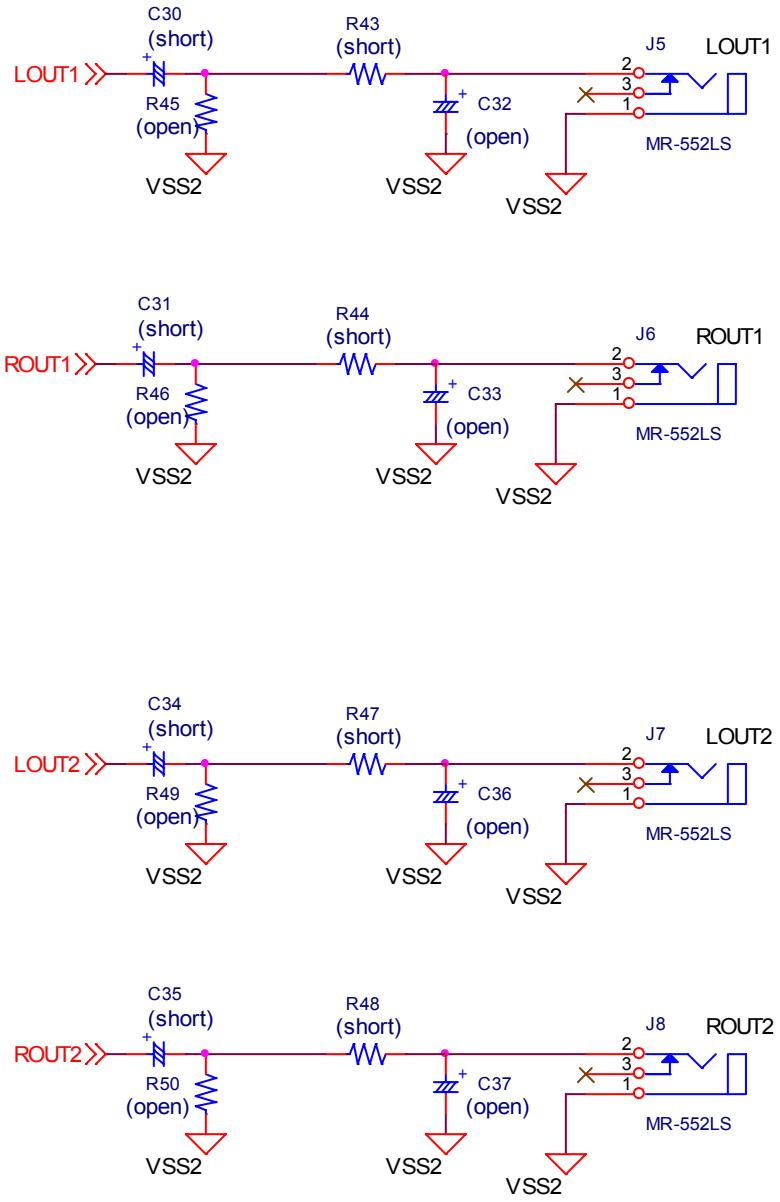


Figure 4. Analog Output Circuit

For analog output, RCA connector: J5 (LOUT1), J6 (ROUT1), J7 (LOUT2), J8 (ROUT2) are available to use.
Analog outputs are single-ended and output range of each channel is 2Vrms(typ) when AVDD1=AVDD2=3.3Vrms.

■ Digital Input Circuit (External DIR: PORT1 RX0, PORT2 RX0)

Figure 5. Digital Input Circuit (External DIR)

For digital input, RCA connector: J12 (PORT1 RX0), J15 (PORT2 RX0) are available.

■ Digital Output Circuit (External DIT: PORT1 TX1)

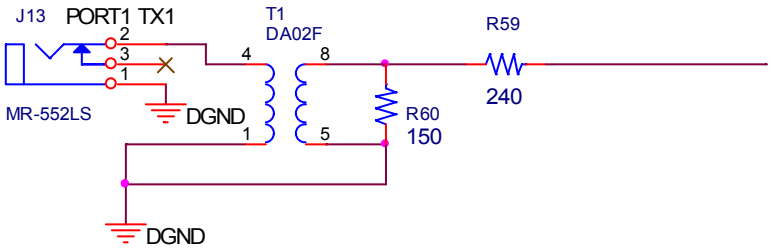


Figure 6. Digital Output Circuit (External DIT)

For digital output, RCA connector: J13 (PORT1 TX1) is available.

Control Soft Manual

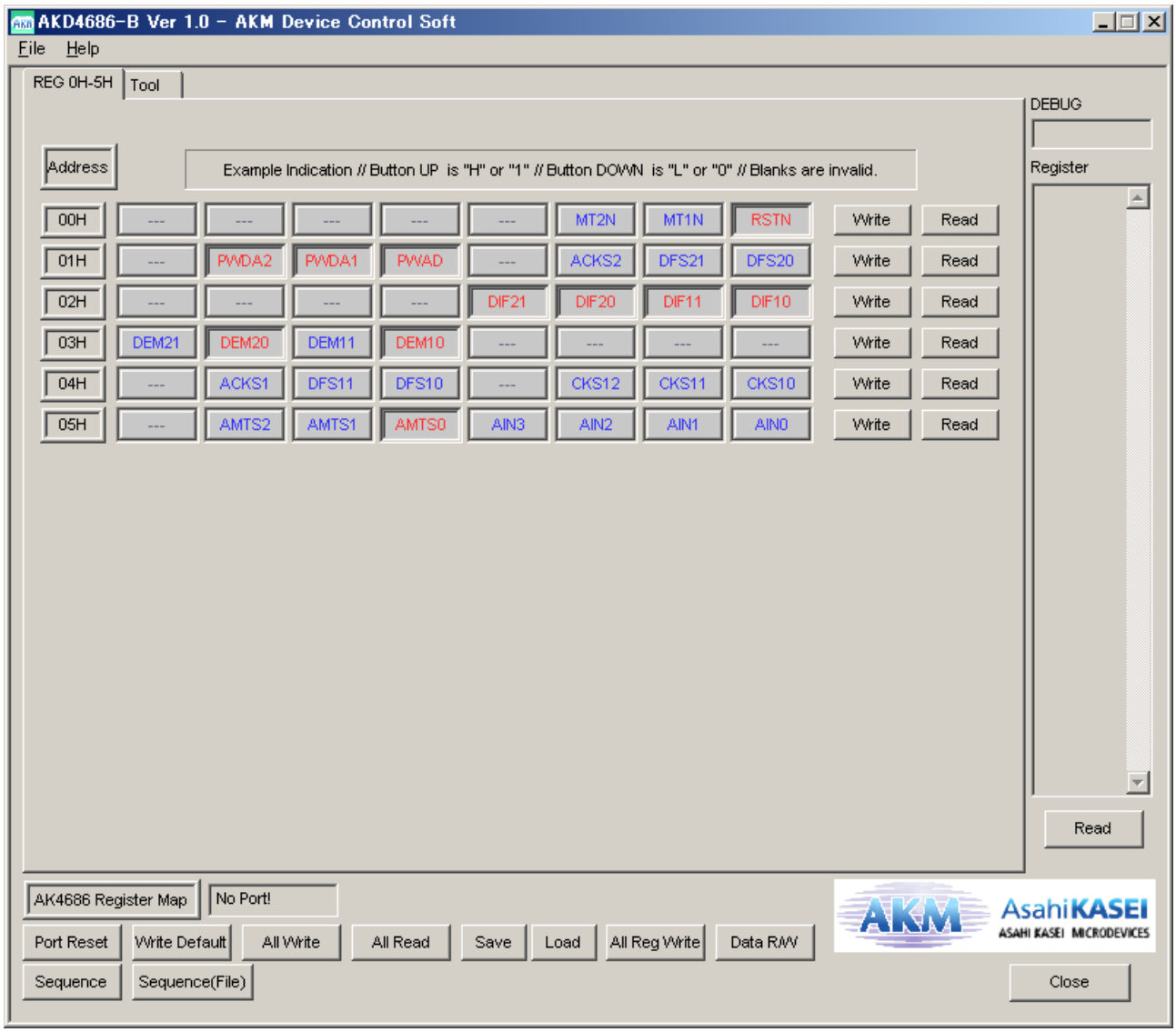
■ Evaluation Board and Control Soft Settings

1. Set an evaluation board properly.
2. Connect the evaluation board to an IBM PC/AT compatible PC by a 10wire flat cable. Be aware of the direction of the 10pin header. When running this control soft on the Windows 2000/XP, the driver which is included in the CD must be installed. Refer to the "Driver Control Install Manual for AKM Device Control Software" for installing the driver. When running this control soft on the windows 95/98/ME, driver installing is not necessary. This control soft does not support the Windows NT.
3. Proceed evaluation by following the process below.

■ Operation Screen

1. Start up the control program following the process above.

The operation screen is shown below.



■ Operation Overview

Function, register map and testing tool can be controlled by this control soft. These controls are selected by upper tabs.

Buttons which are frequently used such as register initializing button “Write Default”, are located outside of the switching tab window. Refer to the “■ Dialog Boxes” for details of each dialog box setting.

1. [Port Reset]: For when connecting to USB I/F board (AKDUSBIF-A)
   Click this button after the control soft starts up when connecting USB I/F board (AKDUSBIF-A).

2. [Write Default]: Register Initializing
   When the device is reset by a hardware reset, use this button to initialize the registers.

3. [All Write]: Executing write commands for all registers displayed.

4. [All Read]: Executing read commands for all registers displayed.

5. [Save]: Saving current register settings to a file.

6. [Load]: Executing data write from a saved file.

7. [All Req Write]: “All Req Write” dialog box is popped up.

8. [Data R/W]: “Data R/W” dialog box is popped up.

9. [Sequence]: “Sequence” dialog box is popped up.

10. [Sequence(File)]: “Sequence(File)” dialog box is popped up.

11. [Read]: Reading current register settings and display on to the Register area (on the right of the main window). This is different from [All Read] button, it does not reflect to a register map, only displaying hexadecimal.

■ Tab Functions

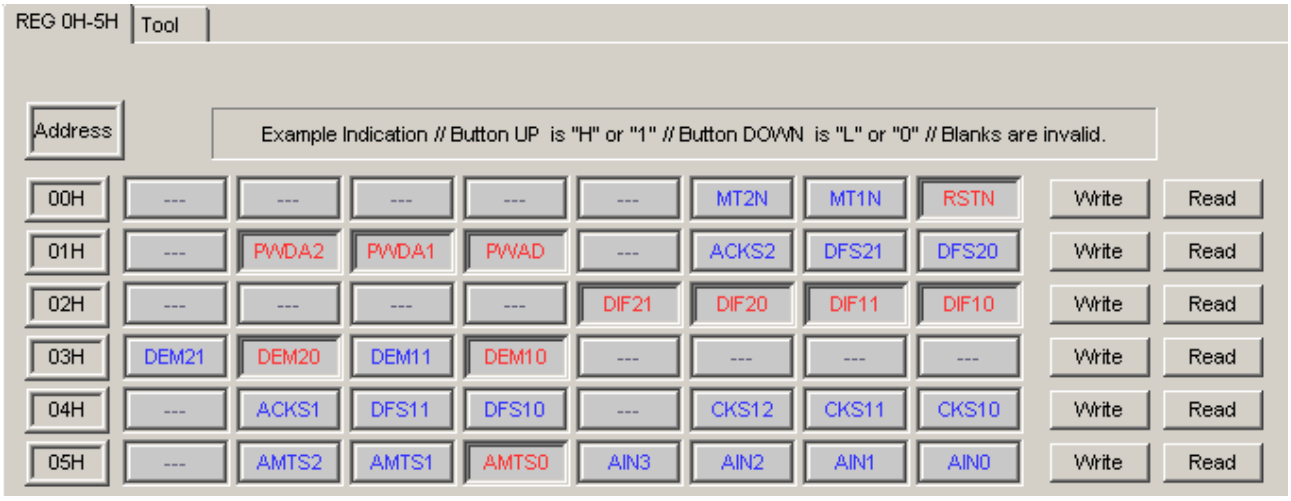
1. [REG 0H～5H]: Register Map

This tab is for a register writing and reading.

Each bit on the register map is a push-button switch.
Button Down indicates “H” or “1” and the bit name is in red (when read only it is in deep red).
Button Up indicates “L” or “0” and the bit name is in blue (when read only it is in gray)

Grayout registers are Read Only registers. They can not be controlled.

The registers which is not defined in the datasheet are indicated as “---”.

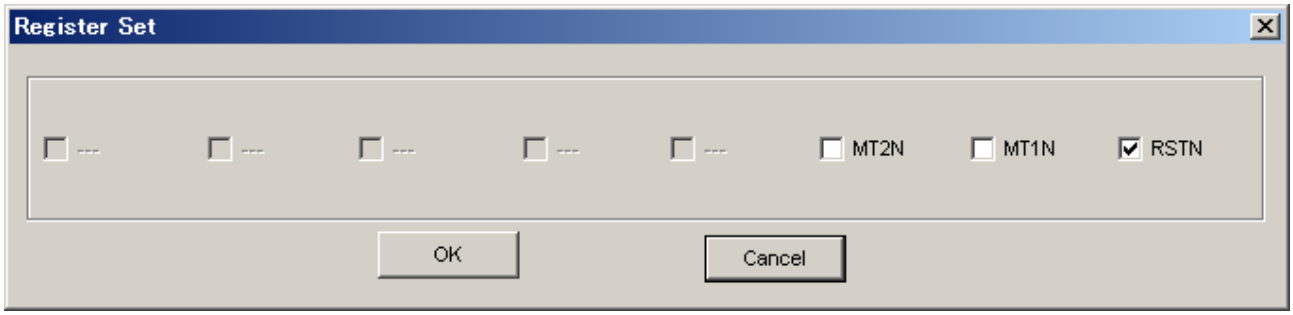


[Write]: Data Writing Dialog

It is for when changing two or more bits on the same address at the same time.

Click [Write] button located on the right of the each corresponded address for a pop-up dialog box.

When checking the checkbox, the register will be “H” or “1”, when not checking the register will be “L” or ”0”.
Click [OK] to write setting value to the registers, or click [Cancel] to cancel this setting.



[Read]: Data Read

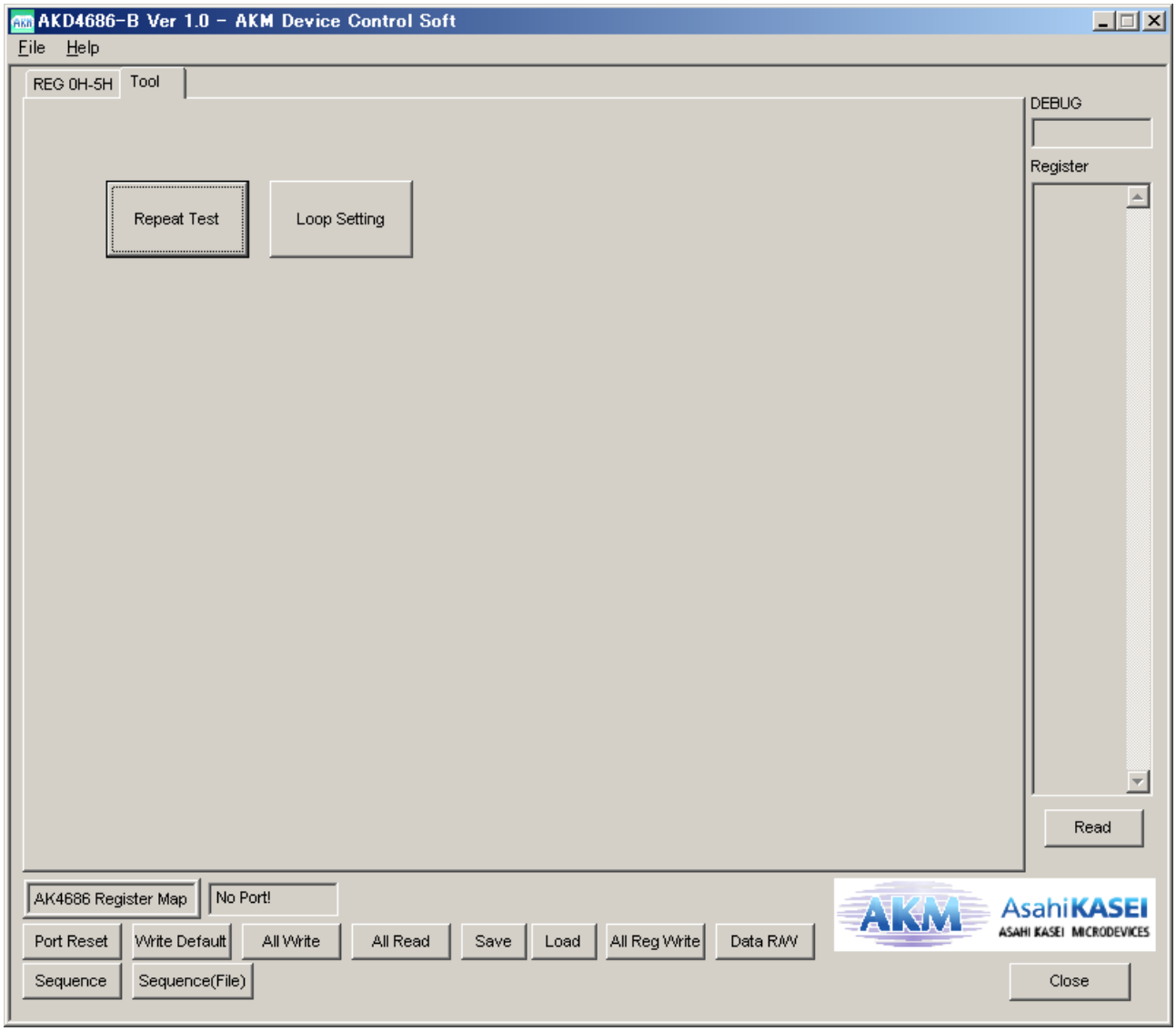
Click [Read] button located on the right of the each corresponded address to execute register reading.

After register reading, the display will be updated regarding to the register status.
Button Down indicates “H” or “1” and the bit name is in red (when read only it is in deep red).
Button Up indicates “L” or “0” and the bit name is in blue (when read only it is in gray)

Please be aware that button statuses will be changed by Read command.

2. [Tool]: Testing Tools

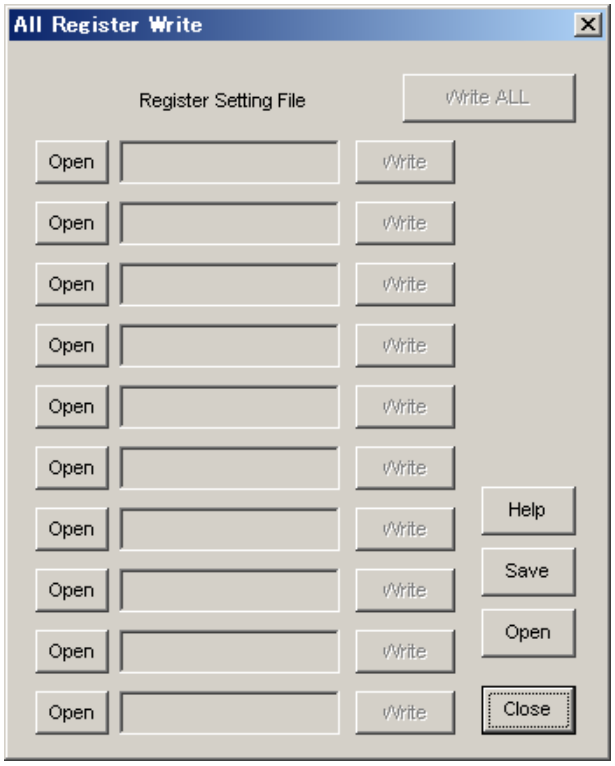
This tab screen is for evaluation testing tool.
Click buttons for each testing tool.



■ Dialog Boxes

1. [All Req Write]: All Req Write dialog box

Click [All Reg Write] button in the main window to open register setting files.
Register setting files saved by [SAVE] button can be applied.



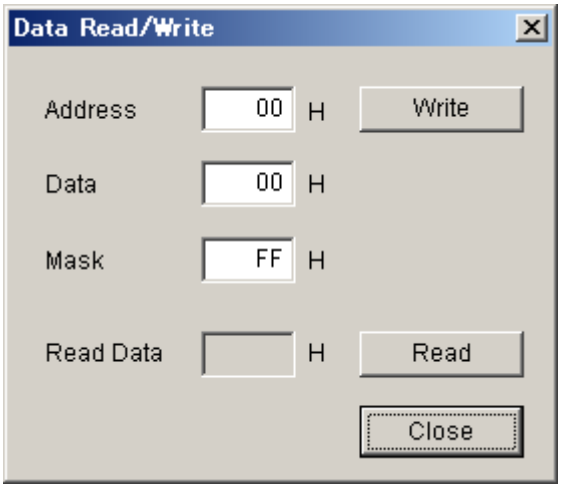
[Open (left)]: Selecting a register setting file (*.akr).
[Write]: Executing register writing.
[Write All]: Executing all register writings.
Writings are executed in descending order.

[Help]: Help window is popped up.
[Save]: Saving the register setting file assignment. The file name is "*.mar".
[Open (right)]: Opening a saved register setting file assignment "*. mar".
[Close]: Closing the dialog box and finish the process.

*Operating Suggestions
(1) Those files saved by [Save] button and opened by [Open] button on the right of the dialog "*.mar" should be stored in the same folder.
(2) When register settings are changed by [Save] button in the main window, re-read the file to reflect new register settings.

2. [Data R/W]: Data R/W Dialog Box

Click the [Data R/W] button in the main window for data read/write dialog box.
Data write is available to specified address.



Address Box: Input data address in hexadecimal numbers for data writing.
Data Box: Input data in hexadecimal numbers.
Mask Box: Input mask data in hexadecimal numbers.
This is "AND" processed input data.

[Write]: Writing to the address specified by "Address" box.

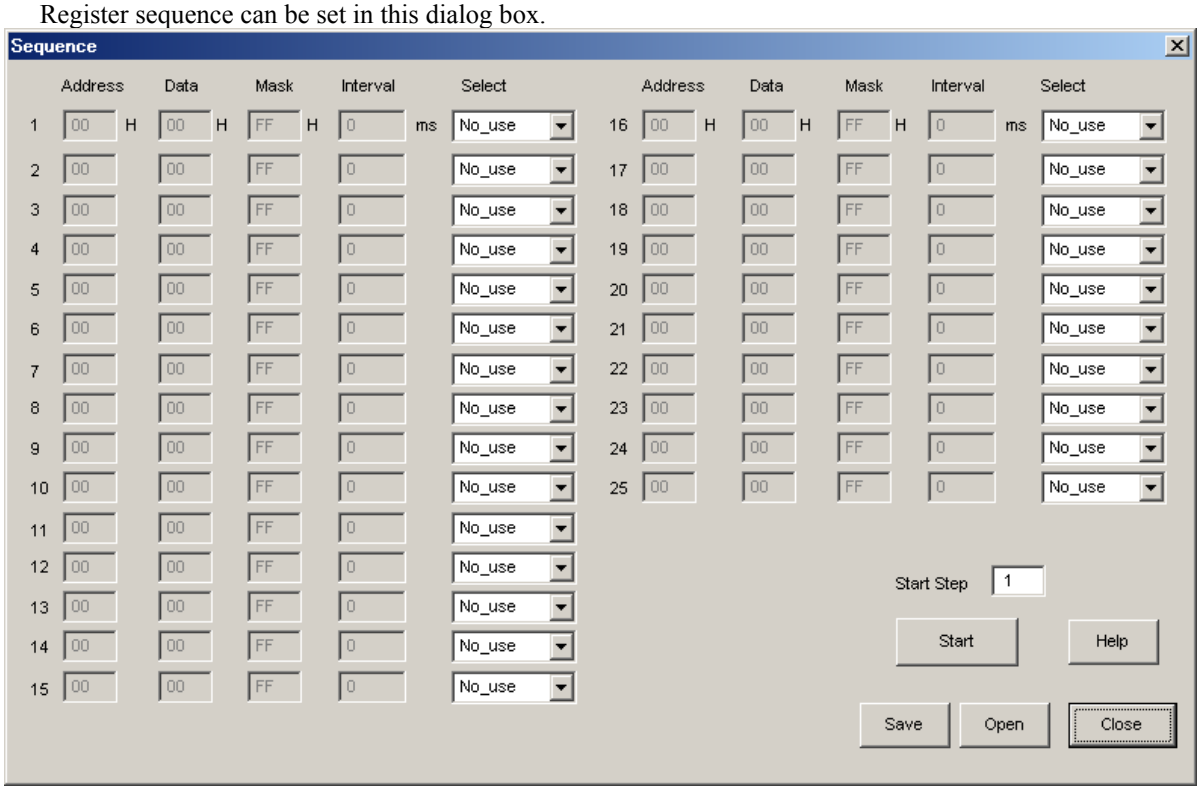
[Read]: Reading from the address specified by "Address" box.
The result will be shown in the Read Data Box in hexadecimal numbers.

[Close]: Closing the dialog box and finish the process.
Data writing can be cancelled by this button instead of [Write] button.

*The register map will be updated after executing [Write] or [Read] commands.

3. [Sequence]: Sequence Dialog Box

Click [Sequence] button to open register sequence setting dialog box.
Register sequence can be set in this dialog box.



Sequence Setting

Set register sequence by following process bellow.

(1)Select a command

Use [Select] pull-down box to choose commands.
Corresponding boxes will be valid.

< Select Pull-down menu >

- No_use: Not using this address
- Register: Register writing
- Reg(Mask): Register writing (Masked)
- Interval: Taking an interval
- Stop: Pausing the sequence
- End: Finishing the sequence

(1) Input sequence

[Address]: Data address
[Data]: Writing data
[Mask]: Mask

[Data] box data is ANDed with [Mask] box data. This is the actual writing data.
When Mask = 0x00, current setting is hold.

When Mask = 0xFF, the 8bit data which is set in the [Data] box is written.

When Mask =0x0F, lower 4bit data which is set in the [Data] box is written.
Upper 4bit is hold to current setting.

[Interval]: Interval time

Valid boxes for each process command are shown bellow.

· No_use: None
· Register: [Address], [Data], [Interval]
· Reg(Mask): [Address], [Data], [Mask], [Interval]
· Interval: [Interval]
· Stop: None
· End: None

Control Buttons

The function of Control Button is shown bellow.

[Start]: Executing the sequence

[Help]: Opening a help window
[Save]: Saving sequence settings as a file. The file name is "*.aks".
[Open]: Opening a sequence setting file "*.aks".
[Close]: Closing the dialog box and finish the process.

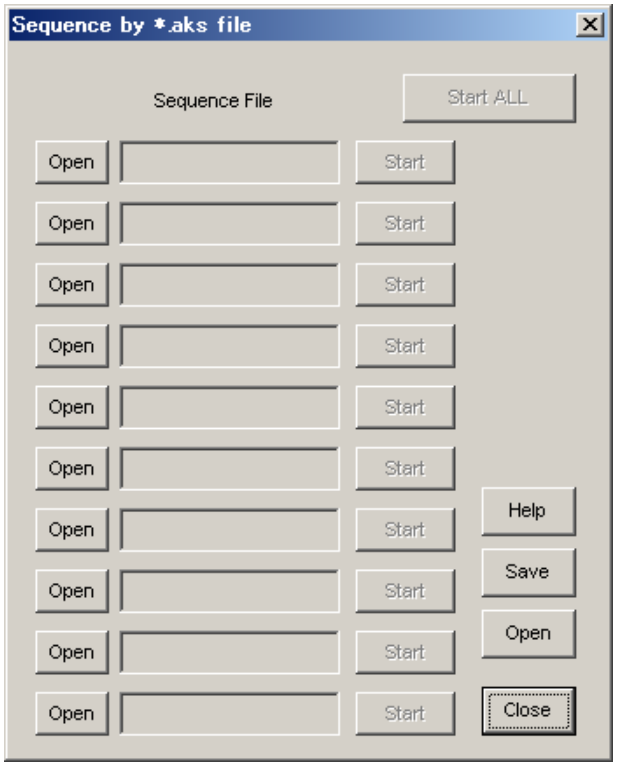
Stop of the sequence

When "Stop" is selected in the sequence, processing is paused and it starts again when [Start] button is clicked. Restarting step number is shown in the "Start Step" box. When finishing the process until the end of sequence, "Start Step" will return to "1".

The sequence can be started from any step by writing the step number to the "Start Step" box.
Write "1" to the "Start Step" box and click [Start] button, when restarting the process from the beginning.

4. [Sequence(File)]: Sequence Setting File Dialog Box

Click [Sequence(File)] button to open sequence setting file dialog box.
Those files saved in the "Sequence setting dialog" can be applied in this dialog.

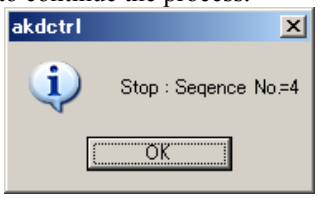


[Open (left)]: Opening a sequence setting file (*.aks).
[Start]: Executing the sequence setting.
[Start All]: Executing all sequence settings.
Sequences are executed in descending order.

[Help]: Pop up the help window.
[Save]: Saving sequence setting file assignment. The file name is "*.mas".
[Open(right)]: Opening a saved sequence setting file assignment "*. mas".
[Close]: Closing the dialog box and finish the process.

*Operating Suggestions

(1) Those files saved by [Save] button and opened by [Open] button on the right of the dialog "*.mas" should be stored in the same folder.
(2) When "Stop" is selected in the sequence the process will be paused and a pop-up message will appear. Click "OK" to continue the process.



Measure Result

1) ADC part

[Measurement condition]

- Measurement unit : Audio Precision SYS-2722
- MCLK : 512fs
- BICK : 64fs
- fs : 48kHz
- BW : 20Hz~20kHz (fs=48kHz)
- Bit : 24bit
- Power Supply : AVDD1=AVDD2=DVDD=CVDD=3.3V
- Interface : External DIT (U4)
- Temperature : Room Temp

Parameter	Input signal	Measurement filter	Results [dB]	
			Lch	Rch
S/(N+D)	1kHz, -1dB	20kLPF	88.1	87.7
DR	1kHz, -60dB	20kLPF, A-weighted	97.5	97.4
S/N	No signal	20kLPF, A-weighted	97.5	97.5

2) DAC part

[Measurement condition]

- Measurement unit : Audio Precision SYS-2722
- MCLK : 512fs (fs=48kHz), 256fs (fs=96kHz), 128fs (fs=192kHz)
- BICK : 64fs
- fs : 48kHz, 96kHz, 192kHz
- BW : 20Hz~20kHz (fs=48kHz), 20Hz~40kHz (fs=96kHz), 20Hz~40kHz (fs=192kHz)
- Resolution : 24bit
- Power Supply : AVDD1=AVDD2=DVDD=CVDD=3.3V
- Interface : External DIR (U4)
- Temperature : Room Temp

fs=48kHz

Parameter	Input signal	Measurement filter	Results [dB]	
			Lch	Rch
S/(N+D)	1kHz, 0dB	20kHz SPCL	88.4	88.9
DR	1kHz, -60dB	20kHz SPCL	97.2	97.5
DR	1kHz, -60dB	20kHz SPCL, A-weighted	100.0	99.9
S/N	“0” data	20kHz SPCL	98.7	98.7
S/N	“0” data	20kHz SPCL, A-weighted	101.0	101.0

fs=96kHz

Parameter	Input signal	Measurement filter	Results [dB]	
			Lch	Rch
S/(N+D)	1kHz, 0dB	40kHz SPCL	87.8	88.1
DR	1kHz, -60dB	40kHz SPCL	95.0	95.1
DR	1kHz, -60dB	40kHz SPCL, A-weighted	100.0	100.0
S/N	“0” data	40kHz SPCL	96.9	97.0
S/N	“0” data	40kHz SPCL, A-weighted	101.7	101.7

fs=192kHz

Parameter	Input signal	Measurement filter	Results [dB]	
			Lch	Rch
S/(N+D)	1kHz, 0dB	40kHz SPCL	87.4	87.7
DR	1kHz, -60dB	40kHz SPCL	95.1	95.2
DR	1kHz, -60dB	40kHz SPCL, A-weighted	100.0	100.0
S/N	“0” data	40kHz SPCL	96.0	96.1
S/N	“0” data	40kHz SPCL, A-weighted	100.8	100.9

1.ADC部 (fs=48kHz)

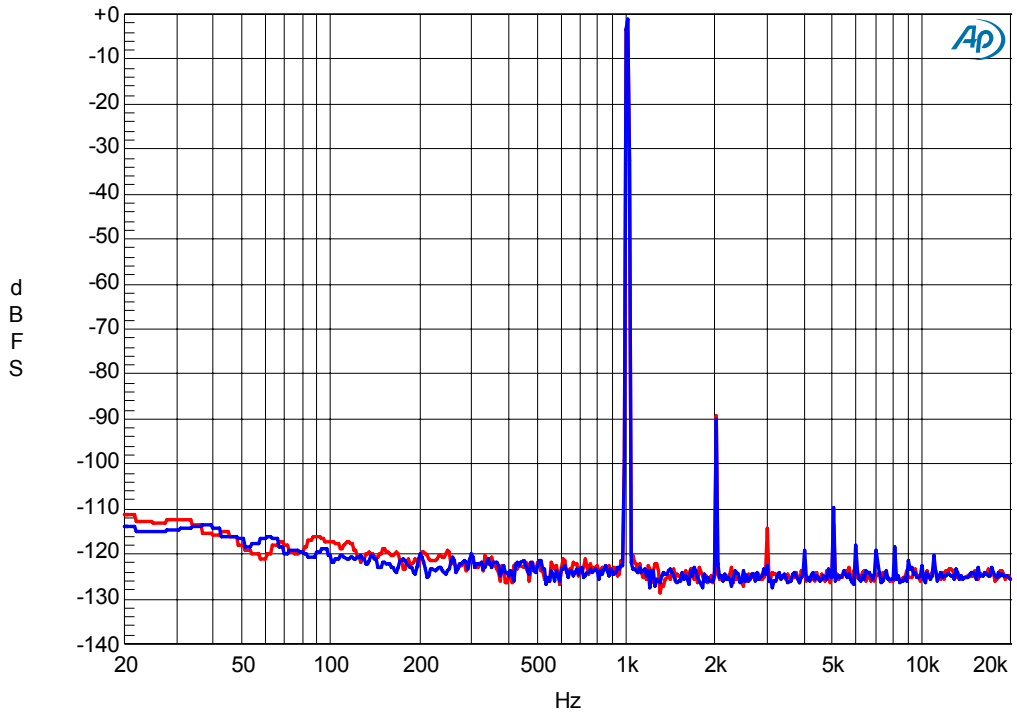


Figure 7. FFT (Input Frequency =1kHz, Input Level=-1dBFS)

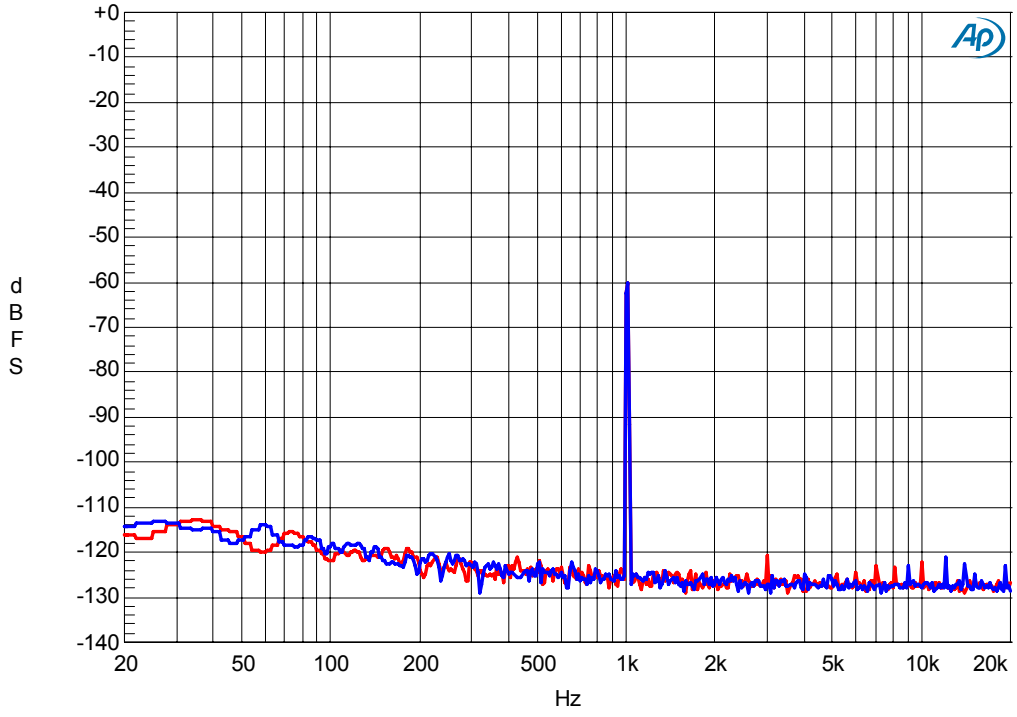


Figure 8. FFT(Input Frequency =1kHz, Input Level=-60dBFS)

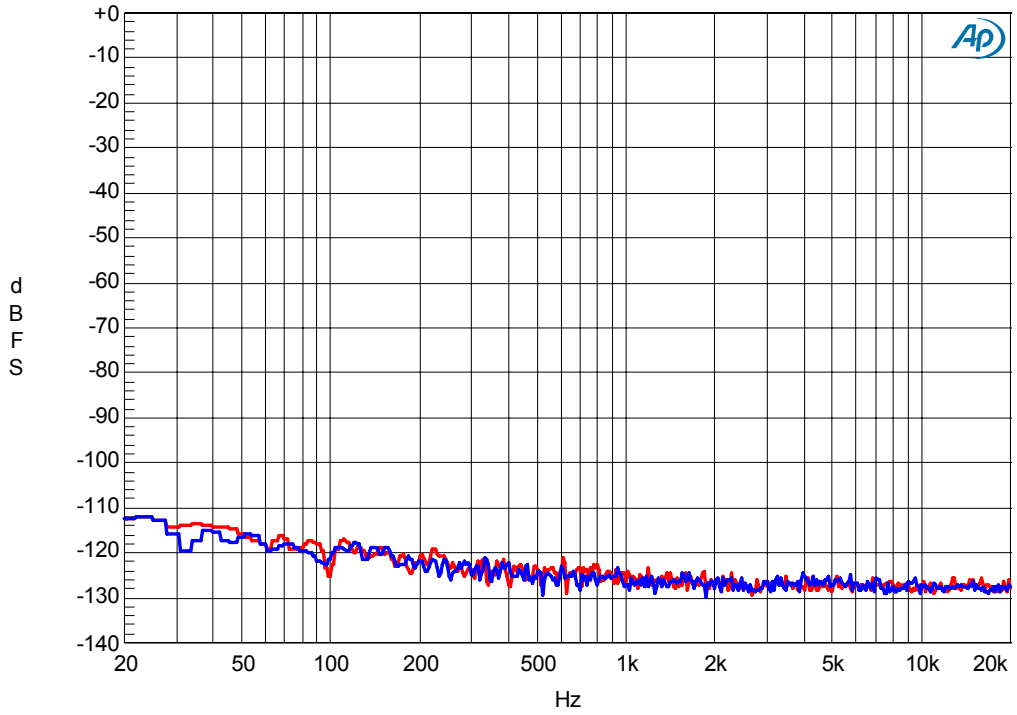


Figure 9. FFT(noise floor)

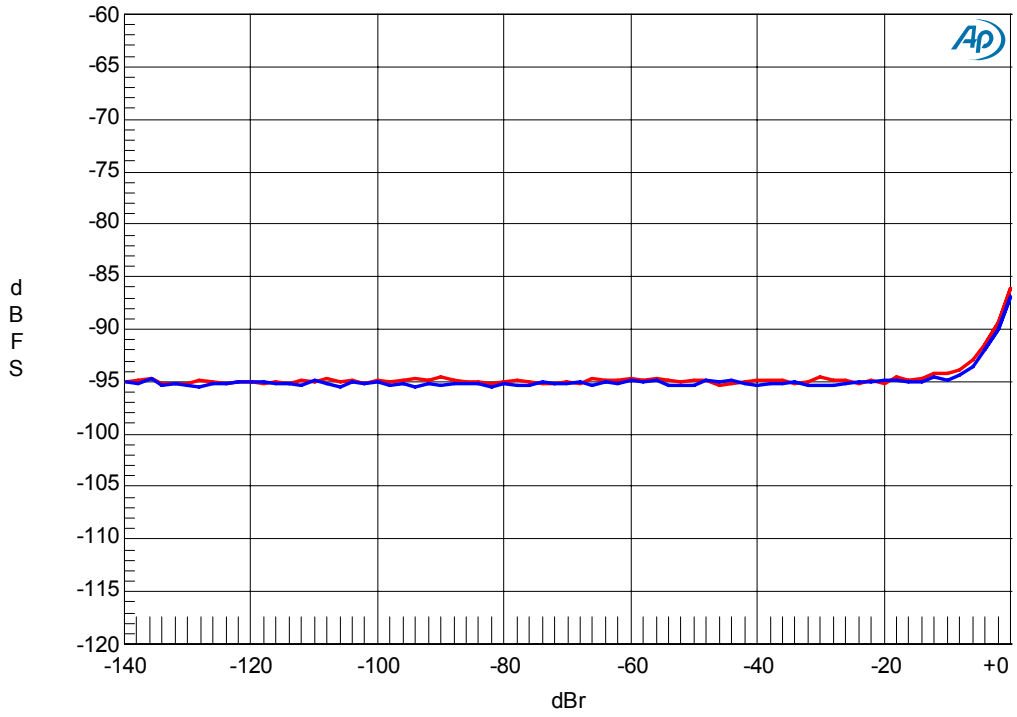


Figure 10. THD + N vs Input Level (Input Frequency =1kHz)

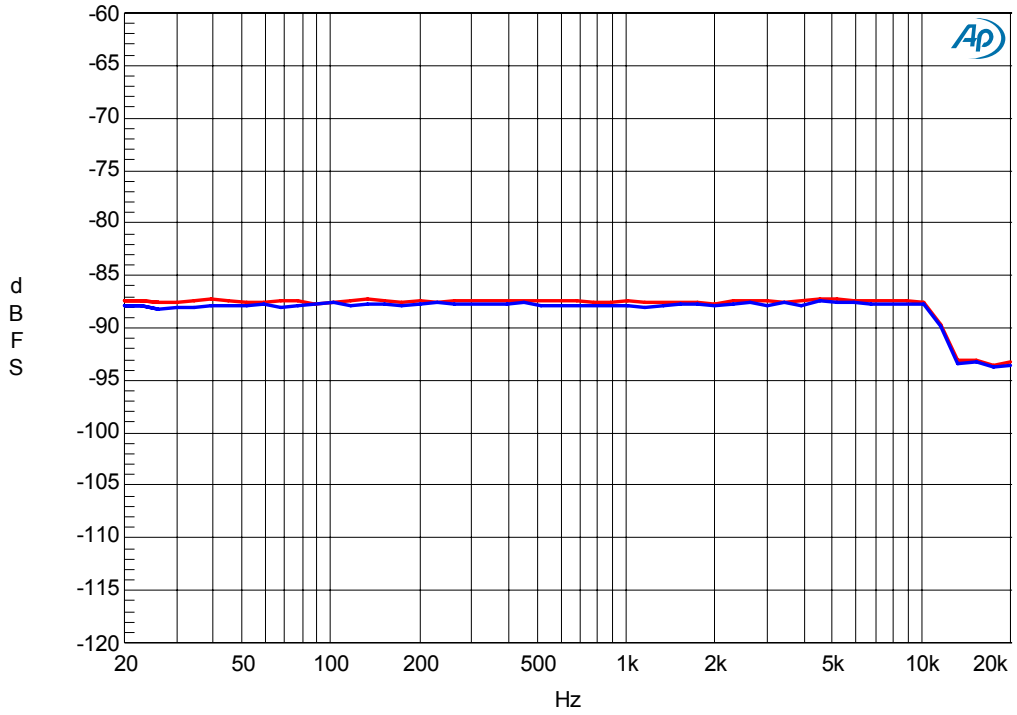


Figure 11. THD + N vs Input Frequency (Input Level=-1.0dBFS)

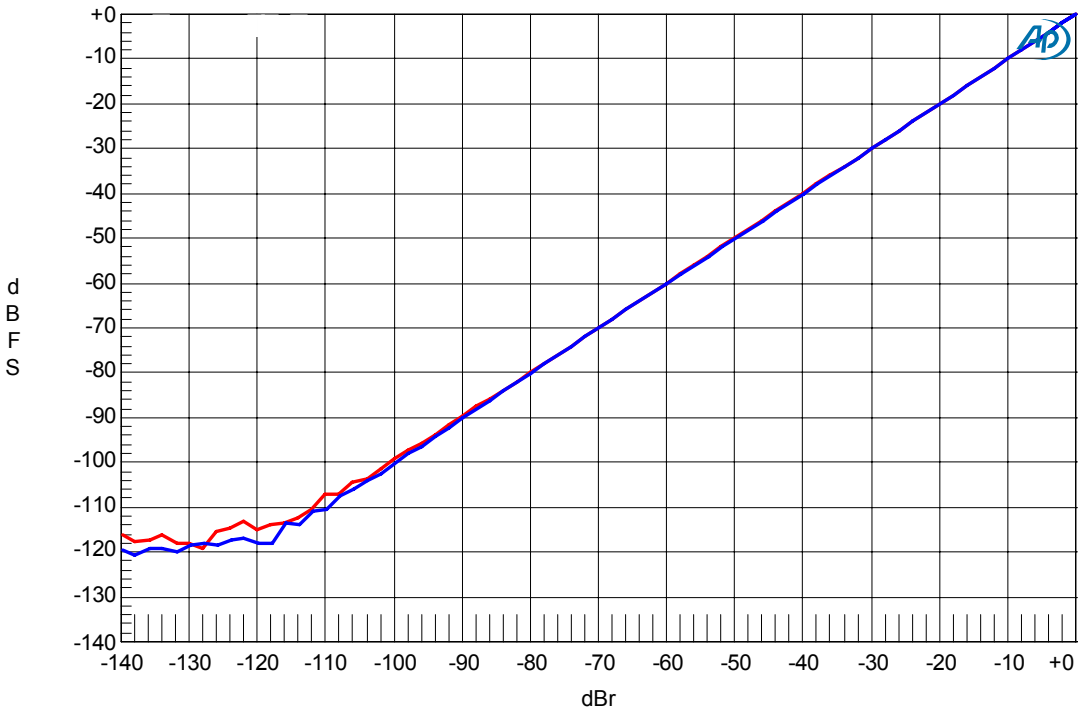


Figure 12. Linearity (Input Frequency =1kHz)

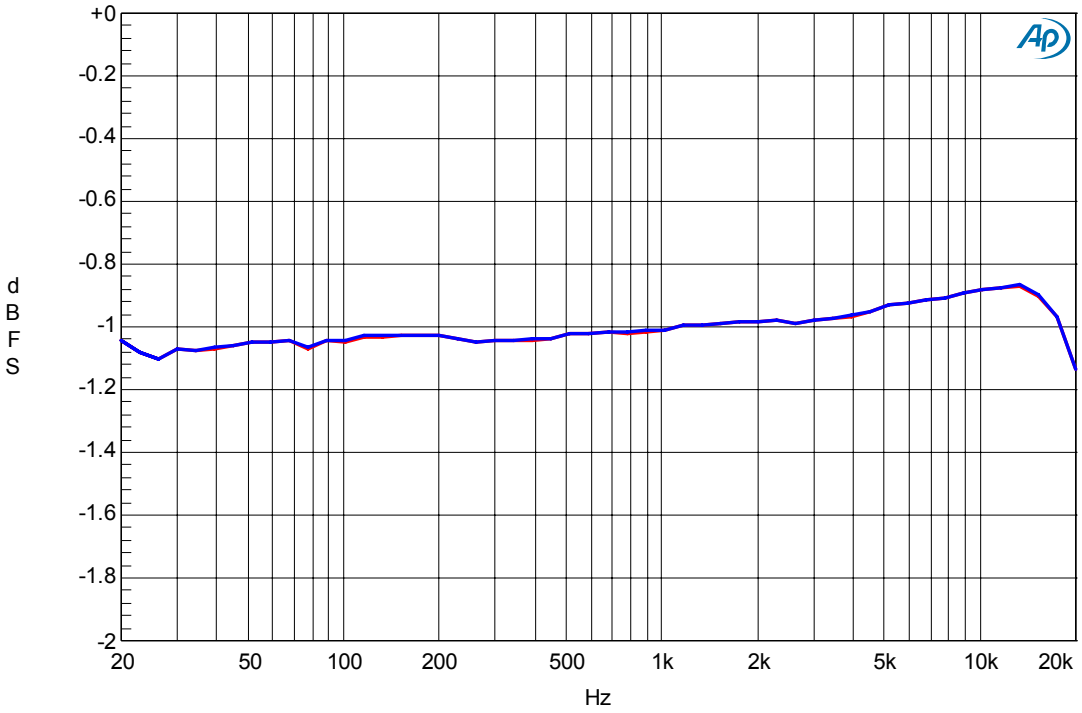


Figure 13. Frequency Response (Input Level=-1.0dBFS)

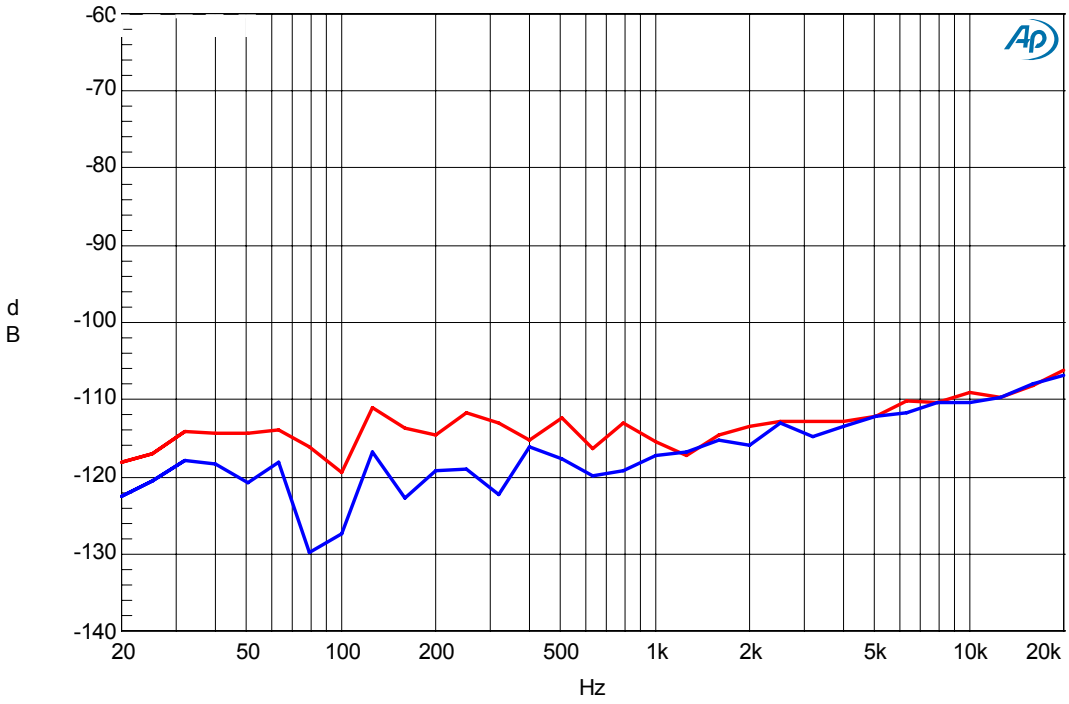


Figure 14. Crosstalk (Input Level=-1.0dBFS)

2.DAC部

(DAC fs=48kHz)

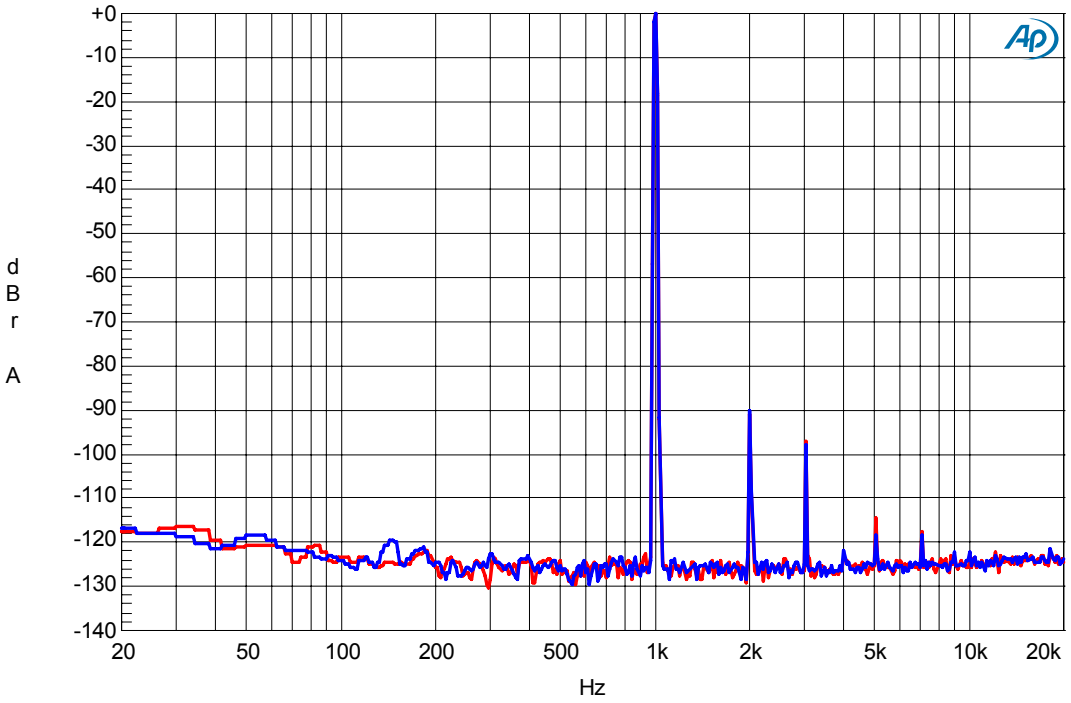


Figure 15. FFT(Input Frequency =1kHz, Input Level=0dBFS)

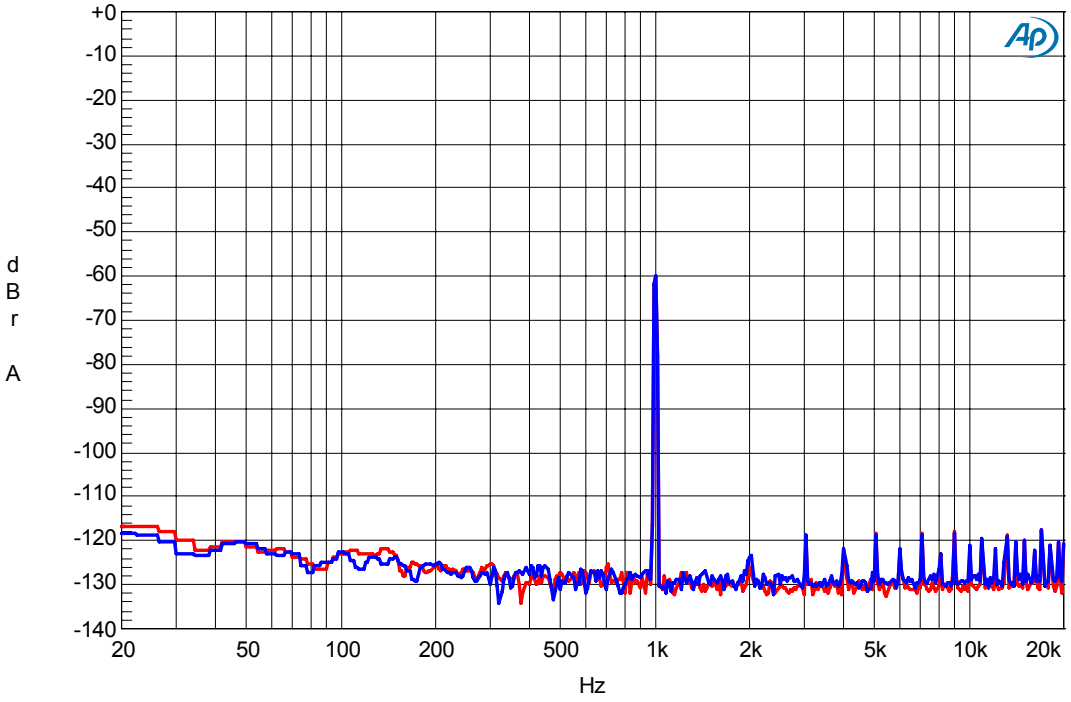


Figure 16. FFT(Input Frequency =1kHz, Input Level=-60dBFS)

(DAC fs=48kHz)

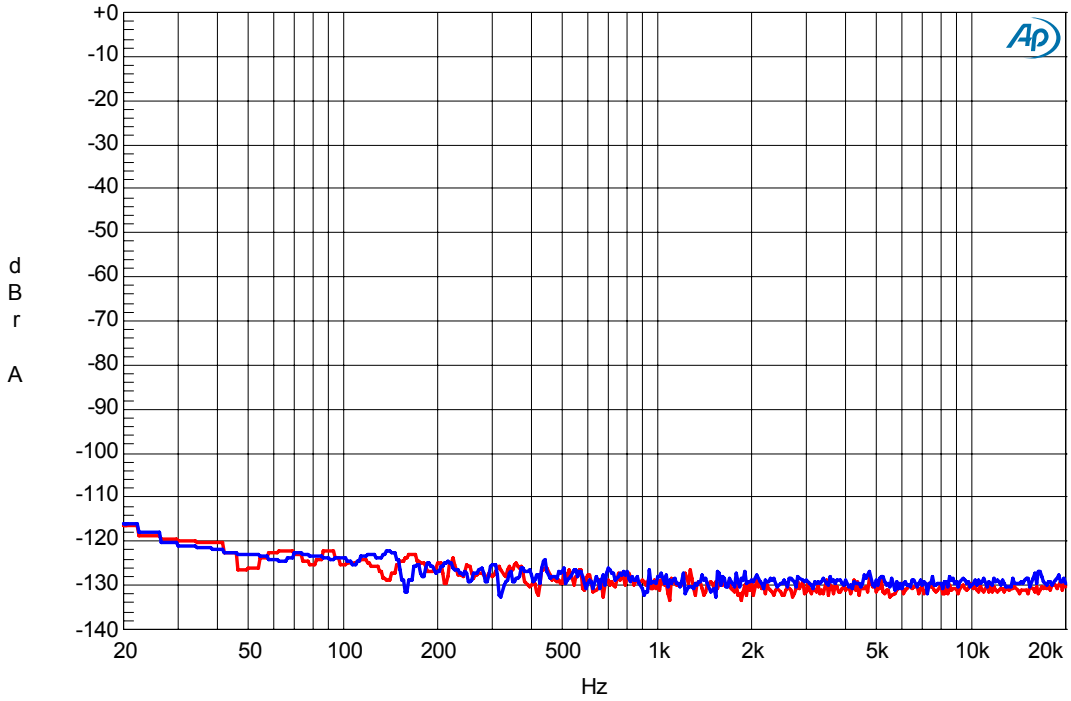


Figure 17. FFT(noise floor)

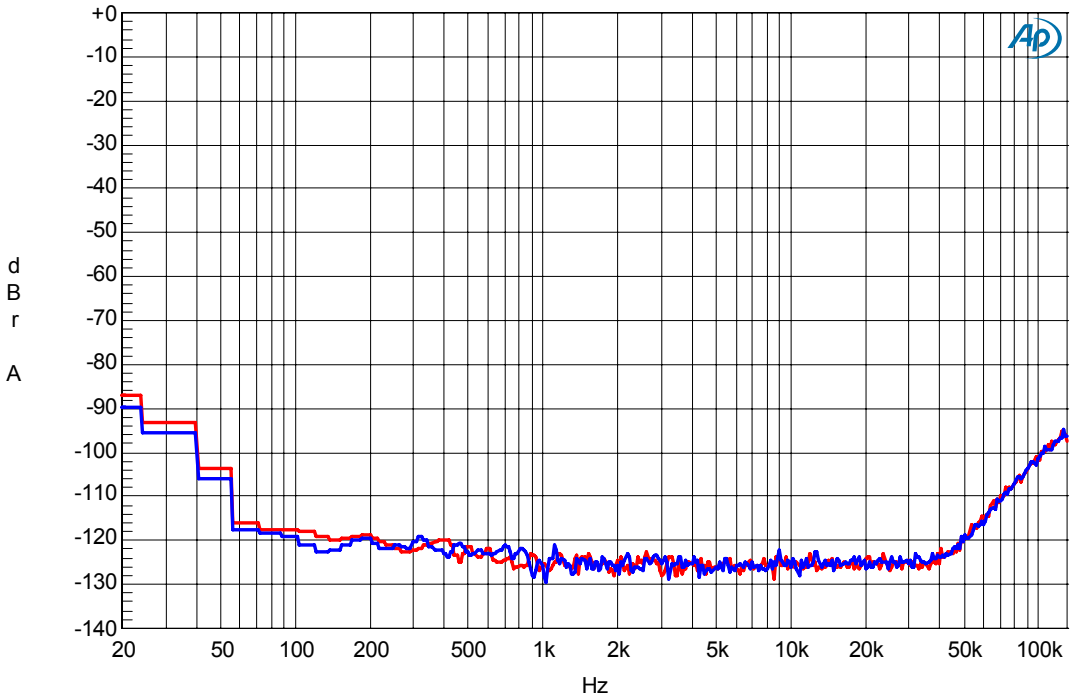


Figure 18. FFT(out-of-band noise)

(DAC fs=48kHz)

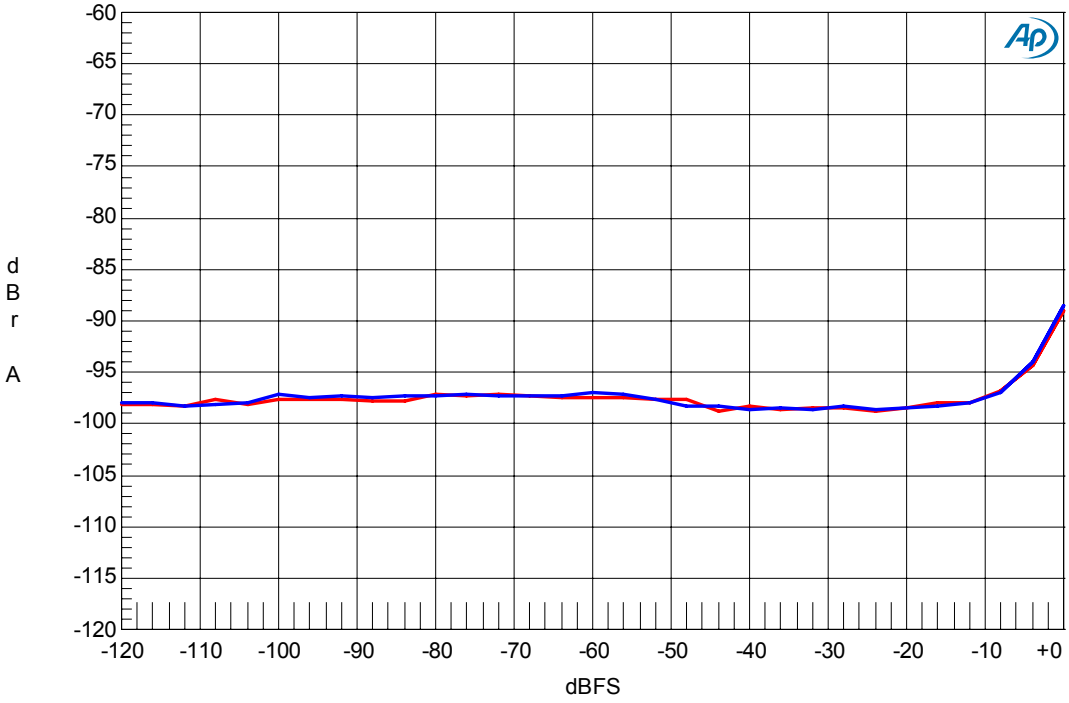


Figure 19. THD+N vs Input Level (Input Frequency =1kHz)

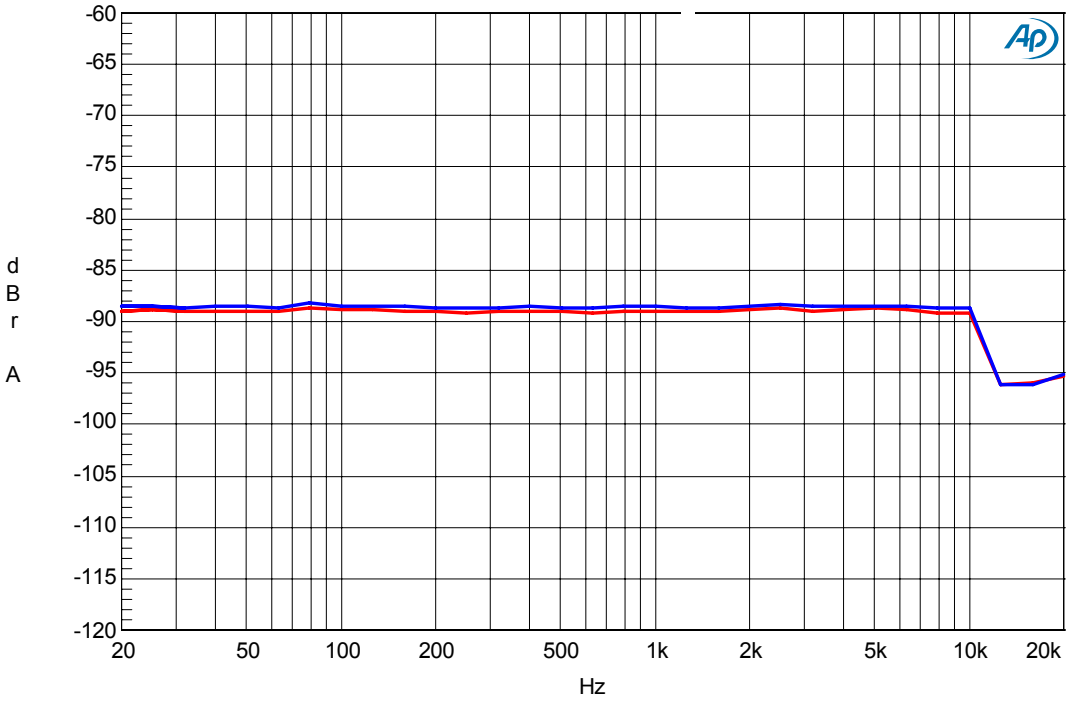


Figure 20. THD+N vs Input Frequency (Input Level=0dBFS)

(DAC fs=48kHz)

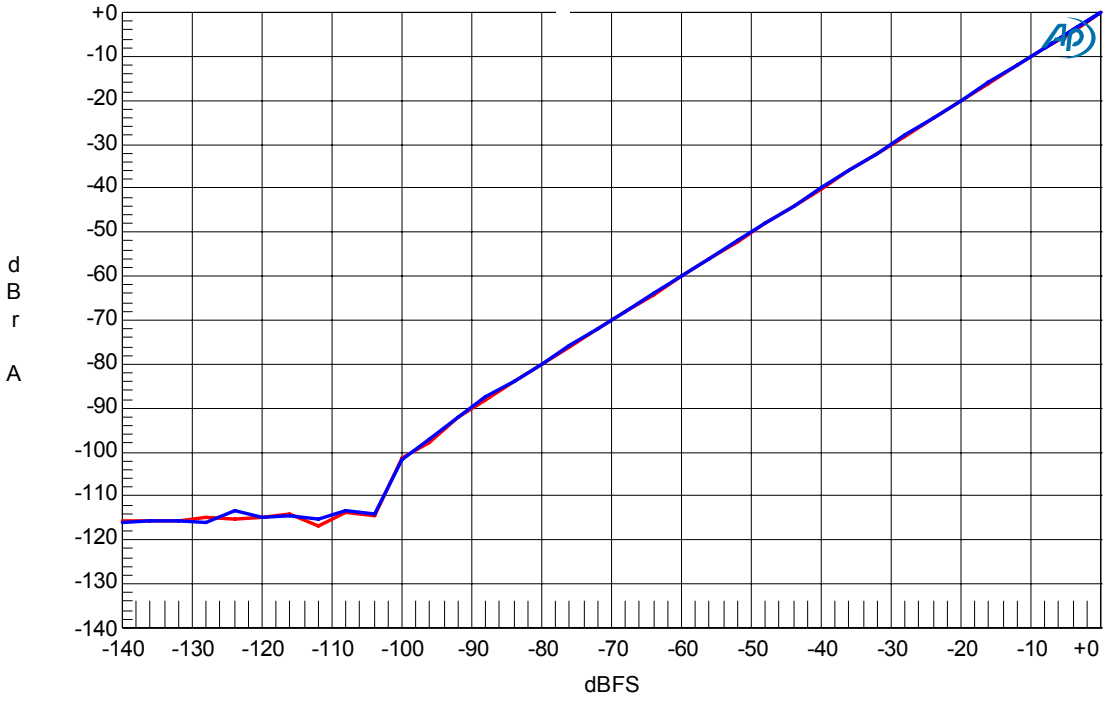


Figure 21. Linearity (Input Frequency =1kHz)

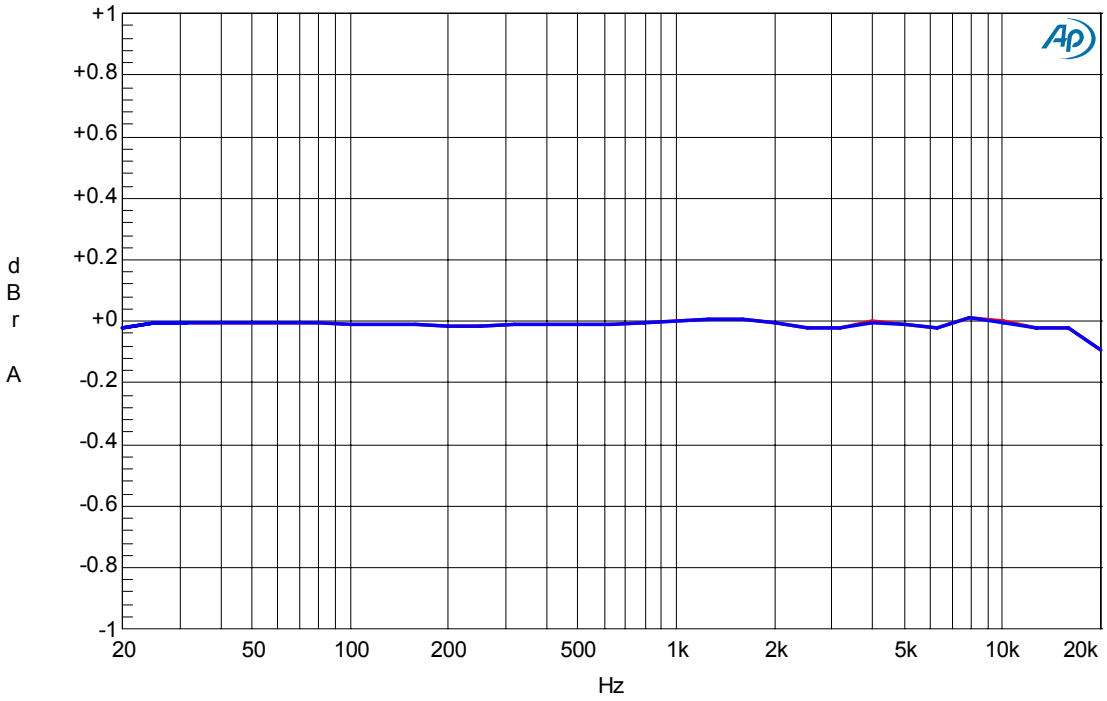


Figure 22. Frequency Response (Input Level=0dBFS)

(DAC fs=48kHz)

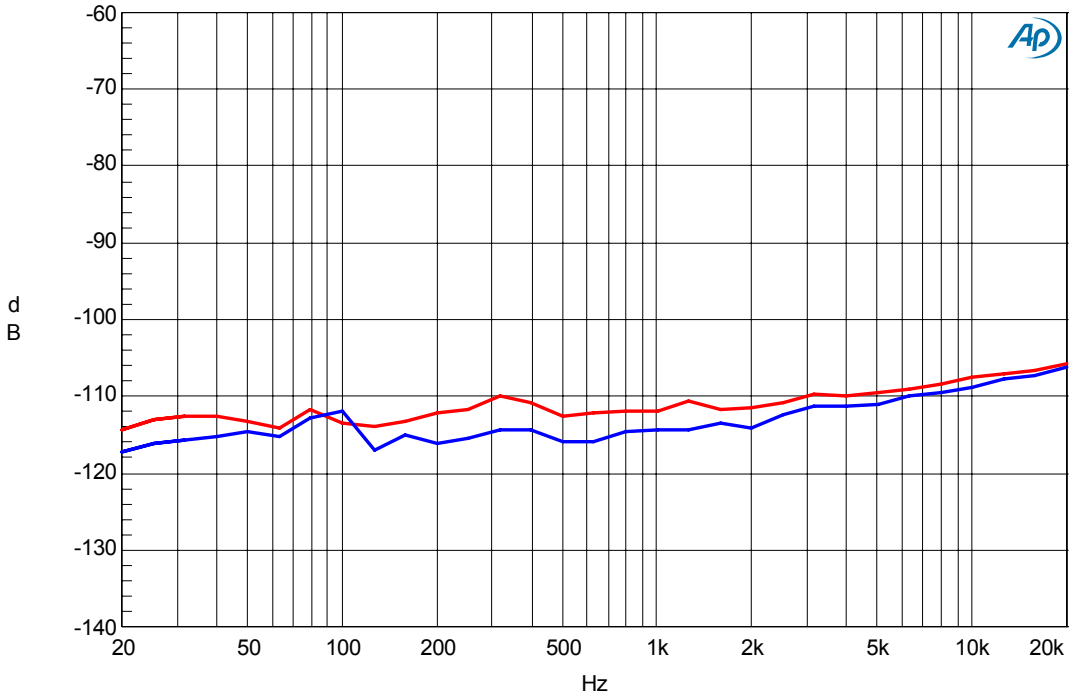


Figure 23. Cross-talk (Input Level=0dBFS)

(DAC fs=96kHz)

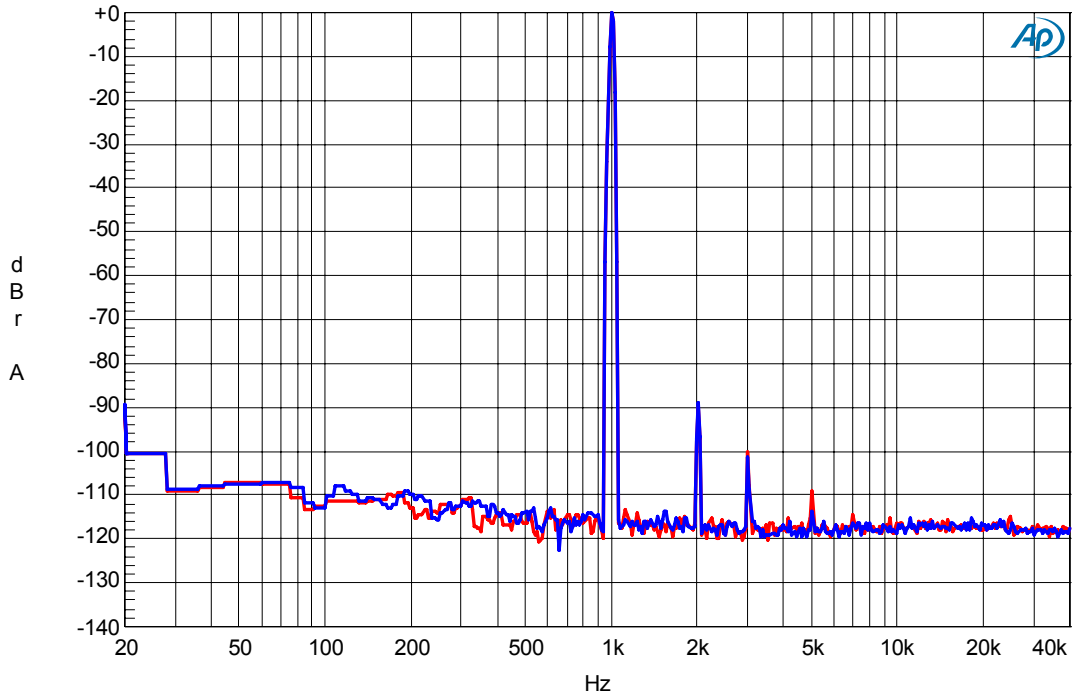


Figure 24. FFT(Input Frequency =1kHz, Input Level=0dBFS)

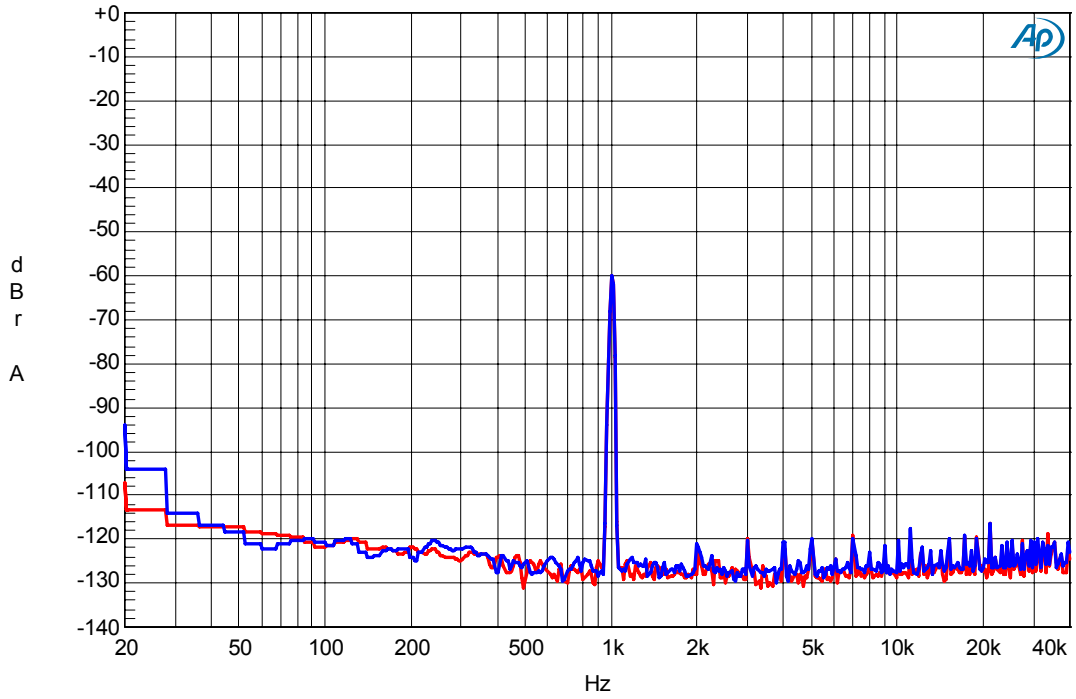


Figure 25. FFT(Input Frequency =1kHz, Input Level=-60dBFS)

(DAC fs=96kHz)

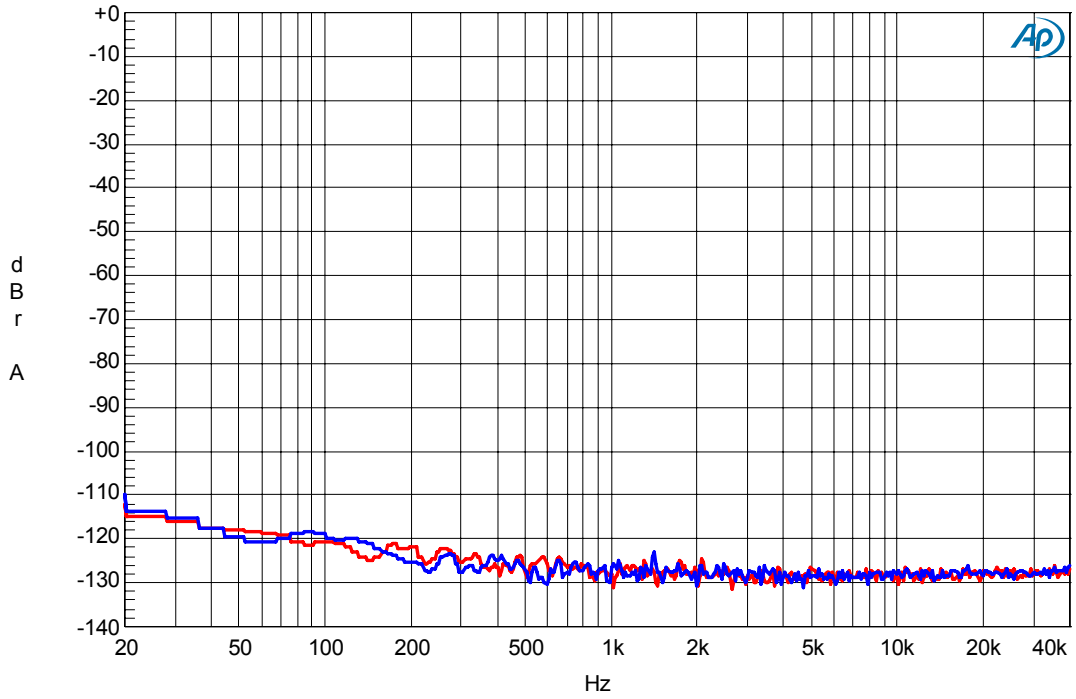


Figure 26. FFT(noise floor)

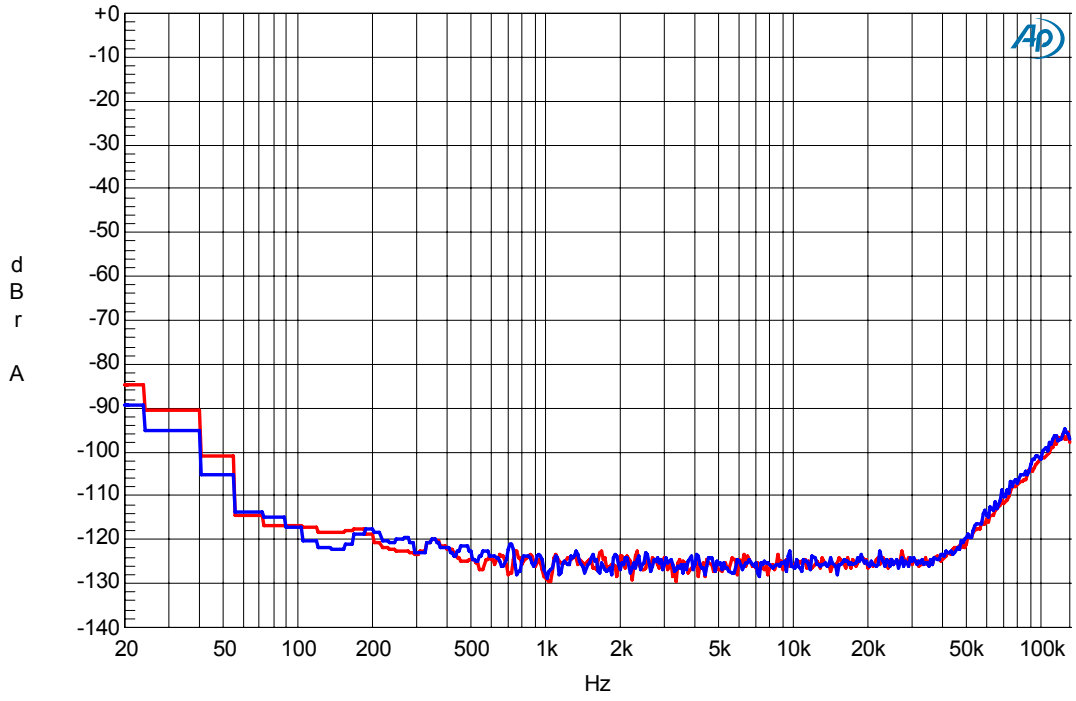


Figure 27. FFT (Out of band Noise)

(DAC fs=96kHz)

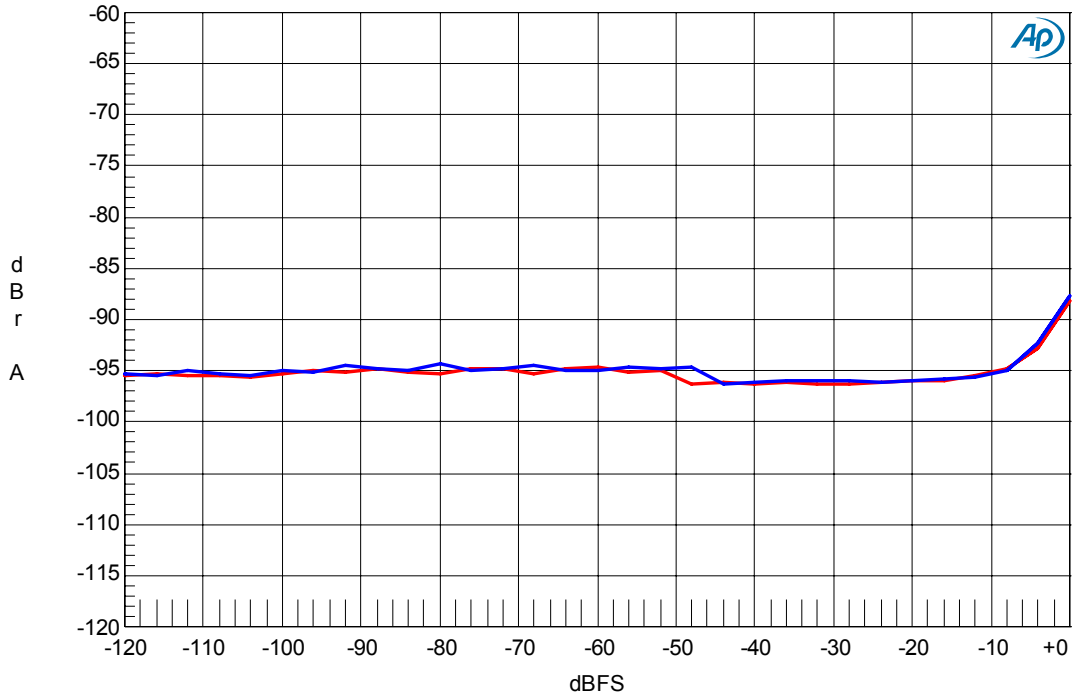


Figure 28. THD+N vs Input Level (Input Frequency =1kHz)

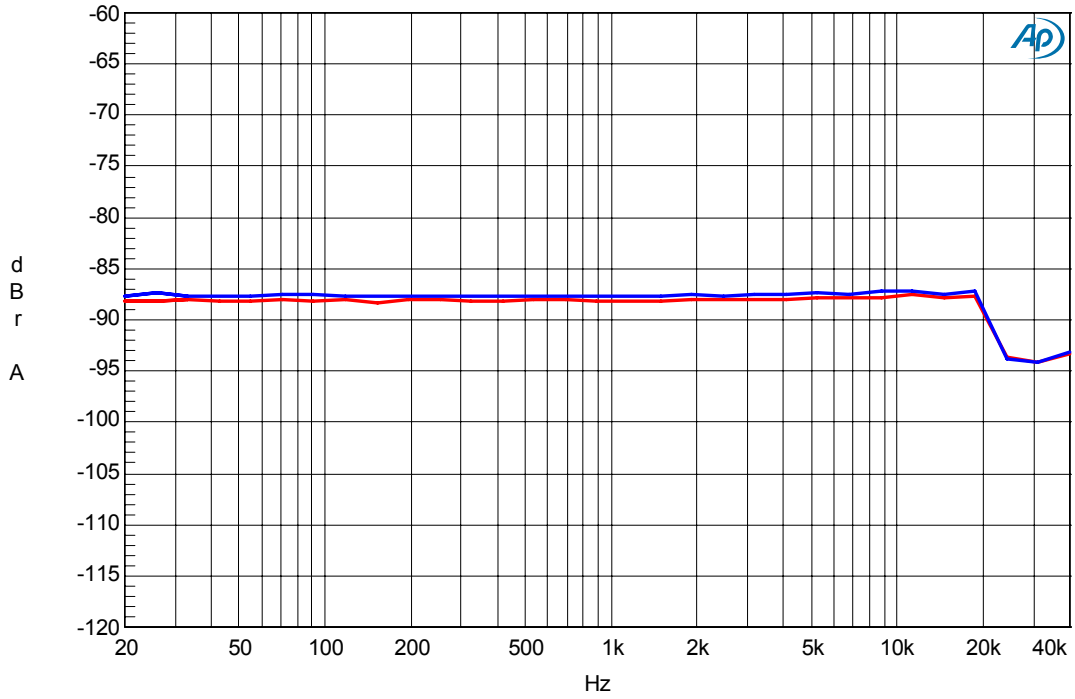


Figure 29. THD+N vs fin (Input Level=0dBFS)

(DAC fs=96kHz)

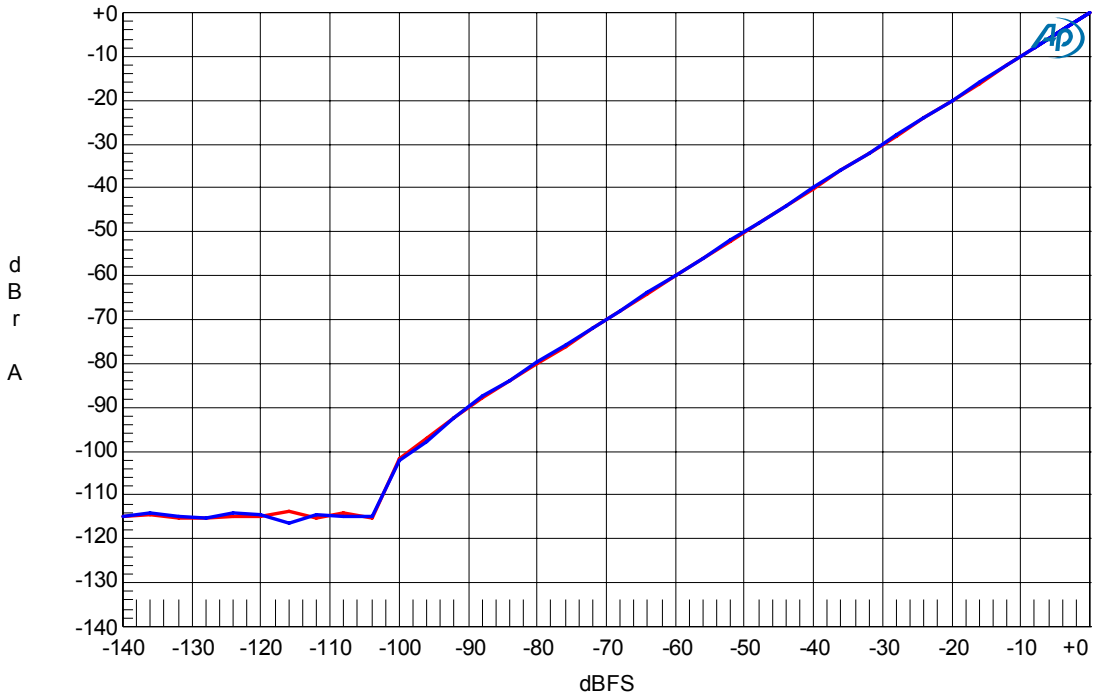


Figure 30. Linearity (Input Frequency =1kHz)

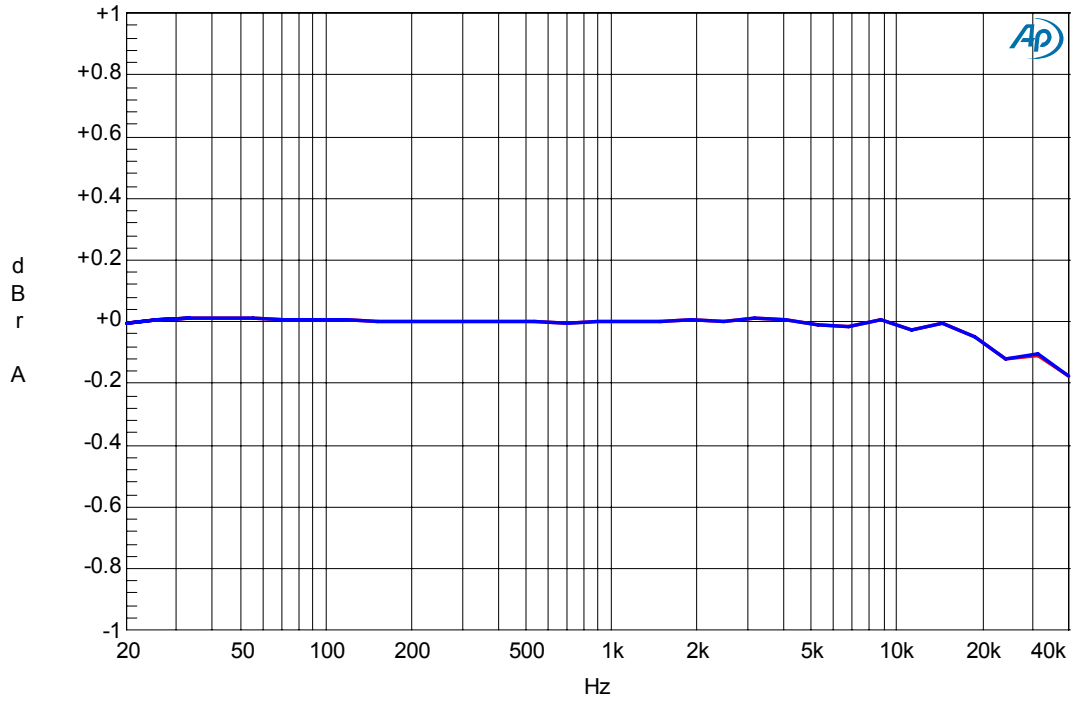


Figure 31. Frequency Response (Input Level=0dBFS)

(DAC fs=96kHz)

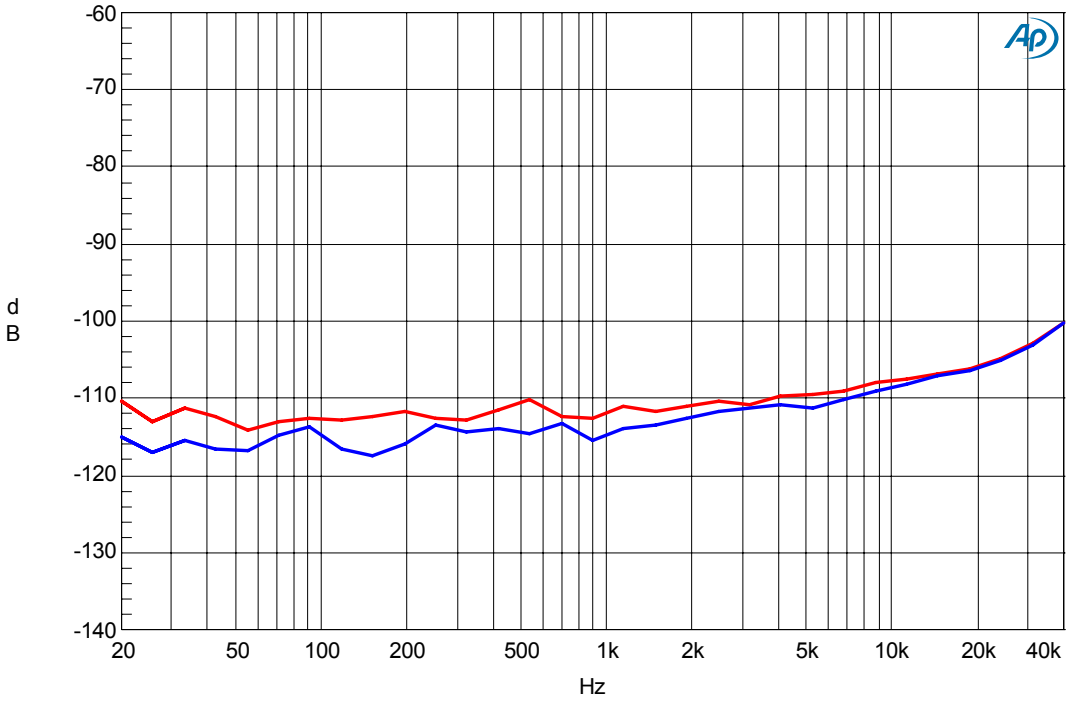


Figure 32. Cross-talk (Input Level=0dBFS)

(DAC fs=192kHz)

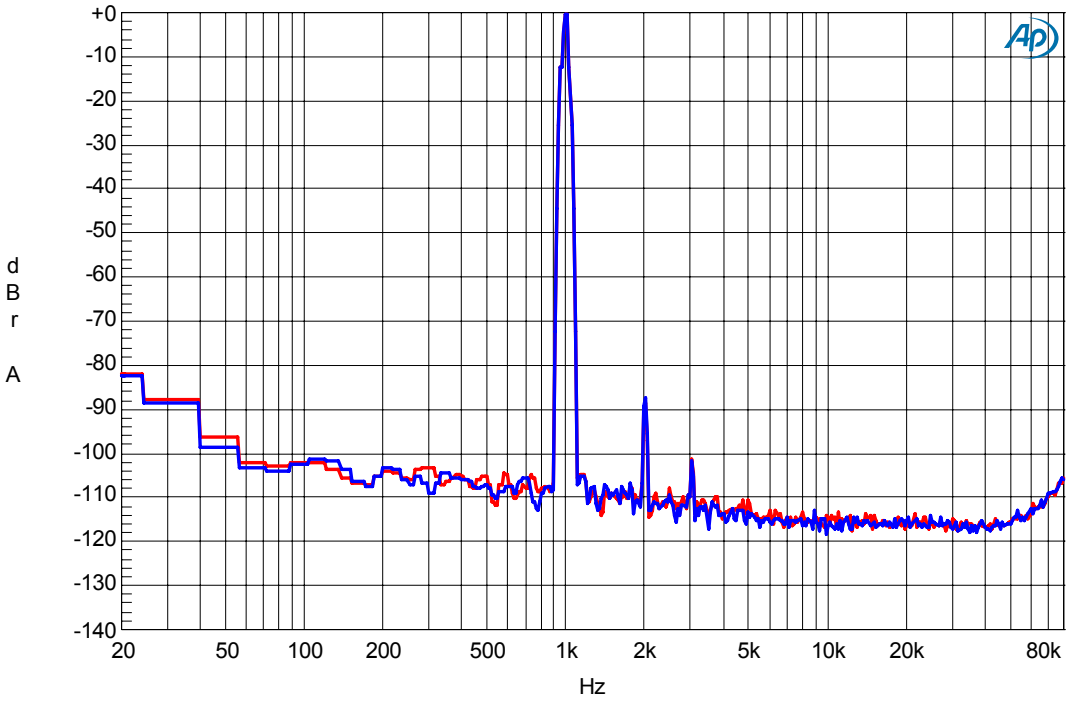


Figure 33. FFT(Input Frequency =1kHz, Input Level=0dBFS)

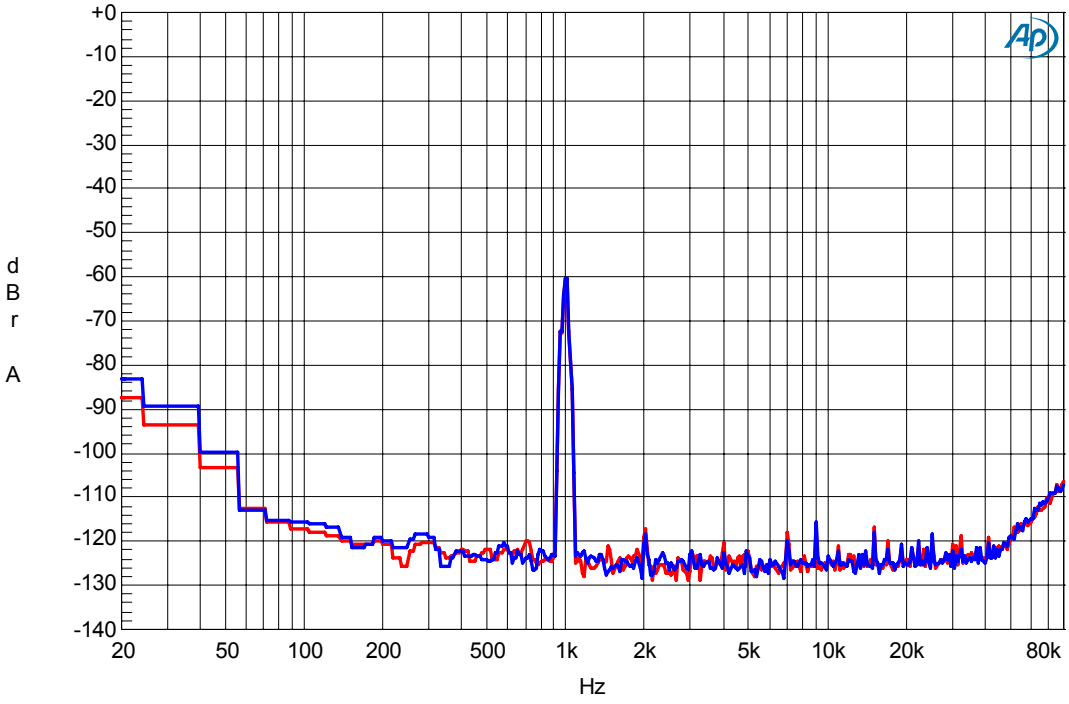


Figure 34. FFT(Input Frequency =1kHz, Input Level=-60dBFS)

(DAC fs=192kHz)

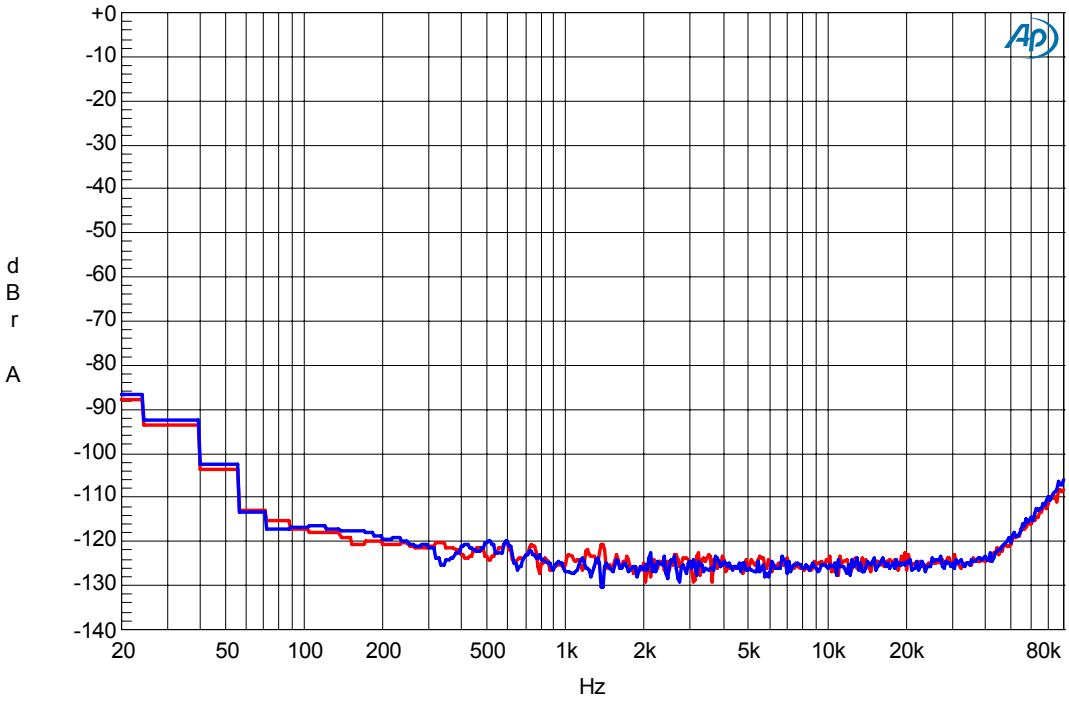


Figure 35. FFT(noise floor)

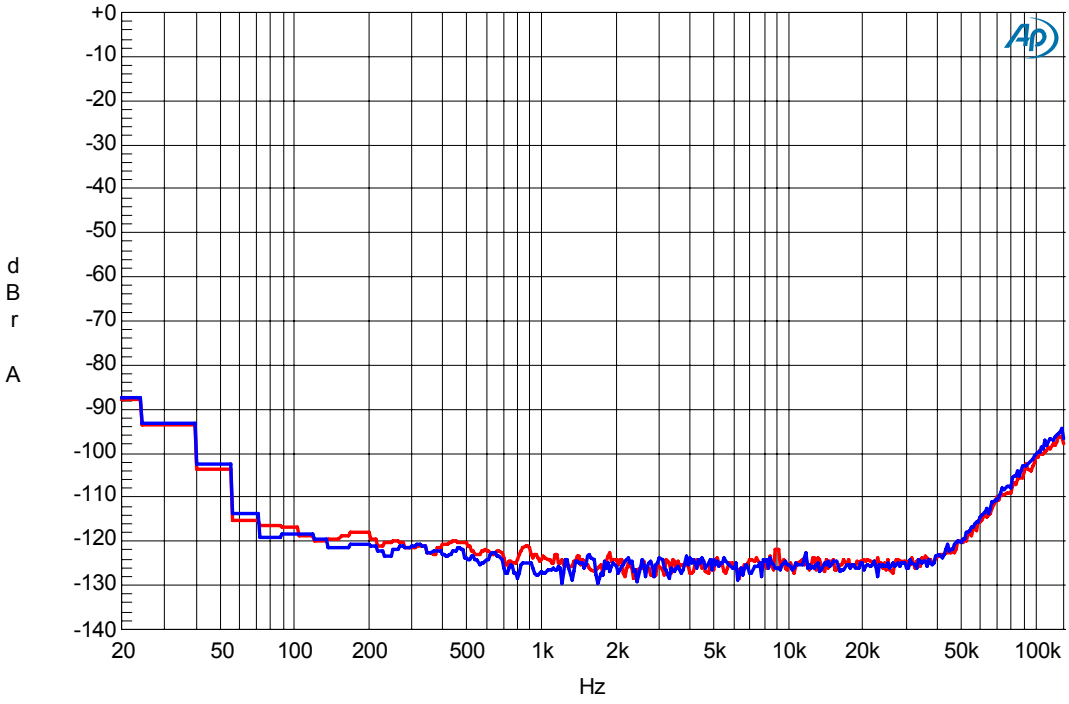


Figure 36. FFT (Out of band Noise)

(DAC fs=192kHz)

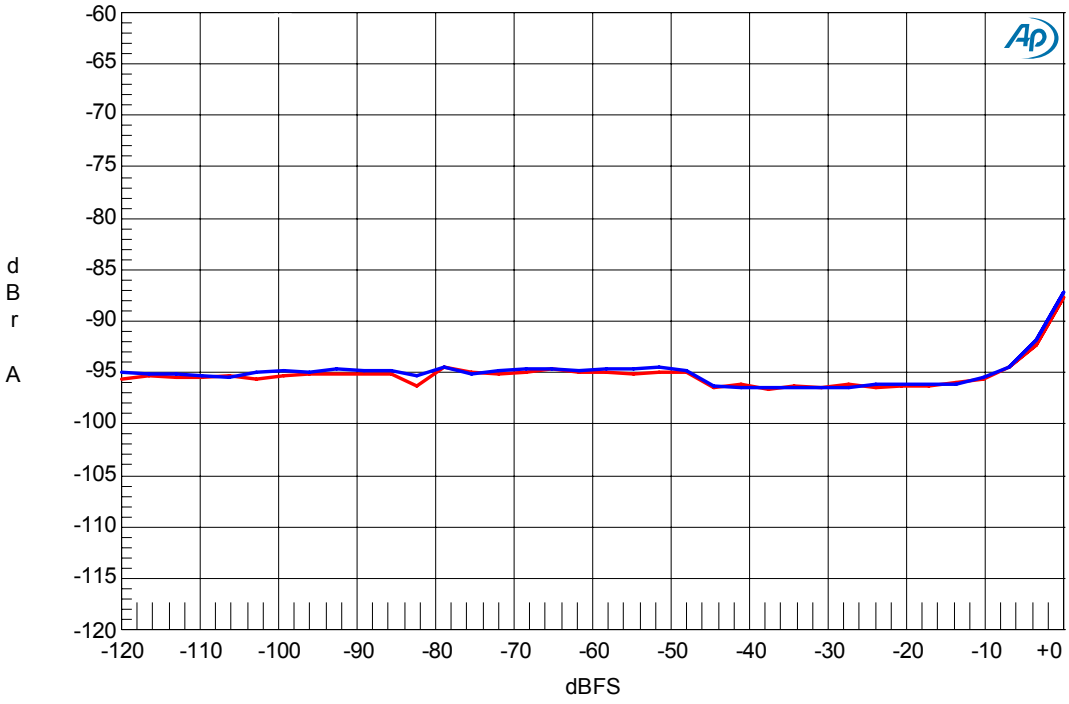


Figure 37. THD+N vs Input Level (Input Frequency =1kHz)

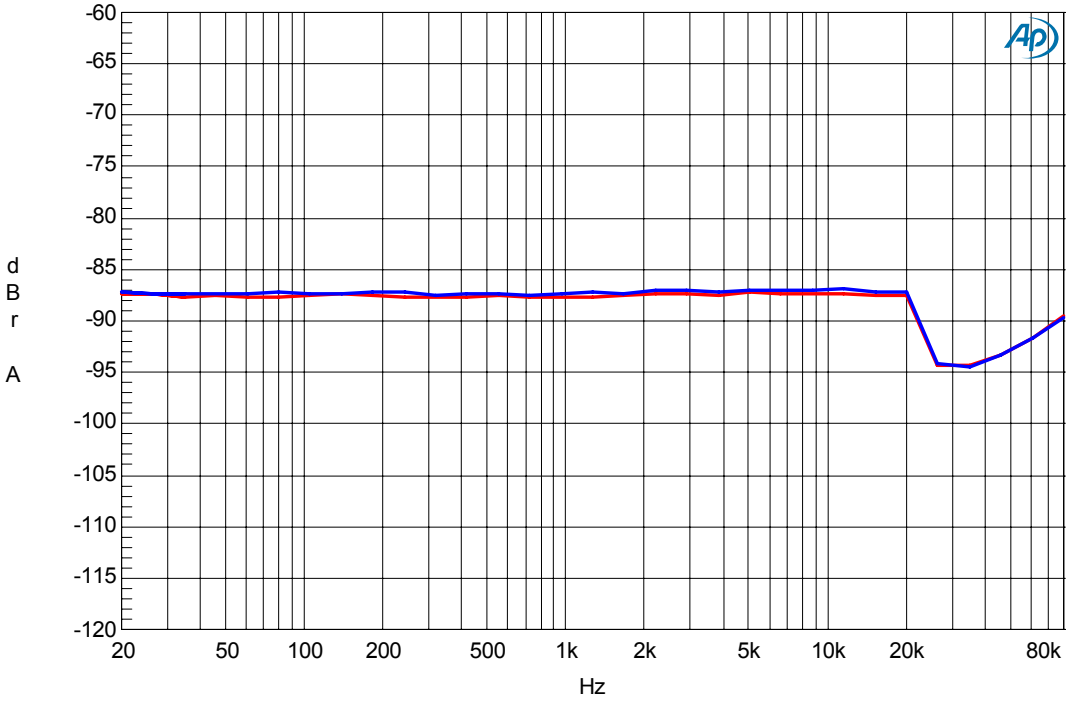


Figure 38. THD+N vs Input Frequency (Input Level=0dBFS)

(DAC fs=192kHz)

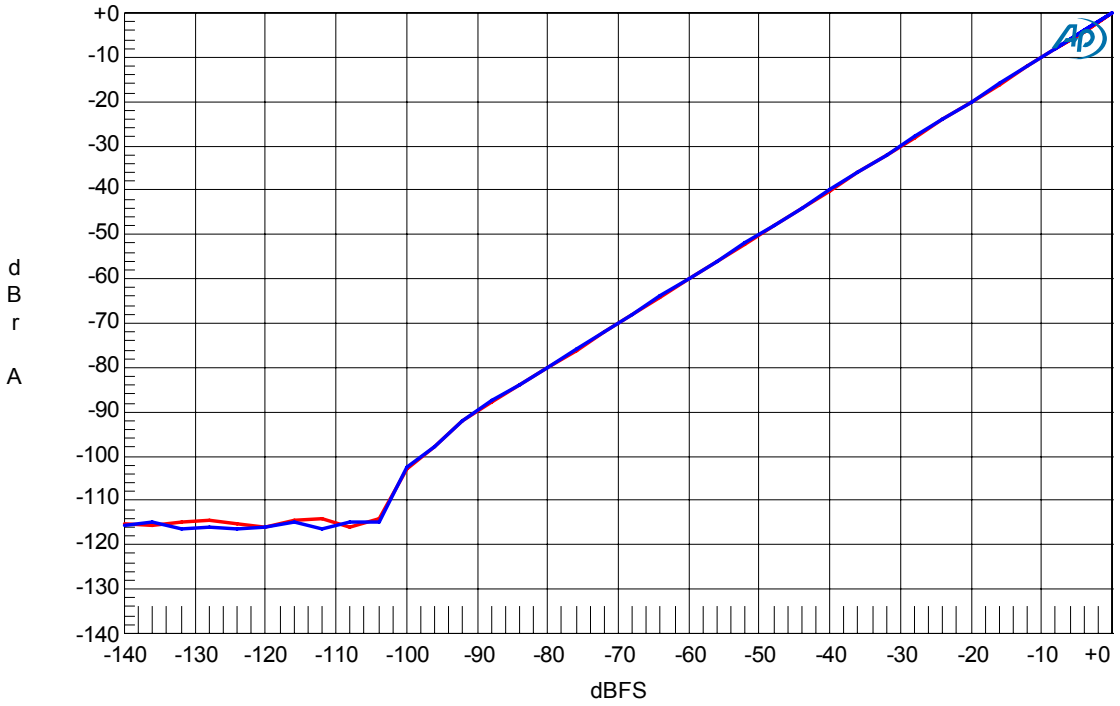


Figure 39. Linearity (f Input Frequency =1kHz)

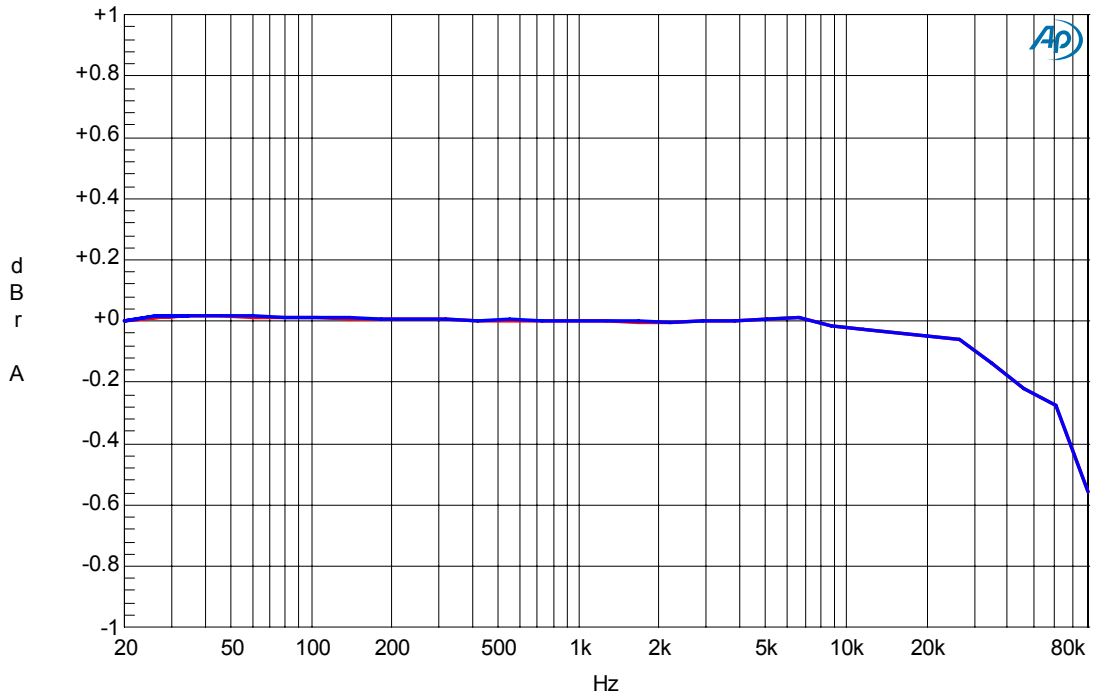


Figure 40. Frequency Response (Input Level=0dBFS)

(DAC fs=192kHz)

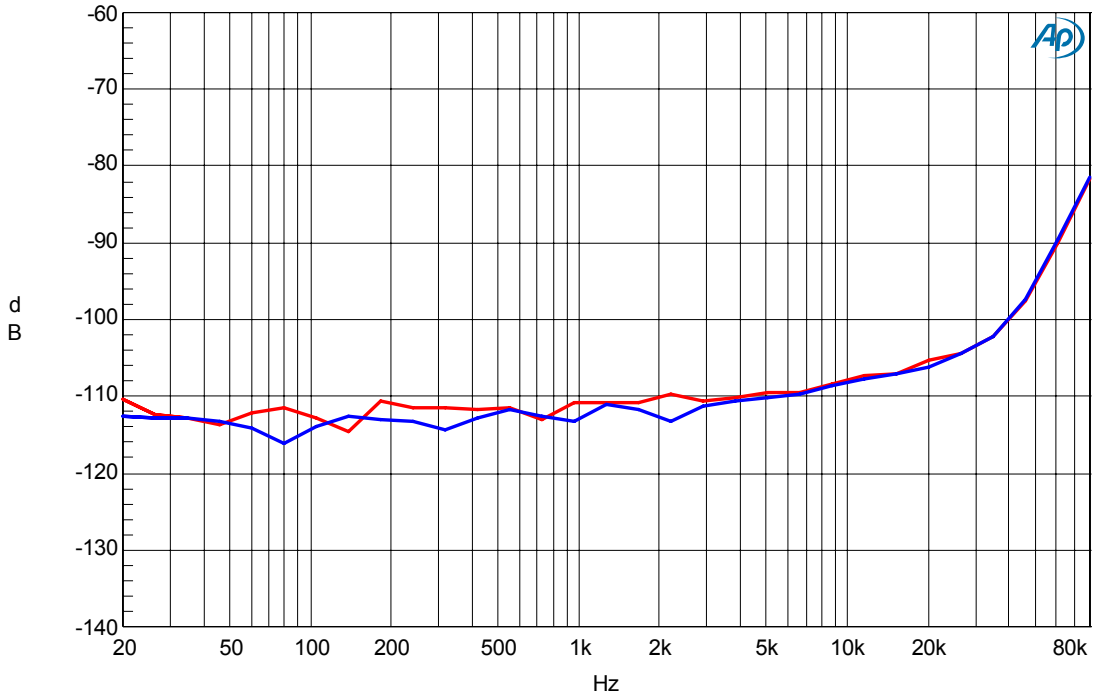


Figure 41. Cross-talk (Input Level=0dBFS)

REVISION HISTORY

Date (yy/mm/dd)	Manual Revision	Board Revision	Reason	Page	Contents
2010/08/13	KM103800	0	First Edition		

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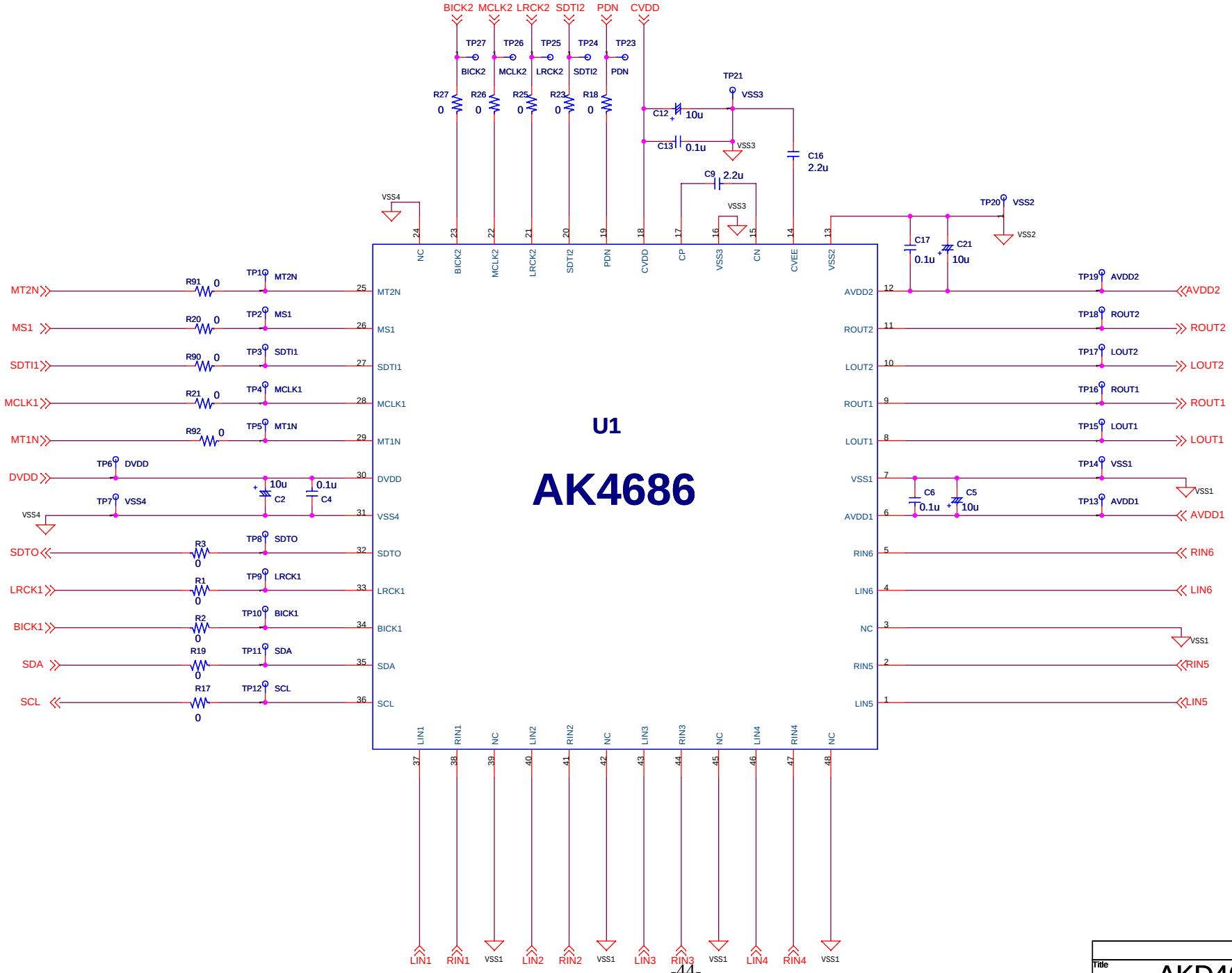

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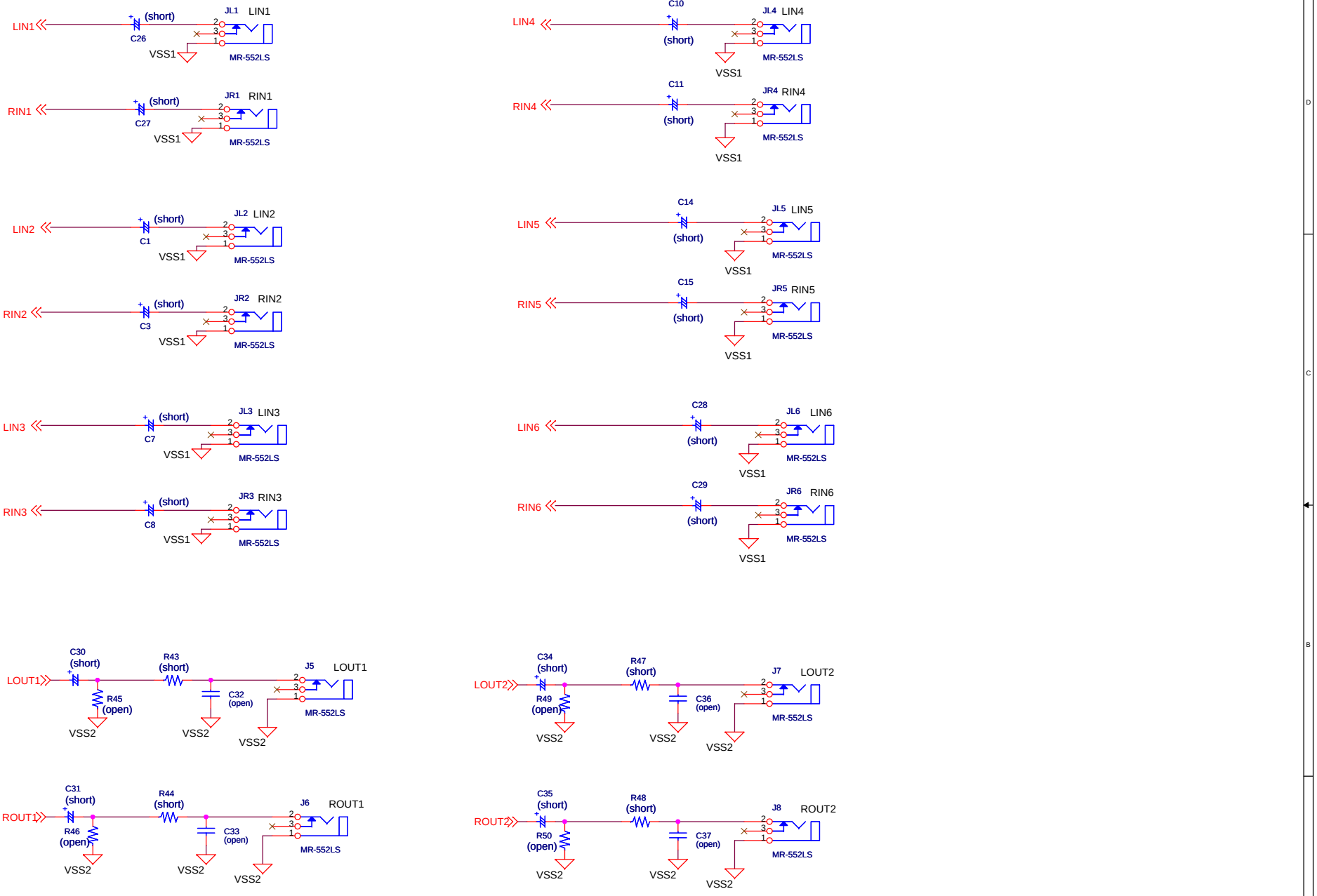
Size A3	Document Number AK4686	Rev 0
Date: Friday, August 13, 2010	Sheet 1 of 6	



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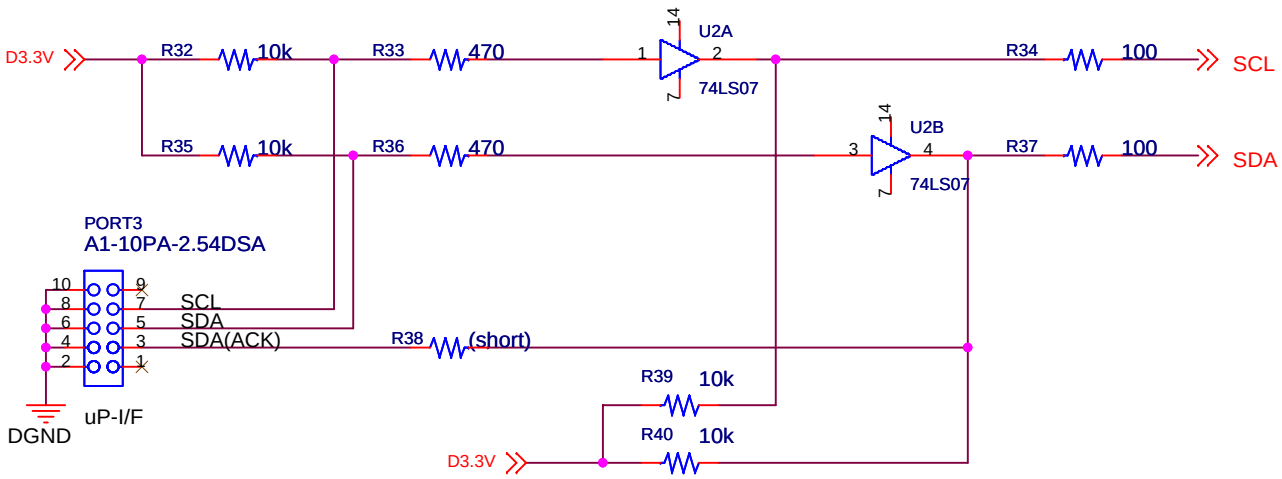
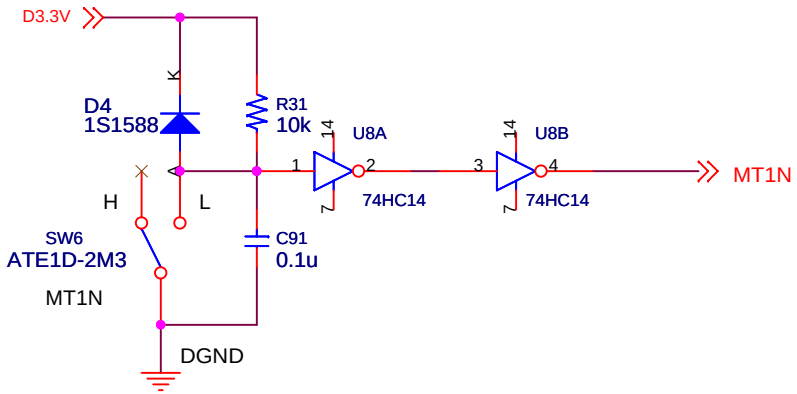
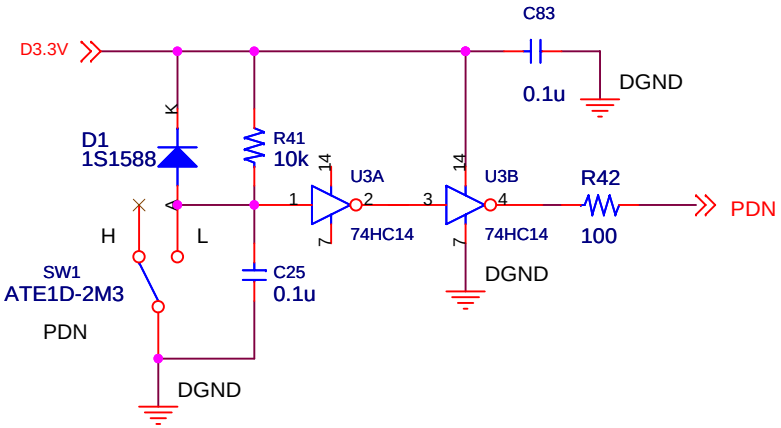
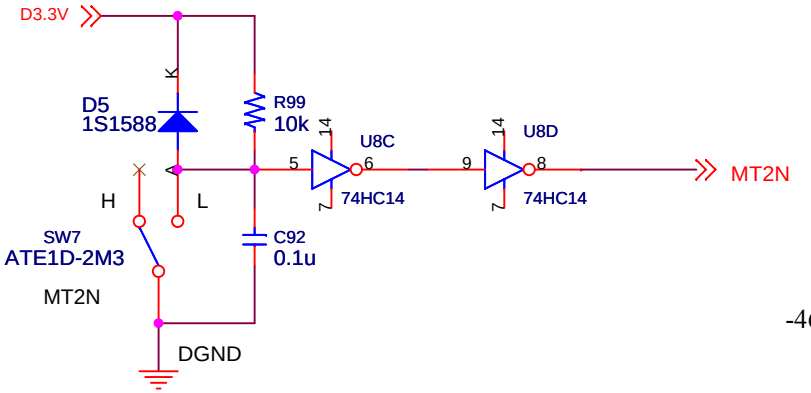
Size A3	Document Number Analog Input/Output	Rev 0
Date: Friday, August 13, 2010	Sheet 2 of 6	









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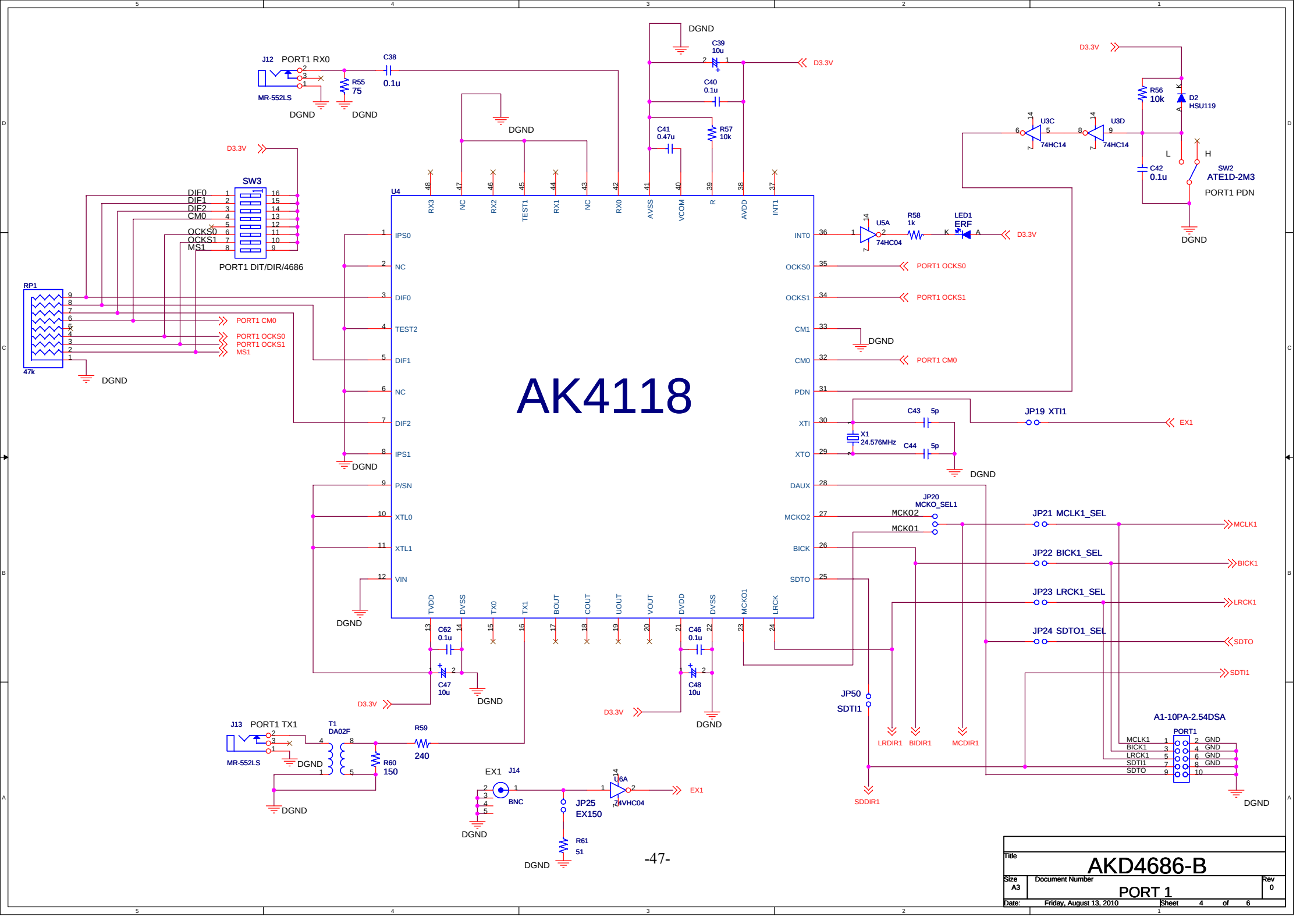
Size A4	Document Number INPUT/OUTPUT	Rev 0
Date: Friday, August 13, 2010	Sheet 3 of 6	



Title	AKD4686-B	
Size A3	Document Number PORT 1	Rev 0
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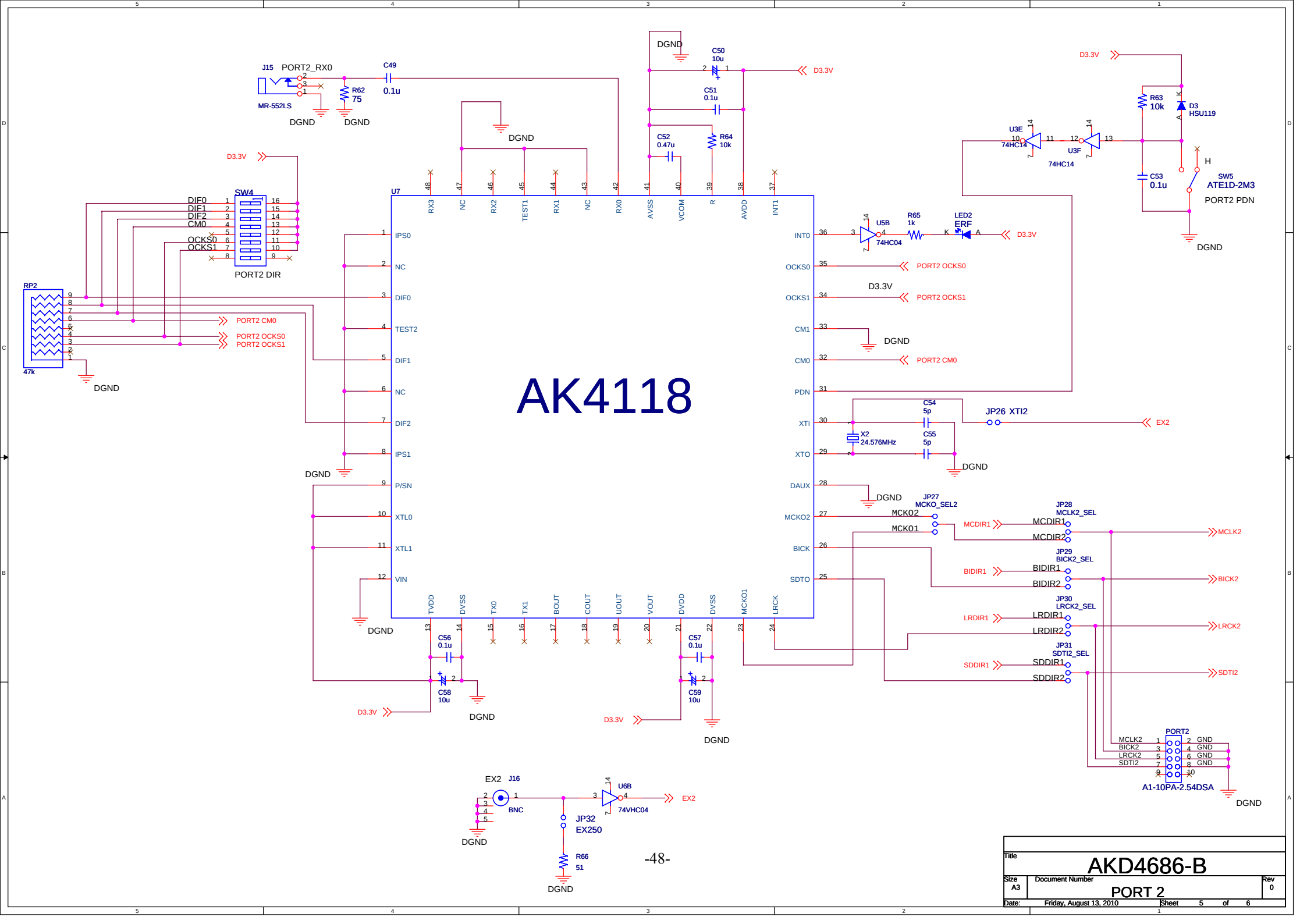
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0.47u
R64
10k
D3.3V
SW4
DIF0
DIF1
DIF2
CM0
OCKS0
OCKS1
PORT2 DIR
RP2
47k
PORT2 CM0
PORT2 OCKS0
PORT2 OCKS1
U7
IPS0
NC
DIF0
TEST2
DIF1
NC
DIF2
IPS1
P/SN
XTL0
XTL1
VIN
INT0
OCKS0
OCKS1
CM1
CM0
PDN
XTI
XTO
DAUX
MCKO2
BICK
SDTO
C56
0.1u
C58
10u
C57
0.1u
C59
10u
U3E
74HC14
U3F
74HC14
R63
10k
D3
HSU119
C53
0.1u
SW5
ATE1D-2M3
PORT2 PDN
U5B
74HC04
R65
1k
LED2
ERF
C54
5p
C55
5p
X2
24.576MHz
JP26 XTI2
EX2
JP27
MCKO_SEL2
MCKO2
MCK01
JP28
MCLK2_SEL
MCDIR1
MCDIR2
MCLK2
JP29
BICK2_SEL
BIDIR1
BIDIR2
BICK2
JP30
LRCK2_SEL
LRDIR1
LRDIR2
LRCK2
JP31
SDTI2_SEL
SDDIR1
SDDIR2
SDTI2
PORT2
MCLK2
BICK2
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JP32
EX250
R66
51
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AKD4686-B
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A3
Document Number
PORT 2
Rev
0
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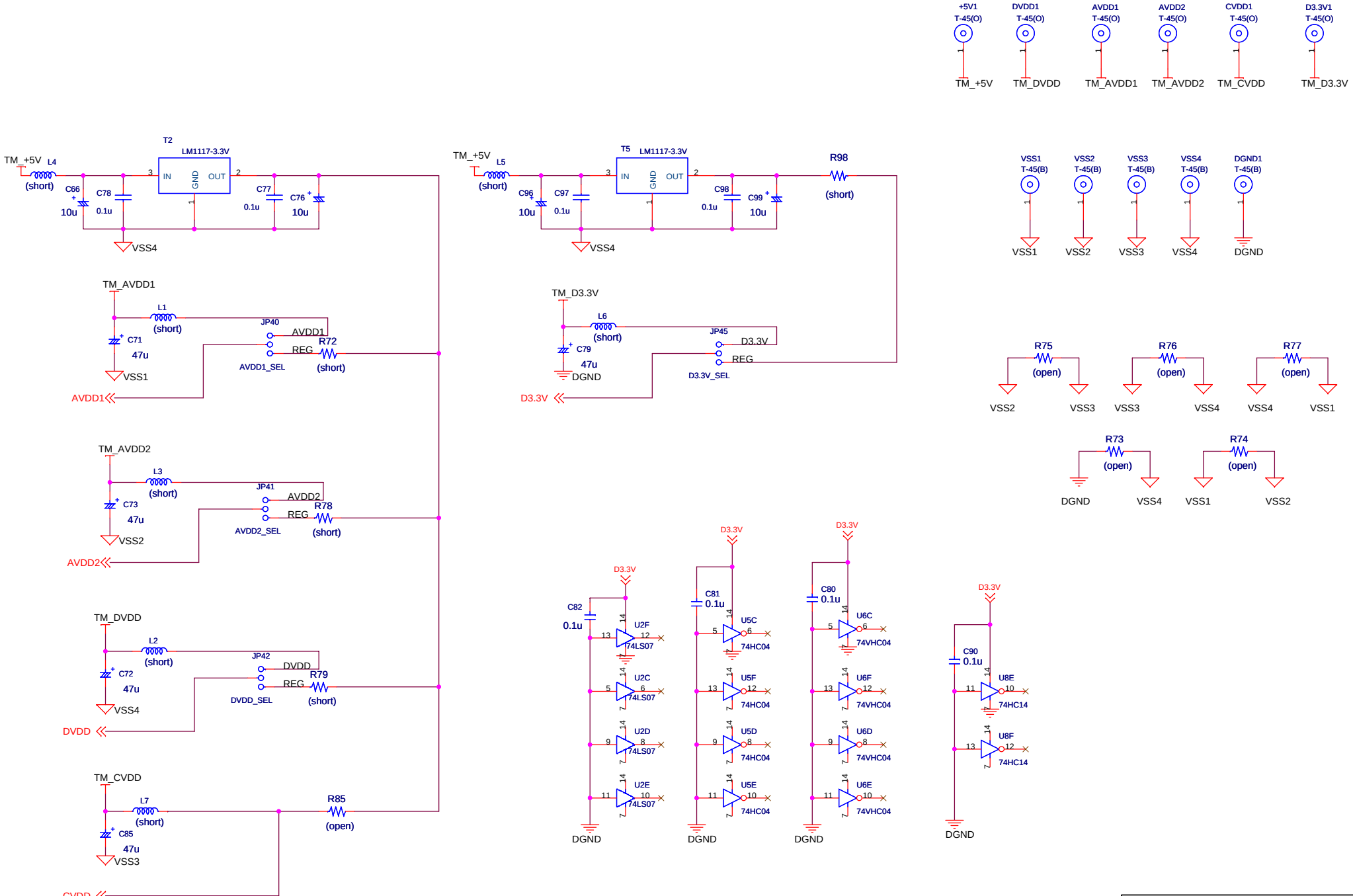
6



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Size A3	Document Number Power Supply	Rev 0
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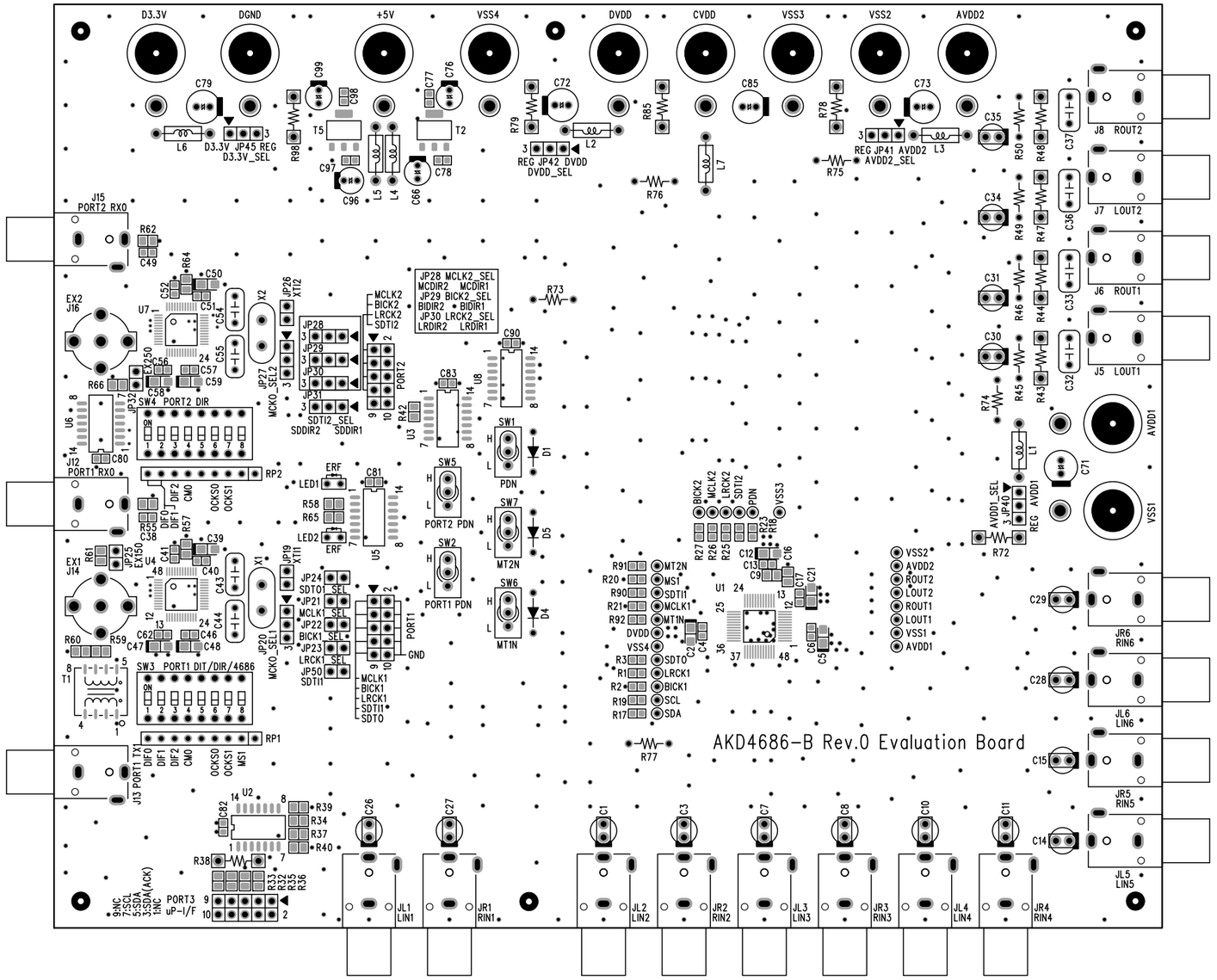
部品面シルク図　　部品面透視図



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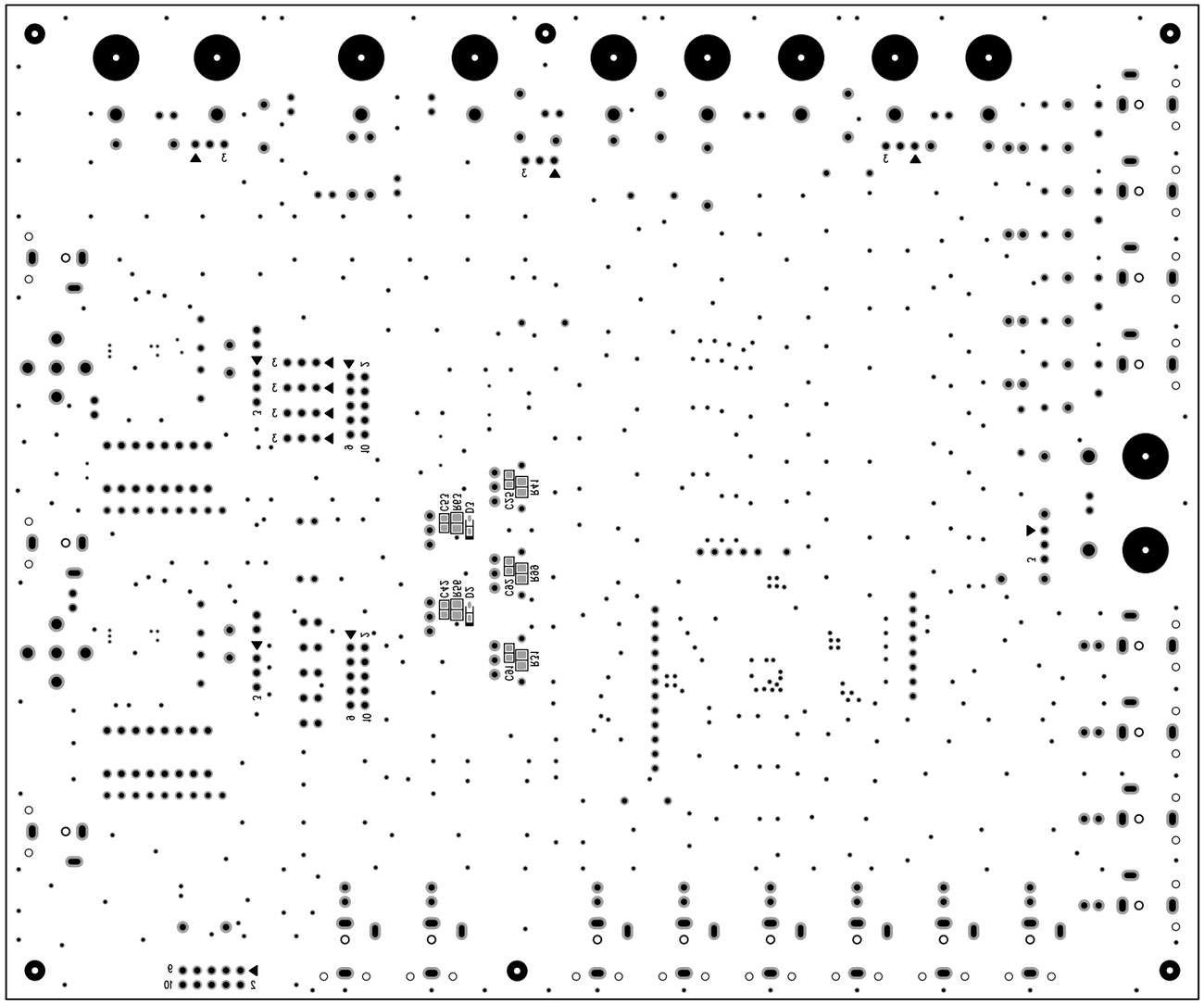
半田面シルク図　　部品面透視図



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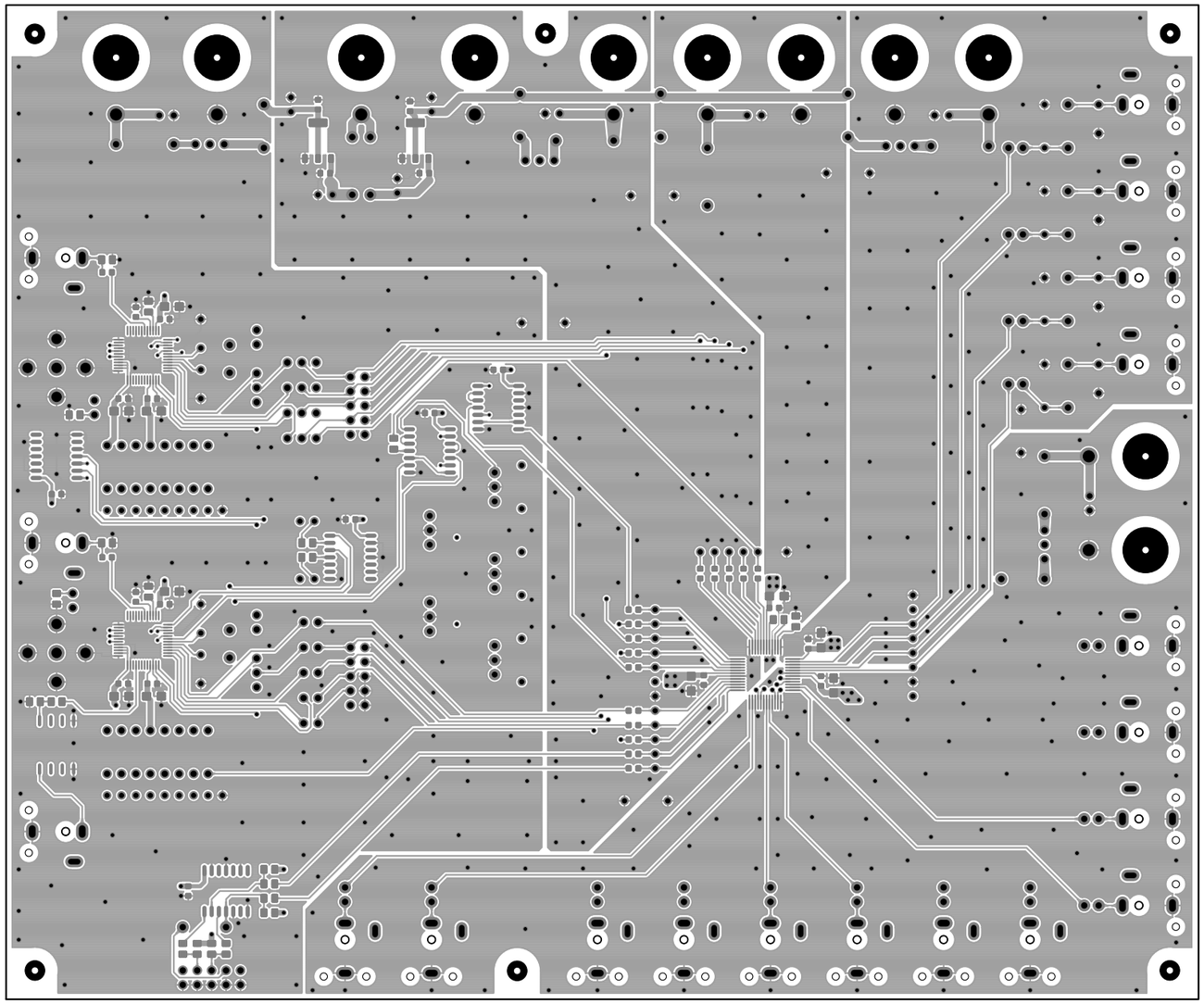

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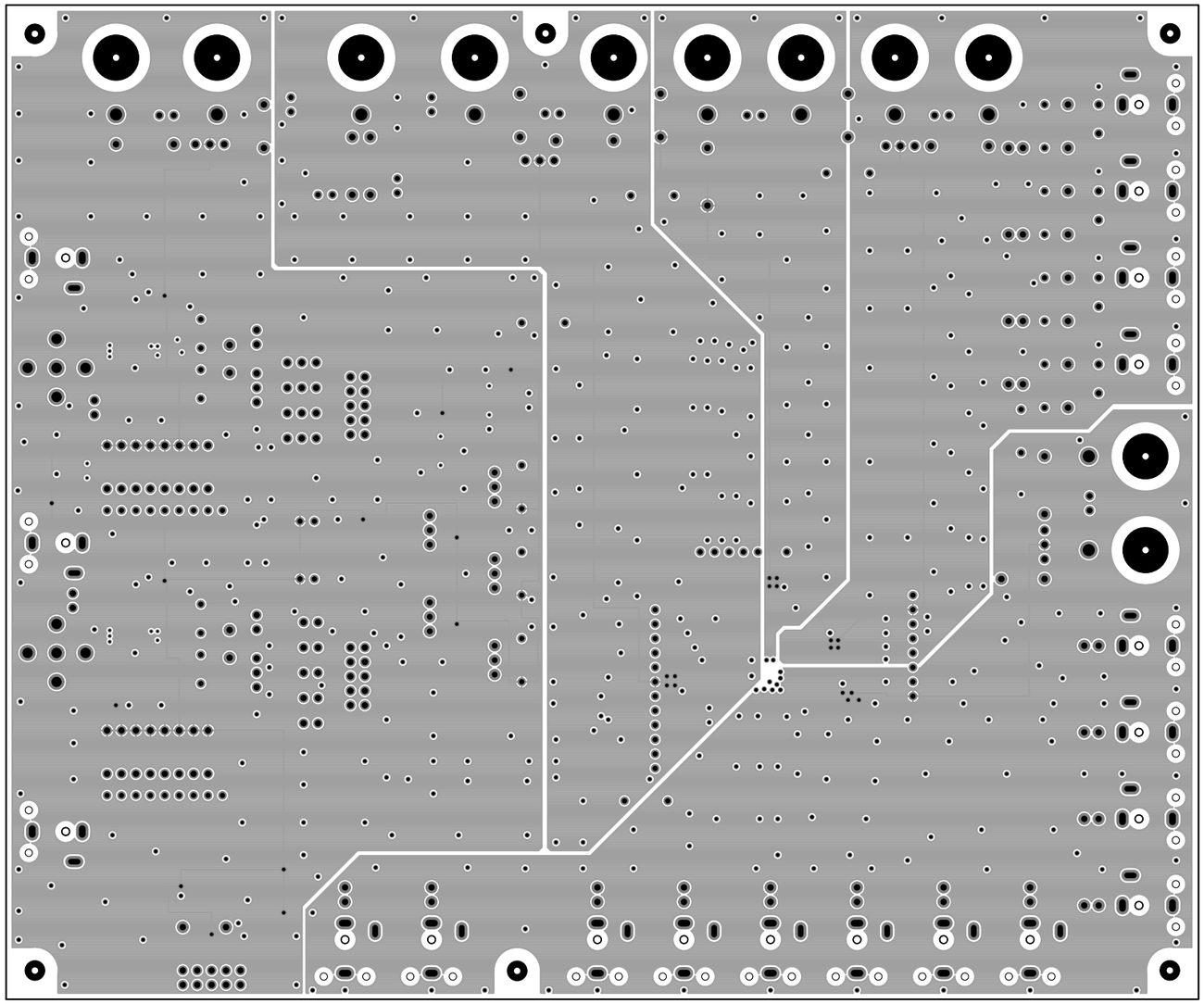

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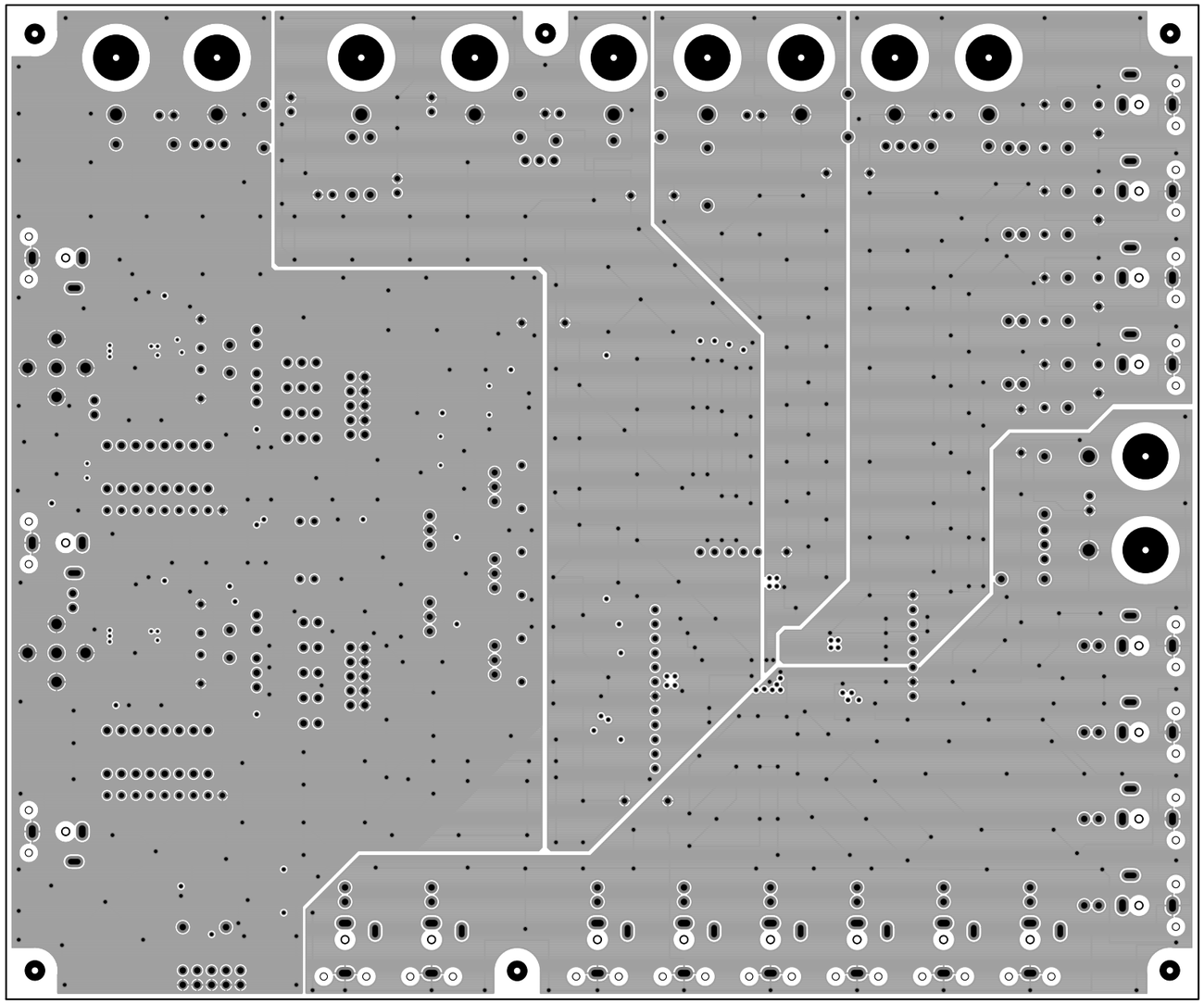

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半田面パターン図　　部品面透視図