HD66779

366-channel Source Driver for 262,144-color Displays (64 grayscale) for Amorphous Silicon, Low-temperature Poly-silicon TFT Panels

REJxxxxxxx-xxxxZ
Rev.1.00
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Description

The HD66779 is a channel source driver LSI compliant to 366-channel graphics display on TFT LCD in 262,144 colors. With an internal timing controller, the HD66779 can adjust LCD signals to an optimum timing.

The HD66779 incorporates 18-bit RGB interface (VSYNC, HSYNC, DOTCLK, ENABLE, and PD 17-0) for moving picture display. As a system interface with microcomputer, the HD66779 adopts a serial interface which enables high quality display and low power consumption through instruction settings.

The HD66779 enables precise management of power by software, which makes this LSI the best solution for medium or small-sized portable products such as digital cellular phones or PDA supporting WWW browser, where long battery life is major concern.

Features

- 366-channel output built-in liquid-crystal display driver circuit
- 6-bit (grayscale data) x RGB data
- 18-bit built-in RGB Interface for moving picture display: VSYNC, HSYNC, DOTCLK, ENABLE, PD17-0
- multicolor display: 262,144 colors simultaneously available
- Built-in timing controller: adjust LCD signals to an optimized timing
- 10 reference power supply voltage pins enables optimum γ compensation according to liquid crystal characteristics
- System interface: Serial Peripheral Interface (SPI)
- Border display: 6-channel border display by mode setting
- Cascade connection
- Reversible source-driver shift direction
- Built-in level shift circuit for LCD signals
- Built-in Vcom generating circuit
- Raster-row inversion drive
- High-speed operation: 10MHz Max.
- Power supply voltage range

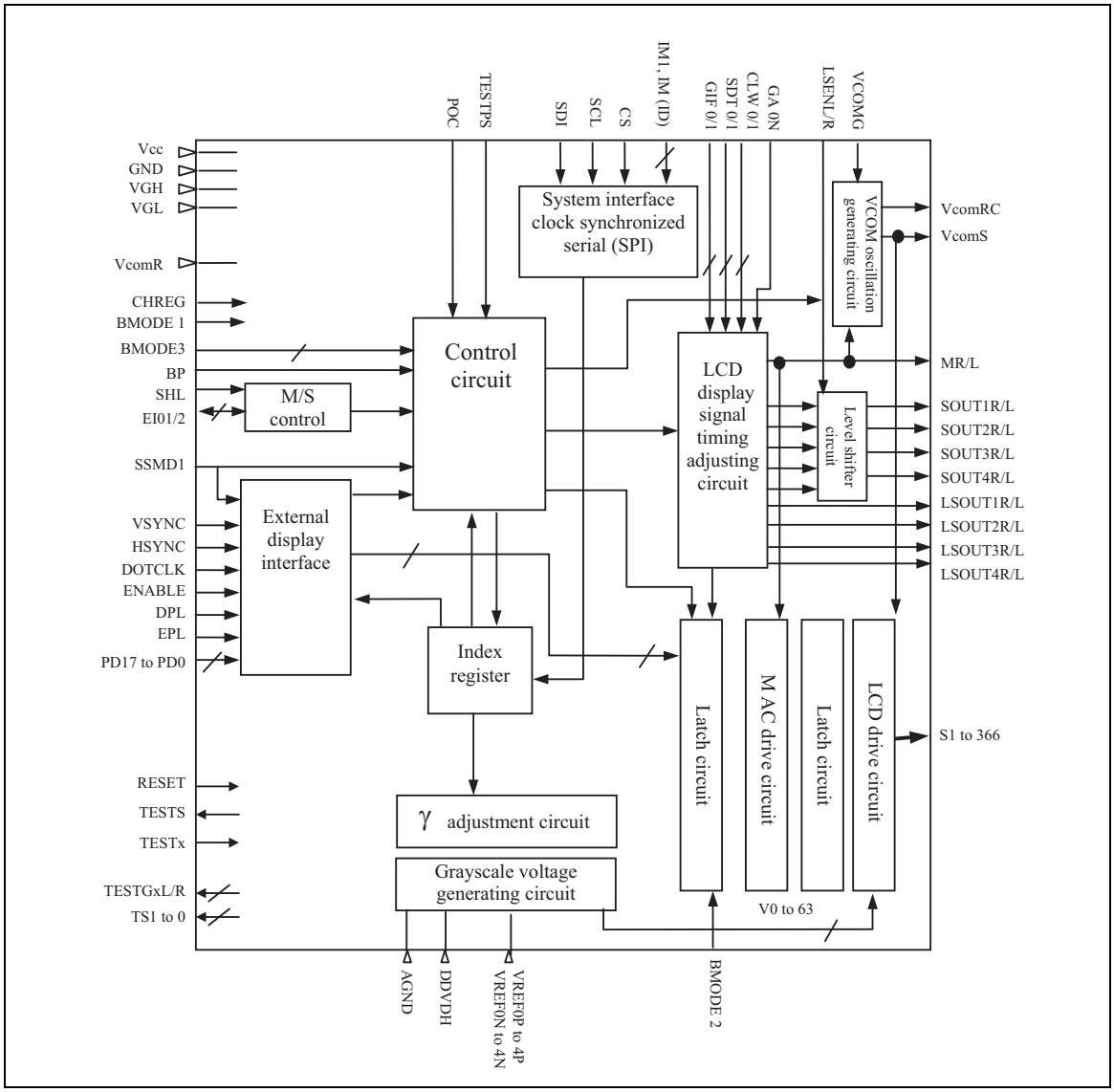
  Input voltage level

  - Logic power supply voltage: Vcc = 2.5V ~ 3.6V
  - Source driver power supply voltage: DDVDH = 3.5V ~ 5.5V
  - Gate driver power supply voltage: VGH –VGL = 16V ~ 35V
VGH –AGND = 8V ~ 20V
VGL –AGND = -15V ~ -8V

  Output voltage level

  - Output for LCD display panel: SOUT1-4R/L = VGL ~ VGH
LSOUT1-4R/L, M = GND ~ Vcc
  - Source output S1 to S366 = AGND + 0.3 ~ DDVDH – 0.3
  - VCOMS output voltage VCOMS = AGND ~ DDVDH

Block Diagram



Block Function

(1) External Display Interface (RGB –I/F)

The HD66779 incorporates RGB-I/F as an external interface for moving picture display. In the RGB-I/F mode, the HD66779 operates in synchronization with externally supplied signals (VSYNC, HSYNC, and DOTCLK), and takes in data according to data enable signal (ENABLE). See "RGB interface timing" for details.

The correspondence between input and output data is as follows.

Input data	PD 17	PD 16	PD 15	PD 14	PD 13	PD 12	PD 11	PD 10	PD 9	PD 8	PD 7	PD 6	PD 5	PD 4	PD 3	PD 2	PD 1	PD 0
RGB assignment	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Output pins	S (3n+1)						S (3n+2)						S (3n+3)					

* n = 0 to 121

(2) Control circuit

Generate internal control signal from each signal.

(3) Grayscale Voltage Generation Circuit

Generates positive-polarity 64 grayscales and negative-polarity 64 grayscales by dividing external input voltage with resistors to enable display in 262,144 colors. See the "Grayscale Amplifier Configuration" for details.

(4) Timing Generator

Generate timing signals for LCD display operation.

(5) LCD Driver Circuit

The LCD driver circuit comprises a 366-source-output (S1-S366) driver. Line-latch display pattern data and output drive waveform. The shift direction of source output is changeable, i.e. (S1, S2, S3) to (S364, s365, S366) or (S364, S365, S366) to (S1, S2, S3), depending on the assembly.

(6) VCOM oscillation generator circuit

Generate oscillation signal VcomS to further generate Vcom, which is supplied to the TFT common electrode. Alternate at amplitude of either VcomR or GND level depending on the AC frequency signal.

(7) Level shifter circuit

Change operation voltage level from that of logic circuit "Vcc to GND" to that of gate drive circuit "VGH to VGL".

(8) System interface clock synchronized serial circuit

Interfacing with a microcomputer enables register setting for each mode setting.

Pin function

Signals	Number of pins	I/O	Connected to	Function
DDVDH	1	I	Power supply	Power supply for the source driver. DDVDH = +3.5 ~ +5.5V. Make sure VGH ≥ DDVDH ≥ VCC.
AGND	1	I	Power supply	Grand for the source driver. AGND = 0V.
Vcc	1	I	Power supply	Power supply for the logic. Vcc = +2.5V ~ +3.6V Make sure VGH ≥ DDVDH ≥ VCC.
GND	1	I	Power supply	Grand for the logic. GND = 0V.
VGH	1	I	Power supply	Power supply for a level shifter. VGH = +8.0V ~+20V Make sure VGH ≥ DDVDH ≥ VCC.
VGL	1	I	Power supply	Power supply for a level shifter. VGL = –15V ~ – 8.0V
VcomR	1	I	Power supply	Input high level of VcomS
VcomRC	1	O	Stabilizing capacitor	Output high level of VcomS
VcomS	1	O	Capacitor	Amplitude signal for alternating operation. Serve as a power supply for the electrode pair (common) of TFT display by coupling with an external circuit.
RESET	1	I	MPU or external CR circuit	Reset pins. Initialized while “Low”. Power-on reset required after turning on the power supply.
VREF0P-4P VREF0N-4N	10	I	Power supply	Power supply for γ compensation. Must observe the following relationships when supplying voltage. ・ DDVDH-0.3V ≥ VREF0P>VREF1P>VREF2P>VREF3P> VREF4P ≥ AGND+0.3V ・DDVDH-0.3V ≥ VREF0N > VREF1N > VREF2N> VREF3N > VREF4N ≥ AGND +0.3V ・ DDVDH-1.0V ≥ VREF1P,VREF1N VREF3P, VREFF3N ≥ GND + 1.0V
TEST1, 5-15 TESTM2 TESTSM2	14	I	GND	Test pins. Must be fixed to GND level.
VTES,VTEST, COMP, TS1-0 COMM	6	O	Open	Test pins. Must be disconnected.
VCOMMH, VCOMHC, VEQ, VCOMC	4	O	Open	Test pins. Must be disconnected.

Signals	Number of pins	I/O	Connected to	Function
TESTG1-3R TESTG1-3L	6	O	Open	Test pins. Must be disconnected.
TESTS	1	O	Open	Test pin. Must be disconnected.
TESTPS TEST4	2	I	Vcc	Test pin. Must be fixed to the Vcc level.
S1 ~ S366	366	O	LCD	Output voltage applied to liquid crystal. The shift direction of source output is changeable with SHL pin. SHL = “High”: (S1, S2, S3) to (S364, S365, S366) SHL = ”Low”: (S364, S365, S366) to (S1, S2, S3)
BMODE1	1	I	GND or Vcc	Select border mode. BMODE1 = “Higih”: border display (360ch display + 6-ch border) BMODE1 = “Low”: No border display (360ch) Border display lasts 320H.
BMODE2	1	I	GND or Vcc	Select pins used for the border mode. BMODE2 = “High”: Right side BMODE2 = “Low”: Left side
BMODE3	1	I	GND or Vcc	Select the border color while using DE transfer mode. With normally white display, BMODE3 = “High”: BLACK BMODE3 = “Low”: WHITE While using DE transfer mode, 6-channel (2RGB) border color is made on the left/right sides only.
POC	1	I	MPU or Vcc	Power control signal. POC = “High”: Normal mode POC = “Low”: Power control mode When POC = “L”, Non-lit display is shown (white display in normally white mode). For details, see “Power Control Mode”. The initialized value for the border is “1” for all.
SHL	1	I	GND or Vcc	Control the shift direction of display data. SHL = “High”: (S364,S365,S366) to (S1,S2,S3) SHL = “Low”: (S1,S2,S3) to (S364, S365, S366)
VCOMG	1	I	GND or Vcc	Vcom generator enable signal **VCOMG** / **Vcom output** H / Vcom generating L / GND
CHREG	1	I	GND or Vcc	Switch between the pin setting and the register setting. CHREG = “High”: Register setting is valid. All pin settings are made invalid. CHREG = “Low”: The settings for pins, POC, POS, BP,GAON, GIFI-0, CLW1-0, SDT1-0 are valid.

Signals	Number of pins	I/O	Connected to	Function
VSYNC	1	I	MPU	Frame synchronizing signal. “Low” active signal.
HSYNC	1	I	MPU	Line synchronizing signal. “Low” active signal.
DOTCLK	1	I	MPU	Dot clock signal. The timing for reading data is selected with DPL pin.
PD17 ~ PD0	18	I	MPU	Input display data of 6-bit (grayscale) x 3 pixels. As data is transferred with these pins, unused pins must be fixed to either “Vcc” or “GND” level. **PD17 to PD12** / **PD11 to PD6** / **PD5 to PD0** MSB·····LSB / MSB·····LSB / MSB·····LSB S (3n+1) / S (3n+2) / Sn (3n+3) * n = 0 to 121
ENABLE (DE)	1	I	MPU	Data enable signal. **EPL** / **ENABLE** / **Data write** L / L / Valid L / H / Invalid H / L / Invalid H / H / Valid
EI01/2	2	I/O	HD66779	Start pulse signal. SHL signal controls the switch between input and output. When the signal is used as output, output the H pulse and start up the next raster-row driver. **SHL** / **EI01** / **EI02** L / Input / Output H / Output / Input When using EI0/2 as input, use as start pulse input or fix to Vcc level.
DPL	1	I	GND or Vcc	Set the polarity of DOTCLK pin while receiving data (PD17 to 0). DPL = “Low”: Read data at DOTCLK falling edge. DPL = “High”: Read data at DOTCLK rising edge.
EPL	1	I	GND or Vcc	Set the polarity of ENABLE pin while receiving data (PD17 to 0). EPL = “L”: When ENABLE = “L”, data write is valid. When ENABLE = “H”, data write is invalid. EPL = “H”: When ENABLE = “L”, data write is invalid. When ENABLE = “H”, data write is valid.

<table>
<tr><th>Signals</th><th>Number of pins</th><th>I/O</th><th>Connected to</th><th>Function</th></tr>
<tr><td>BP</td><td>1</td><td>I</td><td>GND or Vcc</td><td>Set a back porch during vertical period.
BL = “L”: Back porch = 4
Receive data (PD17 to 0) after 4H after VSYNC assertion
BL = “H”: Back porch = 8
Receive data (PD17 to 0) after 8H after VSYNC assertion
* In the DE transfer mode (SSMD1 = “H”), BP setting is made invalid.</td></tr>
<tr><td>CLW0/1</td><td>2</td><td>I</td><td>GND or Vcc</td><td>Set the delay amount of the output signal from SOUT2/ SOUT3.
Delay amount
CLW1 CLW0 Delay time 5MHz (e.g.)
L L 0μS 0 clock
L H 2.0μS 10clocks
H L 4.0μS 20 clocks
H H 6.0μS 30 clocks
* The delay time changes depending on the frequency of DOTCLK.</td></tr>
<tr><td>SDT0/1</td><td>2</td><td>I</td><td>GND or Vcc</td><td>Set the delay amount of source output.
Delay amount
SDT1 SDT0 Delay time 5MHz (e.g.)
L L 2.0μS 10 clocks
L H 3.0μS 15 clocks
H L 4.0μS 20 clocks
H H 5.0μS 25 clocks
* The delay time changes depending on the frequency of DOTCLK.</td></tr>
<tr><td>ML
MR</td><td>2</td><td>O</td><td>Power supply or open</td><td>AC cycle clock signal. (Output logic level)
ML and MR output a same signal. Due to chip layout, ML and MR are arranged on the left and right sides respectively. Use either one of them and left the other open.</td></tr>
<tr><td>SOUT1L
SOUT1R</td><td>2</td><td>O</td><td>Gate circuit</td><td>Frame pulse signal for LCD display. (Level shifter output with operational voltage amplitude VGH-VGL).
SOUT1L and SOUT1R output a same signal. Due to chip layout, SOUT1L and SOUT1R are arranged on the left and right sides respectively. Use either one of them and left the other open. The LSEL/LSER pin function enables to halt output from either one or both.</td></tr>
</table>

Signals	Number of pins	I/O	Connected to	Function
SOUT2R SOUT2L	2	O	Gate circuit	Line cycle clock signal for LCD display. (Level shifter output with operational voltage amplitude VGH-VGL). The line cycle mode is changeable by the combination of gate interface output select signal pins (GIF0, GIF1). SOUT2L and SOUT2R output a same signal. Due to chip layout, SOUT2L and SOUT2R are arranged on the left and right sides respectively. Use either one of them and left the other open. The LSEL/LSER pin function enables to halt output from either one or both.
SOUT3R SOUT3L	2	O	Gate circuit	Signal for LCD display. (Level shifter output with operational voltage amplitude VGH-VGL). The switch between line cycle mode and Gate-all-on control signal is made by the combination of gate interface output select signal pins (GIF0, GIF1). SOUT3L and SOUT3R output a same signal. Due to chip layout, SOUT3L and SOUT3R are arranged on the left and right sides respectively. Use either one of them and left the other open. The LSEL/LSER pin function enables to halt output from either one or both.
SOUT4R SOUT4L	2	O	Gate circuit	Signal for LCD display. (Level shifter output with operational voltage amplitude VGH-VGL). The switch between gate off control signal and Gate-all-on control signal is made by the combination of gate interface output select signal pins (GIF0, GIF1). SOUT4L and SOUT4R output a same signal. Due to chip layout, SOUT4L and SOUT4R are arranged on the left and right sides respectively. Use either one of them and left the other open. The LSEL/LSER pin function enables to halt output from either one or both.
LSENR	1	I	GND or Vcc	Level shifter enable signal. LSENR = “H”: SOUT1/2/3/4R = level shifter output LSENR = “L”: SOUT1/2/3/4/R = “VGL” output
LSENL	1	I	GND or Vcc	Level shifter enable signal. LSENL = “H”: SOUT1/2/3/4L = Level shifter output LSENL = “L”: SOUT1/2/3/4L = “VGL” output
GIF0/1	2	I	MPU or Vcc or GND	Select display signal.

GIF1	GIF0	L/SOUT2	L/SOUT3	L/SOUT4
L	L	Line cycle clock 1	Line cycle clock 2	open
L	H	Line cycle clock 1	Line cycle clock 2	Gate off signal
H	L	Line cycle clock 1	Line cycle clock 2	Gate all on
H	H	Line cycle clock 3	Gate all on	Gate off signal

Signals	Number of pins	I/O	Connected to	Function
LSOUT1R LSOUT1L	2	O	Gate circuit	Frame pulse signal for LCD display. (Output logic level) LSOU1L and LSOUT1R output a same signal. Due to chip layout, LSOUT1L and LSOUT1R are arranged on the left and right sides respectively. Use either one of them and left the other open.
LSTOU2R LSOUT2L	2	O	Gate circuit	Line cycle clock signal for LCD display. (Output logic level) The line cycle mode is changeable by the combination of gate interface output select signal pins (GIF0, GIF1). LSOUT2L and LSOUT2R output a same signal. Due to chip layout, LSOUT2L and LSOUT2R are arranged on the left and right sides respectively. Use either one of them and left the other open.
LSOUT3R LSOUT3L	2	O	Gate circuit	Signal for LCD display. (Output logic level). The switch between line cycle mode and Gate-all-on control signal is made by the combination of gate interface output select signal pins (GIF0, GIF1). SOUT3L and SOUT3R output a same signal. Due to chip layout, SOUT3L and SOUT3R are arranged on the left and right sides respectively. Use either one of them and left the other open.
LSOUT4R LSOUT4L	2	O	Gate circuit	Signal for LCD display. (Output logic level). The switch between gate off control signal and Gate-all-on control signal is made by the combination of gate interface output select signal pins (GIF0, GIF1). LSOUT4L and LSOUT4R output a same signal. Due to chip layout, LSOUT4L and LSOUT4R are arranged on the left and right sides respectively. Use either one of them and left the other open.
GAON	1	I	MPU or GND	Gate-all-on signal. GAON = “1”: Gate output signal “H” GAON = “0”: Gate output signal “L” Output form SOUT3/4 and LSOUT3/4.
DUMMY1-12	12	O	-	Test pins. Must be disconnected.
IM1, IM0(ID)	2	I	GND or Vcc	Select interfacing mode with MPU.

IM1	IM0/ID	MPU interfacing mode	Pins
GND	ID	Serial Peripheral Interface (SPI)	SDI/SCL
Vcc	*	Border color setting (DE transfer mode)	BMODE3

Use IM0 pin to make a device code ID setting.
RGB I/F mode: Use IM1 = GND.
DE transfer mode: Use IM1 = Vcc.

Signals	Number of pins	I/O	Connected to	Function
CS	1	I	MPU	Chip selection signal for Serial Peripheral Interface (SPI). “Low”: Select (accessible) “High”: (inaccessible) When not used, fix to the “Vcc” level.
SCL	1	I	MPU	Synchronizing clock signal for Serial Peripheral Interface (SPI). When not used, fix to the “Vcc” level.
SDI	1	I	MPU	Serial data input pin (SDI) for Serial Peripheral Interface (SPI). When not used, fix it to the “Vcc” level.
SSMD1	1	I	MPU or GND	Specify the transfer mode. SSMD1 = “H”: DE transfer mode (Serial Peripheral Interface (SPI) is not available) SSMD1 = “L”: RGB I/F mode (Serial Peripheral Interface (SPI) is available.)

Pad Arrangement

Chip size: 15.00mm x 1.50mm
Chip thickness: 550µm(typ.)
PAD coordinate: PAD center
Coordinate origin: Chip center

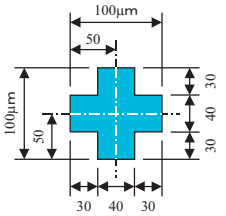
Au bump size:
(1) 63µm x 40µm
Dummy:
No.1 to No.7, No185 to No.191

(2) 59µm x 92µm
Input side:
No.8 to No.184

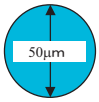
(3) 40µm x 63µm
Laced LCD output side:
No.192 to No.557

Au Bump pitch: Refer to Pad coordinate
Au Bump height: 15µm(typ.)
Numbers in the figure refer to numbers in PAD coordinate.

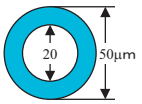
Alignment mark
(1) Arrangement: Two places
Coordinate (X, Y) = (±7294.5, -544.5)

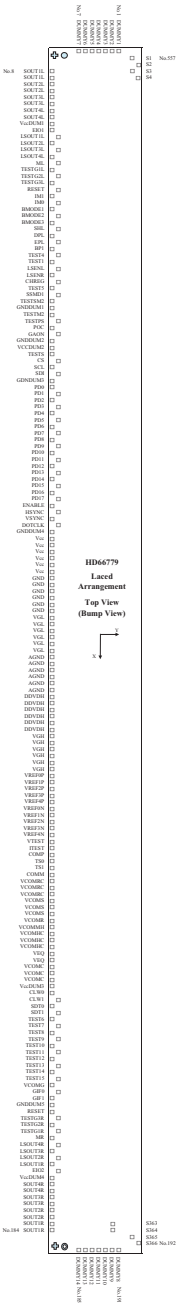


(2-a) Coordinate (X, Y) = (- 7344.5, -402.6)



(2-b) Coordinate (X, Y) = (7344.5, -402.6)





PAD Coordinate

Input, Short side

No.	pad name	X	Y
1	DUMMY1	-7355.9	304.5
2	DUMMY2	-7355.9	217.5
3	DUMMY3	-7355.9	130.5
4	DUMMY4	-7355.9	43.5
5	DUMMY5	-7355.9	-43.5
6	DUMMY6	-7355.9	-130.5
7	DUMMY7	-7355.9	-217.5
8	SOUT1L	-7006.5	-594.9
9	SOUT1L	-6920.9	-594.9
10	SOUT2L	-6835.3	-594.9
11	SOUT2L	-6749.7	-594.9
12	SOUT3L	-6664.1	-594.9
13	SOUT3L	-6578.5	-594.9
14	SOUT4L	-6492.9	-594.9
15	SOUT4L	-6407.3	-594.9
16	VCCDUM1	-6278.3	-594.9
17	EIO1	-6160.6	-594.9
18	LSOUT1L	-6101.8	-466.1
19	LSOUT2L	-6043	-594.9
20	LSOUT3L	-5984.2	-466.1
21	LSOUT4L	-5925.4	-594.9
22	ML	-5866.6	-466.1
23	TESTG1L	-5807.8	-594.9
24	TESTG2L	-5749	-466.1
25	TESTG3L	-5690.1	-594.9
26	RESET	-5631.3	-466.1
27	IM1	-5572.5	-594.9
28	IM0	-5513.7	-466.1
29	BMODE1	-5454.9	-594.9
30	BMODE2	-5396.1	-466.1
31	BMODE3	-5337.3	-594.9
32	SHL	-5278.5	-466.1
33	DPL	-5219.7	-594.9
34	EPL	-5160.8	-466.1
35	BP1	-5102	-594.9
36	TEST4	-5043.2	-466.1
37	TEST1	-4984.4	-594.9
38	LSENL	-4925.6	-466.1
39	LSENR	-4866.8	-594.9
40	CHREG	-4808	-466.1
41	TEST5	-4749.2	-594.9
42	SSMD1	-4690.3	-466.1
43	TESTSM2	-4631.5	-594.9
44	GNDDUM1	-4513.9	-594.9
45	TESTM2	-4396.3	-594.9
46	TESTPS	-4337.5	-466.1
47	POC	-4278.7	-594.9
48	GAON	-4219.8	-466.1
49	GNDDUM2	-4102.2	-594.9
50	VCCDUM2	-3984.6	-594.9
51	TESTS	-3867	-594.9
52	CS	-3808.2	-466.1
53	SCL	-3749.4	-594.9
54	SDI	-3690.5	-466.1
55	GNDDUM3	-3572.9	-594.9
56	PD0	-3455.3	-594.9
57	PD1	-3396.5	-466.1
58	PD2	-3337.7	-594.9
59	PD3	-3278.9	-466.1
60	PD4	-3220	-594.9
61	PD5	-3161.2	-466.1
62	PD6	-3102.4	-594.9
63	PD7	-3043.6	-466.1
64	PD8	-2984.8	-594.9
65	PD9	-2926	-466.1
66	PD10	-2867.2	-594.9
67	PD11	-2808.4	-466.1
68	PD12	-2749.5	-594.9
69	PD13	-2690.7	-466.1
70	PD14	-2631.9	-594.9
71	PD15	-2573.1	-466.1
72	PD16	-2514.3	-594.9
73	PD17	-2455.5	-466.1
74	ENABLE	-2396.7	-594.9
75	HSYNC	-2337.9	-466.1
76	VSYNC	-2279.1	-594.9
77	DOTCLK	-2220.2	-466.1
78	GNDDUM4	-2102.6	-594.9
79	VCC	-2001.2	-594.9
80	VCC	-1914.2	-594.9
81	VCC	-1827.2	-594.9
82	VCC	-1740.2	-594.9
83	VCC	-1653.2	-594.9
84	VCC	-1566.2	-594.9
85	GND	-1452	-594.9
86	GND	-1366.4	-594.9
87	GND	-1280.8	-594.9
88	GND	-1195.2	-594.9
89	GND	-1109.6	-594.9
90	GND	-1024	-594.9
91	VGL	-912.7	-594.9
92	VGL	-827.1	-594.9
93	VGL	-741.5	-594.9
94	VGL	-655.9	-594.9
95	VGL	-570.3	-594.9
96	VGL	-484.7	-594.9
97	AGND	-373.4	-594.9
98	AGND	-287.8	-594.9
99	AGND	-202.2	-594.9
100	AGND	-116.6	-594.9
101	AGND	-31	-594.9
102	AGND	54.6	-594.9
103	DDVDH	202.2	-594.9
104	DDVDH	287.8	-594.9
105	DDVDH	373.4	-594.9
106	DDVDH	459	-594.9
107	DDVDH	544.6	-594.9
108	DDVDH	630.2	-594.9
109	VGH	741.5	-594.9
110	VGH	828.5	-594.9
111	VGH	915.5	-594.9
112	VGH	1002.5	-594.9
113	VGH	1089.5	-594.9
114	VGH	1176.5	-594.9
115	VREF0P	1287.7	-594.9
116	VREF1P	1373.3	-594.9
117	VREF2P	1458.9	-594.9
118	VREF3P	1544.5	-594.9
119	VREF4P	1630.1	-594.9
120	VREF0N	1715.7	-594.9
121	VREF1N	1801.4	-594.9
122	VREF2N	1887	-594.9
123	VREF3N	1972.6	-594.9
124	VREF4N	2058.2	-594.9
125	VTEST	2143.8	-594.9
126	ITEST	2229.4	-594.9
127	COMP	2336.2	-594.9
128	TS0	2441.8	-594.9
129	TS1	2527.4	-594.9
130	COMM	2613	-594.9
131	VCOMRC	2739.8	-594.9
132	VCOMRC	2825.4	-594.9
133	VCOMRC	2911	-594.9
134	VCOMS	2996.6	-594.9
135	VCOMS	3082.2	-594.9
136	VCOMS	3167.8	-594.9
137	VCOMR	3294.6	-594.9
138	VCOMMH	3380.2	-594.9
139	VCOMHC	3507	-594.9
140	VCOMHC	3592.6	-594.9
141	VCOMHC	3678.2	-594.9
142	VEQ	3763.8	-594.9
143	VEQ	3849.5	-594.9
144	VCOMC	4037.2	-594.9
145	VCOMC	4122.8	-594.9
146	VCOMC	4208.4	-594.9
147	VCCDUM3	4348.8	-594.9
148	CLW0	4466.5	-594.9
149	CLW1	4525.3	-466.1
150	SDT0	4584.1	-594.9
151	SDT1	4642.9	-466.1
152	TEST6	4701.7	-594.9
153	TEST7	4760.5	-466.1
154	TEST8	4819.3	-594.9
155	TEST9	4878.1	-466.1
156	TEST10	4937	-594.9
157	TEST11	4995.8	-466.1
158	TEST12	5054.6	-594.9
159	TEST13	5113.4	-466.1
160	TEST14	5172.2	-594.9
161	TEST15	5231	-466.1
162	VCOMG	5289.8	-594.9
163	GIF0	5348.6	-466.1
164	GIF1	5407.5	-594.9
165	GNDDUM5	5525.1	-594.9
166	RESET	5642.7	-594.9
167	TESTG3R	5701.5	-466.1
168	TESTG2R	5760.3	-594.9
169	TESTG1R	5819.1	-466.1
170	MR	5878	-594.9
171	LSOUT4R	5936.8	-466.1
172	LSOUT3R	5995.6	-594.9
173	LSOUT2R	6054.4	-466.1
174	LSOUT1R	6113.2	-594.9
175	EIO2	6172	-466.1
176	VCCDUM4	6289.6	-594.9
177	SOUT4R	6407.3	-594.9
178	SOUT4R	6492.9	-594.9
179	SOUT3R	6578.5	-594.9
180	SOUT3R	6664.1	-594.9
181	SOUT2R	6749.7	-594.9
182	SOUT2R	6835.3	-594.9
183	SOUT1R	6920.9	-594.9
184	SOUT1R	7006.5	-594.9
185	DUMMY14	7355.9	-217.5
186	DUMMY13	7355.9	-130.5
187	DUMMY12	7355.9	-43.5
188	DUMMY11	7355.9	43.5
189	DUMMY10	7355.9	130.5
190	DUMMY9	7355.9	217.5
191	DUMMY8	7355.9	304.5

Laced Output Arrangement

No.	pad name	X	Y
192	S366	7300.5	609.1
193	S365	7260.5	505.5
194	S364	7220.5	609.1
195	S363	7180.5	505.5
196	S362	7140.5	609.1
197	S361	7100.5	505.5
198	S360	7060.5	609.1
199	S359	7020.5	505.5
200	S358	6980.5	609.1
201	S357	6940.5	505.5
202	S356	6900.4	609.1
203	S355	6860.4	505.5
204	S354	6820.4	609.1
205	S353	6780.4	505.5
206	S352	6740.4	609.1
207	S351	6700.4	505.5
208	S350	6660.4	609.1
209	S349	6620.4	505.5
210	S348	6580.4	609.1
211	S347	6540.4	505.5
212	S346	6500.4	609.1
213	S345	6460.4	505.5
214	S344	6420.4	609.1
215	S343	6380.4	505.5
216	S342	6340.4	609.1
217	S341	6300.4	505.5
218	S340	6260.4	609.1
219	S339	6220.4	505.5
220	S338	6180.4	609.1
221	S337	6140.4	505.5
222	S336	6100.4	609.1
223	S335	6060.4	505.5
224	S334	6020.4	609.1
225	S333	5980.4	505.5
226	S332	5940.4	609.1
227	S331	5900.4	505.5
228	S330	5860.4	609.1
229	S329	5820.4	505.5
230	S328	5780.4	609.1
231	S327	5740.4	505.5
232	S326	5700.4	609.1
233	S325	5660.4	505.5
234	S324	5620.4	609.1
235	S323	5580.4	505.5
236	S322	5540.4	609.1
237	S321	5500.4	505.5
238	S320	5460.4	609.1
239	S319	5420.4	505.5
240	S318	5380.4	609.1
241	S317	5340.3	505.5
242	S316	5300.3	609.1
243	S315	5260.3	505.5
244	S314	5220.3	609.1
245	S313	5180.3	505.5
246	S312	5140.3	609.1
247	S311	5100.3	505.5
248	S310	5060.3	609.1
249	S309	5020.3	505.5
250	S308	4980.3	609.1
251	S307	4940.3	505.5
252	S306	4900.3	609.1
253	S305	4860.3	505.5
254	S304	4820.3	609.1
255	S303	4780.3	505.5
256	S302	4740.3	609.1
257	S301	4700.3	505.5
258	S300	4660.3	609.1
259	S299	4620.3	505.5
260	S298	4580.3	609.1
261	S297	4540.3	505.5
262	S296	4500.3	609.1
263	S295	4460.3	505.5
264	S294	4420.3	609.1
265	S293	4380.3	505.5
266	S292	4340.3	609.1
267	S291	4300.3	505.5
268	S290	4260.3	609.1
269	S289	4220.3	505.5
270	S288	4180.3	609.1
271	S287	4140.3	505.5
272	S286	4100.3	609.1
273	S285	4060.3	505.5
274	S284	4020.3	609.1
275	S283	3980.3	505.5
276	S282	3940.3	609.1
277	S281	3900.3	505.5
278	S280	3860.3	609.1
279	S279	3820.2	505.5
280	S278	3780.2	609.1
281	S277	3740.2	505.5
282	S276	3700.2	609.1
283	S275	3660.2	505.5
284	S274	3620.2	609.1
285	S273	3580.2	505.5
286	S272	3540.2	609.1
287	S271	3500.2	505.5
288	S270	3460.2	609.1
289	S269	3420.2	505.5
290	S268	3380.2	609.1
291	S267	3340.2	505.5
292	S266	3300.2	609.1
293	S265	3260.2	505.5
294	S264	3220.2	609.1
295	S263	3180.2	505.5
296	S262	3140.2	609.1
297	S261	3100.2	505.5
298	S260	3060.2	609.1
299	S259	3020.2	505.5
300	S258	2980.2	609.1
301	S257	2940.2	505.5
302	S256	2900.2	609.1
303	S255	2860.2	505.5
304	S254	2820.2	609.1
305	S253	2780.2	505.5
306	S252	2740.2	609.1
307	S251	2700.2	505.5
308	S250	2660.2	609.1
309	S249	2620.2	505.5
310	S248	2580.2	609.1
311	S247	2540.2	505.5
312	S246	2500.2	609.1
313	S245	2460.2	505.5
314	S244	2420.2	609.1
315	S243	2380.2	505.5
316	S242	2340.2	609.1
317	S241	2300.2	505.5
318	S240	2260.1	609.1
319	S239	2220.1	505.5
320	S238	2180.1	609.1
321	S237	2140.1	505.5
322	S236	2100.1	609.1
323	S235	2060.1	505.5
324	S234	2020.1	609.1
325	S233	1980.1	505.5
326	S232	1940.1	609.1
327	S231	1900.1	505.5
328	S230	1860.1	609.1
329	S229	1820.1	505.5
330	S228	1780.1	609.1
331	S227	1740.1	505.5
332	S226	1700.1	609.1
333	S225	1660.1	505.5
334	S224	1620.1	609.1
335	S223	1580.1	505.5
336	S222	1540.1	609.1
337	S221	1500.1	505.5
338	S220	1460.1	609.1
339	S219	1420.1	505.5
340	S218	1380.1	609.1
341	S217	1340.1	505.5
342	S216	1300.1	609.1
343	S215	1260.1	505.5
344	S214	1220.1	609.1
345	S213	1180.1	505.5
346	S212	1140.1	609.1
347	S211	1100.1	505.5
348	S210	1060.1	609.1
349	S209	1020.1	505.5
350	S208	980.1	609.1
351	S207	940.1	505.5
352	S206	900.1	609.1
353	S205	860.1	505.5
354	S204	820.1	609.1
355	S203	780.1	505.5
356	S202	740	609.1
357	S201	700	505.5
358	S200	-660	609.1
359	S199	620	505.5
360	S198	580	609.1
361	S197	540	505.5
362	S196	500	609.1
363	S195	460	505.5
364	S194	420	609.1
365	S193	380	505.5
366	S192	340	609.1
367	S191	300	505.5
368	S190	260	609.1
369	S189	220	505.5
370	S188	180	609.1
371	S187	140	505.5
372	S186	100	609.1
373	S185	60	505.5
374	S184	20	609.1
375	S183	-20	505.5
376	S182	-60	609.1
377	S181	-100	505.5
378	S180	-140	609.1
379	S179	-180	505.5
380	S178	-220	609.1
381	S177	-260	505.5
382	S176	-300	609.1
383	S175	-340	505.5
384	S174	-380	609.1
385	S173	-420	505.5
386	S172	-460	609.1
387	S171	-500	505.5
388	S170	-540	609.1
389	S169	-580	505.5
390	S168	-620	609.1
391	S167	-660	505.5
392	S166	-700	609.1
393	S165	-740	505.5
394	S164	-780.1	609.1
395	S163	-820.1	505.5
396	S162	-860.1	609.1
397	S161	-900.1	505.5
398	S160	-940.1	609.1
399	S159	-980.1	505.5
400	S158	-1020.1	609.1
401	S157	-1060.1	505.5
402	S156	-1100.1	609.1
403	S155	-1140.1	505.5
404	S154	-1180.1	609.1
405	S153	-1220.1	505.5
406	S152	-1260.1	609.1
407	S151	-1300.1	505.5
408	S150	-1340.1	609.1
409	S149	-1380.1	505.5
410	S148	-1420.1	609.1
411	S147	-1460.1	505.5
412	S146	-1500.1	609.1
413	S145	-1540.1	505.5
414	S144	-1580.1	609.1
415	S143	-1620.1	505.5
416	S142	-1660.1	609.1
417	S141	-1700.1	505.5
418	S140	-1740.1	609.1
419	S139	-1780.1	505.5
420	S138	-1820.1	609.1
421	S137	-1860.1	505.5
422	S136	-1900.1	609.1
423	S135	-1940.1	505.5
424	S134	-1980.1	609.1
425	S133	-2020.1	505.5
426	S132	-2060.1	609.1
427	S131	-2100.1	505.5
428	S130	-2140.1	609.1
429	S129	-2180.1	505.5
430	S128	-2220.1	609.1
431	S127	-2260.1	505.5
432	S126	-2300.1	609.1
433	S125	-2340.2	505.5
434	S124	-2380.2	609.1
435	S123	-2420.2	505.5
436	S122	-2460.2	609.1
437	S121	-2500.2	505.5
438	S120	-2540.2	609.1
439	S119	-2580.2	505.5
440	S118	-2620.2	609.1
441	S117	-2660.2	505.5
442	S116	-2700.2	609.1
443	S115	-2740.2	505.5
444	S114	-2780.2	609.1
445	S113	-2820.2	505.5
446	S112	-2860.2	609.1
447	S111	-2900.2	505.5
448	S110	-2940.2	609.1
449	S109	-2980.2	505.5
450	S108	-3020.2	609.1
451	S107	-3060.2	505.5
452	S106	-3100.2	609.1
453	S105	-3140.2	505.5
454	S104	-3180.2	609.1
455	S103	-3220.2	505.5
456	S102	-3260.2	609.1
457	S101	-3300.2	505.5
458	S100	-3340.2	609.1
459	S99	-3380.2	505.5
460	S98	-3420.2	609.1
461	S97	-3460.2	505.5
462	S96	-3500.2	609.1
463	S95	-3540.2	505.5
464	S94	-3580.2	609.1
465	S93	-3620.2	505.5
466	S92	-3660.2	609.1
467	S91	-3700.2	505.5
468	S90	-3740.2	609.1
469	S89	-3780.2	505.5
470	S88	-3820.2	609.1
471	S87	-3860.3	505.5
472	S86	-3900.3	609.1
473	S85	-3940.3	505.5
474	S84	-3980.3	609.1
475	S83	-4020.3	505.5
476	S82	-4060.3	609.1
477	S81	-4100.3	505.5
478	S80	-4140.3	609.1
479	S79	-4180.3	505.5
480	S78	-4220.3	609.1
481	S77	-4260.3	505.5
482	S76	-4300.3	609.1
483	S75	-4340.3	505.5
484	S74	-4380.3	609.1
485	S73	-4420.3	505.5
486	S72	-4460.3	609.1
487	S71	-4500.3	505.5
488	S70	-4540.3	609.1
489	S69	-4580.3	505.5
490	S68	-4620.3	609.1
491	S67	-4660.3	505.5
492	S66	-4700.3	609.1
493	S65	-4740.3	505.5
494	S64	-4780.3	609.1
495	S63	-4820.3	505.5
496	S62	-4860.3	609.1
497	S61	-4900.3	505.5
498	S60	-4940.3	609.1
499	S59	-4980.3	505.5
500	S58	-5020.3	609.1
501	S57	-5060.3	505.5
502	S56	-5100.3	609.1
503	S55	-5140.3	505.5
504	S54	-5180.3	609.1
505	S53	-5220.3	505.5
506	S52	-5260.3	609.1
507	S51	-5300.3	505.5
508	S50	-5340.3	609.1
509	S49	-5380.3	505.5
510	S48	-5420.4	609.1
511	S47	-5460.4	505.5
512	S46	-5500.4	609.1
513	S45	-5540.4	505.5
514	S44	-5580.4	609.1
515	S43	-5620.4	505.5
516	S42	-5660.4	609.1
517	S41	-5700.4	505.5
518	S40	-5740.4	609.1
519	S39	-5780.4	505.5
520	S38	-5820.4	609.1
521	S37	-5860.4	505.5
522	S36	-5900.4	609.1
523	S35	-5940.4	505.5
524	S34	-5980.4	609.1
525	S33	-6020.4	505.5
526	S32	-6060.4	609.1
527	S31	-6100.4	505.5
528	S30	-6140.4	609.1
529	S29	-6180.4	505.5
530	S28	-6220.4	609.1
531	S27	-6260.4	505.5
532	S26	-6300.4	609.1
533	S25	-6340.4	505.5
534	S24	-6380.4	609.1
535	S23	-6420.4	505.5
536	S22	-6460.4	609.1
537	S21	-6500.4	505.5
538	S20	-6540.4	609.1
539	S19	-6580.4	505.5
540	S18	-6620.4	609.1
541	S17	-6660.4	505.5
542	S16	-6700.4	609.1
543	S15	-6740.4	505.5
544	S14	-6780.4	609.1
545	S13	-6820.4	505.5
546	S12	-6860.4	609.1
547	S11	-6900.4	505.5
548	S10	-6940.5	609.1
549	S9	-6980.5	505.5
550	S8	-7020.5	609.1
551	S7	-7060.5	505.5
552	S6	-7100.5	609.1
553	S5	-7140.5	505.5
554	S4	-7180.5	609.1
555	S3	-7220.5	505.5
556	S2	-7260.5	609.1
557	S1	-7300.5	505.5

Instruction

The HD66779 incorporates interface with microcomputer, which enables instruction setting to realize high-quality display and low power consumption. With regard to settings and timing of interface, see "Serial Peripheral Interface (SPI) Function".

The instruction setting can not be made in DE transfer mode.

Index: IR

	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
Instruction	0	0	0	0	0	0	0	0	0	0	0	0	0	ID2	ID1	ID0
Initialized value	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Specifies an index registor to be accessed. Do not try to access to the register to which instruction is not assigned.

Power save, Color control: R01h

	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
Instruction	0	0	0	0	0	0	POC	1	0	0	0	0	0	0	0	0
Initialized value	-	-	-	-	-	-	0	-	-	-	-	-	-	-	-	-

POC: Power control function.

POC = "1": Normal operation mode. Both input/output interfaces are operable.
POC = "0": Power control mode. White display is shown for the entire screen.

Note 1) When "CHREG" = "H", "POC" of instruction register R01 become valid.
Note 2) See "Power Control Function" for details.
Note 3) The setting becomes effective in the next VSYNC assert timing.

Border color control (1): R02h

	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
Instruction	0	0	0	0	0	0	0	0	0	0	BCOL17	BCOL16	BCOL15	BCOL14	BCOL13	BCOL12
Initialized value	-	-	-	-	-	-	-	-	-	-	1	1	1	1	1	1

Border color control (2): R03h

	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
Instruction	0	0	BCOL11	BCOL10	BCOL9	BCOL8	BCOL7	BCOL6	0	0	BCOL5	BCOL4	BCOL3	BCOL2	BCOL1	BCOL0
Initialized value	-	-	1	1	1	1	1	1	-	-	1	1	1	1	1	1

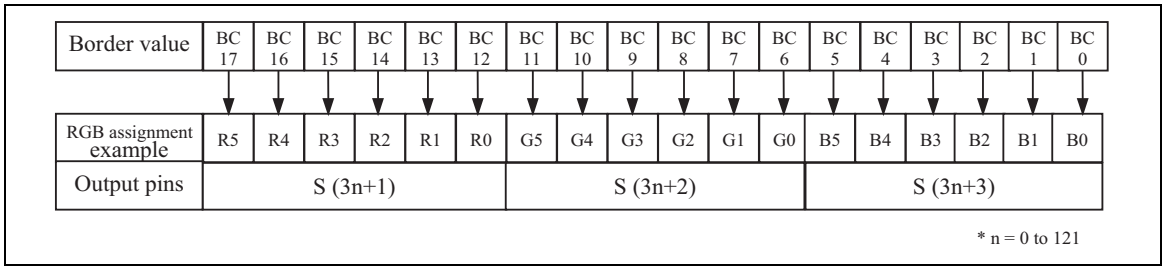
BCOL17-0: Set value for the border color.

The assignment of the value to each register is as follows.

BCOL17-12: S (3n+1)
BCOL11-6: S (3n+2)
BCOL5-0: S (3n+3)

Note 1) The border pin assignment changes according to the setting for the border color control.
BMODE2 = “H”: n = 0 to 1
BMODE2 = “L”: n = 120 to 121
Note 2) Vertical border area is made by 2 raster-rows each at the top and bottom of the screen.
Note 3) Horizontal border area is made by 6 channels (two RGBs) each at the left and right sides of the screen.
Note 4) The settings for the border control must be made during non-display period.
Note 5) The setting becomes effictive from the next VSYNC assert timing.
Note 6) The setting is invalid while the border function is not used.
Note 7) The border color control functon is valid only in RGBI/F mode.

The set values are assigned as follows.



LCD driving waveform control, Source output control: R04h

	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
Instruction	0	0	0	0	0	0	NW1	NW0	0	0	0	0	RB3	RB2	RB1	RB0
Initialized value	-	-	-	-	-	-	0	1	-	-	-	-	1	0	0	0

NW2-0: Selects AC timing.

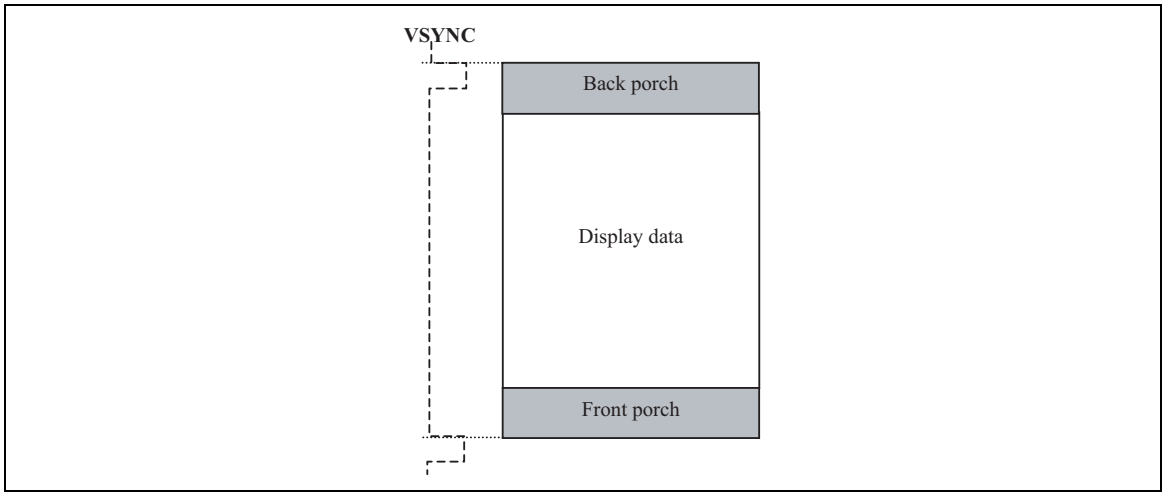
NW1	NW0	Alternating timing
0	0	Frame inversion
0	1	Inversion by line
1	0	Inversion by 2 lines
1	1	Setting disabled

Note 1) For details, see “LCD AC drive”.
Note 2) The setting becomes effective from the next VSYNC assert timing.

BP3-0: Set the blank period (back porch) in the following figure. BP3-0 set the number of raster-rows for the back porch. The number of raster-rows for the back porch should be:

14 raster-rows ≥ the number of raster-rows for the back porch – the number of raster-rows for the border ≥ 2 raster-rows

Note 1) When “CHREG” = “H”, instruction registers “BP3”, “BP2”, “BP1”, “BP0” become valid.
When “CHREG” = “L”, “BP” pin function becomes valid.
(“BP”= 0: back porch 4 lines, “BP”=1: back porch 8 lines)
Note 2) A front porch lasts from the end of the display pixel transfer to the next VSYNC assert.
Note 3) The setting becomes effective from the next assert timing.



BP3	BP2	BP1	BP0	Back porch line
0	0	0	0	Setting disabled
0	0	0	1	Setting disabled
0	0	1	0	Two lines
0	0	1	1	Three lines
0	1	0	0	Four lines
1	1	0	0	12 lines
1	1	0	1	13 lines
1	1	1	0	14 lines
1	1	1	1	Setting disabled

Gate Non Overlap Control, Border Color Control: R05h

	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
Instruction	0	0	0	DTE	0	0	NO1	NO0	0	0	0	0	0	0	0	GAON
Initialized value	-	-	-	1	-	-	0	0	-	-	-	-	-	-	-	0

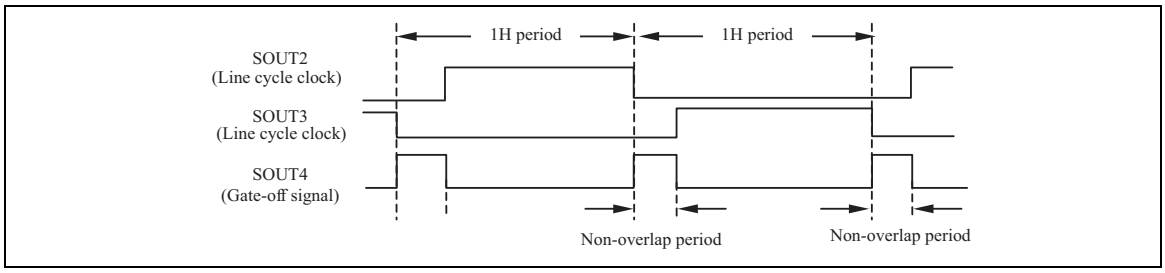
DTE : Output gate off signal.
"DTE" = "0": Fix to GND.
"DTE" = "1": Output gate off signal.

The setting becomes effective from the next VSYNC assert timing.

NO1-0: Set the non-overlap period of gate off signal.

NO1	NO0	Amount of non-overlap	
		Delay time	5MHz (e.g.)
0	0	0μs	0 clock
0	1	4.0μs	20 clocks
1	0	6.0μs	30 clocks
1	1	8.0μs	40 clocks

Note) The delay time changes according to the DOTCLK frequency.



Note) When the setting is made with pins, the non-overlap amount of gate off signal equals to that set with CLW1-0.

GAON: Output gate-all-on signal.
GAON = "0": Gate output signal L/SOUT4 = "0"
GAON = "1": Gate ouput signal L/SOUT4 = "1"

Note 1) When "CHREG" = "H", "GAON" of instruction register R05 becomes valid.
Note 2) With regard to the selection of output pin, see "LCD display signal control".
Note 3) The setting becomes effective from the next VSYNC assert timing.

Display Signal Select Control, Flame Control 1: R06h

	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
Instruction	0	0	DSC 1	DSC 0	0	0	GIF1	GIF0	FHN	0	FTH 1	FTH 0	0	0	FWH 1	FWH 0
Initialized value	-	-	0	1	-	-	0	0	1	-	1	0	-	-	1	1

DSC1-0: Controls start/halt of LCD signals.

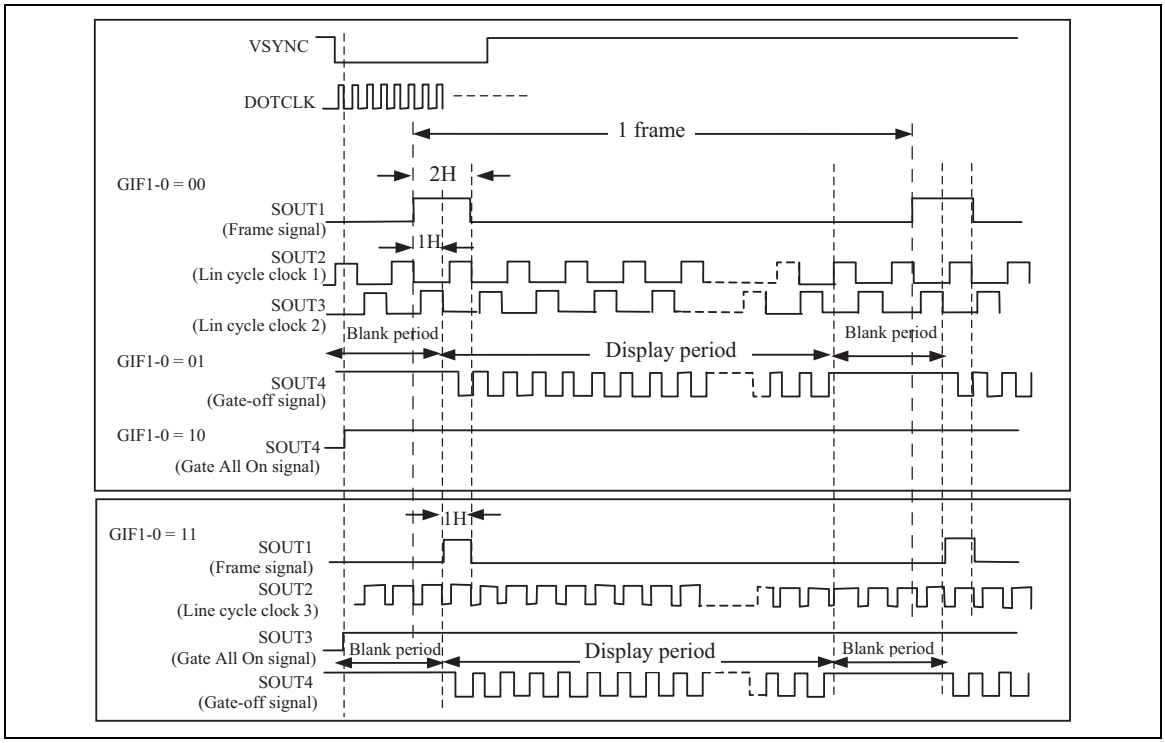
DSC1	DSC0	Selective signal for LCD display
0	0	Halt LCD display signal
0	1	SOUT1/2/3/4
1	0	LSOUT 1/2/3/4
1	1	L/SOUT1/2/3/4

Note 1) SOUT1/2/3/4 is a level shifter output (voltage between VGH and VGL), and LSOUT1/2/3/4 is a logic output (voltage between Vcc and GND).
Note 2) The setting becoms effective from the next VSYNC assert timing.

GIF1-0: Select the function of LCD display signal.

GIF1	GIF0	L/SOUT2	L/SOUT3	L/SOUT4
0	0	Line frequency clock 1	Line frequency clock 2	Disconnect pins
0	1	Line frequency clock 1	Line frequency clock 2	Gete off signal
1	0	Line frequency clock 1	Line frequency clock 2	Gate All On
1	1	Line frequency clock 3	Gate All On	Gate off signal

Note 1) When “CHREG” = “H”, “GIF1” and “GIF0” of instruction registers R06 become effective.
Note 2) The setting becoms effective from the next VSYNC assert timing.
Note 3) When “GIF1-0” = 11, “FHN” = “0”(1H assert).



GIF1-0: timing chart

FHN: Set the assert period of SOUT1 signal (frame timing signal) during horizontal period.
FHN = "0": the assert available for 1H period.
FHN = "1": the assert available for 2H period.

The setting becomes effective from the next VSYNC assert timing. The assert period is 2H in DE transfer mode (1H, when GIF1-0 = "11").

FTI1-0: Set the assert timing of SOUT1 signal (frame timing signal) during horizontal period.

FTI1	FTI0	Assert timing	
		Delay time	5MHz (e.g.)
0	0	0μs	0 clock
0	1	1.5μs	7.5 clocks
1	0	3.5μs	17.5 clocks
1	1	7.5μs	37.5 clocks

Note) The delay time cahges according to the DOTCLK frequency.

The setting becomes effective from the next VSYNC assert timing.

FWI1-0: Set the pulse width of SOUT1 signal (frame timing signal) during "High".

FWI1	FWI0	"High" period	
		Delay time	5MHz (Ex.)
0	0	2μs	10 clocks
0	1	8μs	40 clocks
1	0	16μs	80 clocks
1	1	Until the end of 1H period	—

The setting becomes effective from the next VSYNC assert timing.

Instruction List

		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
	index	0	0	0	0	0	0	0	0	0	0	0	0	0	ID2	ID1	ID0
R01h	Power control Color control	0	0	0	0	0	0	*POC 0	1	0	0	0	0	0	0	0	0
R02h	Border color control (1)	0	0	0	0	0	0	0	0	0	0	BCOL17 1	BCOL16 1	BCOL15 1	BCOL14 1	BCOL13 1	BCOL12 1
R03h	Border color control (2)	0	0	BCOL11 1	BCOL10 1	BCOL9 1	BCOL8 1	BCOL7 1	BCOL6 1	0	0	BCOL5 1	BCOL4 1	BCOL3 1	BCOL2 1	BCOL1 1	BCOL0 1
R04h	LCD drive AC control, Display control	0	0	0	0	0	0	NW1 0	NW0 1	0	0	0	0	*BP3 1	*BP2 0	*BP1 0	*BP0 0
R05h	Gate output non-overlap control, All gate ON control	0	0	0	DTE 1	0	0	NO1 0	NO0 1	0	0	0	0	0	0	0	*GAON 0
R06h	Signal select control for LCD display, FLM control	0	0	DSC1 0	DSC0 1	0	0	*GIF1 0	*GIF0 0	FHN 1	0	FTI1 1	FTI0 0	0	0	FWI1 1	FWI0 1

Note 1) The initialized value is shown at the bottom of each instruction bit cell.

Note 2) Do not try to access to the register where instruction setting is disabled.

Note 3) The setting in the instruction bit with "*" conflicts with the pin setting. When the pin "CHREG" is set to "H", the setting of the instruction bit takes precedence over the pin setting.

Note 4) In the DE transfer mode, the setting of the bit without "*" is not changeable and initialized value is retained.

Reset Function

The HD66779 is internally initialized with the input of RESET. During reset period, the intenal state of the HD66779 is busy and no external access is accepted. With the reset input to the HD66779, the settings for the gate-driver/power supply IC are not automatically initialized and separate resetting is required for the gate-driver/power supply IC. The reset input period must be held for 1 ms at least. Do not transfer initialized instruction sets or data during the power-on reset when power is turned on.

1. Initial state of instruction set : See description for each instruction

2. Initial level of output pin :

LCD display output:	SOUT1-4R/L	Output “VGL” level.
	LSOUT1-4R/L	Output “GND”level.
AC drive amplitude signal	VCOMS	Output “GND” level.

LCD Signal Output Timing Control Function

Adjust output timing of LCD display signal with external pins.

CLW0/1: Set output position of line cycle clock for display.

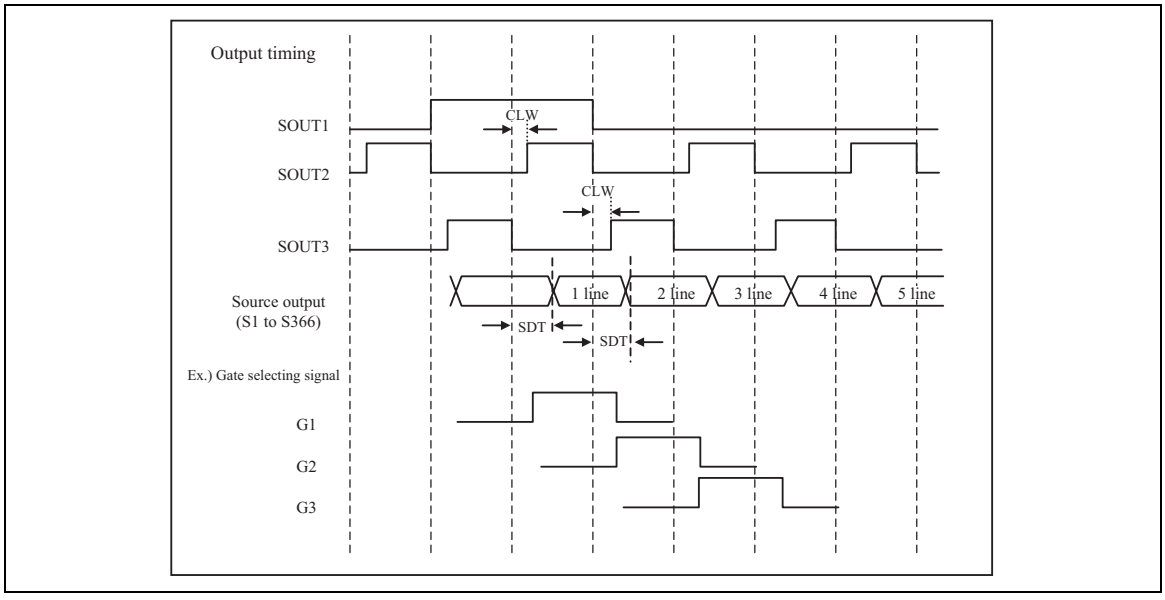
CLW1	CLW0	Delay amount	
		Delay time	5MHz (e.g.)
L	L	0 μS	0 clock
L	H	2.0 μS	10 clocks
H	L	4.0 μS	20 clocks
H	H	6.0 μS	30 clocks

Note) The delay time changes according to the DOTCLK frequency.

SDT0/1: Set output position of source output.

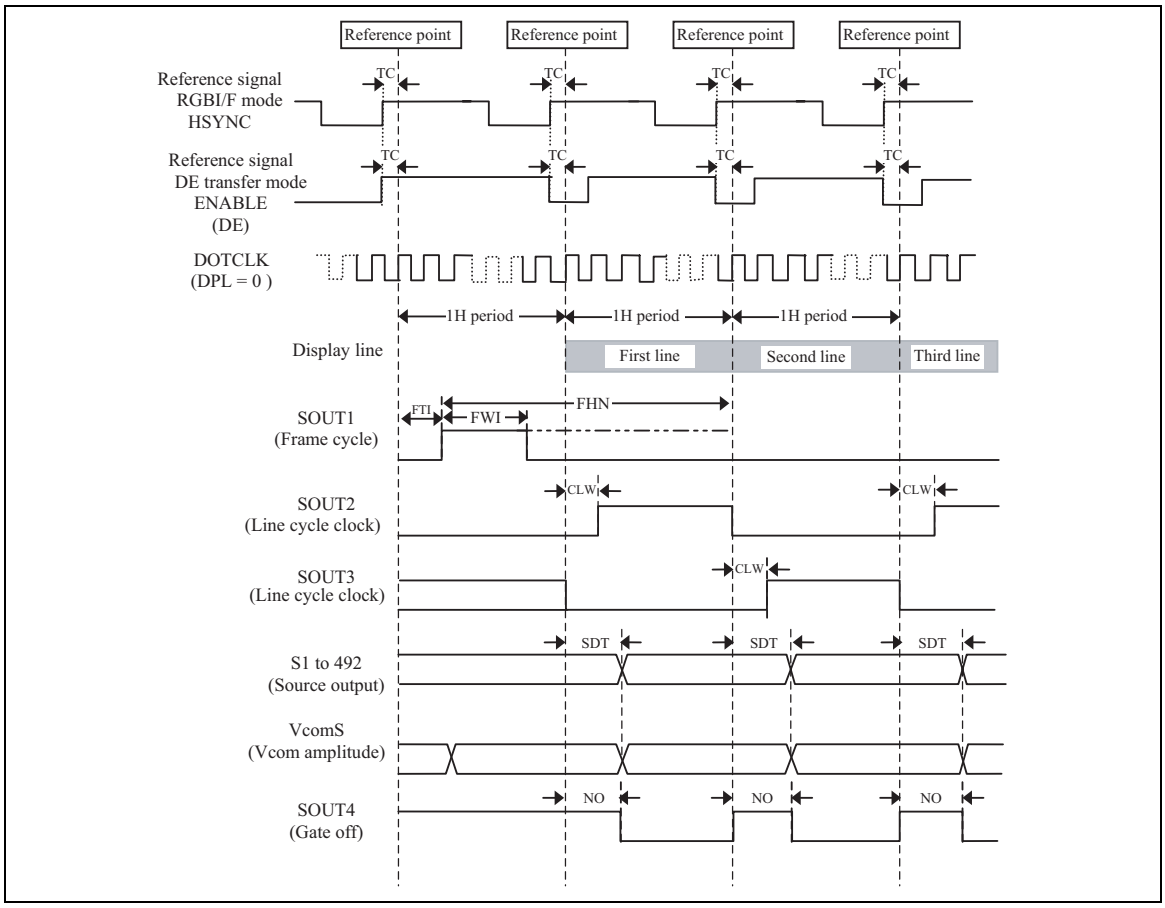
SDT1	SDT0	Delay amount	
		Delay time	5MHz (e.g.)
L	L	2 μS	10 clocks
L	H	3.0 μS	15 clocks
H	L	4.0 μS	20 clocks
H	H	5.0 μS	25 clocks

Note) The delay time changes according to the DOTCLK frequency.



LCD Signal Timing Control Function

The timing chart of control signals is illustrated as follows.



Note 1) There are some constraints when the pin setting is effective.

- L/SOUT1 (Frame) signal is FHN = “1” (2H assert)
- When FTI1-0 = “10” (DE transfer mode: FTI1-0 = “00”), FWI1-0 = “11”.
- The non-overlap amount of L/SOUT4 (gate-off signal) equals to that set by CLW1-0.

Note 2) There are some constraints when GIF1-0 = “11”.

- FHN = “0” (1H assert) irrespective of the pin setting and SPI setting (FHN = “1”).
- When the pin setting is effective, FTI1-0 = “00”, FWI1-0 = “11”.

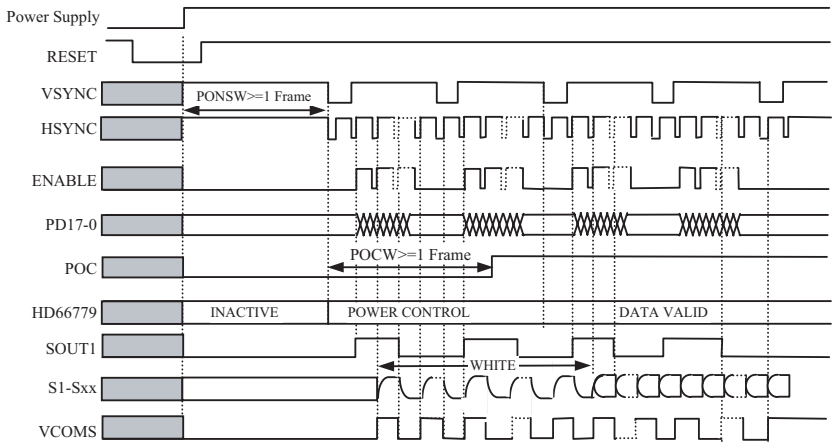
Power Control Function

Power control function (POC)

When POC = “L”, a white display is shown.

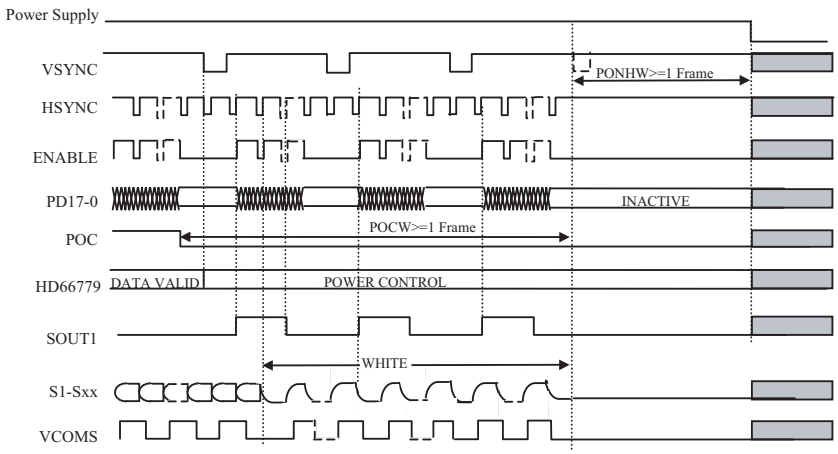
Note 1) The panel display signal (SOUT*) is output normally.
Note 2) The set value of POC changes with VSYNC and the source output becomes effective from the next timing.

Power Supply On Sequence (Example of Usage)



PONSW: the period from power supply on to the start of H/V synchronizing signal assert
POCW: Power on control period

Power Supply Off Sequence (Example of Usage)



PONSW: the period from the end of H/V synchronizing signal to power supply off
POCW: Power on control period

POC / VCOMG / LSENR/L output control

The relationship among these signals is as follows.

Source output (Sn) and Vcom output (VCOMS) control by POC

Input	Output		
POC	Operation mode	Source output (Sn)	Vcom output
0	Power control mode	WHITE	VCOMS
1	Normal operation mode	Input data or Border data	VCOMS

Panel display signal (SOUT*/LSOUT*) control by LSENL/LSENR

Input		Output			
		VGH-VGL		Vcc-GND	
LSENL	**LSENR**	**SOUT1/2/3/4L**	**SOUT1/2/3/4R**	**LSOUT1/2/3/4L**	**LSOUT1/2/3/4R**
0	0	VGL	VGL	Vcc – GND	Vcc - GND
0	1	VGL	VGH – VGL		
1	0	VGH – VGL	VGL		
1	1	VGH – VGL	VGH – VGL		

VCOM (VCOMS) control by VCOMG

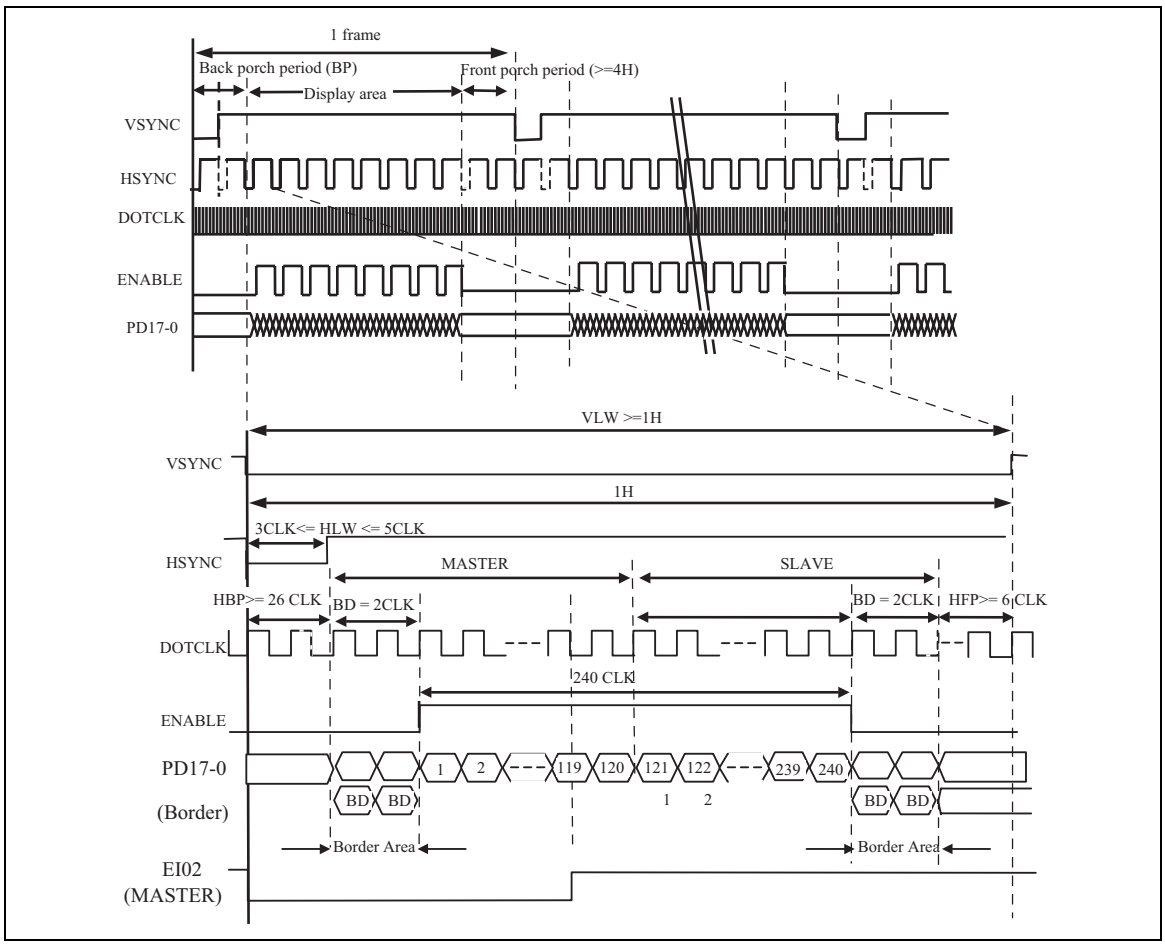
Input	Output
VCOMG	VCOMS
0	GND
1	VCOMS

Interface

RGB interface timing 1 (366ch x 2 / With Border)

The timing chart of RGB interface signal is as follows.

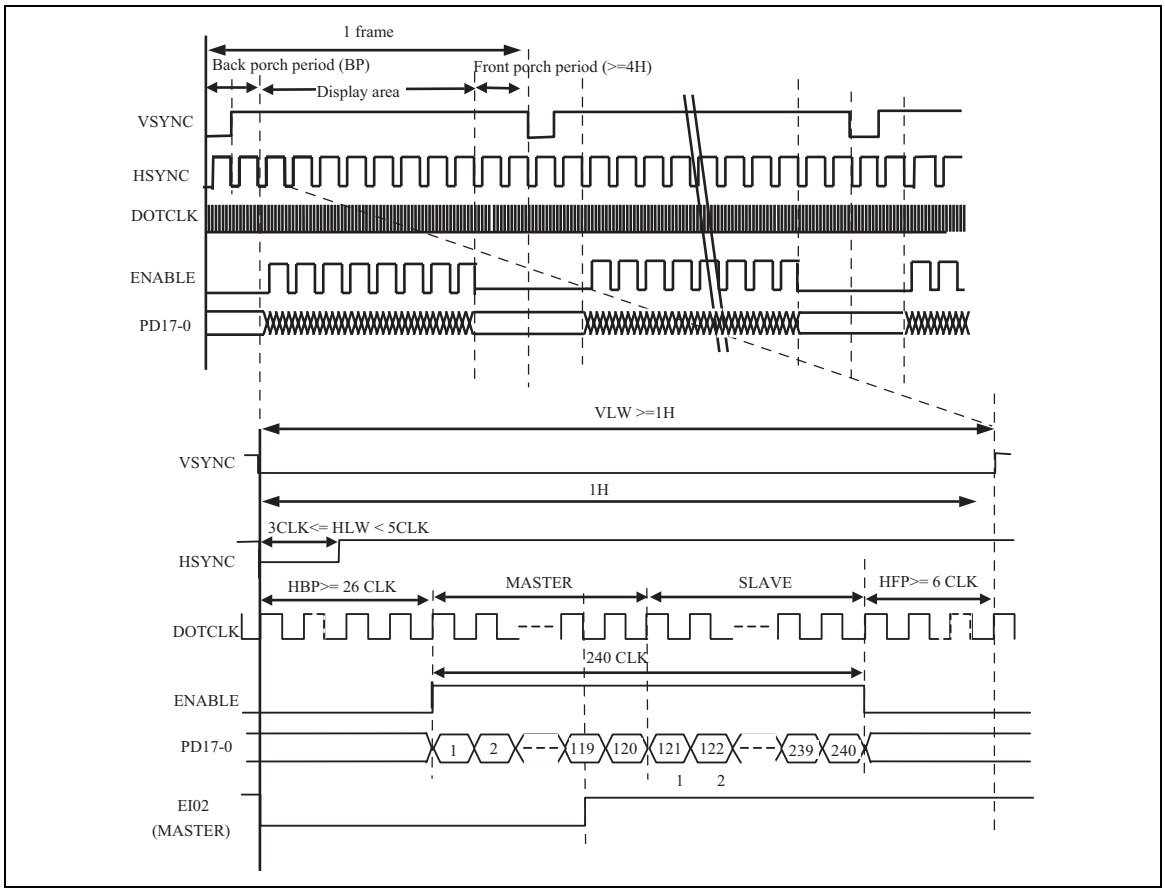
The value for the border is the one received through SPI.



VLW: VSYNC “Low” period
HLW: HSYNC “ Low” period
HBP: Horizontal period back porch
HFP: Horizontal period front porch
BD: Border Area

RGB interface timing 2 (360ch x 2 / Without Border)

The timing chart of signals in RGB interface is as follows.

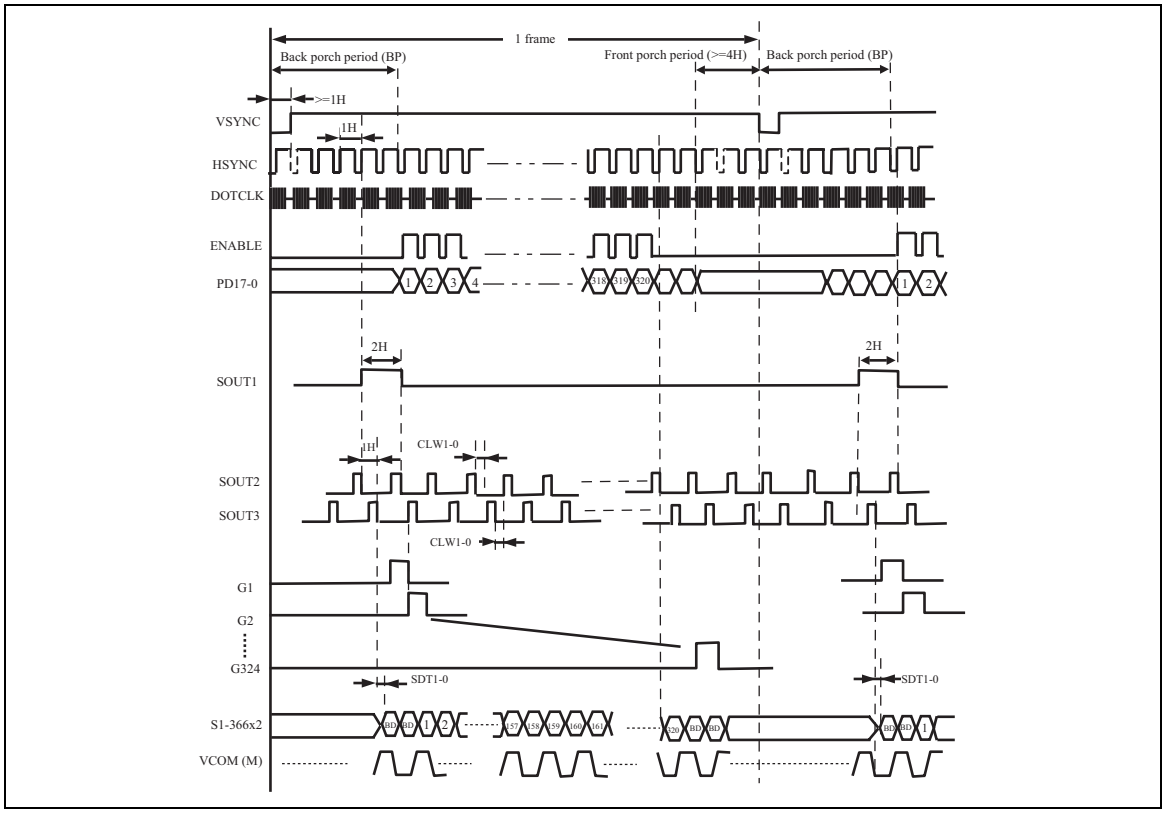


VLW: VSYNC “Low” period
HLW: HSYNC “ Low” period
HBP: Horizontal period back porch
HFP: Horizontal period front porch

LCD panel interface timing 1 (366ch x 2 / With Border)

The timing chart of RGB interface signal is as follows.

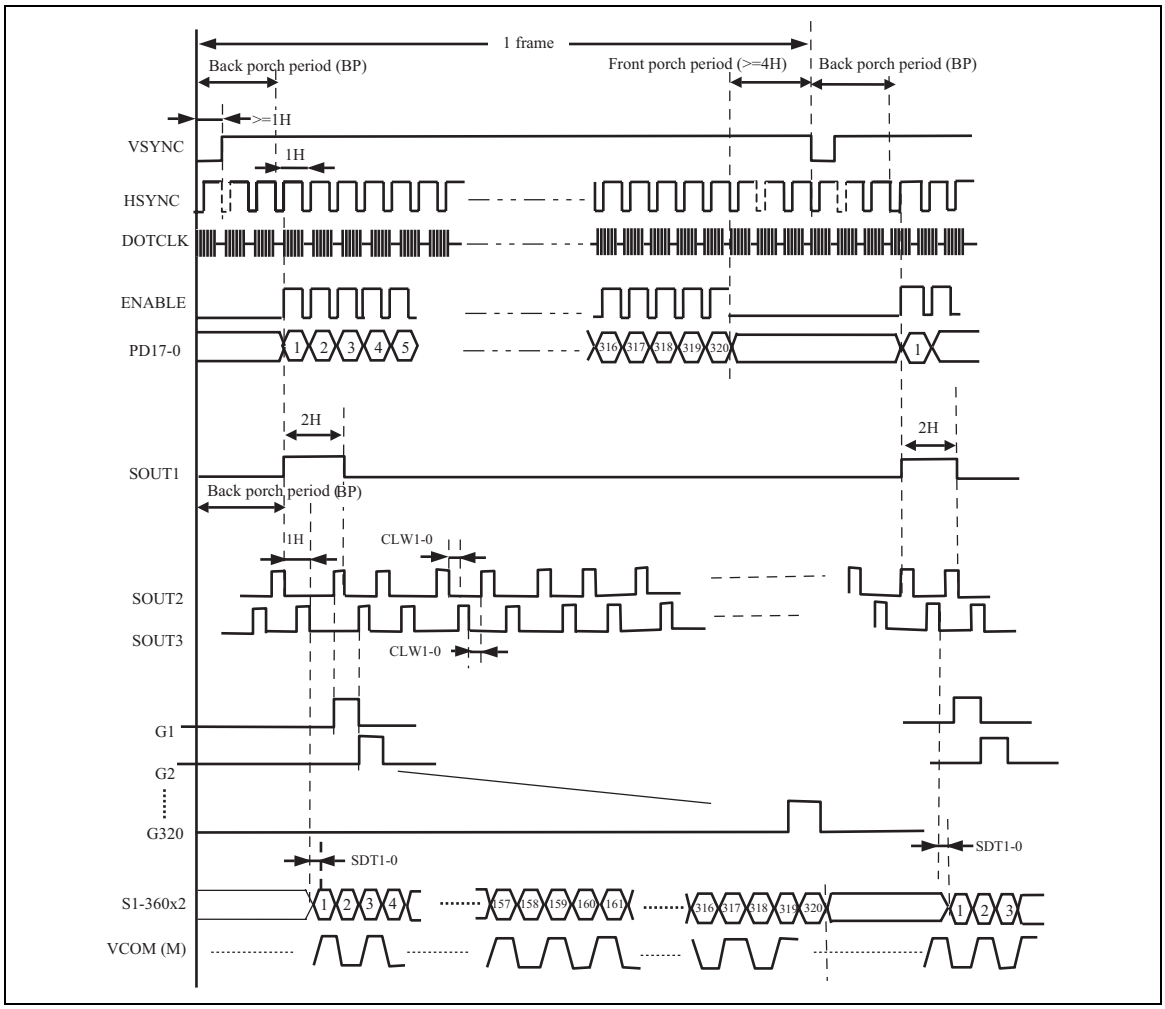
The value for the border is the one received through SPI.



Note) See “LCD Signal Timing Control Function” for details of setting the timing.

LCD panel interface timing 2 (366ch x 2 / Without Border)

The timing chart of RGB interface signal and LCD panel signal is as follows.

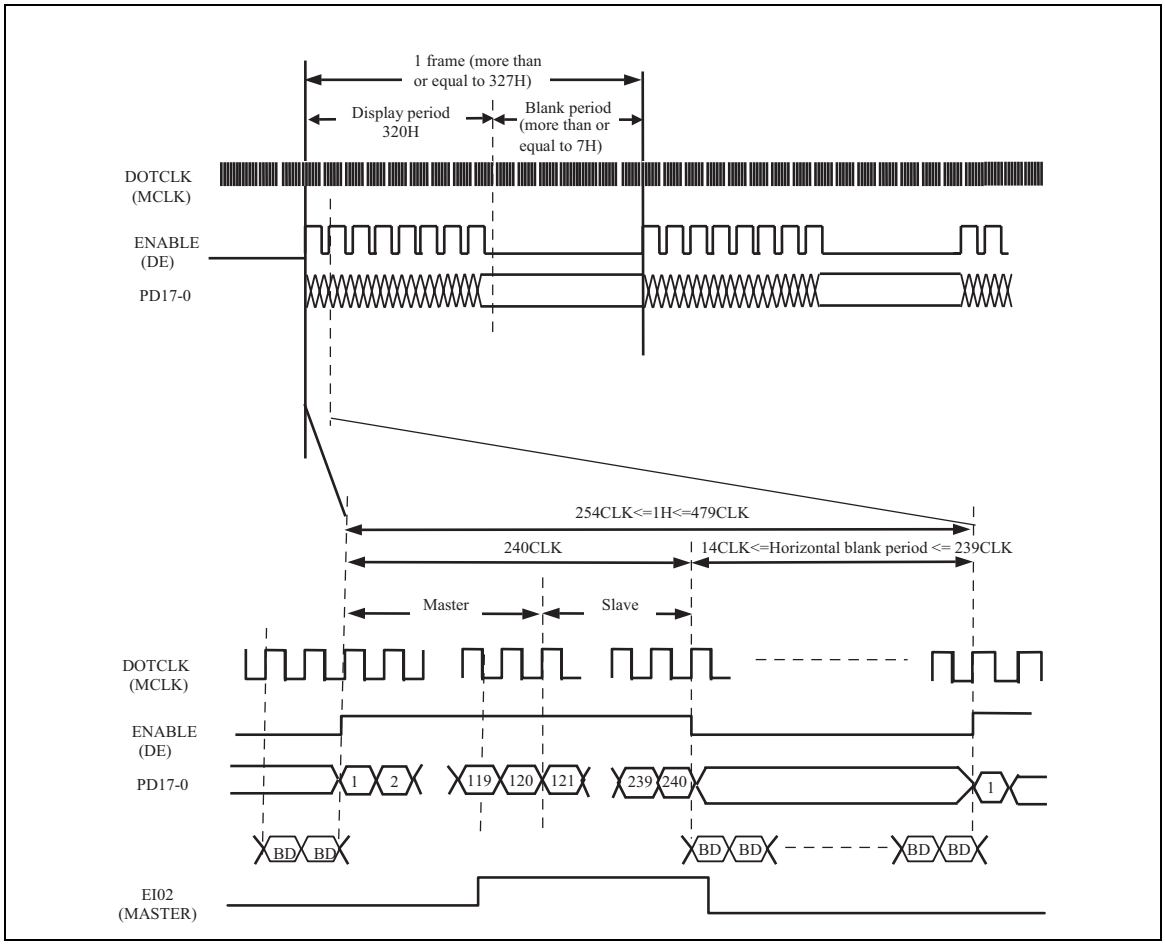


Note) See “LCD Signal Timing Control Function” for details of setting the timing.

DE transfer mode 1 (366ch x 2 / With Border)

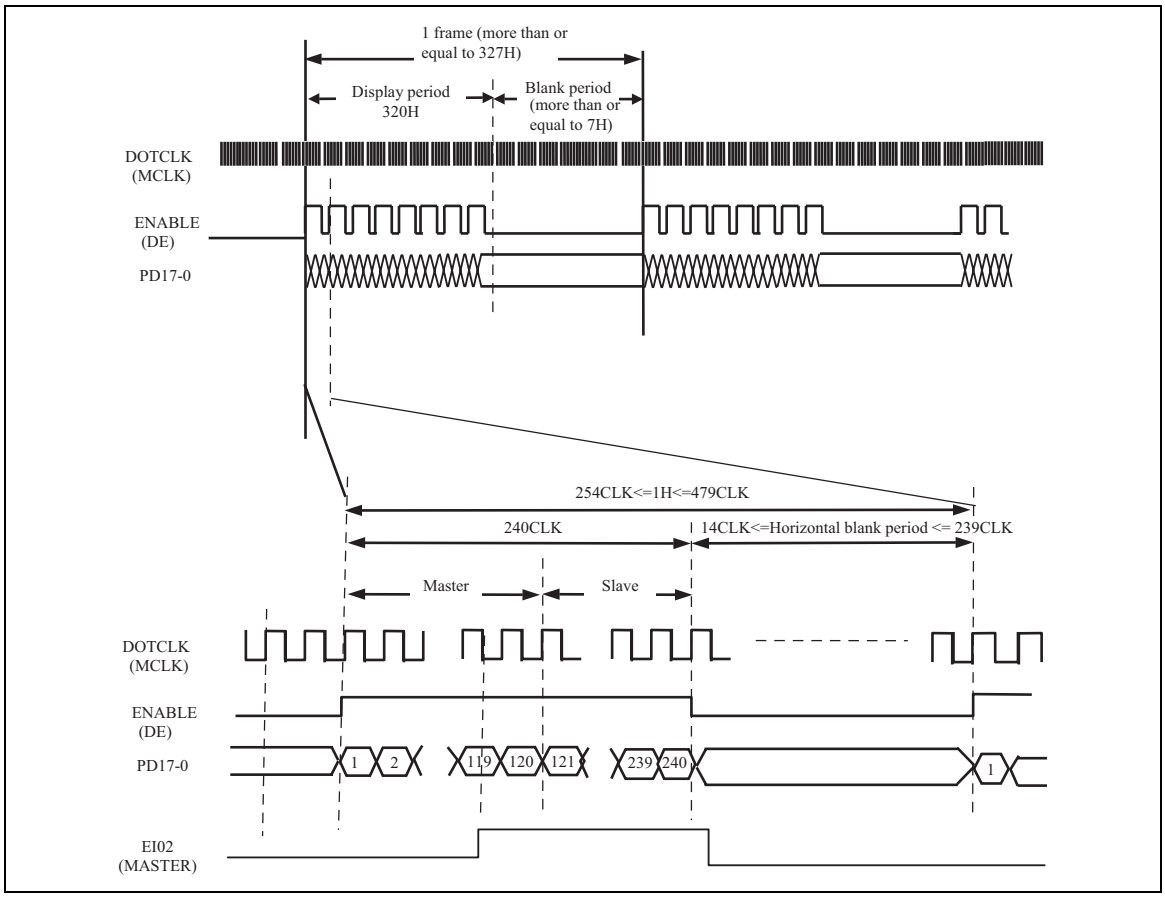
The timing chart of DE transfer mode signal is as follows.

The border color in DE transfer mode is either black or white to be switchted with BMODE3 pin.



DE transfer mode 2 (366ch x 2 / Without Border)

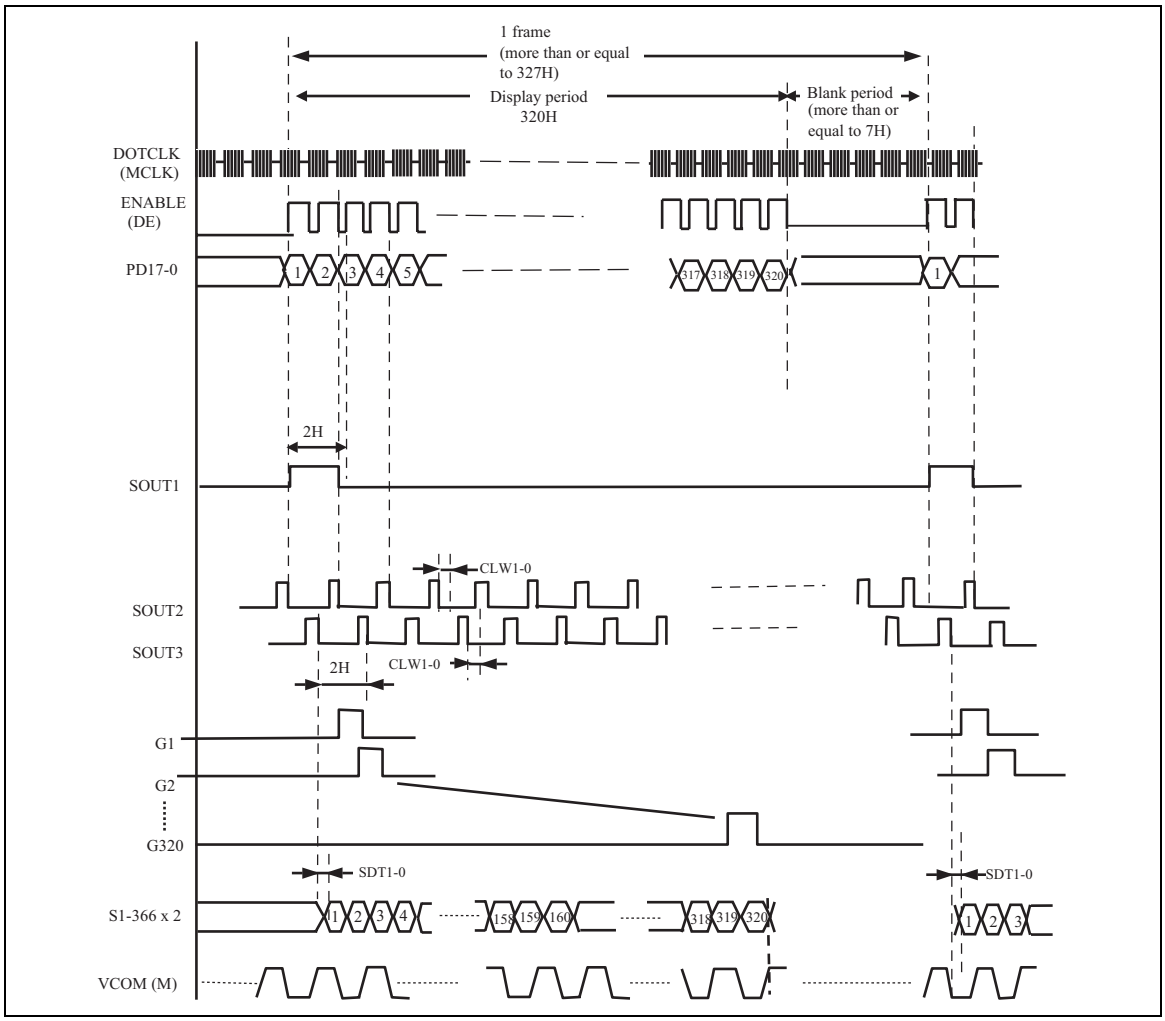
The timing chart of DE transfer mode signal is as follows.



LCD panel interface timing while DE transfer mode 1 (With Border)

The relationship between the DE transfer mode signal and the LCD panel signal is as follows.

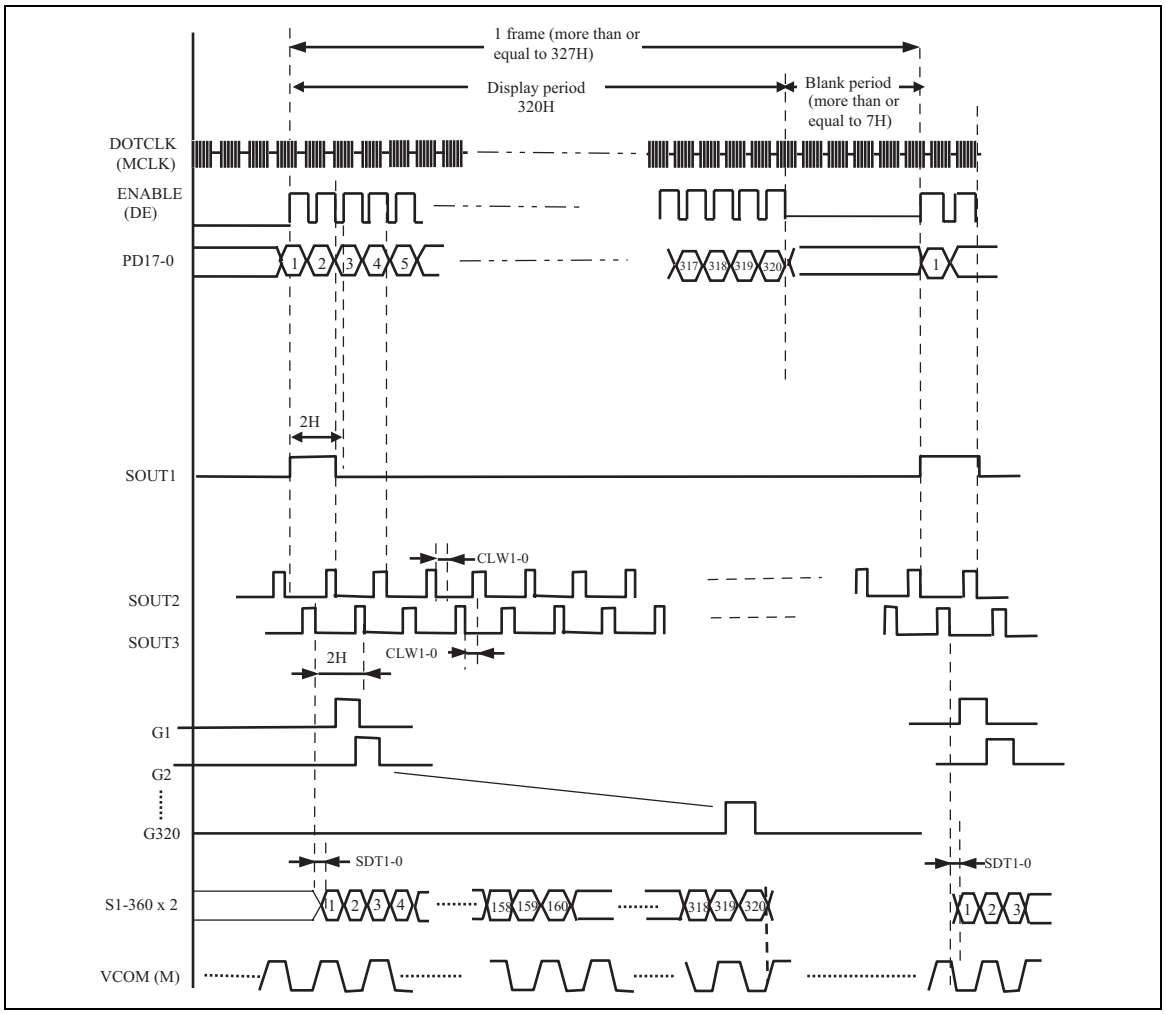
Note 1) The border color control while using DE transfer mode is on the 6 channels each at left and right side.
Note 2) The border color in DE transfer mode is only black and white to be switched with BMODE3 pin.



Note) See “LCD Signal Timing Control Function” for details of setting the timing.

LCD panel interface timing while DE transfer mode 2 (Without Border)

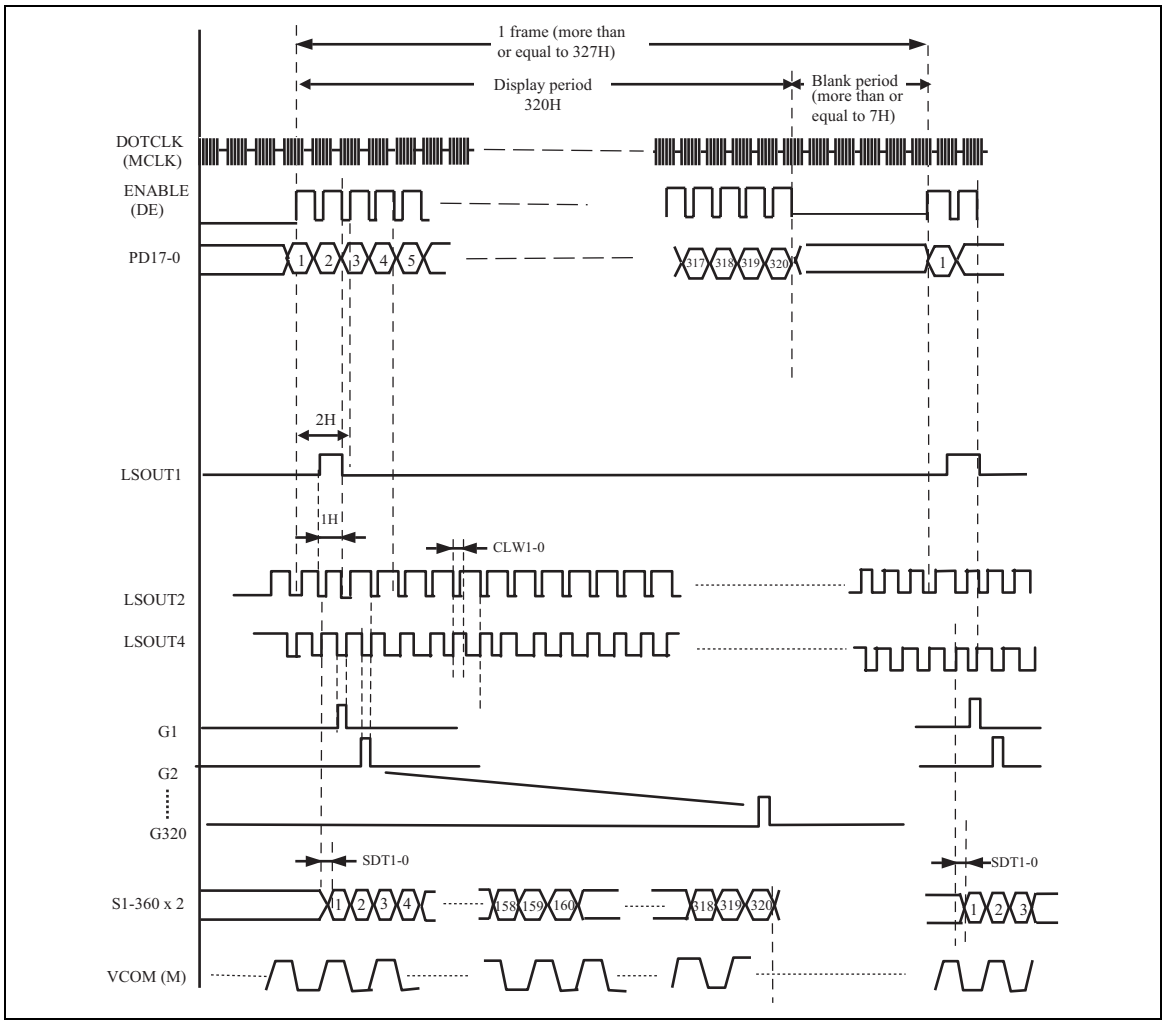
The relationship between the DE transfer mode signal and the LCD panel signal is as follows.



Note) See “LCD Signal Timing Control Function” for details of setting the timing.

LCD panel interface timing while DE transfer mode 3

The relationship between the DE transfer mode signal, gate driver outputs and the LCD panel signal is as follows.



Note) See “LCD Signal Timing Control Function” for details of setting the timing.

Serial Peripheral Interface (SPI) Function

(Only available with RGB I/F)

Serial Peripheral Interface (SPI) transfer is made by setting IM1/ pin to the GND level. The interfacing is executed through chip select line (CS*), serial transfer clock line (SCL), and serial input data (SDI). The HD66779 initiates serial data transfer by recognizing the falling edge of CS* input as a start and then start the transfer of the start byte. The condition for the end of data transfer is that the HD66779 recognizes the rising edge of CS* input as an end of transfer.

The HD66779 is selected when the 6-bit chip address in the start byte from the transmission side and the 6-bit device identification code assigned to the HD66779 are compared and matches with each other. The HD66779, when selected, receives data from the subsequent data string. The least significant bit of the identification code can be specified with ID pin. The upper five bits of the device ID code must be 01110. The 7th bit of the start byte is assigned to the selection of HD66779's register (RS) and when this bit is set to 0, index register write is executed and when this bit is set to 1, instruction write is executed. Accordingly, two chip addresses must be assigned to one HD66779.

After receiving the start byte, the HD66779 receives and transfers data by byte. The transfer data format is MSB first. The instruction of the HD66779 comprise 16 bits. The instruction is executed internally after 2-byte (D15-0) transfer with MSB first.

Start byte format

Example of transfer bit	**S**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
Start byte format	Start	Device ID code						RS	0
		0	1	1	1	0	ID		

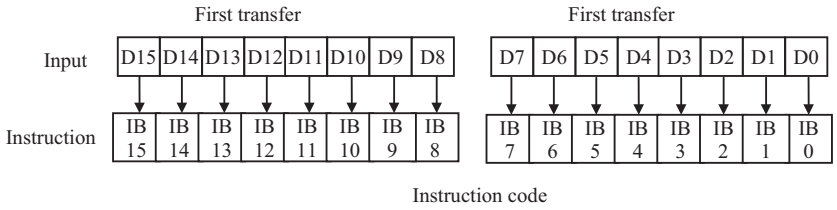
Note) ID bit is selected with IM0/ID pins.

RS bit function

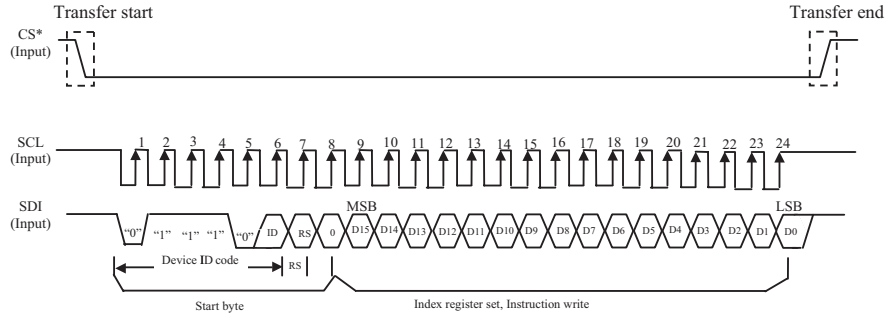
RS	**Function**
0	Set Index register
1	Instruction write

Data format for Serial Peripheral Interface (SPI)

Instruction



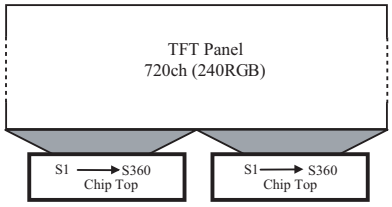
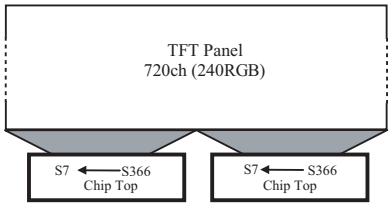
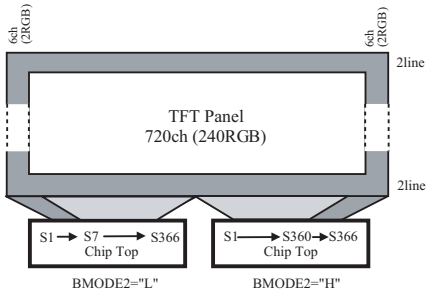
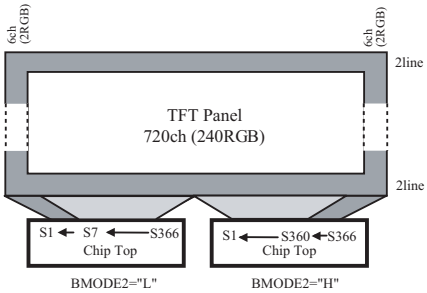
Cclock synchronized sireal transfer (Basic Transfer)



Settings for Data Shift Direction/Boder mode

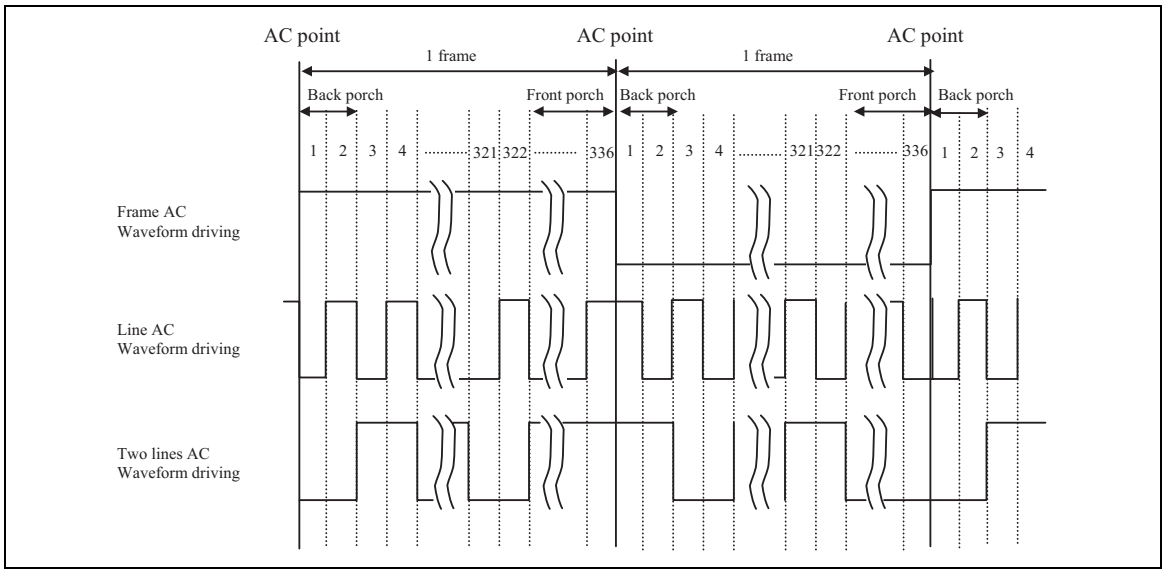
The data shift direction is changeable by setting according to the panel size and the assembly.

The border color control is only on the 6 channels (2RGBs) each at the left and right sides in DE transfer mode. See page 53, “System Configuration Example 4”.

BMODE 1	SHL	Panel Configuration Example (without border)	Make settings for Data shift direction & Border mode only with pin settings
L	L		Possible
L	H		Possible
BMODE 1	SHL	Panel Configuration Example (with border)	Make settings for Data shift direction & Border mode only with pin settings
H	L		Impossible
H	H		Impossible

LCD AC Drive

The HD66779 supports n-raster-row inversion AC drive to alternate signals by arbitrary n raster-rows, where "n" is from 1 to 2, in addition to LCD inversion drive by frame. When deciding the number of "n", by which alternation occurs, with NW bit, check the quality of display on the actual LCD panel. If the number of raster rows for alternation is set small, the LCD alternation frequency becomes high and the charged/discharged current will increase on the LCD cell.



LCD Display Signal Control

The HD66779 allows selection of an optimum LCD display signal for the configuration of a system. See "Display Signal Select Control" in the "Instruction" section, with regard to the timing of signal.

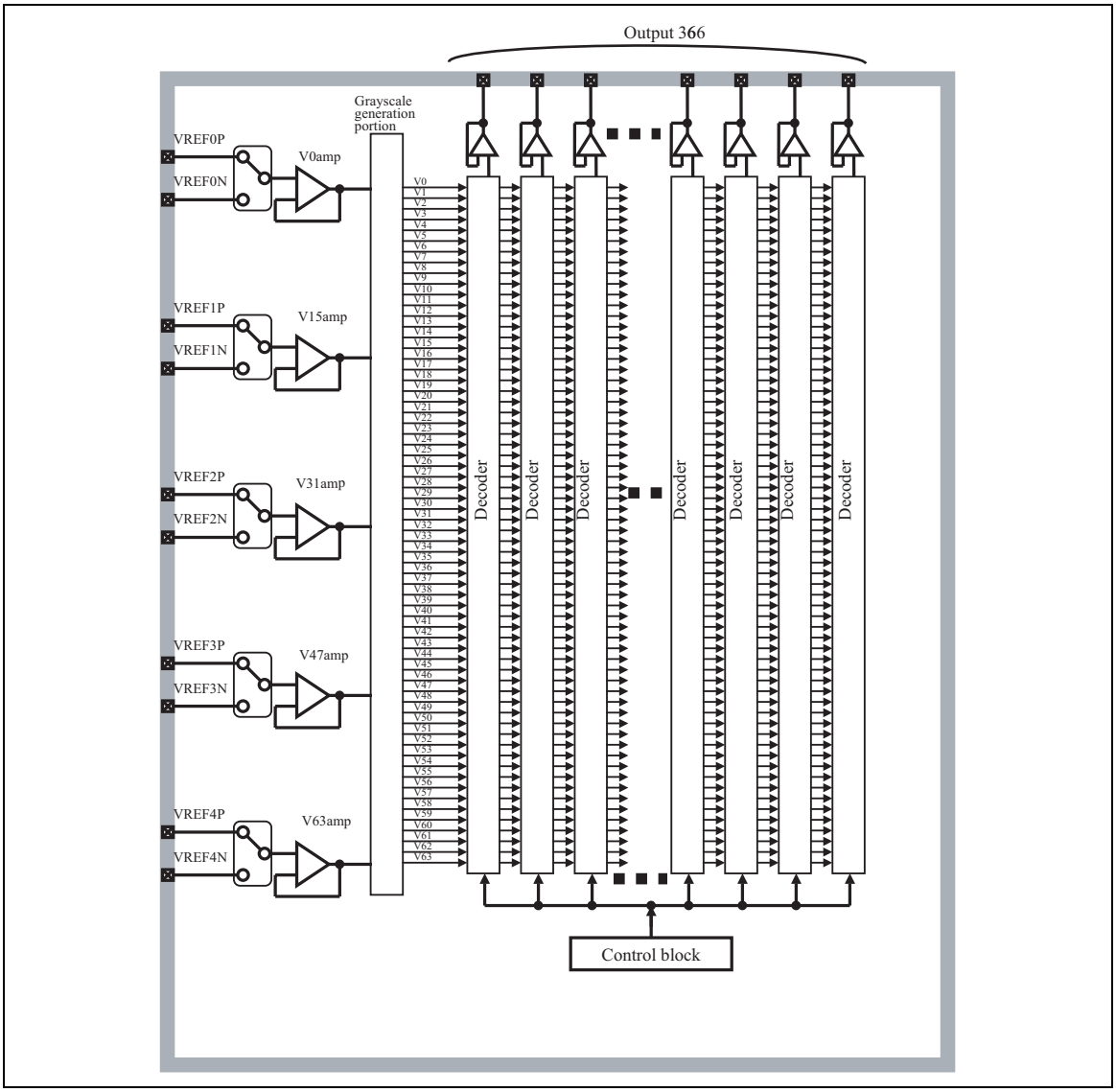
Register setting

DSC1	DSC0	GIF1	GIF0	Level shifter voltage output (VGH-VGL)			Logic voltage output (Vcc-GND)		
				SOUT2	SOUT3	SOUT4	LSOUT2	LSOUT3	LSOUT4
0	0	0	0	—	—	—	—	—	—
		0	1	—	—	—	—	—	—
		1	0	—	—	—	—	—	—
		1	1	—	—	—	—	—	—
0	1	0	0	Line cycle clock 1	Line cycle clock 2	—	—	—	—
		0	1	Line cycle clock 1	Line cycle clock 2	Gate off signal	—	—	—
		1	0	Line cycle clock 1	Line cycle clock 2	Gate-all-on signal	—	—	—
		1	1	Line cycle clock 3	Gate-all-on signal	Gate off signal	—	—	—
1	0	0	0	—	—	—	Line cycle clock 1	Line cycle clock 2	—
		0	1	—	—	—	Line cycle clock 1	Line cycle clock 2	Gate off signal
		1	0	—	—	—	Line cycle clock 1	Line cycle clock 2	Gate-all-on signal
		1	1	—	—	—	Line cycle clock 3	Gate all ON signal	Gate off signal
1	1	0	0	Line cycle clock 1	Line cycle clock 2	—	Line cycle clock 1	Line cycle clock 2	—
		0	1	Line cycle clock 1	Line cycle clock 2	Gate off signal	Line cycle clock 1	Line cycle clock 2	Gate off signal
		1	0	Line cycle clock 1	Line cycle clock 2	Gate all ON signal	Line cycle clock 1	Line cycle clock 2	Gate-all-on signal
		1	1	Line cycle clock 3	Gate-all-on signal	Gate off signal	Line cycle clock 3	Gate-all-on signal	Gate off signal

Note) Leave open for "—".

Grayscale Amplifier Configuration

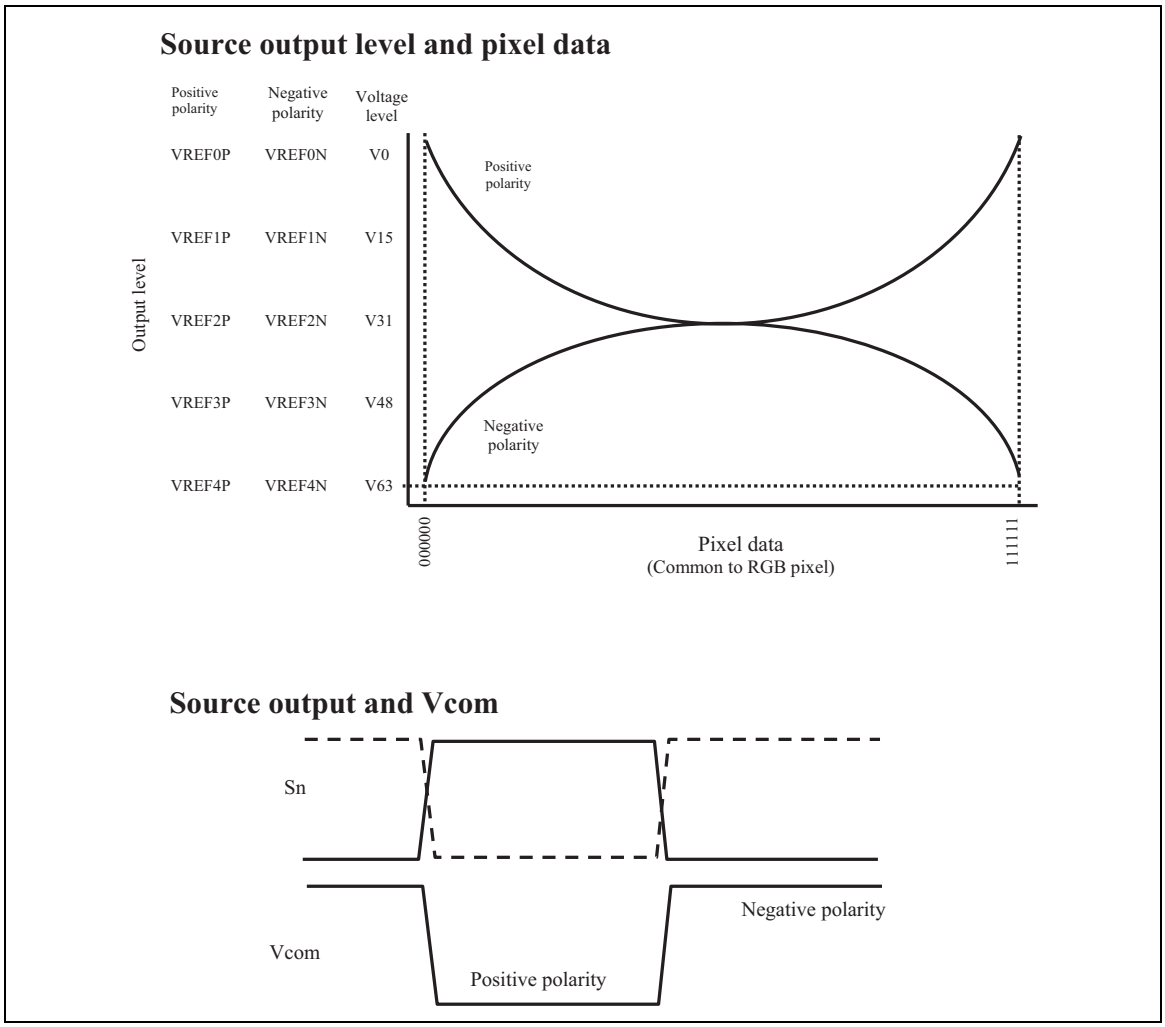
The following figure illustrates the configuration of a grayscale amplifier. The input power into VREF0P ~ VREFF4P, VREF0N ~ VREF4N is divided internally with internal resistor of HD66779 to generate voltages from V0 to V63.



Note) Electric potential must be supplied externally to all VREF0P~VREF4P, VREF0N~VREF4N.

The Relationship between Input Data and Output Level

The following figure shows the relationship between the pixel data and the source output level.



Voltage calculation formula (positive polarity)

Grayscale voltage	Formula
V0	VREF0P
V1	V15+(V0-V15)*(134/154)
V2	V15+(V0-V15)*(124/154)
V3	V15+(V0-V15)*(114/154)
V4	V15+(V0-V15)*(104/154)
V5	V15+(V0-V15)*(94/154)
V6	V15+(V0-V15)*(84/154)
V7	V15+(V0-V15)*(74/154)
V8	V15+(V0-V15)*(64/154)
V9	V15+(V0-V15)*(54/154)
V10	V15+(V0-V15)*(44/154)
V11	V15+(V0-V15)*(34/154)
V12	V15+(V0-V15)*(25/154)
V13	V15+(V0-V15)*(16/154)
V14	V15+(V0-V15)*(8/154)
V15	VREP1P
V16	V31+(V15-V31)*(77/84)
V17	V31+(V15-V31)*(70/84)
V18	V31+(V15-V31)*(63/84)
V19	V31+(V15-V31)*(57/84)
V20	V31+(V15-V31)*(51/84)
V21	V31+(V15-V31)*(45/84)
V22	V31+(V15-V31)*(39/84)
V23	V31+(V15-V31)*(34/84)
V24	V31+(V15-V31)*(29/84)
V25	V31+(V15-V31)*(24/84)
V26	V31+(V15-V31)*(20/84)
V27	V31+(V15-V31)*(16/84)
V28	V31+(V15-V31)*(12/84)
V29	V31+(V15-V31)*(8/84)
V30	V31+(V15-V31)*(4/84)
V31	VREF2P
V32	V48+(V31-V48)*(55/59)
V33	V48+(V31-V48)*(51/59)
V34	V48+(V31-V48)*(47/59)
V35	V48+(V31-V48)*(44/59)
V36	V48+(V31-V48)*(41/59)
V37	V48+(V31-V48)*(38/59)
V38	V48+(V31-V48)*(35/59)
V39	V48+(V31-V48)*(32/59)
V40	V48+(V31-V48)*(29/59)
V41	V48+(V31-V48)*(26/59)
V42	V48+(V31-V48)*(23/59)
V43	V48+(V31-V48)*(20/59)
V44	V48+(V31-V48)*(16/59)
V45	V48+(V31-V48)*(12/59)
V46	V48+(V31-V48)*(8/59)
V47	V48+(V31-V48)*(4/59)
V48	VREF3P
V49	V63+(V48-V63)*(85/89)
V50	V63+(V48-V63)*(81/89)
V51	V63+(V48-V63)*(77/89)
V52	V63+(V48-V63)*(73/89)
V53	V63+(V48-V63)*(69/89)
V54	V63+(V48-V63)*(64/89)
V55	V63+(V48-V63)*(59/89)
V56	V63+(V48-V63)*(54/89)
V57	V63+(V48-V63)*(48/89)
V58	V63+(V48-V63)*(42/89)
V59	V63+(V48-V63)*(35/89)
V60	V63+(V48-V63)*(28/89)
V61	V63+(V48-V63)*(21/89)
V62	V63+(V48-V63)*(14/89)
V63	VREF4P

Note: the following relationship must be observed.

DDVDH-0.3V>=VREF0P>VREF1P>VREF2P>VREF3P>VREF4P>=GND-0.3V
DDVDH-0.3V>=VREF0N>VREF1N>VREF2N>VREF3N>VREF4N>=GND+0.3V
DDVDH-1.0V>=VREF1P, VREF1N
VREF3P, VREF3N>=GND+1.0V
Vn-Vn-1>20mV(n=0-62)

Voltage calculation formula (Negative polarity)

Grayscal volage	Formula
V0	VREF0N
V1	V15+ (V0-V15) * (75/89)
V2	V15+ (V0-V15) * (68/89)
V3	V15+ (V0-V15) * (61/89)
V4	V15+ (V0-V15) * (54/89)
V5	V15+ (V0-V15) * (47/89)
V6	V15+ (V0-V15) * (41/89)
V7	V15+ (V0-V15) * (35/89)
V8	V15+ (V0-V15) * (30/89)
V9	V15+ (V0-V15) * (25/89)
V10	V15+ (V0-V15) * (20/89)
V11	V15+ (V0-V15) * (16/89)
V12	V15+ (V0-V15) * (12/89)
V13	V15+ (V0-V15) * (8/89)
V14	V15+ (V0-V15) * (4/89)
V15	VREF1N
V16	V32+ (V15-V32) * (55/59)
V17	V32+ (V15-V32) * (51/59)
V18	V32+ (V15-V32) * (47/59)
V19	V32+ (V15-V32) * (43/59)
V20	V32+ (V15-V32) * (39/59)
V21	V32+ (V15-V32) * (36/59)
V22	V32+ (V15-V32) * (33/59)
V23	V32+ (V15-V32) * (30/59)
V24	V32+ (V15-V32) * (27/59)
V25	V32+ (V15-V32) * (24/59)
V26	V32+ (V15-V32) * (21/59)
V27	V32+ (V15-V32) * (18/59)
V28	V32+ (V15-V32) * (15/59)
V29	V32+ (V15-V32) * (12/59)
V30	V32+ (V15-V32) * (8/59)
V31	V32+ (V15-V32) * (4/59)
V32	VREF2N
V33	V48+ (V32-V48) * (80/84)
V34	V48+ (V32-V48) * (76/84)
V35	V48+ (V32-V48) * (72/84)
V36	V48+ (V32-V48) * (68/84)
V37	V48+ (V32-V48) * (64/84)
V38	V48+ (V32-V48) * (60/84)
V39	V48+ (V32-V48) * (55/84)
V40	V48+ (V32-V48) * (50/84)
V41	V48+ (V32-V48) * (45/84)
V42	V48+ (V32-V48) * (39/84)
V43	V48+ (V32-V48) * (33/84)
V44	V48+ (V32-V48) * (27/84)
V45	V48+ (V32-V48) * (21/84)
V46	V48+ (V32-V48) * (14/84)
V47	V48+ (V32-V48) * (7/84)
V48	VREF3N
V49	V63+ (V48-V63) * (146/154)
V50	V63+ (V48-V63) * (138/154)
V51	V63+ (V48-V63) * (129/154)
V52	V63+ (V48-V63) * (120/154)
V53	V63+ (V48-V63) * (110/154)
V54	V63+ (V48-V63) * (100/154)
V55	V63+ (V48-V63) * (90/154)
V56	V63+ (V48-V63) * (80/154)
V57	V63+ (V48-V63) * (70/154)
V58	V63+ (V48-V63) * (60/154)
V59	V63+ (V48-V63) * (50/154)
V60	V63+ (V48-V63) * (40/154)
V61	V63+ (V48-V63) * (30/154)
V62	V63+ (V48-V63) * (20/154)
V63	VREF4N

Note: the following relationship must be observed.

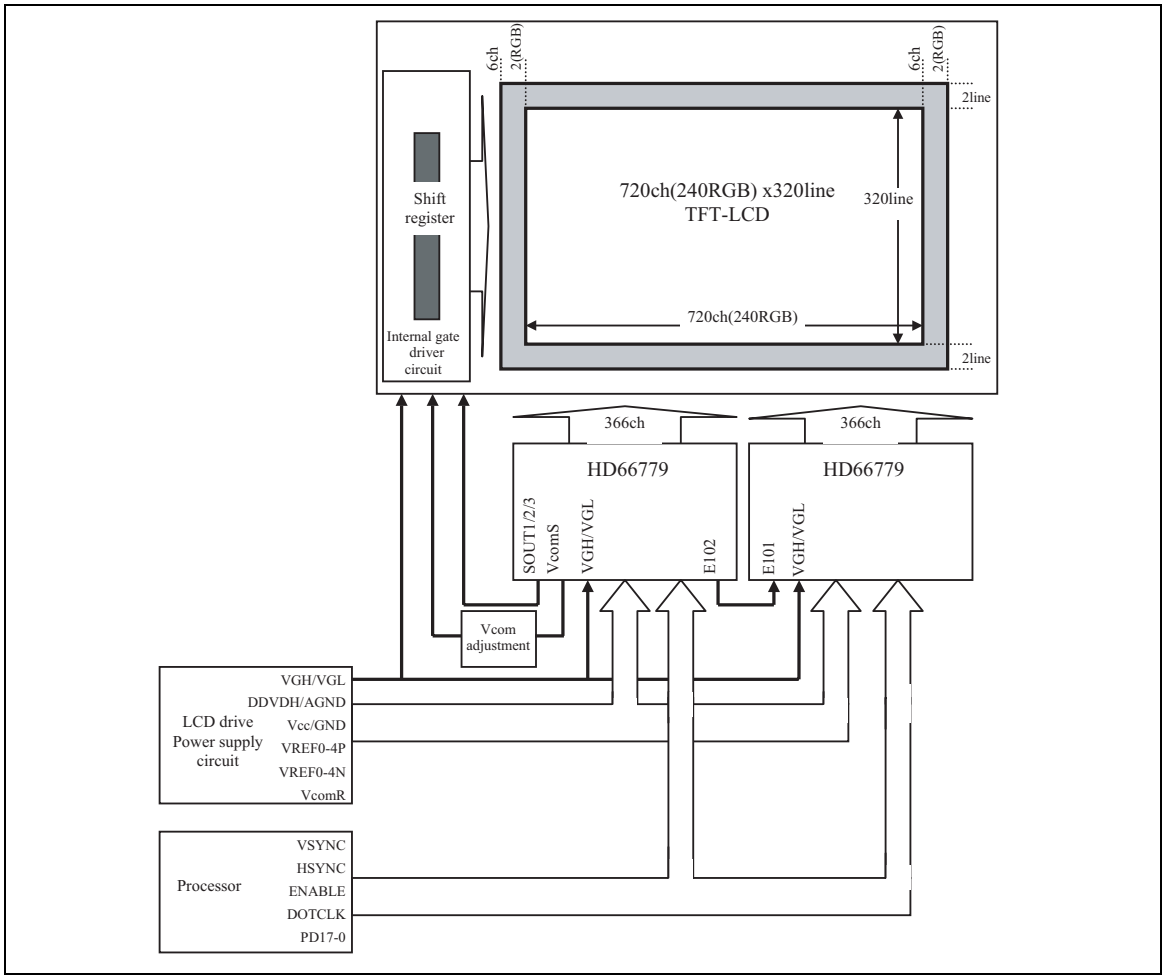
DDVDH-0.3V>=VREF0P>VREF1P>VREF2P>VREF3P>VREF4P>=GND- 0.3V
DDVDH-0.3V>=VREF0N>VREF1N>VREF2N>VREF3N>VREF4N>=GND- 0.3V
DDVDH-1.0V>=VREF1P, VREF1N
VREF3P, VREF3N>=GND-1. 0V
Vn-Vn+1>20mV(n=0-62)

System Configuration Examples

System Configuration Example 1

240(horizontal) x 320(vertical) pixels only with pin settings, No SPI

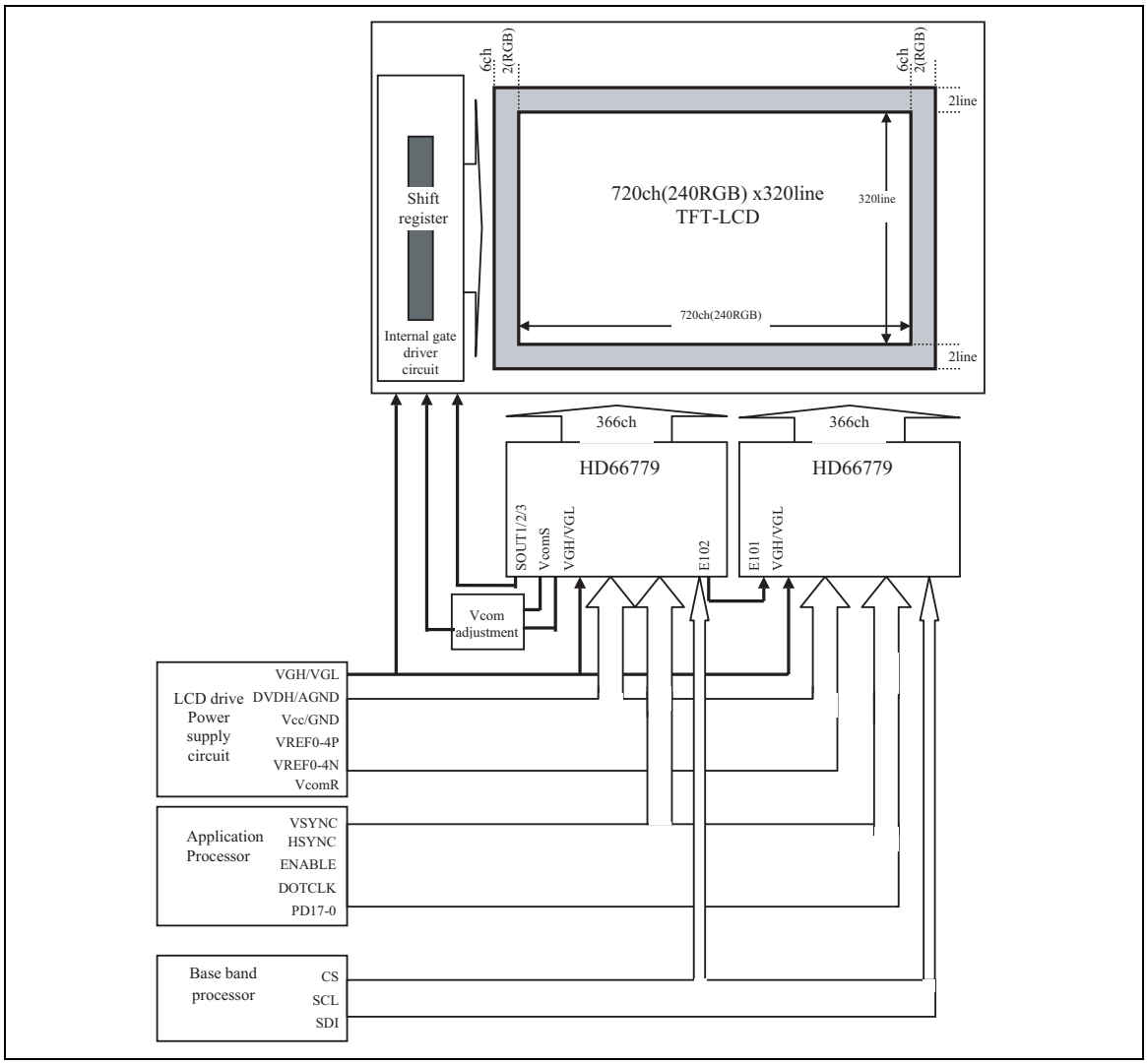
The following figure illustrates an example of adopting HD66779 for TFT-LCD panel with an incorporated gate driver.



System Configuration Example 2

240(horizontal) x 320(vertical) pixels with SPI

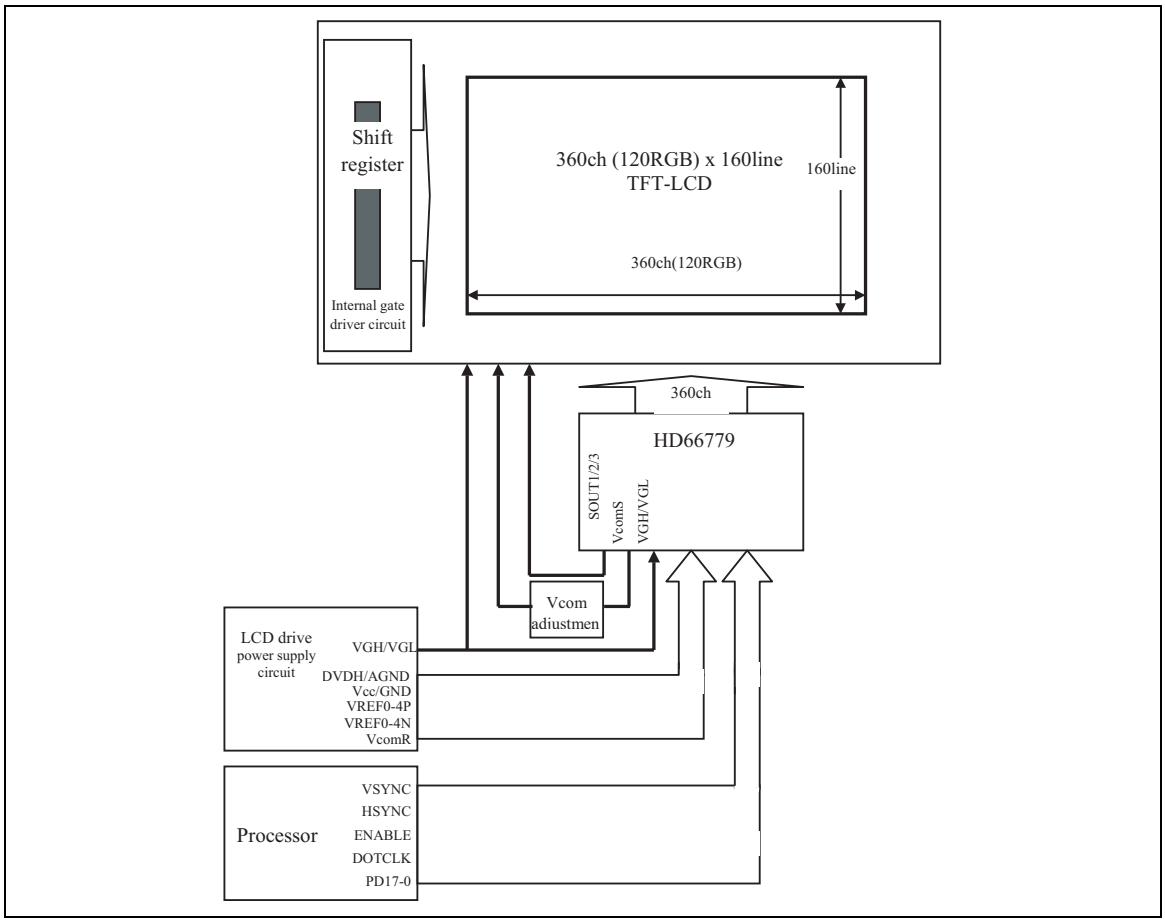
The following figure illustrates an example of adopting HD66779 for TFT-LCD panel with an incorporated gate driver.



System Configuration Example 3

120(horizontal) x 160(vertical) pixels only with pin settings, No SPI

The following figure illustrates an example of adopting HD66779 for TFT-LCD panel with an incorporated gate driver.

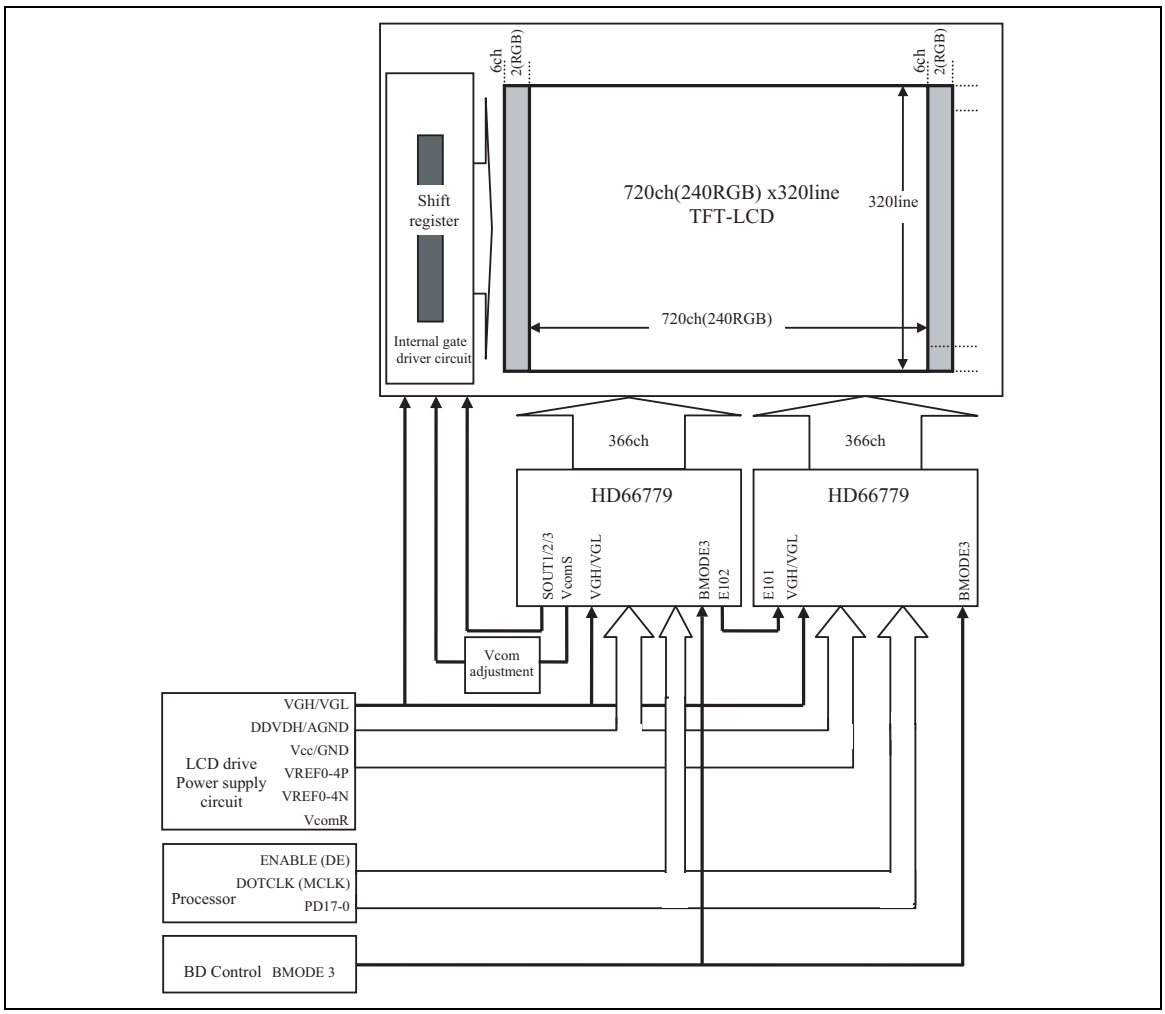


System Configuration Example 4

120(horizontal) x 160(vertical) pixels only with pin settings, DE transfer mode

The following figure illustrates an example of adopting HD66779 for TFT-LCD panel with an incorporated gate driver.

Note 1) The border color control while using DE transfer mode is on the 6 channels each at left and right side.
Note 2) The border color in DE transfer mode is only black and white to be switched with BMODE3 pin.

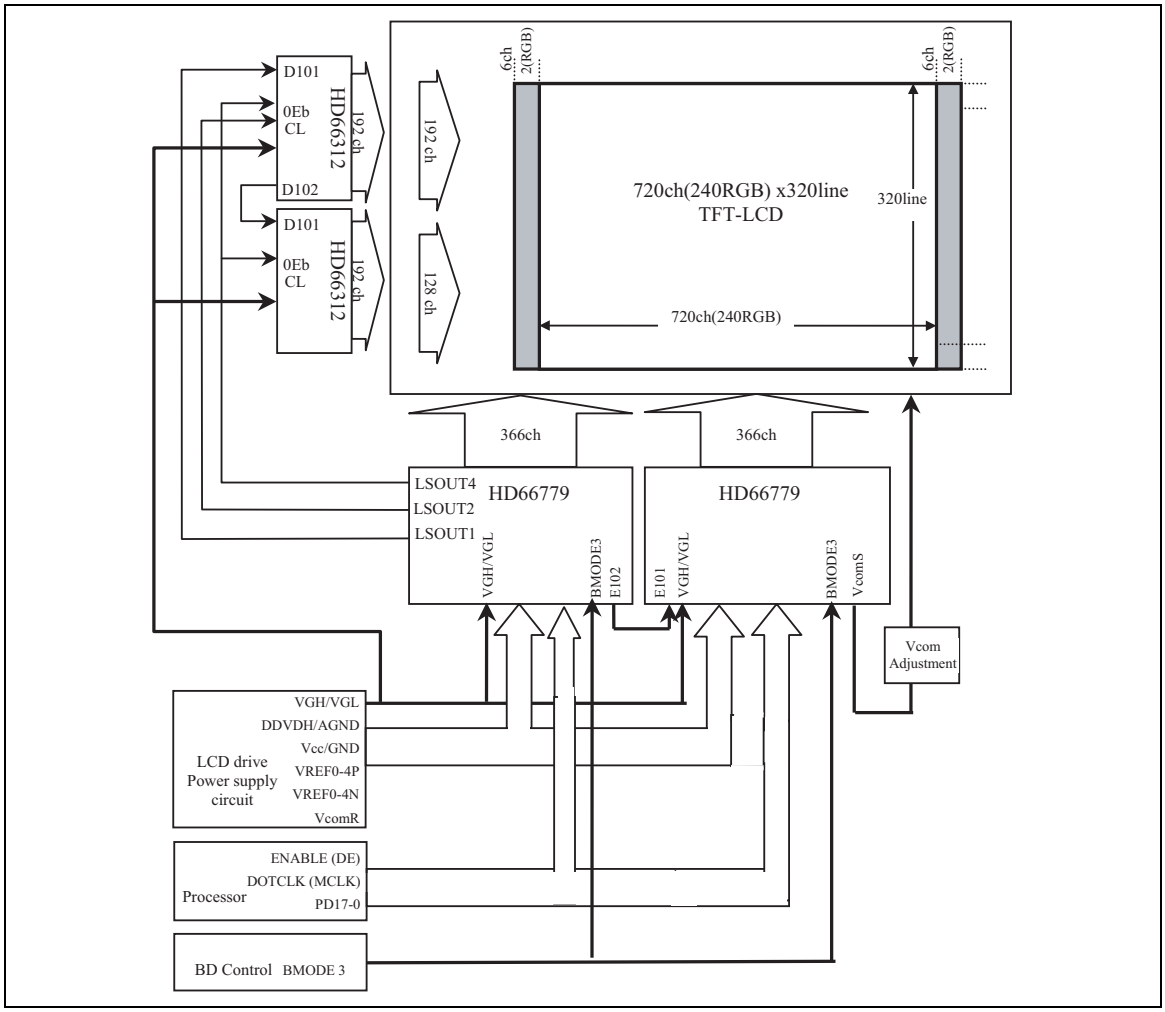


System Configuration Example 5

240(horizontal) x 320(vertical) pixels only with pin settings, DE transfer mode

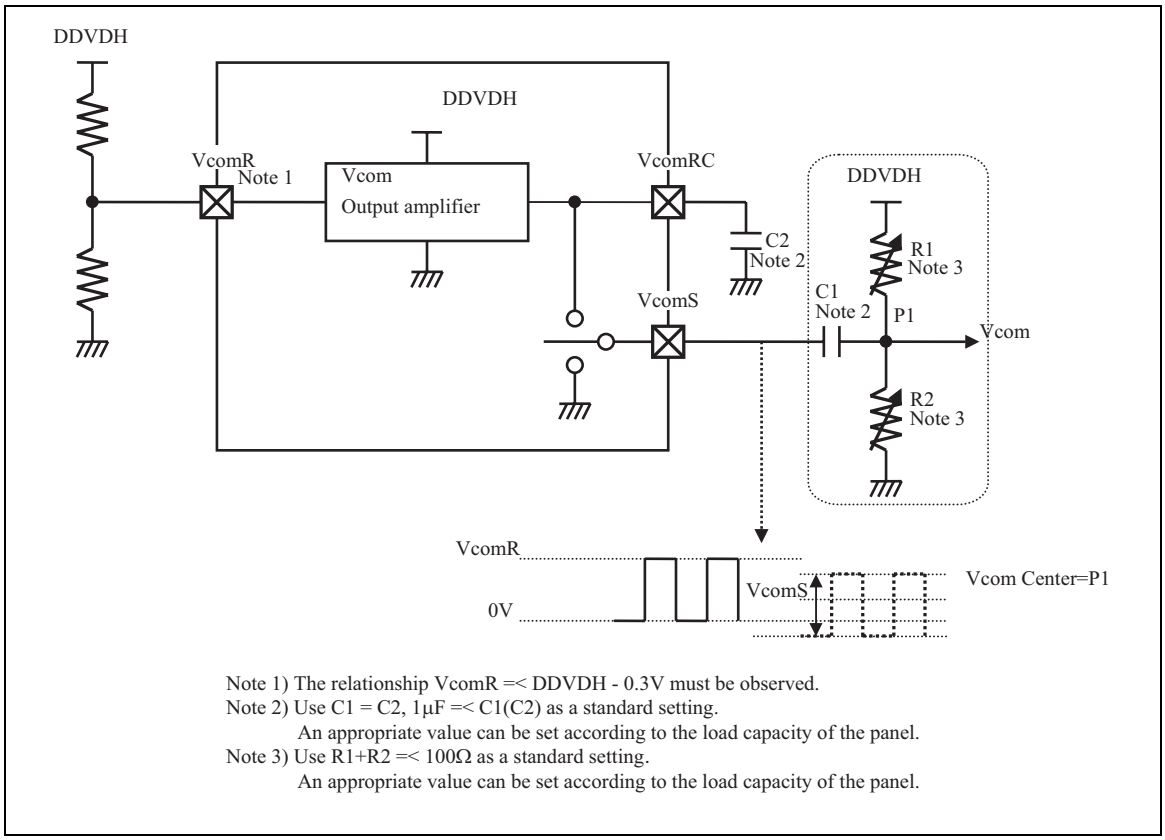
The following figure illustrates an example of adopting HD66779 for TFT-LCD panel with an incorporated gate driver.

Note 1) The border color control while using DE transfer mode is on the 6 channels each at left and right side.
Note 2) The border color in DE transfer mode is only black and white to be switched with BMODE3 pin.



Vcom Generation

Vcom is generated from VcomR, a reference voltage of Vcom, by coupling method with an external circuit, which is supplied with the TFT display common electrode.

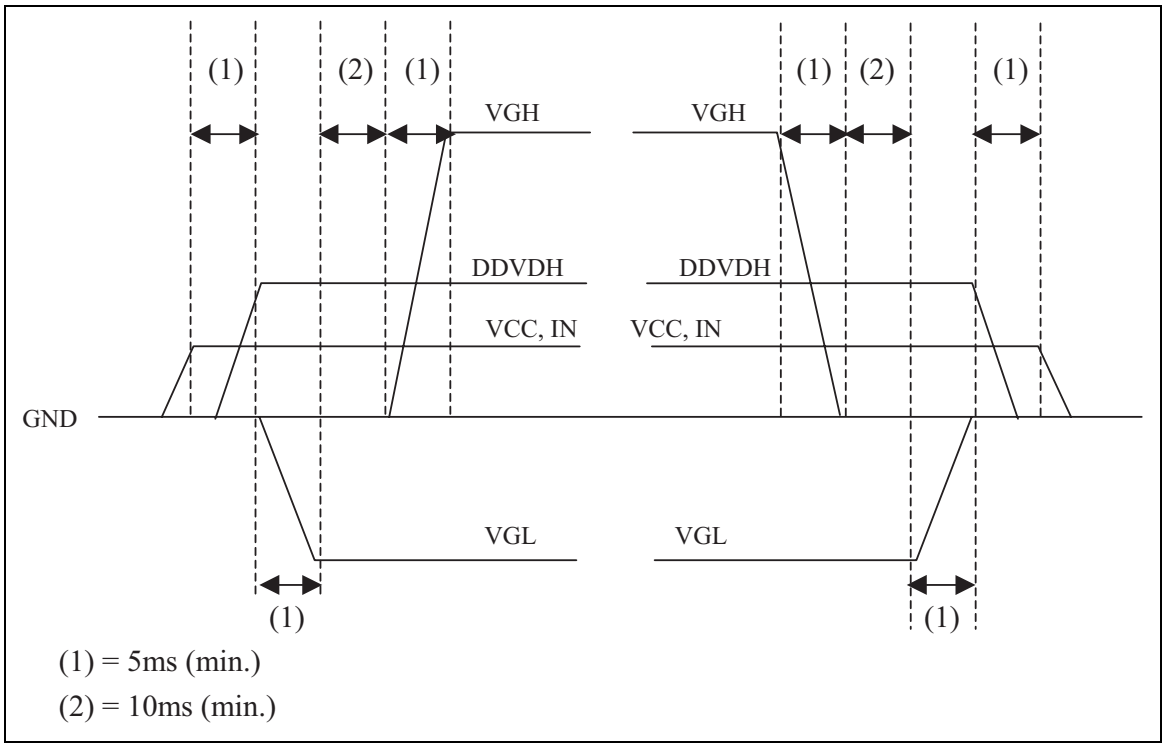


Note 1) The relationship VcomR =< DDVDH - 0.3V must be observed.
Note 2) Use C1 = C2, 1µF =< C1(C2) as a standard setting.
An appropriate value can be set according to the load capacity of the panel.
Note 3) Use R1+R2 =< 100Ω as a standard setting.
An appropriate value can be set according to the load capacity of the panel.

The external capacitor “C1” must be lowered to GND when VcomS is halted.

Voltage Application and insulation sequence

The voltage application/insulation sequence illustrated as follows must be observed.



Absolute Maximum Ratings

Items	Symbol	Unit	Rated value	Notes
Power supply voltage (1)	Vcc	V	- 0.3 ~ +4.3	(1), (2)
Power supply voltage (2)	DDVDH-GND	V	- 0.3 ~ + 6.0	(1), (3)
Power supply voltage (3)	VGH-AGND	V	- 0.3 ~ + 22.0	(1), (4)
Power supply voltage (4)	AGND-VGL	V	- 0.3 ~ + 16.5	(1), (5)
Input voltage	Vt	V	- 0.3 ~ Vcc + 0.3	(1)
Operational temperature	Topr	ºC	- 40 ~ +85	(1), (6)
Storage temperature	Tstg	ºC	- 55 ~ +110	(1)

Note1: If the LSI is used above these absolute maximum ratings, it may be permanently damaged. Using the LSI within the limit of electrical characteristics is strongly recommended during normal operation. The use of LSI under a condition above the limit may lead to malfunction and loss of credibility of LSI.

Note2: Vcc (High) ≥ GND (Low) must be observed.

Note3: DDVDH (High) ≥ GND (Low) must be observed.

Note4: VGH (High) ≥ AGND (Low) must be observed.

Note5: AGND (High) ≥ VGL (Low) must be observed.

Note6: The DC/AC characteristics of die and wafer products is guaranteed at 85 ºC.

Electrical characteristics

DC characteristics

Vcc = 2.5V ~ 3.6V, Ta = -40ºC ~ +85ºC: See Note 1

Items		Symbol	Unit	Measurement Condition	min.	typ.	max.	Notes
Input “High” level voltage		V_{IH}	V	Vcc = 2.5V ~ 3.6V	0.7Vcc	—	Vcc	(2),(3)
Input “Low” level voltage		V_{IL}	V	Vcc = 2.5V ~ 3.6V	-0.3	—	0.15Vcc	(2),(3)
Output “High” level voltage		V_{OH}	V	IOH = -0.1mA	0.7Vcc	—	—	(2)
Output “Low” level voltage		V_{OL}	V	IOL = 0.1mA	—	—	0.15Vcc	(2)
input/output leak current		I_{Li}	μA	Vin = 0 ~ Vcc	-5	—	5	(4)
Current Consumption (Vcc ~ GND)	Normal operation mode	I_{OP}	mA	Vcc = 3V, DDVDH = 5H, VGH = 12V, VGL = -8V, DOTCLK = 8MHz, 1H period = 45μS, 366ch Ta = 25ºC	—	1.1	1.35	(5)
	Static state	I_{ST}	μA	Vcc = 3V, DDVDH = 5V, VGH = 12V, VGL = -8V, DOTCLK = 8MHz, 1H period = 45μS, 366ch Ta = 25ºC	—	5	10	(5)
LCD power supply voltage (DDVDH ~ AGND)	DDVDH – AGND	I_{DDP}	mA	Vcc = 3V, DDVDH = 5V, VGH = 12V, VGL = -8V, DOTCLK = 8MHz, 1H period = 45μS, 366ch Ta = 25ºC	—	1.7	1.9	(5)
	AGND – VGL	I_{VLP}	μA	Vcc = 3V, DDVDH = 5V, VGH = 12V, VGL = -8V, DOTCLK = 8MHz, 1H period = 45μS, 366ch Ta = 25ºC	—	80	110	(5)

Items		Symbol	Unit	Measurement Condition	min.	typ.	max.	Notes
LCD power supply voltage (DDVDH ~ AGND)	VGH - AGND	I_{VHP}	μA	Vcc = 3V, DDVDH = 5V, VGH = 12V, VGL = -8V, DOTCLK = 8MHz, 1H period = 45μS, 366ch Ta = 25ºC	—	80	110	(5)
Output voltage difference		ΔVo	mV	—	—	+/-15	+/-25	(7)
Average output voltage fluctuation		ΔVΔ	mV	—	—	+/-15	—	(8)

Serial Peripheral Interface Timing Characteristics

Vcc = 2.5 ~ 3.6 V

Item	Symbol	Unit	Timing diagram	Min	Typ	Max
Serial clock cycle time	t_{SCYC}	μs	Figure 1	0.2	—	40
Serial clock “High”-level pulse width	t_{SCH}	ns	Figure 1	80	—	—
Serial clock “Low”-level pulse width	t_{SCL}	ns	Figure 1	80	—	—
Serial clock rise/fall time	t_{scr}, t_{scf}	ns	Figure 1	—	—	40
Chip select set up time	t_{CSU}	ns	Figure 1	40	—	—
Chip select hold time	t_{CH}	ns	Figure 1	120	—	—
Serial input data set up time	t_{SISU}	ns	Figure 1	60	—	—
Serial input data hold time	t_{SIH}	ns	Figure 1	60	—	—

Reset Timing Characteristics

V_{CC} = 2.5 to 3.6 V

Item	Symbol	Unit	Timing diagram	Min	Typ	Max
Reset “Low”-level width	t_{RES}	ms	Figure 2	1	—	—
Reset rise time	t_{rRES}	μs	Figure 2	—	—	10

RGB interface timing characteristics

RGB interface, Vcc = 2.5V ~ 3.6V

Item	Symbol	Unit	Timing diagram	min.	typ.	max.
VSYNC/HSYNC Set up time	tSYNCS	ns	Figure 3	20	—	
ENABLE Set up time	tENS	ns	Figure 3	30	—	—
ENABLE Hold time	tENH	ns	Figure 3	30	—	—
DOTCLK “Low”-level pulse width	PW_{DL}	ns	Figure 3	40	—	—
DOTCLK “High”-level pulse width	PW_{DH}	ns	Figure 3	40	—	—
DOTCLK cycle time	tCYCD	ns	Figure 3	100	—	—
Data Set up time	tPDS	ns	Figure 3	30	—	—
Data Hole time	tPDH	ns	Figure 3	30	—	—
DOTCLK, VSYNC, HSYNC rise/fall time	trgbr, trgbf	ns	Figure 3	—	—	25

Switching characteristics

RGB interface, Vcc = 2.5V to 3.6 V

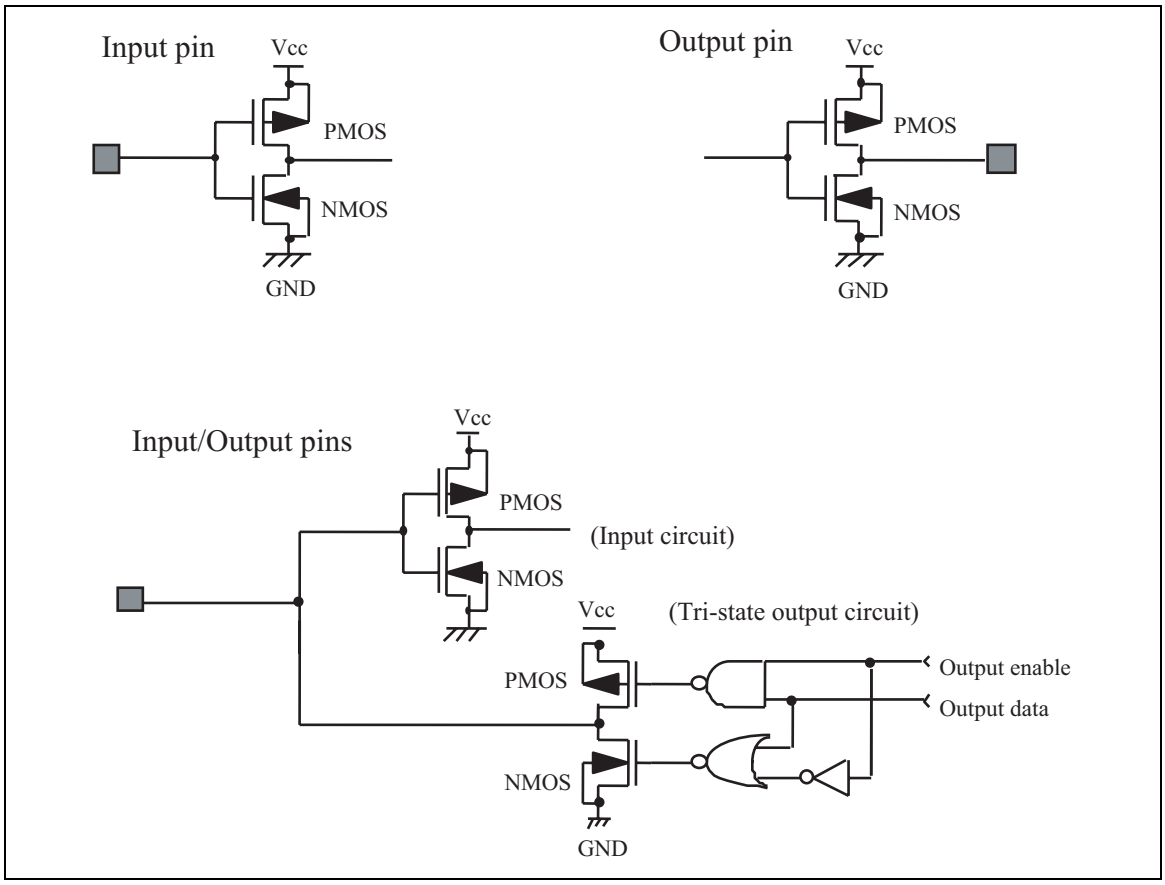
Item	Symbol	Unit	Timing diagram	min.	typ.	max.
Start pulse set up time	tSWS	ns	Figure 4	20	—	—
Start pulse delay time	tSWO	ns	Figure 4	—	—	80

LCD driver output characteristics

Item	Symbol	Unit	Test Condition	min.	typ.	max.	Note
Driver output delay time	tDD	μs	Vcc = 3V, DDVDH = 5V, VGH = 8V, VGL = 0V, Ta = 25ºC, DOTCLK = 8MHz, All pins undergo a same change from same grayscale level Time required to reach +/- 25 mV during VCOMS polarity change Load resistance R = 10kΩ, Load capacity 50pF	—	20	35	(10)

Notes to Electrical Characteristics

1. The DC/AC electrical characteristics of bare die and wafer products are guaranteed at 85°C.
2. The following figures illustrate the configurations of I pin, I/O pin, and O pin.

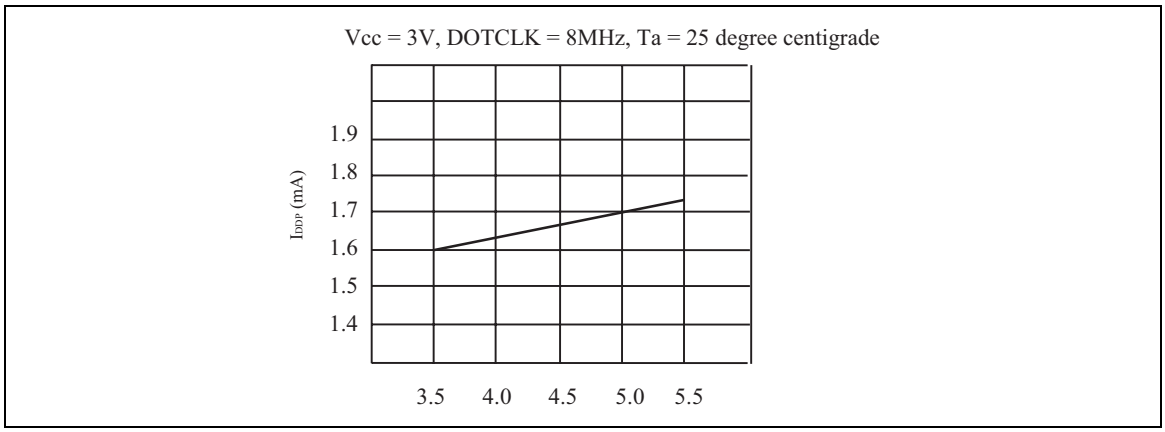


3. TEST, IM1, IM0/ID pins must be grounded or connected to Vcc.

4. This excludes the current through output drive MOS.

5. This excludes the current through the input/output units. The input level must be fixed to a certain level because penetrating current increases in the input circuit when CMOS input level takes a middle level. The current consumption is unchanged irrespective of "High" or "Low" of CS*pin while the HD66779 is not accessed through interface pins.

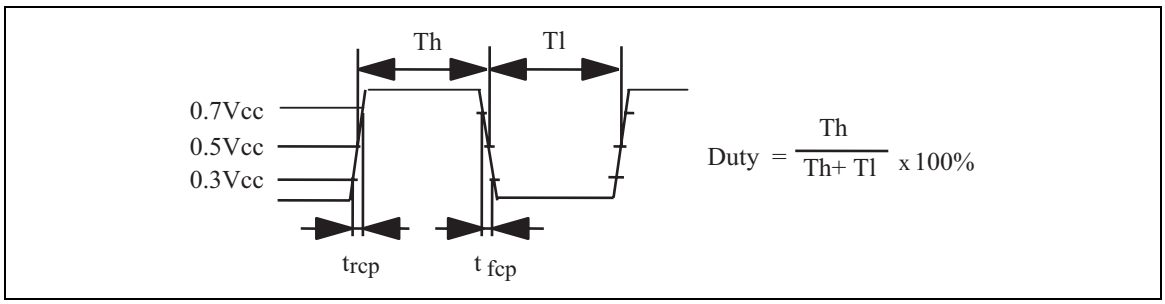
6. The relationship between operational condition and current consumption is as follows.



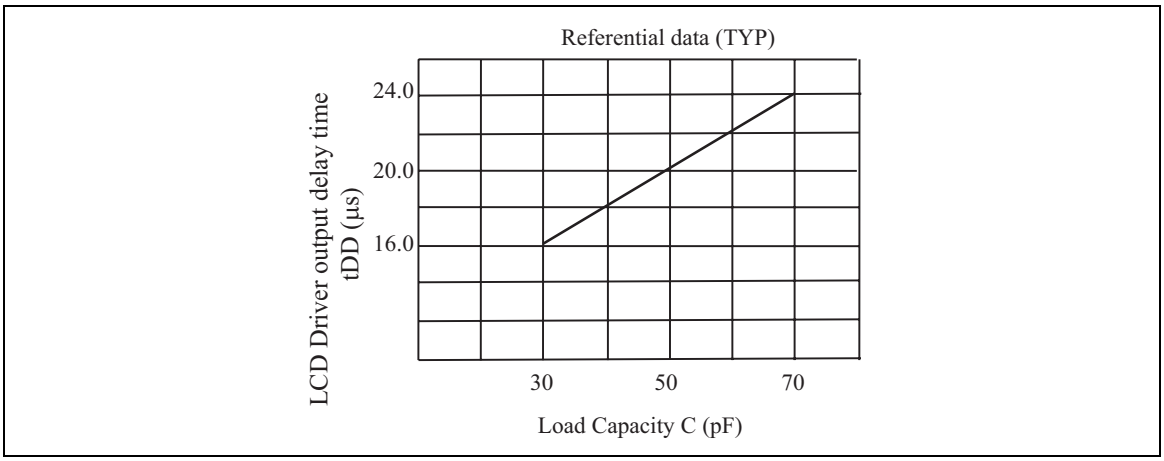
7. The output voltage difference is the difference in the neighboring output voltages for a same display (within a chip). The output voltage difference in offset cancel operation is within +/- 10mV.

8. The average output voltage fluctuation is the difference in the average output voltages among different chips. The average output voltage is an average voltage within a chip for a same display. This value is just for a referential purpose.

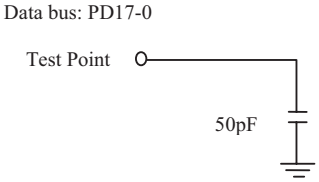
9. This applies to the case when clocks are supplied externally.



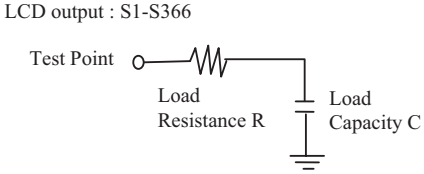
10. The LCD driver output delay time depends on the load on the LCD panel. Check the quality of display on the actual LCD panel before making settings for the frame frequency and one-line cycle.



Load circuit for
AC characteristics mesurement



Load circuit for
LCD driver output characteristics measurement



Timing diagram

Serial Peripheral Interface Operation

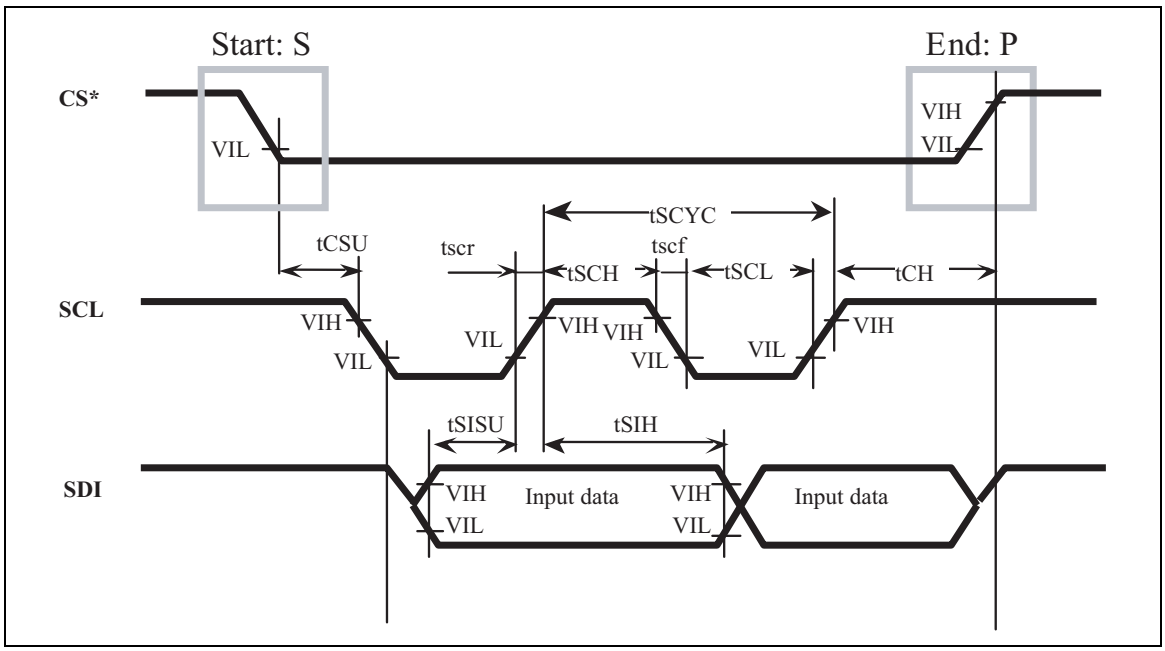


Figure 1

Reset Operation

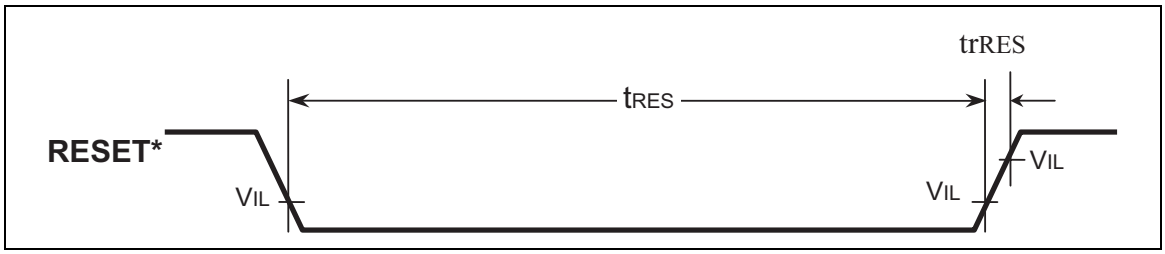


Figure 2

Interfacing Operation

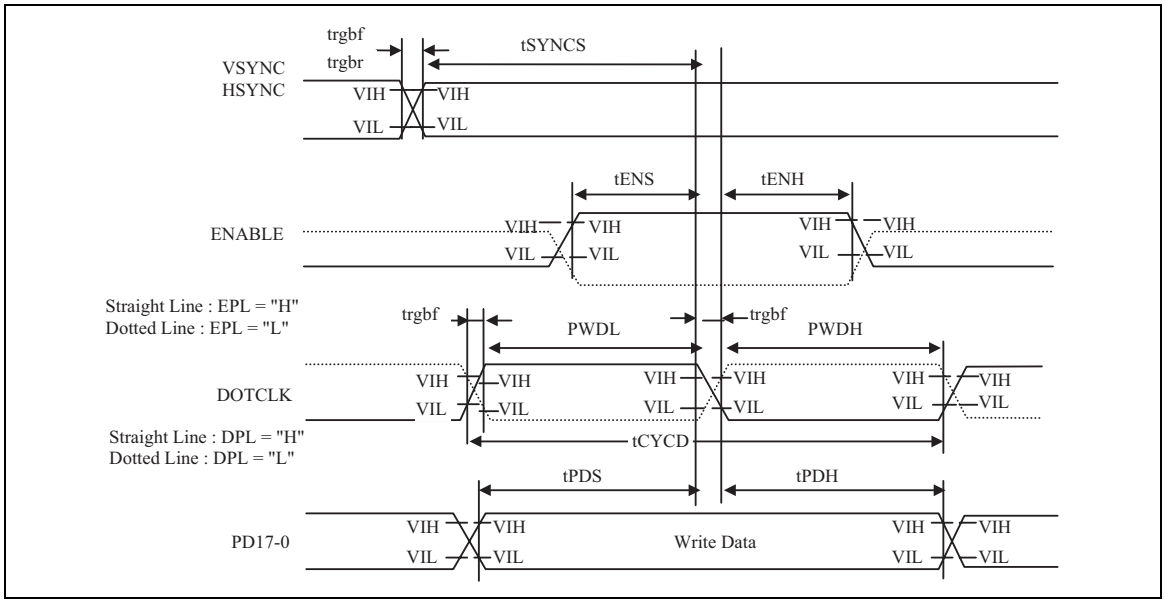


Figure 3

Switching Operation

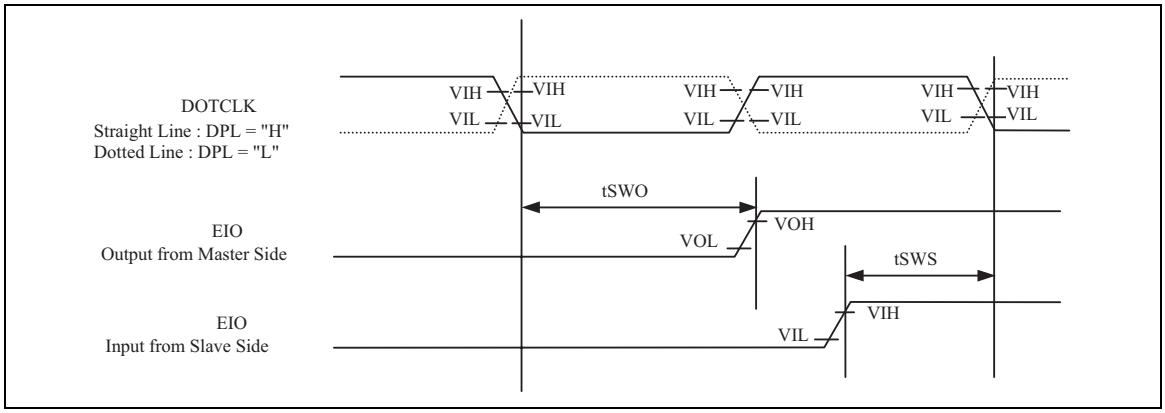


Figure 4

LCD Driver Output Characteristics

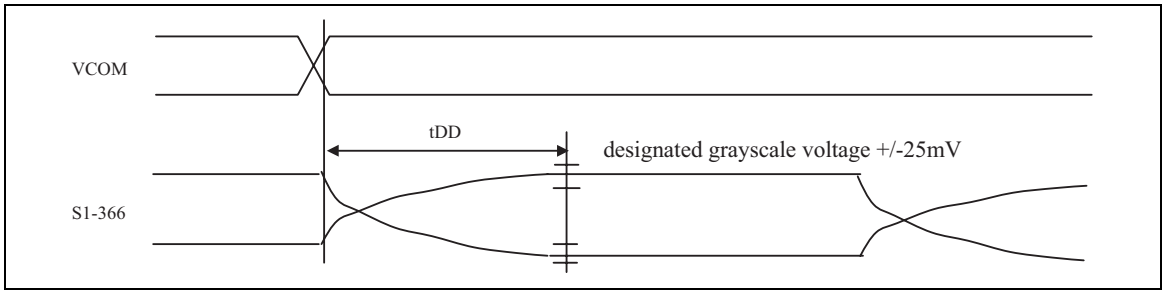


Figure 5

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Colophon 0.0

Revision Record

Rev.	Date	Page	Contents of Modification	Approved by
0.2	2002.10.25		First issue	
0.3	2002.12.13	4	Figure 1: Change “POS” to “TESTPS”	
		5	Change the explanation for (1) External Display Interface.	
		6	Add “TESTPS” to Talbe 1.	
		7	Add “When using border display, display period is 320H.” to Function of BMODE1.	
			Delete “POS” from Table 1.	
		8	Change Function of DOTCLK.	
			Add “(DE)” to the Signal name “ENABLE”.	
			Add “When using DE transfer mode (SSMD1 = “H”), BP setting is invalid.” to Function of BP.	
		10	Change Function of GAON.	
		12	Revise PAD arrangement figure to Rev.0.1.	
		13	Revise Pad coordinate (Input) to Rev. 0.1.	
		15	Delete “POS” from Figure 5.	
			Delete the explanation of “POS”.	
		17	Change “14 lines>=BP>=2 lines” in the explanation of BP3-0 to “14 lines >= Number of back porch lines minus number of border lines”.	
		19	Change the waveform of SOUT4 upside down in Figure 12.	
			Chage the note added to Figure 12.	
		20	Add a note “” to the explanation of FHN.	
		21	Delete “*POS” and “0” in bit 9 of R01h, and add “1” instead of “POS”.	
		22	Delete “Source output: S1 - S366 Output “GND” level” from 2. Initial level of output pin.	
		24	Change Figure 16 and its note.	
		25	Delete the explantion of “Power save function (POS)”.	
			Change Figure 18.	
		26	Delete Table 13 and add new Table 13, 14, and 15.	
		29	Add “For the detail setting of timing, refer to “Signal timing control function for LCD display” to Figure 21.	
		30	Add the same note added to Figure 21 to Figure 22.	
		33	Add the same note added to Figure 21 to Figure 25.	
		34	Add the same note added to Figure 21 to Figure 26.	
		35	Add the same note added to Figure 21 to Figure 27.	
		40	Delete Table 17(old) Wire setting.	
		40	Correct Table 18.	

Rev.	Date	Page	Contents of Modification	Approved by
0.3	2002.12.13	51	Correct “VCC” to “VCC, IN” in Figure 44.	
		53	Change Table 22. (T.B.D → Decided)	
		54	Change Table 23 and 24. (T.B.D →Decided)	
		55	Change Talbe 24, 25, and 26. (T.B.D → Decided)	
		57	Correct “+/- 2m” to “+/- 10m” in note 7.	
		60	Change Figure 56 and 57.	
1.0	2002.6.13	9	Error Correction. Change “GND” to “Vcc” to which TEST4 is connected. Change “TEST1, 4-15” to “TEST1, 5-15” and number of pins from “15” to “14”.	
			Addition to function column. “Make sure VGH ≥ DDVDH ≥ VCC”	
		5, 14, 19, 26, 32~35, 54, 57	Error Corrections	
		58, 60, 61, 63, 64, 67	Addition of measurement to the electrical characteristics tables where marked with “TBD”.	