

Low-Voltage CMOS Octal D-Type Flip-Flop Flow Through Pinout With 5V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

The MC74LCX574 is a high performance, non-inverting octal D-type flip-flop operating from a 2.3 to 3.6V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5V allows MC74LCX574 inputs to be safely driven from 5V devices.

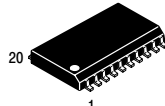
The MC74LCX574 consists of 8 edge-triggered flip-flops with individual D-type inputs and 3-state true outputs. The buffered clock and buffered Output Enable (\overline{OE}) are common to all flip-flops. The eight flip-flops will store the state of individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the \overline{OE} LOW, the contents of the eight flip-flops are available at the outputs. When the \overline{OE} is HIGH, the outputs go to the high impedance state. The \overline{OE} input level does not affect the operation of the flip-flops. The LCX574 flow through design facilitates easy PC board layout.

- Designed for 2.3 to 3.6V V_{CC} Operation
- 5V Tolerant — Interface Capability With 5V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When $V_{CC} = 0V$
- LVTTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10 μ A)
Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V

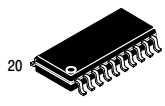
MC74LCX574

LCX

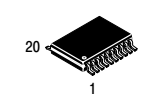
LOW-VOLTAGE CMOS OCTAL D-TYPE FLIP-FLOP



DW SUFFIX
PLASTIC SOIC
CASE 751D-04



M SUFFIX
PLASTIC SOIC EIAJ
CASE 967-01



DT SUFFIX
PLASTIC TSSOP
CASE 948E-02

PIN NAMES

Pins	Function
\overline{OE}	Output Enable Input
CP	Clock Pulse Input
D0-D7	Data Inputs
O0-O7	3-State Outputs

MC74LCX574

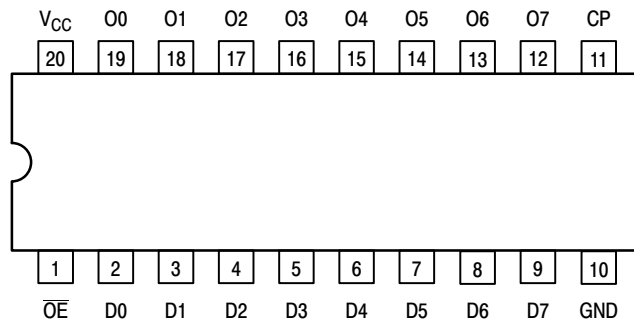


Figure 1. Pinout: 20-Lead (Top View)

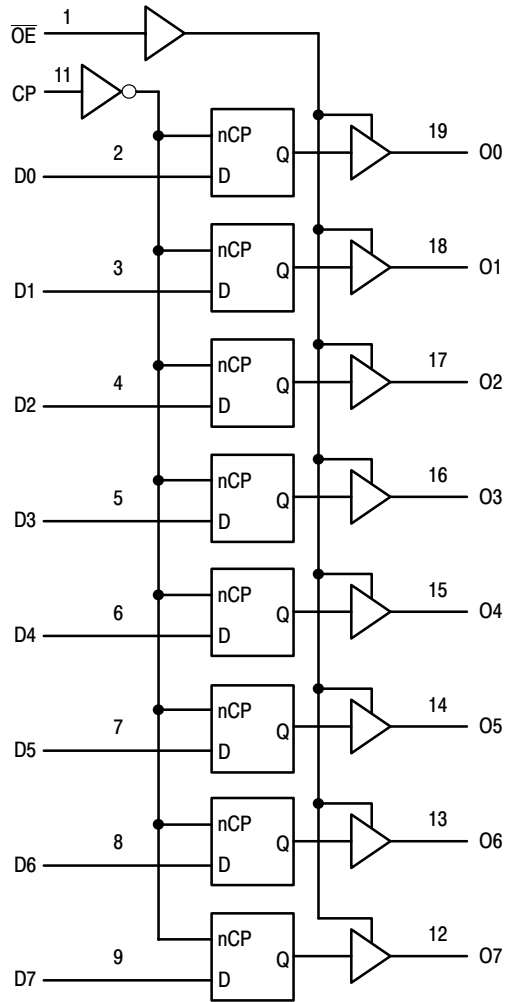


Figure 2. LOGIC DIAGRAM

MC74LCX574

INPUTS			INTERNAL LATCHES	OUTPUTS	OPERATING MODE
\overline{OE}	CP	Dn	Q	On	
L L	\uparrow \uparrow	l h	L H	L H	Load and Read Register
L	\uparrow	X	NC	NC	Hold and Read Register
H	\uparrow	X	NC	Z	Hold and Disable Outputs
H H	\uparrow \uparrow	l h	L H	Z Z	Load Internal Register and Disable Outputs

H = High Voltage Level; h = High Voltage Level One Setup Time Prior to the Low-to-High Clock Transition; L = Low Voltage Level; l = Low Voltage Level One Setup Time Prior to the Low-to-High Clock Transition; NC = No Change; X = High or Low Voltage Level and Transitions are Acceptable; Z = High Impedance State; \uparrow = Low-to-High Transition; \uparrow = Not a Low-to-High Transition; For I_{CC} Reasons DO NOT FLOAT Inputs

MC74LCX574

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Condition	Unit
V _{CC}	DC Supply Voltage	-0.5 to +7.0		V
V _I	DC Input Voltage	-0.5 ≤ V _I ≤ +7.0		V
V _O	DC Output Voltage	-0.5 ≤ V _O ≤ +7.0	Output in 3-State	V
		-0.5 ≤ V _O ≤ V _{CC} + 0.5	Note 1.	V
I _{IK}	DC Input Diode Current	-50	V _I < GND	mA
I _{OK}	DC Output Diode Current	-50	V _O < GND	mA
		+50	V _O > V _{CC}	mA
I _O	DC Output Source/Sink Current	±50		mA
I _{CC}	DC Supply Current Per Supply Pin	±100		mA
I _{GND}	DC Ground Current Per Ground Pin	±100		mA
T _{STG}	Storage Temperature Range	-65 to +150		°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

1. Output in HIGH or LOW State. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	Operating	3.3	3.6	V
		Data Retention Only	1.5	3.6	
V _I	Input Voltage	0		5.5	V
V _O	Output Voltage (HIGH or LOW State) (3-State)	0		V _{CC}	V
		0		5.5	
I _{OH}	HIGH Level Output Current, V _{CC} = 3.0V – 3.6V			-24	mA
I _{OL}	LOW Level Output Current, V _{CC} = 3.0V – 3.6V			24	mA
I _{OH}	HIGH Level Output Current, V _{CC} = 2.7V – 3.0V			-12	mA
I _{OL}	LOW Level Output Current, V _{CC} = 2.7V – 3.0V			12	mA
T _A	Operating Free-Air Temperature	-40		+85	°C
Δt/ΔV	Input Transition Rise or Fall Rate, V _{IN} from 0.8V to 2.0V, V _{CC} = 3.0V	0		10	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T _A = -40°C to +85°C		Unit
			Min	Max	
V _{IH}	HIGH Level Input Voltage (Note 2.)	2.7V ≤ V _{CC} ≤ 3.6V	2.0		V
V _{IL}	LOW Level Input Voltage (Note 2.)	2.7V ≤ V _{CC} ≤ 3.6V		0.8	V
V _{OH}	HIGH Level Output Voltage	2.7V ≤ V _{CC} ≤ 3.6V; I _{OH} = -100μA	V _{CC} - 0.2		V
		V _{CC} = 2.7V; I _{OH} = -12mA	2.2		
		V _{CC} = 3.0V; I _{OH} = -18mA	2.4		
		V _{CC} = 3.0V; I _{OH} = -24mA	2.2		
V _{OL}	LOW Level Output Voltage	2.7V ≤ V _{CC} ≤ 3.6V; I _{OL} = 100μA		0.2	V
		V _{CC} = 2.7V; I _{OL} = 12mA		0.4	
		V _{CC} = 3.0V; I _{OL} = 16mA		0.4	
		V _{CC} = 3.0V; I _{OL} = 24mA		0.55	

2. These values of V_I are used to test DC electrical characteristics only.

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DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Characteristic	Condition	T _A = -40°C to +85°C		Unit
			Min	Max	
I _I	Input Leakage Current	2.7V ≤ V _{CC} ≤ 3.6V; 0V ≤ V _I ≤ 5.5V		±5.0	μA
I _{OZ}	3-State Output Current	2.7 ≤ V _{CC} ≤ 3.6V; 0V ≤ V _O ≤ 5.5V; V _I = V _{IH} or V _{IL}		±5.0	μA
I _{OFF}	Power-Off Leakage Current	V _{CC} = 0V; V _I or V _O = 5.5V		10	μA
I _{CC}	Quiescent Supply Current	2.7 ≤ V _{CC} ≤ 3.6V; V _I = GND or V _{CC}		10	μA
		2.7 ≤ V _{CC} ≤ 3.6V; 3.6 ≤ V _I or V _O ≤ 5.5V		±10	μA
ΔI _{CC}	Increase in I _{CC} per Input	2.7 ≤ V _{CC} ≤ 3.6V; V _{IH} = V _{CC} - 0.6V		500	μA

AC CHARACTERISTICS (t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω)

Symbol	Parameter	Waveform	Limits				Unit
			T _A = -40°C to +85°C				
			V _{CC} = 3.0V to 3.6V		V _{CC} = 2.7V		
			Min	Max	Min	Max	
f _{max}	Clock Pulse Frequency	1	150				MHz
t _{PLH} t _{PHL}	Propagation Delay CP to On	1	1.5 8.5	8.5 1.5	1.5 9.5	9.5 1.5	ns
t _{PZH} t _{PZL}	Output Enable Time to HIGH and LOW Levels	2	1.5 8.5	8.5 1.5	1.5 9.5	9.5 1.5	ns
t _{PHZ} t _{PLZ}	Output Disable Time from HIGH and LOW Levels	2	1.5 6.5	6.5 1.5	1.5 7.0	7.0 1.5	ns
t _s	Setup Time, HIGH or LOW Dn to CP	1	2.5		2.5		ns
t _h	Hold Time, HIGH or LOW Dn to CP	1	1.5		1.5		ns
t _w	CP Pulse Width, HIGH or LOW	3	3.3		3.3		ns
t _{OSSL} t _{OSLH}	Output-to-Output Skew (Note 3.)			1.0 1.0			ns

3. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSSL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

DYNAMIC SWITCHING CHARACTERISTICS

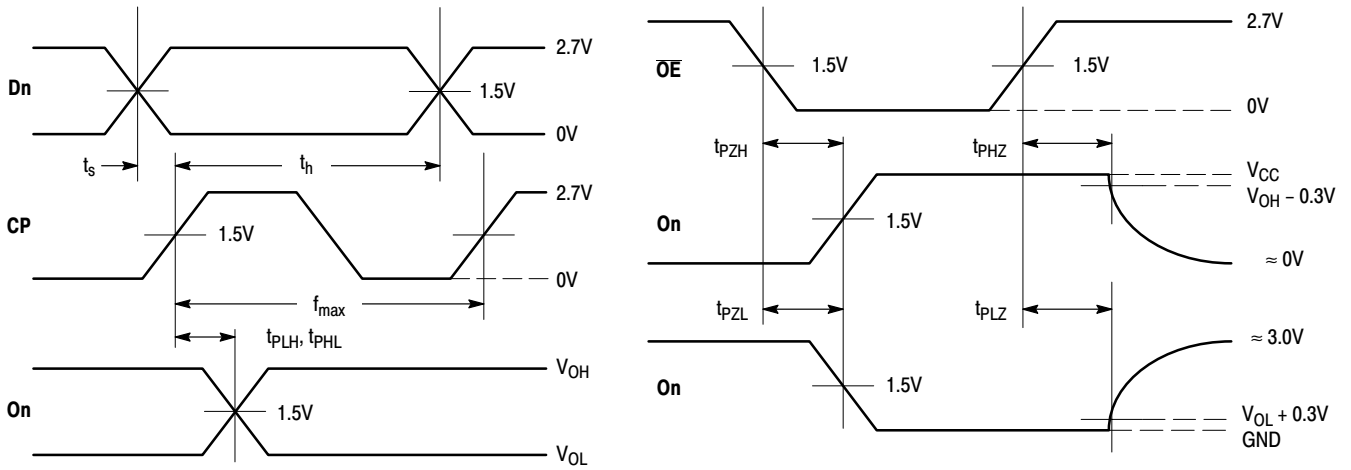
Symbol	Characteristic	Condition	T _A = +25°C			Unit
			Min	Typ	Max	
V _{OLP}	Dynamic LOW Peak Voltage (Note 4.)	V _{CC} = 3.3V, C _L = 50pF, V _{IH} = 3.3V, V _{IL} = 0V		0.8		V
V _{OLV}	Dynamic LOW Valley Voltage (Note 4.)	V _{CC} = 3.3V, C _L = 50pF, V _{IH} = 3.3V, V _{IL} = 0V		0.8		V

4. Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

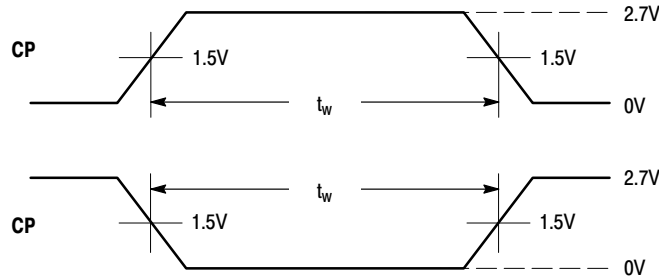
Symbol	Parameter	Condition	Typical	Unit
C _{IN}	Input Capacitance	V _{CC} = 3.3V, V _I = 0V or V _{CC}	7	pF
C _{OUT}	Output Capacitance	V _{CC} = 3.3V, V _I = 0V or V _{CC}	8	pF
C _{PD}	Power Dissipation Capacitance	10MHz, V _{CC} = 3.3V, V _I = 0V or V _{CC}	25	pF

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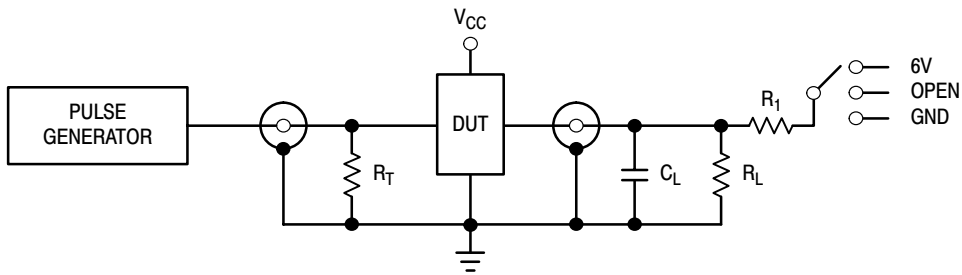
WAVEFORM 1 - PROPAGATION DELAYS, SETUP AND HOLD TIMES
 $t_R = t_F = 2.5\text{ns}$, 10% to 90%; $f = 1\text{MHz}$; $t_W = 500\text{ns}$

WAVEFORM 2 - OUTPUT ENABLE AND DISABLE TIMES
 $t_R = t_F = 2.5\text{ns}$, 10% to 90%; $f = 1\text{MHz}$; $t_W = 500\text{ns}$



WAVEFORM 3 - PULSE WIDTH
 $t_R = t_F = 2.5\text{ns}$ (or fast as required) from 10% to 90%;
 Output requirements: $V_{OL} \leq 0.8\text{V}$, $V_{OH} \geq 2.0\text{V}$

Figure 3. AC Waveforms



TEST	SWITCH
t_{PLH} , t_{PHL}	Open
t_{PZL} , t_{PLZ}	6V
Open Collector/Drain t_{PLH} and t_{PHL}	6V
t_{PZH} , t_{PHZ}	GND

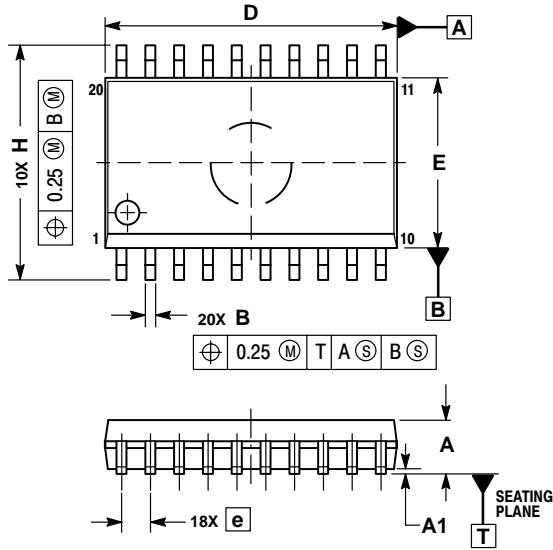
$C_L = 50\text{pF}$ or equivalent (Includes jig and probe capacitance)
 $R_L = R_1 = 500\Omega$ or equivalent
 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 4. Test Circuit

MC74LCX574

OUTLINE DIMENSIONS

DW SUFFIX
 PLASTIC SOIC PACKAGE
 CASE 751D-04
 ISSUE E

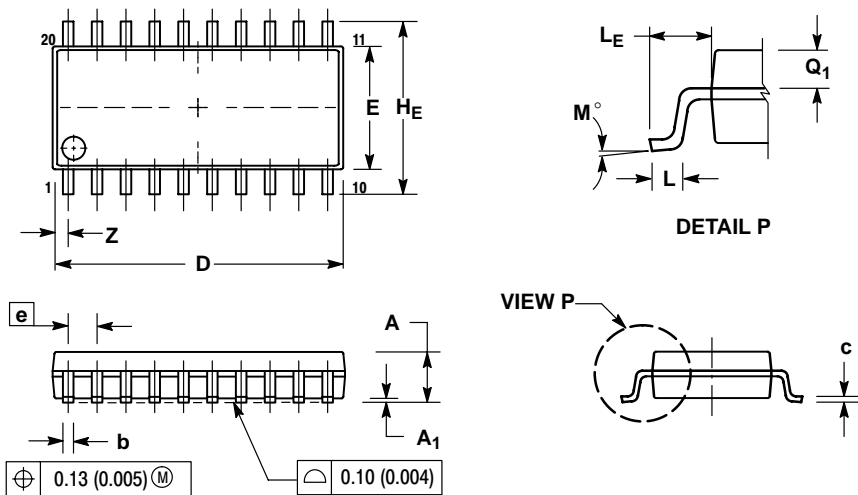


NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
theta	0°	7°

M SUFFIX
 PLASTIC SOIC EIAJ PACKAGE
 CASE 967-01
 ISSUE O



NOTES:

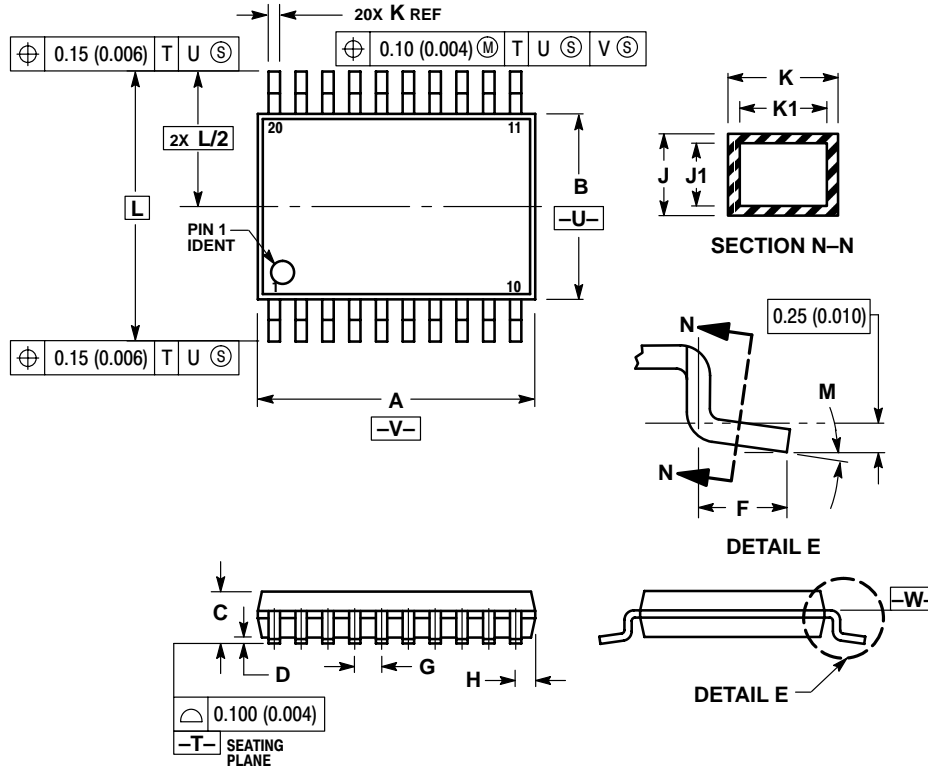
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	12.35	12.80	0.486	0.504
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
HE	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q1	0.70	0.90	0.028	0.035
Z	---	0.81	---	0.032

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OUTLINE DIMENSIONS


DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948E-02
ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

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