### **FEATURES**

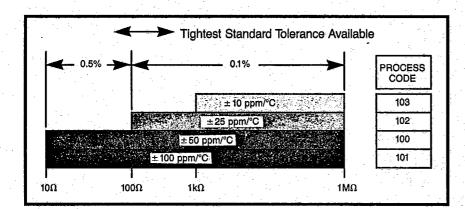
The CTN series of nichrome on silicon, center-tapped, single-value, resistor chips combine excellent stability and power-handling. Two bonding pads per termination allow greater flexibility in hybrid circuit layouts. By connecting to the center-tap, half the value is attainable and by connecting the two values in parallel, one quarter of the value is achieved.

These chips provide the tightest ratio tolerances, best TCR tracking and highest stability between halves available on silicon substrates. They are manufactured using state-of-the-art thin-film techniques, are 100% electrically tested for value, and are visually inspected to Mil-Std-883.

- Center tap feature
- Tight ratio tolerances
- Resistance range  $10\Omega$  to  $1~M\Omega$
- Chip size 30 mil square
- High Stability

- Oxidized silicon substrate for good power dissipation
- Low cost
- · Quick delivery
- Resistor Material NiCr

## TOR WALUES AND TOLERANCES



# ELECTRICAL CHARACTERISTICS

TCR tracking between halves  $(R_A, R_B)$ 

Center tap ratio tolerance, R<sub>A</sub>/R<sub>B</sub>

Noise, MIL-STD-202, Method 308;  $100\Omega$  -  $250~\text{k}\Omega$ 

Stability, 1000 hr., + 125°C, 125 mw

Operating temperature range

Dielectric voltage breakdown

Insulation resistance

Operating voltage

DC power rating at +70°C, (derated to zero at +175°C)

\* 5 ppm/°C for R<100 20 ppm/°C for R<20 ±1 ppm/°C\*

 $\pm 0.01\%$ 

-35 dB max.

 $\pm 0.06\% \Delta R/R$ 

-55°C to +125°C

400 V

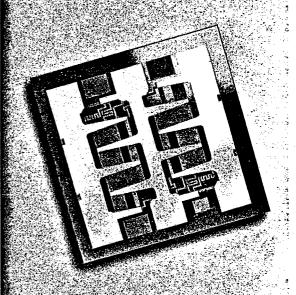
 $10^{12}\Omega$ min.

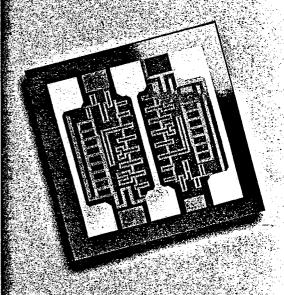
100 V max.

250 mw

# CTN SERIES THIN-FILM CENTER-TAPPED RESISTORS

T-62-05

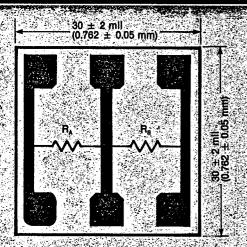




# Semi **[** Films Division

P.O. Box 188
West Hurley, NY 12491
Tel. (914) 338-7714
Fax (914) 338-6329



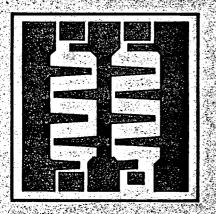


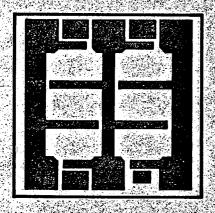
STANDARD CTN CONFIGURATION Six locations: All pads 5 mil x 5 mil

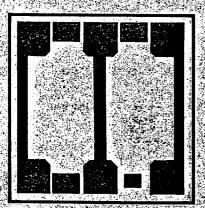
SCHEMATIC

$$R_1 = R_A + R_B$$









■ 3181532 0000173 4 ■ T-62-05

ELECTRO-FILMS INC/ SEMI-24E D

Chip size  $30 \times 30 \pm 2 \text{ mil } (0.762 \times 0.762 \pm 0.05 \text{ mm})$ 

 $8 \pm 3 \text{ mil } (0.203 \pm 0.08 \text{ mm})$ Chip thickness Chip substrate material Oxidized silicon, 10 kÅ min. SiO

Resistor material NiCr.

Bonding pads  $5 \times 5 \, \text{mil} \, (0.127 \times 0.127 \, \text{mm})$ 

No. of pads

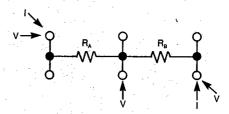
Pad material 10 kÅ min. aluminum, 15 kÅ gold Backing None, lapped semiconductor silicon

OPTIONS: Alphanumeric part marking, up to six characters

Gold backing for eutectic die attach Center-tap ratio tolerances to 0.01%

The CTN center-tapped resistor chips are used mainly in feedback circuits of amplifiers, where ratio matching and tracking between two resistors is critical.

For low values the resistance of the six bonding-pad configurations can vary, depending on the method of measurement used. SEMI-FILMS measures low-value resistors by the four-wire Kelvin technique. The measuring method illustrated here is critical for resistors of less than  $100\Omega$ :



Two probes for Kelvin sensing are used on diagonally opposite bonding pads.

Example: 100% visualled,  $10k\Omega$ ,  $\pm 1\%$ ,  $\pm 100$  ppm TCR P/N: CTR - 101 1000 **Product Family** Tolerance Code: 0.05% Multiplier Code: **ABCDFGHJK** Process Code 0.1% 0.0001 See MATRIX table 0.2% CBA0123 0.001 0.5% 0.01 1% 2% 2.5% Value: Use first four significant digits 5% of the Resistance (Rt) 100 10% 100Č 25% Inspection/Packaging 50%

Use – W for 100% visually inspected parts
X for sample, visually inspected loaded in matrix trays (4% AQL)
Y for sample, visually inspected die loaded in vials (4% AQL)