BUF-02

HIGH-SPEED BIFET BUFFER/VOLTAGE FOLLOWER

FEATURES

- **Output Error Fully Specified ..... 1.5mV Maximum**
- **Low Input Offset Voltage ..... 1.0mV Maximum**
- **Pin Compatible with LM110 in Unnulled Applications**
- **Low Gain Error 0.001%**
- **High Gain ..... 0.9999 V/V Minimum**
- **Excellent Power Supply Rejection Ratio ..... 100dB Typical**
- **Low Output Impedance ..... 0.03Ω Typical**
- **High Slew Rate ..... 24V/μs Typical**
- **Very Low Input Current ..... 0.3nA Maximum**

GENERAL DESCRIPTION

The BUF-02 is the first high-speed voltage follower tested and guaranteed with a Maximum Output Error specification. Comprised of a wide array of input and output loads and input voltage test conditions, this specification assures that the BUF-02 will drive a 10kΩ load over a ±10V output voltage range with less than 1.5mV error referred to the input. Pin compatible with the LM110 in unnulled applications, the BUF-02 features low output impedance (0.03Ω typical), high gain, and excellent power supply rejection (100dB typical) with very low input bias current.

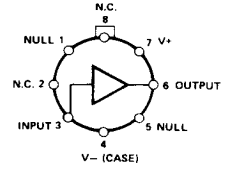
ORDERING INFORMATION†

$T_A = 25°C$ V_{OS} MAX (mV)	PACKAGE TO-99 8-PIN	PACKAGE HERMETIC DIP 8-PIN	OPERATING TEMP. RANGE
1.5	BUF02AJ*	BUF02AZ*	MIL
1.5	BUF02EJ	BUF02EZ	COM
4.0	BUF02BJ*	BUF02BZ*	MIL
4.0	BUF02FJ	BUF02FZ	COM

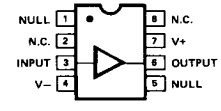
* Also available with MIL-STD-883B processing. To order add/883 as a suffix to the part number.

† All listed parts are available with 160 hour burn-in. See Ordering Information, Section 2.

PIN CONNECTIONS

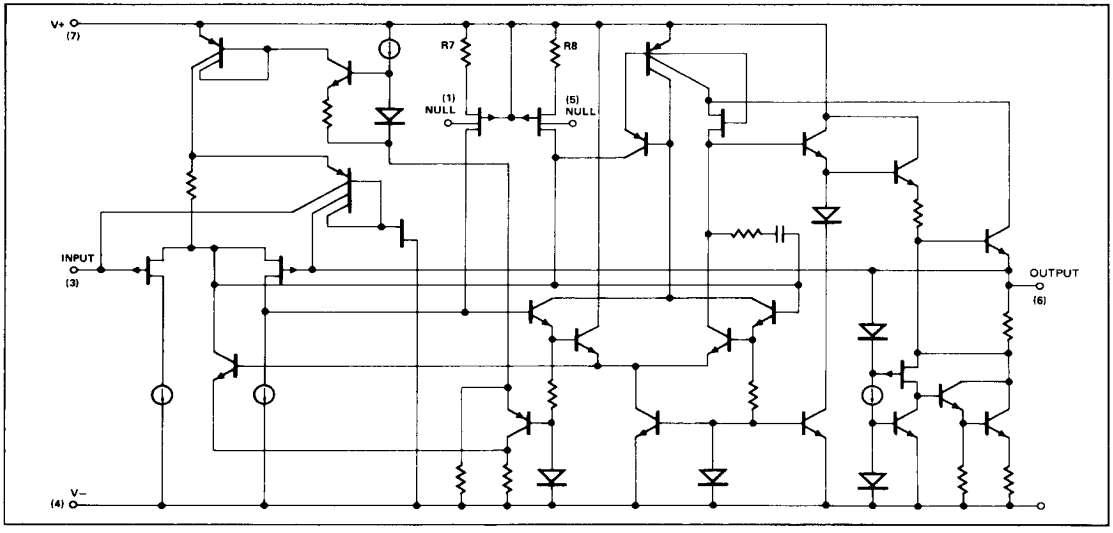


TO-99 (J-SUFFIX)



8-PIN HERMETIC DIP (Z-SUFFIX)

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±18V
Internal Power Dissipation (Note 1) 500mW
Input Voltage (Note 2) ..... ±15V
Output Short Circuit Duration ..... Indefinite
Storage Temperature Range ..... −65°C to +150°C
Operating Temperature Range
BUF-02A, BUF-02B ..... −25°C to +125°C
BUF-02E, BUF-02F ..... 0°C to +70°C
Lead Temperature Range (Soldering 60 sec.) ..... 300°C

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (J)	80°C	7.1mW/°C
8-Pin Hermetic Dip (Z)	75°C	6.7mW/°C

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	BUF-02A BUF-02E MIN	BUF-02A BUF-02E TYP	BUF-02A BUF-02E MAX	BUF-02B BUF-02F MIN	BUF-02B BUF-02F TYP	BUF-02B BUF-02F MAX	UNITS
Maximum Output Error	OUT_{error}	$V_{IN} = +10V, 0V, -10V$ $R_S = 0$ to 20kΩ $R_L \geq 10k\Omega$, in all combinations.	—	0.8	1.5	—	1.5	4.0	mV
Input Offset Voltage	V_{OS}	$V_{IN} = 0V$, $R_S \leq 50\Omega$	—	0.5	1.0	—	1.0	3.0	mV
Input Current	I_{IN}	(Note 4)	—	0.1	0.2	—	0.2	0.5	nA
Input Resistance	R_{IN}		—	10^{12}	—	—	10^{12}	—	Ω
Large Signal Voltage Gain Error	A_{VE}	$R_L \geq 10k\Omega$, $\Delta V_{IN} = \pm 10V$	—	0.001	0.015	—	0.001	0.04	%
Output Resistance	R_O		—	0.03	—	—	0.03	—	Ω
Input Voltage Range	V_{IN}		±10.5	±11.5	—	±10.5	±11.5	—	V
Input Noise Voltage Density	e_n	$R_S = 100\Omega$, f = 100Hz	—	15	—	—	15	—	$nV/\sqrt{Hz}$
Input Noise Current Density	i_n	f = 100Hz	—	0.01	—	—	0.01	—	$pA/\sqrt{Hz}$
Slew Rate	SR	$R_L \geq 10k\Omega$ (Note 3)	12	24	—	9.0	18	—	V/μs
Power Consumption	P_d	$V_O = 0V$	—	150	210	—	160	240	mW
Output Current		$-5V \leq V_O \leq +5V$	—	10	—	—	10	—	mA
Power Supply Rejection	PSRR	$\pm 10V \leq V_S \leq \pm 15V$	—	10	57	—	20	63	μV/V
Settling Time	t_s	$\Delta V_{IN} = 10V$, to 0.1% $\Delta V_{IN} = 10V$, to 0.02%	— —	0.7 1.5	— —	— —	0.7 1.5	— —	μs

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-25°C \leq T_A \leq +125°C$ for BUF-02A and BUF-02B, and for $0°C \leq T_A \leq +70°C$ for BUF-02E and BUF-02F, unless otherwise noted. (Note 5)

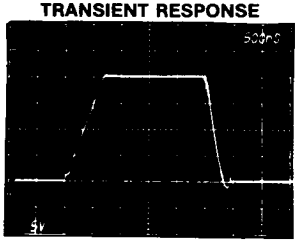
PARAMETER	SYMBOL	CONDITIONS	BUF-02A BUF-02E MIN	BUF-02A BUF-02E TYP	BUF-02A BUF-02E MAX	BUF-02B BUF-02F MIN	BUF-02B BUF-02F TYP	BUF-02B BUF-02F MAX	UNITS
Maximum Output Error	OUT_{error}	$V_{IN} = +10V, 0V, -10V$; $R_S = 0$ to 20kΩ $R_L \geq 10k\Omega$ in all combinations.	—	1.0	2.5	—	2.0	6.0	mV
Input Offset Voltage	V_{OS}	$V_{IN} = 0V$, $R_S = 50\Omega$	—	0.7	1.5	—	1.5	5.0	mV
Large Signal Voltage Gain Error	A_{VE}	$R_L \geq 10k\Omega$, $\Delta V_{IN} = \pm 10V$	—	0.01	0.025	—	0.01	0.06	%
Average Input Offset Voltage Drift	TCV_{OS}	$R_S = 50\Omega$	—	2.0	—	—	5.0	—	μV/°C
Change in Input Offset Drift with V_{OS} Adjust	$\frac{\Delta TCV_{OS}}{\Delta V_{OS}}$	$R_S = 50\Omega$	—	0.5	—	—	0.5	—	$\frac{\mu V/°C}{mV}$
Input Current	I_{IN}	$T_A \leq 125°C$ (Note 4) $T_A \leq 70°C$ (Note 4)	— —	3 0.4	10 1.0	— —	8 0.8	25 2.0	nA
Input Voltage Range	V_{IN}		±10.4	±11.3	—	±10.4	±11.3	—	V
Power Supply Rejection Ratio	PSRR	$\pm 10V \leq V_S \leq \pm 15V$	—	16	100	—	32	200	μV/V
Power Consumption	Pd	$V_O = 0V$	—	180	240	—	190	270	mW

NOTES:

1. See table for maximum ambient temperature rating and derating factor.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Parameter is guaranteed by design.
4. The input bias currents are junction leakage currents which approximately double for every 18°C increase in the junction temperature. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_d
5. Military grade devices are tested at 0°C ambient temperature. This is equivalent to a −25°C ambient temperature test with the device warmed up.

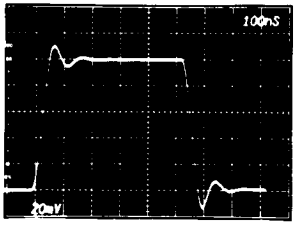
TYPICAL PERFORMANCE CURVES

LARGE-SIGNAL TRANSIENT RESPONSE



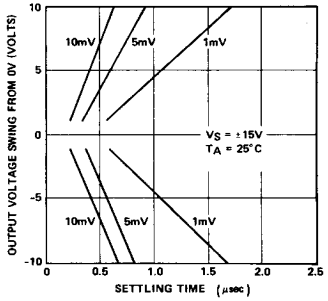
$V_S = \pm 15V, T_A = 25°C$

SMALL-SIGNAL TRANSIENT RESPONSE

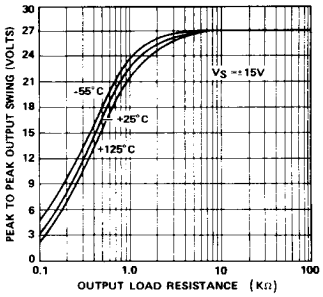


$V_S = \pm 15V, T_A = 25°C$

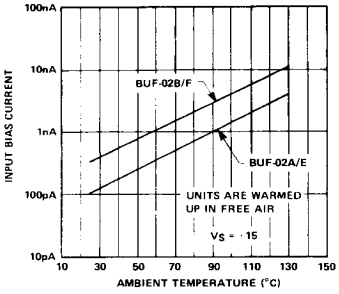
SETTLING TIME vs STEP SIZE



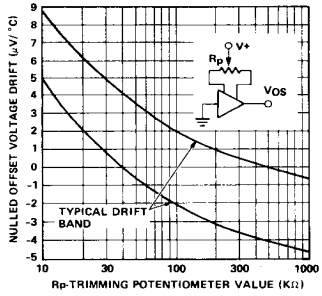
OUTPUT VOLTAGE vs LOAD RESISTANCE



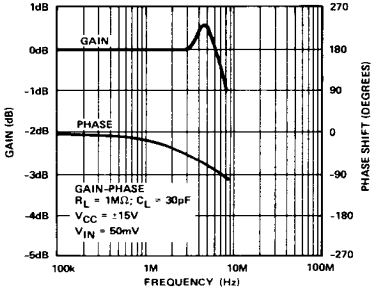
INPUT CURRENT vs AMBIENT TEMPERATURE



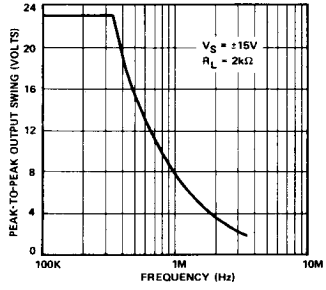
OFFSET VOLTAGE vs TEMPERATURE OF REPRESENTATIVE UNITS



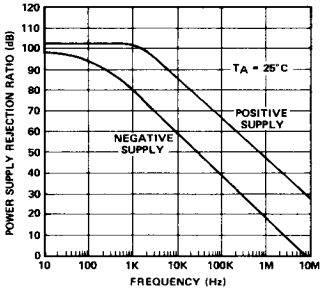
SMALL SIGNAL FREQUENCY RESPONSE



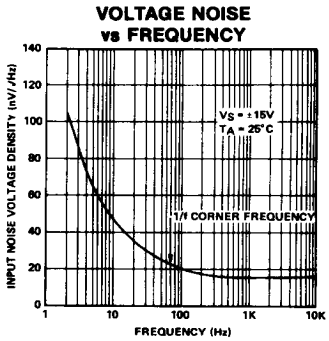
LARGE SIGNAL FREQUENCY RESPONSE



POWER SUPPLY REJECTION vs FREQUENCY

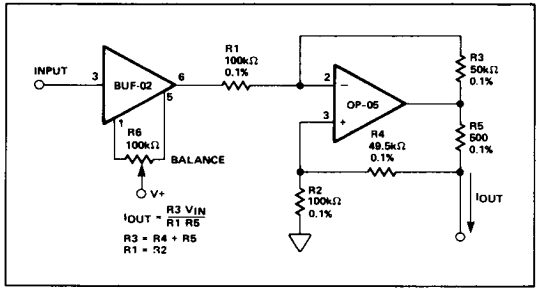


TYPICAL PERFORMANCE CURVES

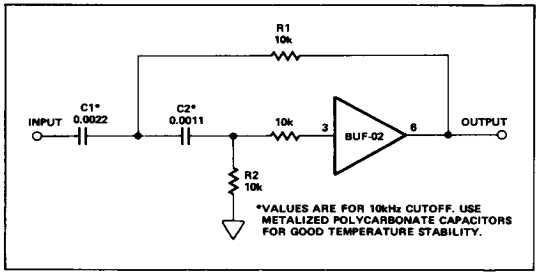


TYPICAL APPLICATIONS

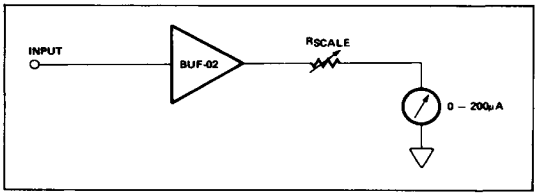
BILATERAL CURRENT SOURCE



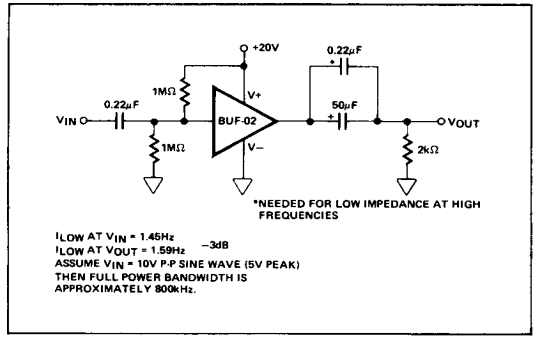
SECOND-ORDER HIGH-PASS ACTIVE FILTER



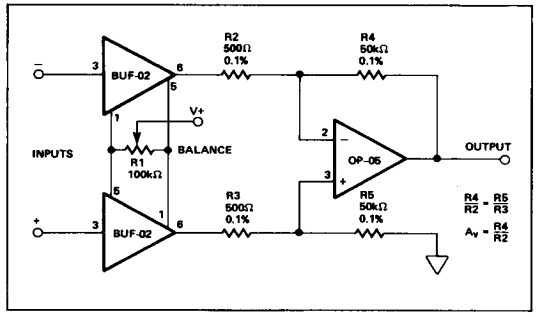
HIGH IMPEDANCE METER DRIVER



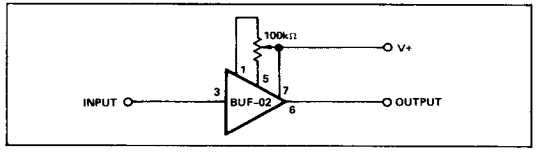
HIGH-SPEED SINGLE-SUPPLY AC BUFFER



DIFFERENTIAL INPUT INSTRUMENTATION AMPLIFIER



OPTIONAL OFFSET NULLING CIRCUIT



MAXIMUM OUTPUT ERROR

The **Maximum Output Error** specification combines errors introduced by offset voltage, input bias current, gain, CMRR and device output impedance. The specification is 100% tested for a given combination of source resistance, load resistance and input voltages. The tedious chore of performing a worst case summation of component error terms is not necessary.

The individual parameters of offset voltage, input current, voltage gain and PSRR are also given.

It should be noted that an error analysis may yield a figure higher than the Maximum Output Error specification. This is due to the potential cancellation of the effects of one error source by another. In situations such as this, the Maximum Output Error specification supersedes results from any error analysis.