UMC

T-46-23-14

UM62256 Series

32K× 8 CMOS SRAM

Standard SRAM

Features

- Single +5 volt power supply
- Access times: 100/120/150 ns (max.)
- Current:
  - Standard version: Operating: 70 mA (max.)
    Standby: 2 mA (max.)
  - Low power version: Operating: 70 mA (max.)
    Standby: 100 μA (max.)
- Fully static operation, no clock or refreshing required
- Directly TTL compatible: All inputs and outputs
- Common I/O using three-state output.
- Data retention voltage: 2V (min.) for low power version
- Available in 28 pin DIP or SOP packages (See ordering information)

General Description

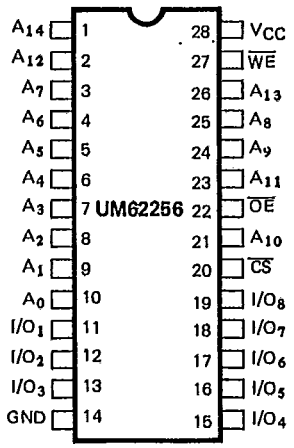
The UM62256 is a high-speed, low-power 262,144-bit static random access memory organized as 32,768 words by 8 bits and operates on a single 5-volt power supply. It is built using UMC's high performance CMOS process.

Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

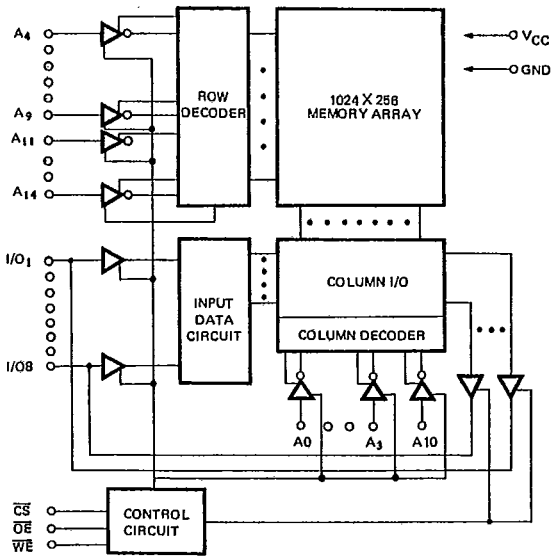
Minimum standby power is drawn by this device when $\overline{CS}$ is at a high level, independent of the other input levels.

Data retention is guaranteed at a power supply voltage as low as 2V for the low power version.

Pin Configuration



Block Diagram



Pin Description

Designation	Description
$A_0 - A_{14}$	Address Input
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{CS}$	Chip Select
$I/O_1 - I/O_8$	Data Input/Output
V_{CC}	Power Supply (+5V)
GND	Ground

Recommended DC Operating Conditions

(T_A = 0°C to +70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	3.5	V_{CC} + 0.5V	V
V_{IL}	Input Low Voltage	−0.3	0	+0.8	V
C_L	Output Load	—	—	100	pF
TTL	Output Load	—	—	1	—

Absolute Maximum Ratings*

V_{CC} to GND ..... −0.5V to +7.0V
IN, IN/OUT Volt to GND ..... −0.5V to V_{CC} +0.5V
Operating Temperature, T_{opr} ..... 0°C to +70°C
Storage Temperature, T_{stg} ..... −55°C to +125°C
Temperature Under Bias, T_{bias} ..... −10°C to +85°C
Power Dissipation, P_T 1.0W/SOP 0.7W
Soldering Temp. & Time ..... 206°C, 10 sec

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

(T_A = 0°C to +70°C, V_{CC} = 5V ± 10%, GND = 0V)

Symbol	Parameter	UM62256-10/12/15		UM62256-10L/12L/15L		Unit	Test Conditions
		Min.	Max.	Min.	Max.		
$\|I_{LI}\|$	Input Leakage Current	—	2	—	2	μA	V_{IN} = GND to V_{CC}
$\|I_{LO}\|$	Output Leakage Current	—	2	—	2	μA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = GND to V_{CC}
I_{CC}	Active Power Supply Current	—	70	—	70	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA
I_{CC1}	Dynamic Operating Current	—	70	—	70	mA	Min. Cycle, Duty = 100% $\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA
I_{SB}	Standby Power Supply Current	—	5	—	3	mA	$\overline{CS}$ = V_{IH}
I_{SB1}		—	2	—	0.1	mA	$\overline{CS}$ ≥ V_{CC} − 0.2, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V
V_{OL}	Output Low Voltage	—	0.4	—	0.4	V	I_{OL} = 4 mA
V_{OH}	Output High Voltage	2.4	—	2.4	—	V	I_{OH} = −1.0 mA

Truth Table

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O Operation	Supply Current
Standby	H	X	X	High Z	I_{SB}, I_{SB1}
Output Disable	L	H	H	High Z	I_{CC}, I_{CC1}
Read	L	L	H	D_{OUT}	I_{CC}, I_{CC1}
Write	L	X	L	D_{IN}	I_{CC}, I_{CC1}

Note: X : H or L

Capacitance (T_A = 25°C, f = 1.0 MHz)

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
C_{IN}*	Input Capacitance		6	pF	V_{IN} = 0V
$C_{I/O}$*	Input/Output Capacitance		8	pF	$V_{I/O}$ = 0V

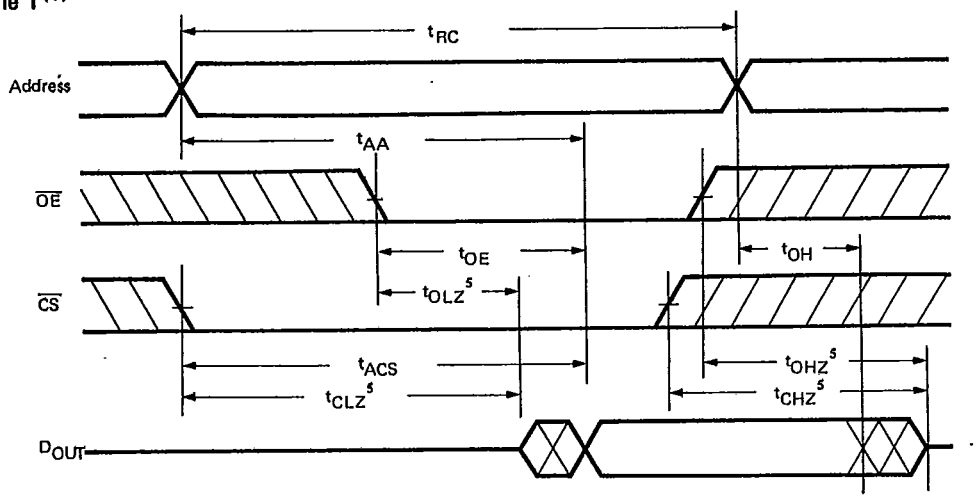
* This parameter is sampled and not 100% tested.

AC Characteristics (T_A = 0°C to +70°C, V_{CC} = 5V ± 10%)

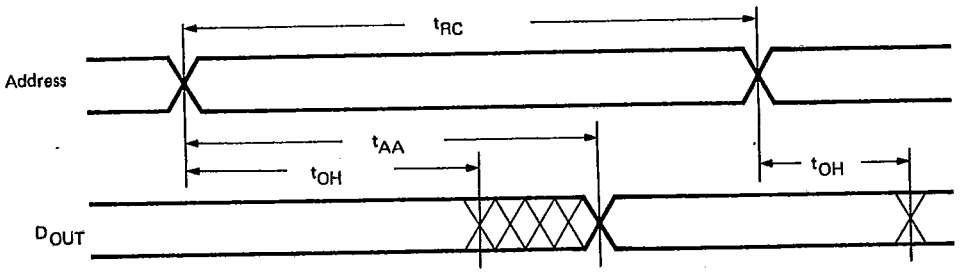
Symbol	Parameter	UM62256-10 UM62256-10L Min.	Max.	UM62256-12 UM62256-12L Min.	Max.	UM62256-15 UM62256-15L Min.	Max.	Unit
Read Cycle								
t_{RC}	Read Cycle Time	100	–	120	–	150	–	ns
t_{AA}	Address Access Time	–	100	–	120	–	150	ns
t_{ACS}	Chip Select Access Time	–	100	–	120	–	150	ns
t_{OE}	Output Enable to Output Valid	–	50	–	60	–	70	ns
t_{CLZ}	Chip Selection to Output in Low Z	10	–	10	–	10	–	ns
t_{OLZ}	Output Enable to Output in Low Z	5	–	5	–	5	–	ns
t_{CHZ}	Chip Deselection to Output in High Z	0	35	0	40	0	50	ns
t_{OHZ}	Output Disable to Output in High Z	0	35	0	40	0	50	ns
t_{OH}	Output Hold from Address Change	10	–	10	–	10	–	ns
Write Cycle								
t_{WC}	Write Cycle Time	100	–	120	–	150	–	ns
t_{CW}	Chip Selection to End of Write	80	–	85	–	100	–	ns
t_{AS}	Address Set up Time	0	–	0	–	0	–	ns
t_{AW}	Address Valid to End of Write	80	–	85	–	100	–	ns
t_{WP}	Write Pulse Width	60	–	70	–	90	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	ns
t_{WHZ}	Write to Output in High Z	0	35	0	40	0	50	ns
t_{DW}	Data to Write Time Overlap	40	–	50	–	60	–	ns
t_{DH}	Data Hold from Write Time	0	–	0	–	0	–	ns
t_{OHZ}	Output Disable to Output in High Z	0	35	0	40	0	50	ns
t_{OW}	Output Active from End of Write	10	–	10	–	10	–	ns

Timing Waveforms

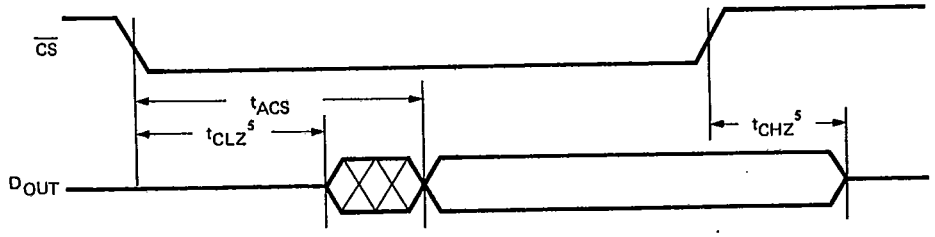
Read Cycle 1 (1)



Read Cycle 2 (1, 2, 4)



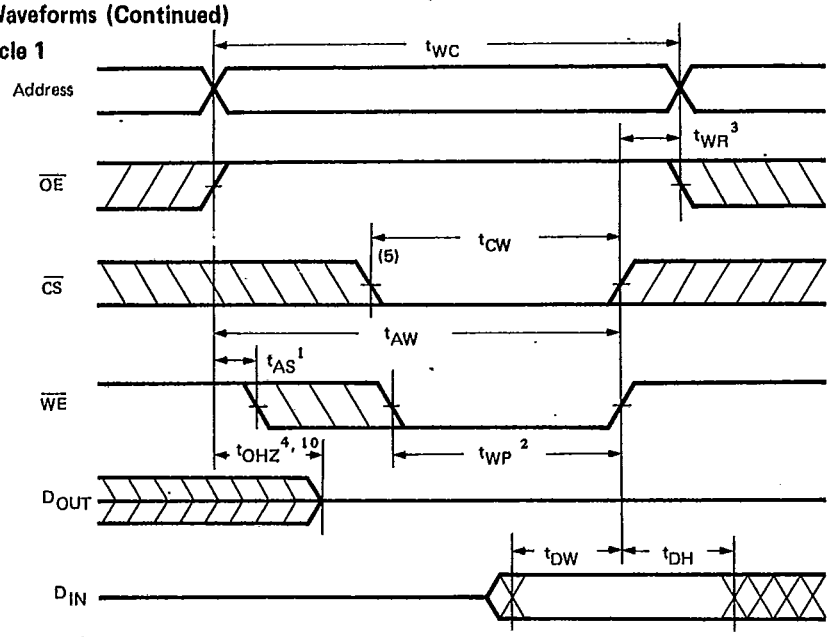
Read Cycle 3 (1, 3, 4)



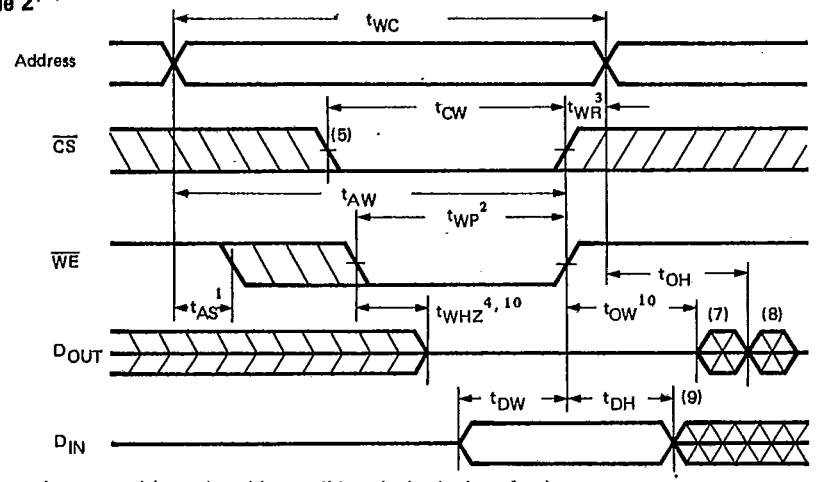
Notes: 1. $\overline{WE}$ is High for Read Cycle,
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured ± 500mV from steady state. This parameter is sampled and not 100% tested.

Timing Waveforms (Continued)

Write Cycle 1



Write Cycle 2 (6)



Notes:
1. t_{AS} is measured from the address valid to the beginning of write.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Data input signals of opposite phase to the outputs must not be applied to I/O pins.
10. Transition is measured ± 500mV from steady state. This parameter is sampled and not 100% tested.

AC Test Conditions

Input Pulse Levels	0.8V to 2.2V
Input Rise and Fall Times	5 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1, 2

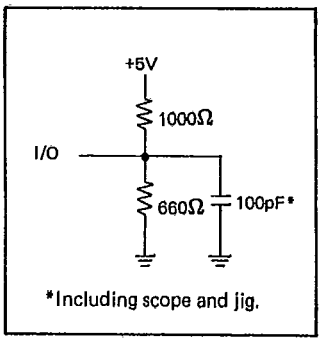


Figure 1. Output Load

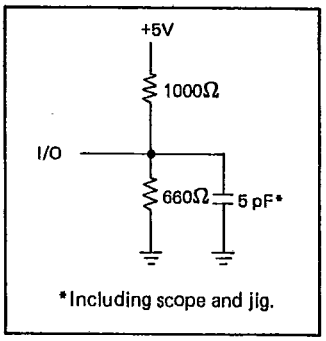


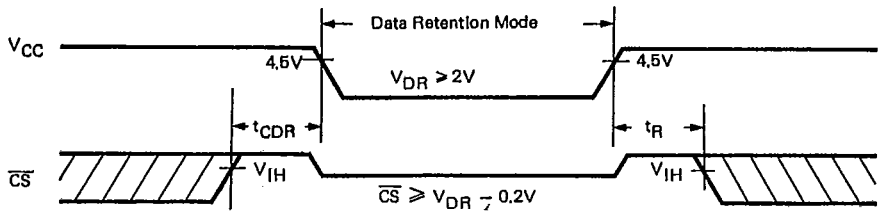
Figure 2. Output Load for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, and t_{OW}

Data Retention Characteristics (T_A = 0°C to +70°C; L version only)

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{DR}	V_{CC} for Data Retention	2.0	5.5	V	$\overline{CS} \geq V_{CC} - 0.2V$
I_{CCDR}	Data Retention Current	–	50	μA	V_{CC} = 3.0V, $\overline{CS} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$
t_{CDR}	Chip Deselect to Data Retention Time	0	–	ns	See Retention Waveform
t_R	Operation Recovery Time	t_{RC}*	–	ns	

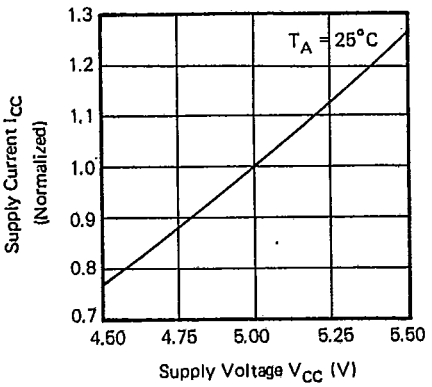
*t_{RC} = Read Cycle Time

Timing Waveform Low V_{CC} Data Retention Waveform

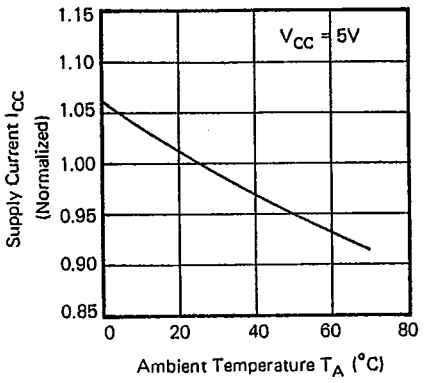


Characteristic Curves

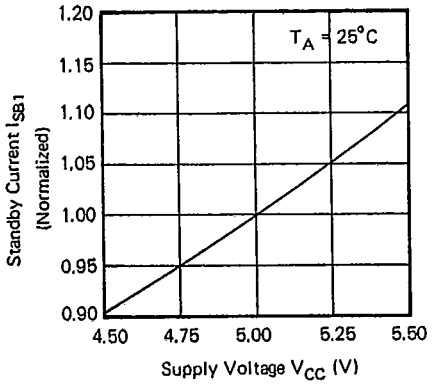
I_{CC} vs. V_{CC}



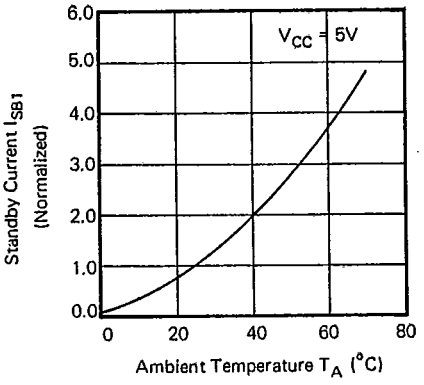
I_{CC} vs. T_A



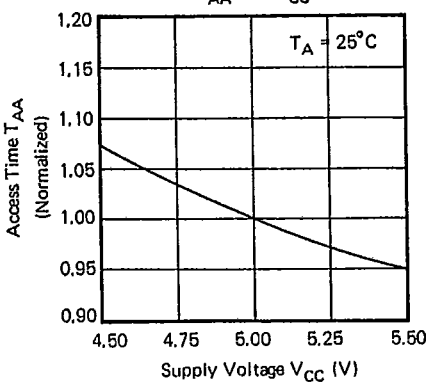
I_{SB1} vs. V_{CC}



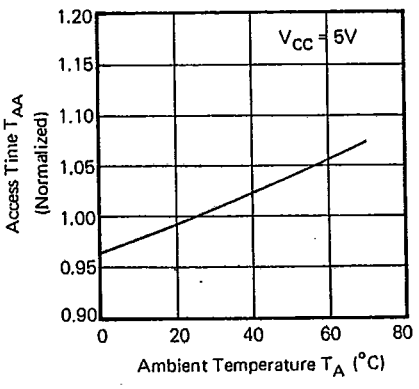
I_{SB1} vs. T_A



T_{AA} vs. V_{CC}



T_{AA} vs. T_A



Standard SRAM

Ordering Information

Part No.	Access Time (ns)	Operating Current Max. (mA)	Standby Current Max. (mA)	Package
UM62256-10	100 ns	70	2	28L DIP
UM62256-10L	100 ns	70	0.1	28L DIP
UM62256M-10	100 ns	70	2	28L SOP
UM62256M-10L	100 ns	70	0.1	28L SOP
UM62256-12	120 ns	70	2	28L DIP
UM62256-12L	120 ns	70	0.1	28L DIP
UM62256M-12	120 ns	70	2	28L SOP
UM62256M-12L	120 ns	70	0.1	28L SOP
UM62256-15	150 ns	70	2	28L DIP
UM62256-15L	150 ns	70	0.1	28L DIP
UM62256M-15	150 ns	70	2	28L SOP
UM62256M-15L	150 ns	70	0.1	28L SOP