UHF/VHF remote control receiver UAA3201T

FEATURES

- Oscillator with external SAW resonator
- Wide frequency range: 150 to 450 MHz
- High sensitivity
- Low power consumption
- Automotive temperature range
- Superheterodyne architecture
- Applicable to fulfil FTZ17TR2100
- High integration level, few external components
- Inexpensive external components
- IF-filter bandwidth determined by application.

APPLICATIONS

- Car alarm systems
- Remote control systems
- Security systems
- Gadgets, toys
- Telemetry.

GENERAL DESCRIPTION

The UAA3201T is a fully integrated single chip receiver, primarily intended for use in VHF and UHF systems employing direct AM Return-to-Zero (RZ) Amplitude Shift Keying (ASK) modulation.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		3.5	–	6.0	V
I_{CC}	supply current		–	3.4	4.8	mA
P_{ref}	sensitivity	f_i = 433.92 MHz; data rate 250 bits/s; BER $\leq 3 \times 10^{-2}$	–	–	−105	dBm
T_{amb}	operating ambient temperature		−40	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UAA3201T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

BLOCK DIAGRAM

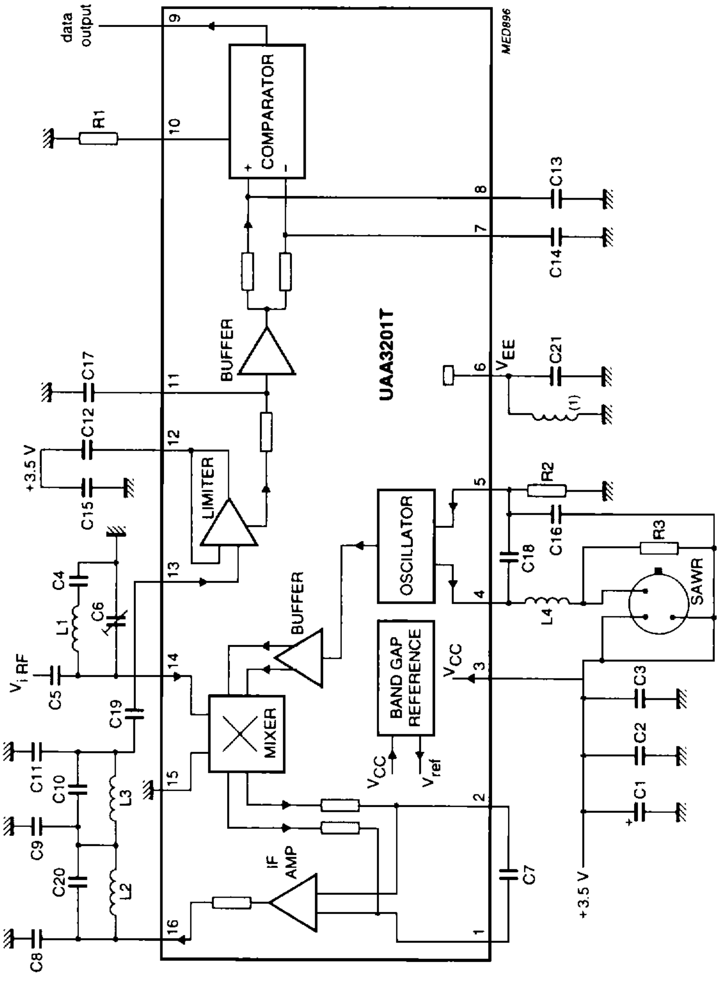


Fig.1 Block diagram, test and application circuit (f_i = 433.92 MHz); see Table 1.

(1) Stray inductance: see Chapter "Layout of printed circuit board for test circuit (f_i = 433.92 MHz)".

Table 1 Application component list for Fig.1

COMPONENT	VALUE	TOLERANCE	DESCRIPTION
R1	27 kΩ	±2%	TC = +50 ppm/K
R2	680 Ω	±2%	TC = +50 ppm/K
R3	220 Ω	±2%	TC = +50 ppm/K
C1	4.7 µF	±20%	–
C2	150 pF	±10%	TC = 0 ±30 ppm/K; tan $\delta \leq 10 \times 10^{-4}$; f = 1 MHz
C3	1 nF	±10%	TC = 0 ±30 ppm/K; tan $\delta \leq 10 \times 10^{-4}$; f = 1 MHz
C4	820 pF	±10%	TC = 0 ±30 ppm/K; tan $\delta \leq 10 \times 10^{-4}$; f = 1 MHz
C5	3.3 pF	±10%	TC = 0 ±150 ppm/K; tan $\delta \leq 30 \times 10^{-4}$; f = 1 MHz
C6	2.5 to 6 pF	–	TC = 0 ±300 ppm/K; tan $\delta \leq 20 \times 10^{-4}$; f = 1 MHz
C7	56 pF	±10%	TC = 0 ±30 ppm/K; tan $\delta \leq 10 \times 10^{-4}$; f = 1 MHz
C8	150 pF	±10%	TC = 0 ±30 ppm/K; tan $\delta \leq 10 \times 10^{-4}$; f = 1 MHz
C9	220 pF	±10%	TC = 0 ±30 ppm/K; tan $\delta \leq 10 \times 10^{-4}$; f = 1 MHz
C10	27 pF	±10%	TC = 0 ±30 ppm/K; tan $\delta \leq 20 \times 10^{-4}$; f = 1 MHz
C11	150 pF	±10%	TC = 0 ±30 ppm/K; tan $\delta \leq 10 \times 10^{-4}$; f = 1 MHz
C12	100 nF	±10%	tan $\delta \leq 25 \times 10^{-3}$; f = 1 kHz
C13	2.2 nF	±10%	tan $\delta \leq 25 \times 10^{-3}$; f = 1 kHz
C14	33 nF	±10%	tan $\delta \leq 25 \times 10^{-3}$; f = 1 kHz
C15	150 pF	±10%	TC = 0 ±30 ppm/K; tan $\delta \leq 10 \times 10^{-4}$; f = 1 MHz
C16	3.9 pF	±10%	TC = 0 ±150 ppm/K; tan $\delta \leq 30 \times 10^{-4}$; f = 1 MHz
C17	10 nF	±10%	tan $\delta \leq 25 \times 10^{-3}$; f = 1 kHz
C18	3.3 pF	±10%	TC = 0 ±150 ppm/K; tan $\delta \leq 30 \times 10^{-4}$; f = 1 MHz
C19	68 pF	±10%	TC = 0 ±30 ppm/K; tan $\delta \leq 10 \times 10^{-4}$; f = 1 MHz
C20	6.8 pF	±10%	TC = 0 ±150 ppm/K; tan $\delta \leq 30 \times 10^{-4}$; f = 1 MHz
C21	47 pF	±5%	TC = 0 ±30 ppm/K; tan $\delta \leq 10 \times 10^{-4}$; f = 1 MHz
L1	10 nH	±10%	Q_{min} = 50/450 MHz; TC = +25 to +125 ppm/K
L2	330 µH	±10%	Q_{min} = 45/800 kHz; $C_{stray} \leq 1$ pF
L3	330 µH	±10%	Q_{min} = 45/800 kHz; $C_{stray} \leq 1$ pF
L4	33 nH	±10%	Q_{min} = 45/450 MHz; TC = +25 to +125 ppm/K

Table 2 SAWR (Surface Acoustic Wave Resonator) data

DESCRIPTION	SPECIFICATION
Type	one-port (e.g. RFM R02112)
Centre frequency	433.42 MHz ±75 kHz
Maximum insertion loss	1.5 dB
Typical loaded Q	1600 (50 Ω load)
Temperature drift	0.032 ppm/K^2
Turnover temperature	43 °C

PINNING

SYMBOL	PIN	DESCRIPTION
MON	1	negative mixer output
MOP	2	positive mixer output
V_{CC}	3	positive supply voltage
OSC	4	oscillator collector
OSE	5	oscillator emitter
V_{EE}	6	negative supply voltage
CPB	7	comparator input B
CPA	8	comparator input A
DATA	9	data output
CPO	10	comparator offset adjustment
CPC	11	comparator input C
LFB	12	limiter feedback
LIN	13	limiter input
MIXIN	14	mixer input
V_{EM}	15	negative supply voltage for mixer
FA	16	output to elliptic filter

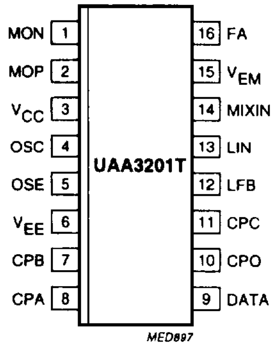


Fig.2 Pin configuration.

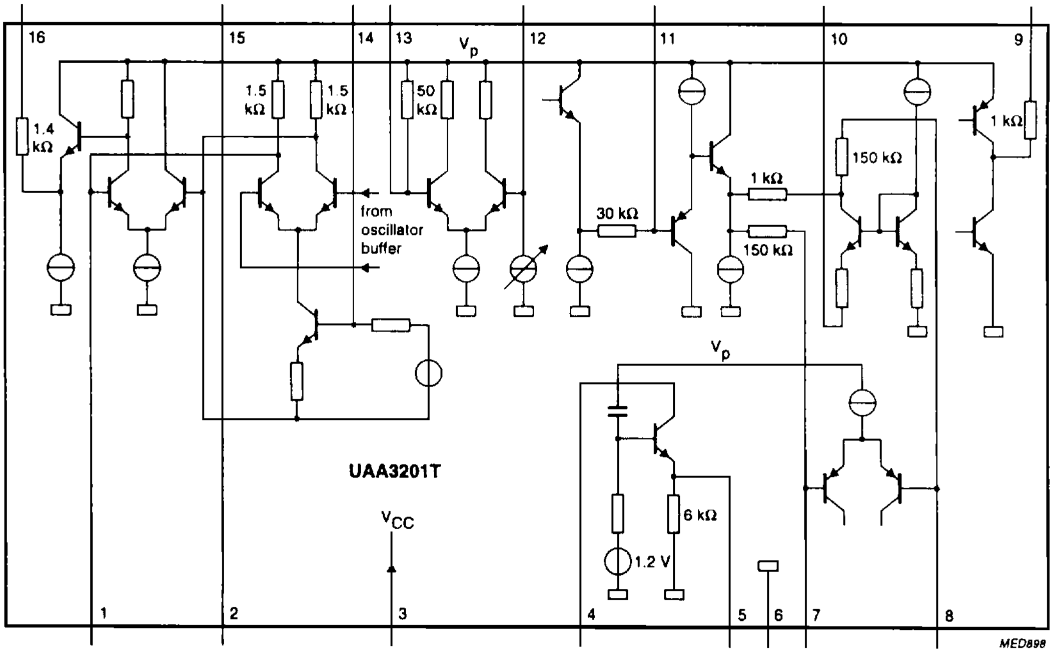


Fig.3 Internal circuits.

FUNCTIONAL DESCRIPTION

The RF signal is fed directly into the mixer stage where it is mixed down to nominal 500 kHz IF by the integrated SAWR controlled oscillator. The IF signal is then passed to the IF amplifier which increases the level. A 5th order elliptic low-pass filter acts as the main IF filtering. The output voltage of that filter is demodulated by a limiting amplifier that rectifies the incoming IF. The demodulated signal passes two RC filter stages and is then limited by a data comparator which makes it available at the data output pin.

Mixer

The mixer is a single balanced emitter coupled pair with internally set bias current. The optimum impedance is 320 Ω at 430 MHz. Capacitor C5 is used to transform a 50 Ω generator impedance to the optimum value.

Oscillator

The oscillator consists of a transistor in common base configuration and a tank circuit including the SAWR. R2 is used to control the bias current through the transistor. R3 is required to reduce unwanted responses of the tank circuit.

IF amplifier

The IF amplifier is a differential input, single ended output emitter coupled pair. It is used to decouple the first and the second IF filter and to provide some additional gain in order to reduce the influence of the noise of the limiter on the total noise figure.

IF filters

The first IF filter is an RC filter formed by internal resistors and an external capacitor. The second IF filter is an external elliptic filter. The source impedance is 1.4 kΩ, the load is high impedance. The bandwidth of the IF filter in the given application is 800 kHz due to the centre frequency spread of the SAWR. It may be reduced when SAWRs with less tolerances are used or temperature range requirements are lower. A smaller bandwidth of the filter will yield a higher sensitivity of the receiver. As the RF is mixed down to a low IF there is no image rejection possible.

Limiter

The limiting amplifier consists of three DC-coupled amplifier stages, with a total gain of 60 dB. An RSSI signal is generated by rectifying the IF signal. The limiter has a lower frequency limit of 100 kHz, which can be controlled by C12 and C19, and an upper frequency limit of 3 MHz.

Comparator

The 2 × IF component in the RSSI signal is removed by the first order low-pass capacitor C17. After passing a buffer stage the signal is split into two paths, leading via RC filters to the inputs of a voltage comparator. The time constant of one path (C14) is compared to the bit duration. Consequently the potential at the negative comparator input represents the average magnitude of the RSSI signal, the second path with a short time constant (C13) allows the signal at the positive comparator input to follow the RSSI signal instantaneously. This results in a variable comparator threshold, depending on the field strength of the incoming signal.

Hence the comparator output is switched on, when the RSSI signal exceeds its average value, i.e. when an ASK ON signal is received.

The low-pass filter capacitor C13 rejects the unwanted 2 × IF and reduces the noise bandwidth of the data filter. The resistor R1 is used to set the current of an internal source. This current is drawn from the positive comparator input thereby applying an offset and driving the output into the OFF state during the absence of an input signal. This offset can be increased by lowering the value of R1 yielding a higher noise immunity at the expense of reduced sensitivity.

Band gap reference

The band gap reference controls the biasing of the whole circuit. In this block currents are generated that are constant over temperature and currents that are proportional to absolute temperature.

The current consumption of the receiver rises with increasing temperature, because the blocks with the highest current consumption are biased by currents that are proportional to absolute temperature.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS.	MIN.	MAX.	UNIT
V_{CC}	supply voltage		−0.3	+8.0	V
T_{amb}	operating ambient temperature		−40	+85	°C
T_{stg}	storage temperature		−55	+125	°C
V_{es}	electrostatic handling	note 1			
	pins 4 and 5		−2000	+1500	V
	pins 12 and 14		−1500	+2000	V
	all other pins		−	±2000	V

Note

1. Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

DC CHARACTERISTICS

All voltages referenced to V_{EE}; V_{CC} = 3.5 V; T_{amb} = −40 to +85 °C; typical values for T_{amb} = +25 °C; for test circuit see Fig.1; SAWR disconnected; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		3.5	−	6.0	V
V_{DATA}	data output voltage	I_{DATA} = −10 µA (HIGH); note 1	V_{CC} − 0.5	−	−	V
		I_{DATA} = +200 µA (LOW); note 1	−	−	0.6	V
I_{CC}	supply current	R_2 = 680 Ω	−	3.4	4.8	mA

Note

1. I_{DATA} is defined to be positive when current flows into the DATA pin.

AC CHARACTERISTICS

V_{CC} = 3.5 V; T_{amb} = +25 °C; test circuit (see Fig.1); R1 disconnected; for test board see Figs 10 and 11; for AC test conditions see Section "AC test conditions"; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_{ref}	input sensitivity	BER $\leq 3 \times 10^{-2}$; note 1	–	–	−105	dBm
$P_{i(max)}$	maximum input power	BER $\leq 3 \times 10^{-2}$	–	–	−30	dBm
P_{spur}	spurious radiation	note 2	–	–	−60	dBm
$IP3_{mix}$	intercept point (mixer)		−20	−17	–	dBm
$IP3_{IF}$	intercept point (mixer + IF amplifier)		−38	−35	–	dBm
$P_{1\,dB}$	1 dB compression point (mixer)		−38	−35	–	dBm
t_{on}	receiver turn-on time	note 3	–	–	10	ms

Notes

1. P_{ref} is the maximum available power at the input of the test board. The Bit Error Rate (BER) is measured using the test facility shown in Fig.9.
2. Valid only for the reference PCB (see Figs 10 and 11). Spurious radiation is strongly dependent on the PCB layout.
3. C1 disconnected. The supply voltage V_{CC} is pulsed as explained in the Section "AC test conditions".

TEST INFORMATION

Tuning procedure for AC tests

1. Turn on the signal generator (f_i = 433.92 MHz; no modulation; RF input level = 1 mV).
2. Tune C6, RF stage input, to obtain a peak audio voltage on pin LIN.
3. Check that data is appearing on the data output pin, DATA, and proceed with the AC tests.

AC test conditions

Table 3 Test signals

The reference signal level P_{ref} for the following tests is defined as the minimum input level in dBm to give a BER $\leq 3 \times 10^{-2}$ (e.g. 7.5 bit errors per second for 250 bits/s).

TEST SIGNAL	FREQUENCY (MHz)	DATA SIGNAL	MODULATION	MODULATION INDEX
1	433.92	250 bits/s square wave	RZ signal with duty cycle = 66% for logic 1; RZ signal with duty cycle = 33% for logic 0	100%
2	434.02	–	no modulation	–
3	433.92	–	no modulation	–

Table 4 Test results

P_1 is the maximum available power from signal generator 1 at the input of the test board; P_2 is the maximum available power from signal generator 2 at the input of the test board.

TEST	GENERATOR		RESULT
	1	2	
Maximum input power (see Fig.5)	modulated test signal 1; P_1 = −30 dBm (minimum P_{max})	–	BER ≤ 3×10^{-2} (e.g. 7.5 bit errors per second for 250 bits/s)
Receiver turn-on time; see note 1 and Fig.5	test signal 1; $P_1 = P_{ref} + 10$ dB; error counting is started 10 ms after V_{CC} is switched on	–	check that the first 10 bits are correct
Intercept point (mixer) see note 2 and Fig.6	test signal 3; P_1 = −50 dBm	test signal 2; $P_2 = P_1$	$IP3 = P_1 + \frac{1}{2} \times IM3$ (dB); $IP3 \geq -20$ dBm (minimum $IP3_{mix}$)
Intercept point (mixer + IF amplifier) see note 3 and Fig.6	test signal 3; P_1 = −50 dBm	test signal 2; $P_2 = P_1$	$IP3 = P_1 + \frac{1}{2} \times IM3$ (dB); $IP3 \geq -38$ dBm (minimum $IP3_{IFa}$)
Spurious radiation see note 4 and Fig.7	–	–	no spuriouses (25 MHz – 1 GHz) with level higher than −60 dBm (maximum P_{spur})
1 dB compression point (mixer) see note 5 and Fig.8	test signal 3; P_{11} = −70 dBm; P_{12} = −38 dBm (minimum $P_{1\,dB}$)	–	$(P_{o1} + 70\text{ dB}) - [P_{o2} + 38\text{ dB}$ (minimum $P_{1\,dB})] \leq 1$ dB, where P_{o1}, P_{o2} is the output power for test signals with P_{11} or P_{12}, respectively

Notes

1. The supply voltage V_{CC} of the test circuit alternates between ‘on’ (100 ms) and ‘off’ (100 ms); see Fig.4.
2. Differential probe of spectrum analyser connected to MOP and MON.
3. Probe of spectrum analyser connected to LIN.
4. Spectrum analyser connected to the input of the test board.
5. Probe of spectrum analyser connected to either MOP or MON.

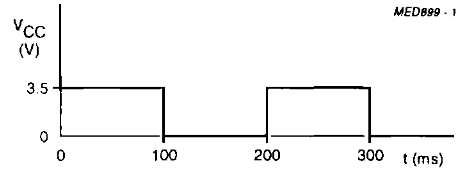
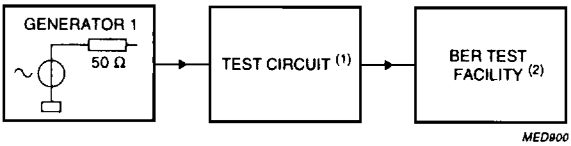


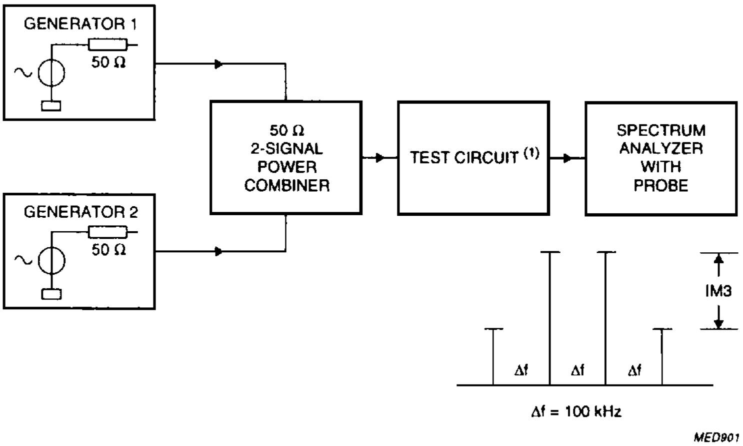
Fig.4 Timing diagram for pulsed supply voltage.



(1) For test circuit see Fig.1.

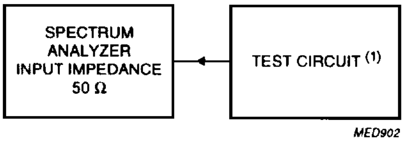
(2) For BER test facility see Fig.9.

Fig.5 Test configuration A (single generator).



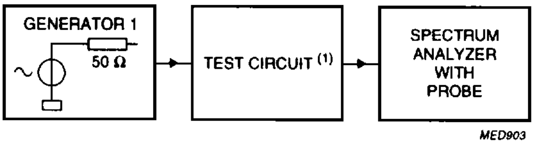
(1) For test circuit see Fig.1.

Fig.6 Test configuration B (IP3).



(1) For test circuit see Fig.1.

Fig.7 Test configuration C (spurious radiation).



(1) For test circuit see Fig.1.

Fig.8 Test configuration D (1 dB compression point).

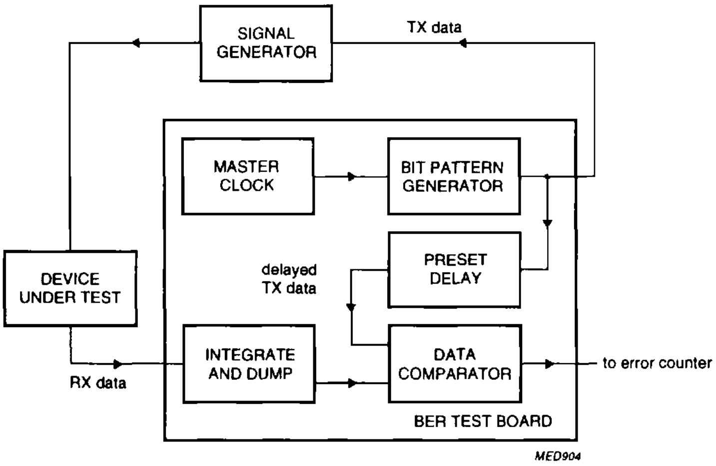


Fig.9 BER test facility.

LAYOUT OF PRINTED CIRCUIT BOARD FOR TEST CIRCUIT (f_i = 433.92 MHz)

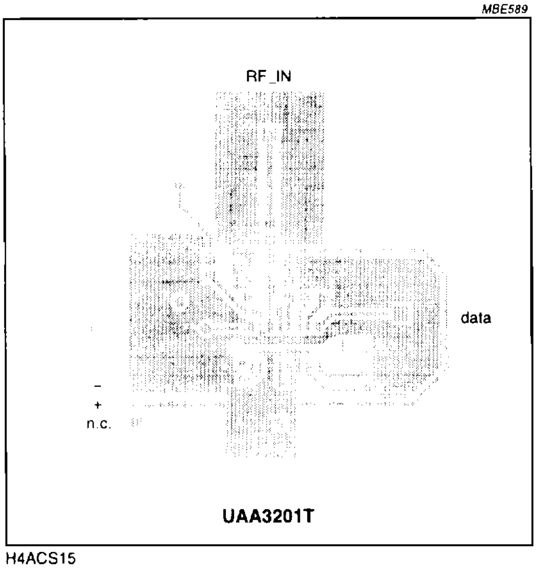


Fig.10 Layout (top side).

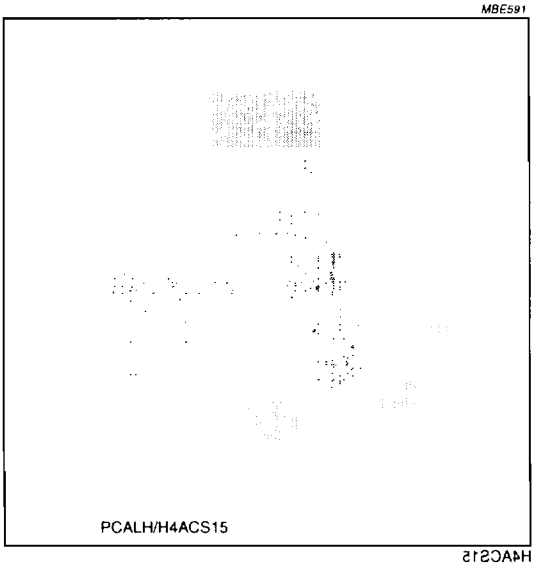


Fig.11 Layout (bottom side).

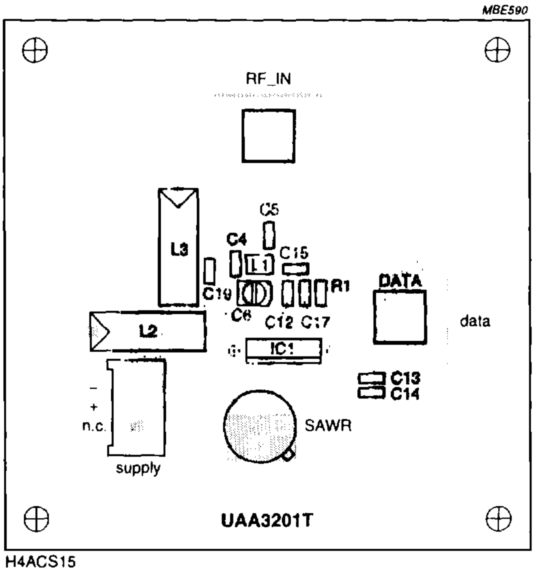


Fig.12 Top side with components.

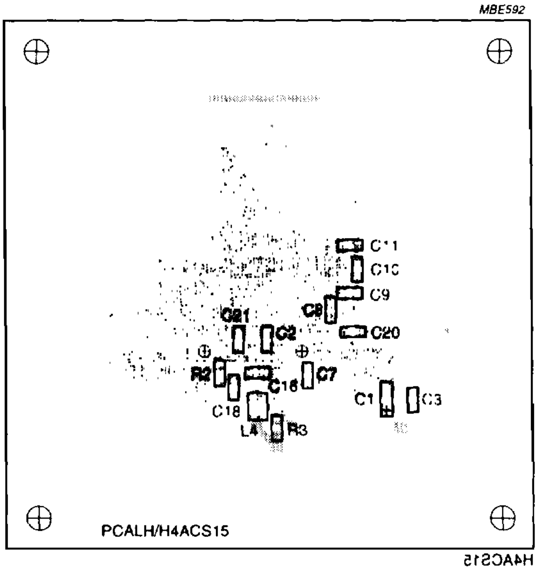


Fig.13 Bottom side with components.