

**MONOLITHIC 6-CHANNEL H BRIDGE DRIVER****DESCRIPTION**

The  $\mu$ PD168102 is a monolithic 6-channel H bridge driver IC consisting of a CMOS controller and a MOS output stage. Because it uses a MOS process, this driver IC consumes less current and loses less voltage at the output stage than conventional driver ICs that use bipolar transistors. In addition, the  $\mu$ PD168102 employs P-channel MOSFETs in its output stage, eliminating the need for an on-chip the charge pump circuit. Therefore, the current consumption during circuit operation can be significantly reduced.

Of the six output channels, four channels are voltage drive type and two channels are current drive type (voltage drive is also possible). The current drive method of the  $\mu$ PD168102 is the output chopping method, which realizes lower power consumption drive than the conventional high-power-dissipation linear drive method.

The  $\mu$ PD168102 is housed in a 48-pin WQFN to decrease the mounting area and height. The  $\mu$ PD168102 can simultaneously drive two stepper motors and two DC motors and is ideal for the motor driver of digital still cameras.

**FEATURES**

- Six H bridge circuits employing power MOSFETs
- Voltage drive type: 4 channels, current drive type (constant current chopping type): 2 channels
- Low current consumption due to elimination of charge pump circuit
- Input logic frequency: 100 kHz supported
- 3 V power supply supported
  - Minimum operating supply voltage: 2.5 V
- Low voltage malfunction prevention circuit
  - Internal circuit shutdown at  $V_{DD} < 2.5$  V
- On-chip overheat protection circuit
- 48-pin WQFN (7 mm  $\times$  7 mm)

**ORDERING INFORMATION**

Part Number	Package
$\mu$ PD168102K9-5B4	48-pin plastic WQFN (7 mm $\times$ 7 mm)

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

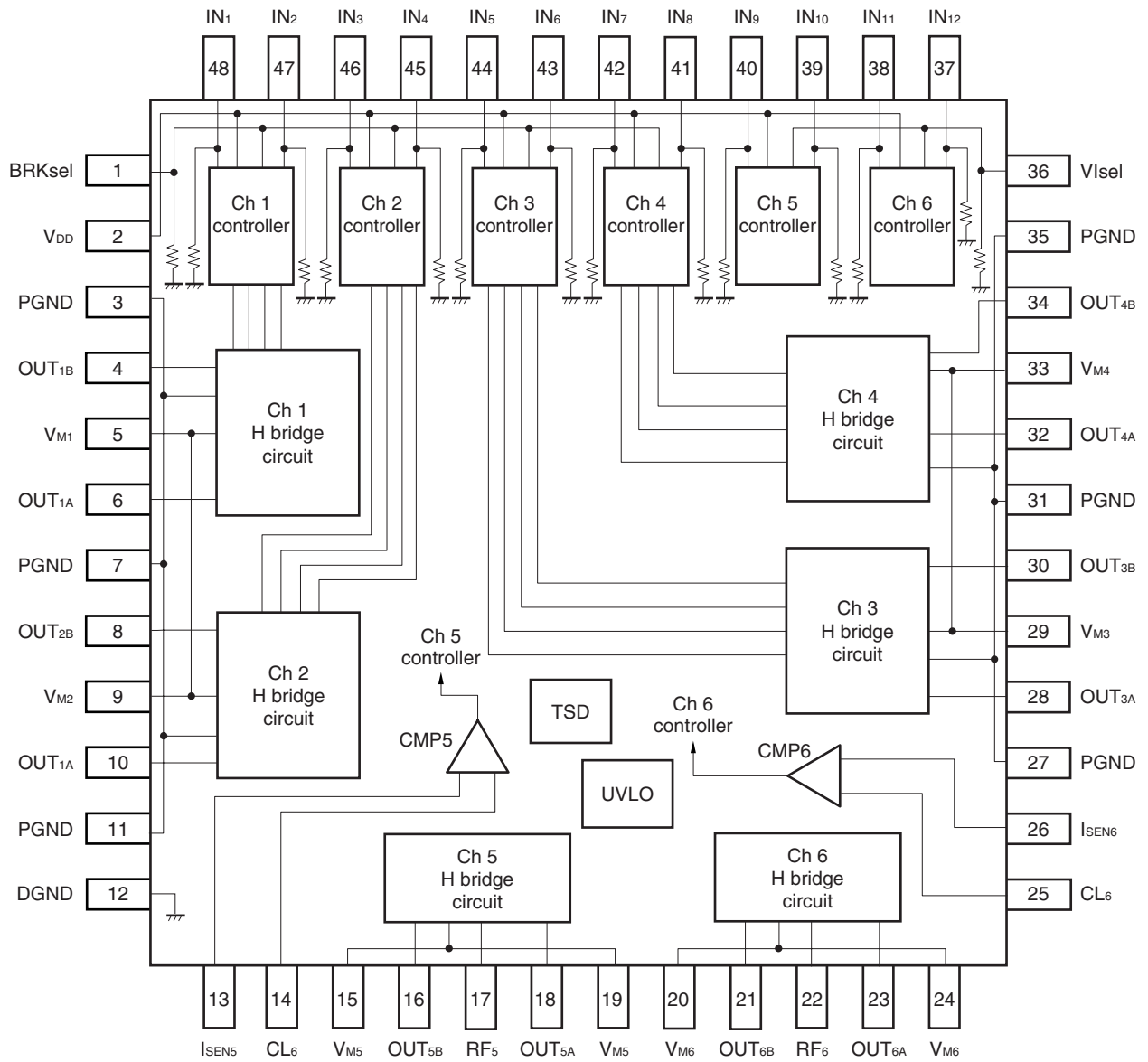
## PIN FUNCTIONS

Package: 48-pin WQFN (7 mm × 7 mm)

Pin No.	Pin Name	Pin Function
1	BRKsel	Stop mode switching pin when output open
2	V <sub>DD</sub>	Control block power supply pin
3	PGND	Output GND pin
4	OUT <sub>1B</sub>	Ch 1 output pin
5	V <sub>M1</sub>	Ch 1 output block power supply pin
6	OUT <sub>1A</sub>	Ch 1 output pin
7	PGND	Output block GND pin
8	OUT <sub>2B</sub>	Ch 2 output pin
9	V <sub>M2</sub>	Ch 2 output block power supply pin
10	OUT <sub>2A</sub>	Ch 2 output pin
11	PGND	Output block GND pin
12	DGND	Control block GND pin
13	I <sub>SEN5</sub>	Ch 5 current sense signal input pin
14	CL <sub>5</sub>	Ch 5 reference voltage input pin
15	V <sub>M5</sub>	Ch 5 output block power supply pin
16	OUT <sub>5B</sub>	Ch 5 output pin
17	RF <sub>5</sub>	Ch 5 sense resistor connection pin
18	OUT <sub>5A</sub>	Ch 5 output pin
19	V <sub>M5</sub>	Ch 5 output block power supply pin
20	V <sub>M6</sub>	Ch 6 output block power supply pin
21	OUT <sub>6B</sub>	Ch 6 output pin
22	RF <sub>6</sub>	Ch 6 sense resistor connection pin
23	OUT <sub>6A</sub>	Ch 6 output pin
24	V <sub>M6</sub>	Ch 6 output block power supply pin
25	CL <sub>6</sub>	Ch 6 reference voltage input pin
26	I <sub>SEN6</sub>	Ch 6 current sense signal input pin
27	PGND	Output block GND pin
28	OUT <sub>3A</sub>	Ch 3 output pin
29	V <sub>M3</sub>	Ch 3 output block power supply pin
30	OUT <sub>3B</sub>	Ch 3 output pin
31	PGND	Output block GND pin
32	OUT <sub>4A</sub>	Ch 4 output pin
33	V <sub>M4</sub>	Ch 4 output block power supply pin
34	OUT <sub>4B</sub>	Ch 4 output pin
35	PGND	Output block GND pin
36	V <sub>I</sub> sel	Voltage/current control switching pin (ch 5, ch 6)
37	IN <sub>12</sub>	Ch 6 input pin
38	IN <sub>11</sub>	Ch 6 input pin
39	IN <sub>10</sub>	Ch 5 input pin
40	IN <sub>9</sub>	Ch 5 input pin
41	IN <sub>8</sub>	Ch 4 input pin
42	IN <sub>7</sub>	Ch 4 input pin
43	IN <sub>6</sub>	Ch 3 input pin
44	IN <sub>5</sub>	Ch 3 input pin
45	IN <sub>4</sub>	Ch 2 input pin
46	IN <sub>3</sub>	Ch 2 input pin
47	IN <sub>2</sub>	Ch 1 input pin
48	IN <sub>1</sub>	Ch 1 input pin

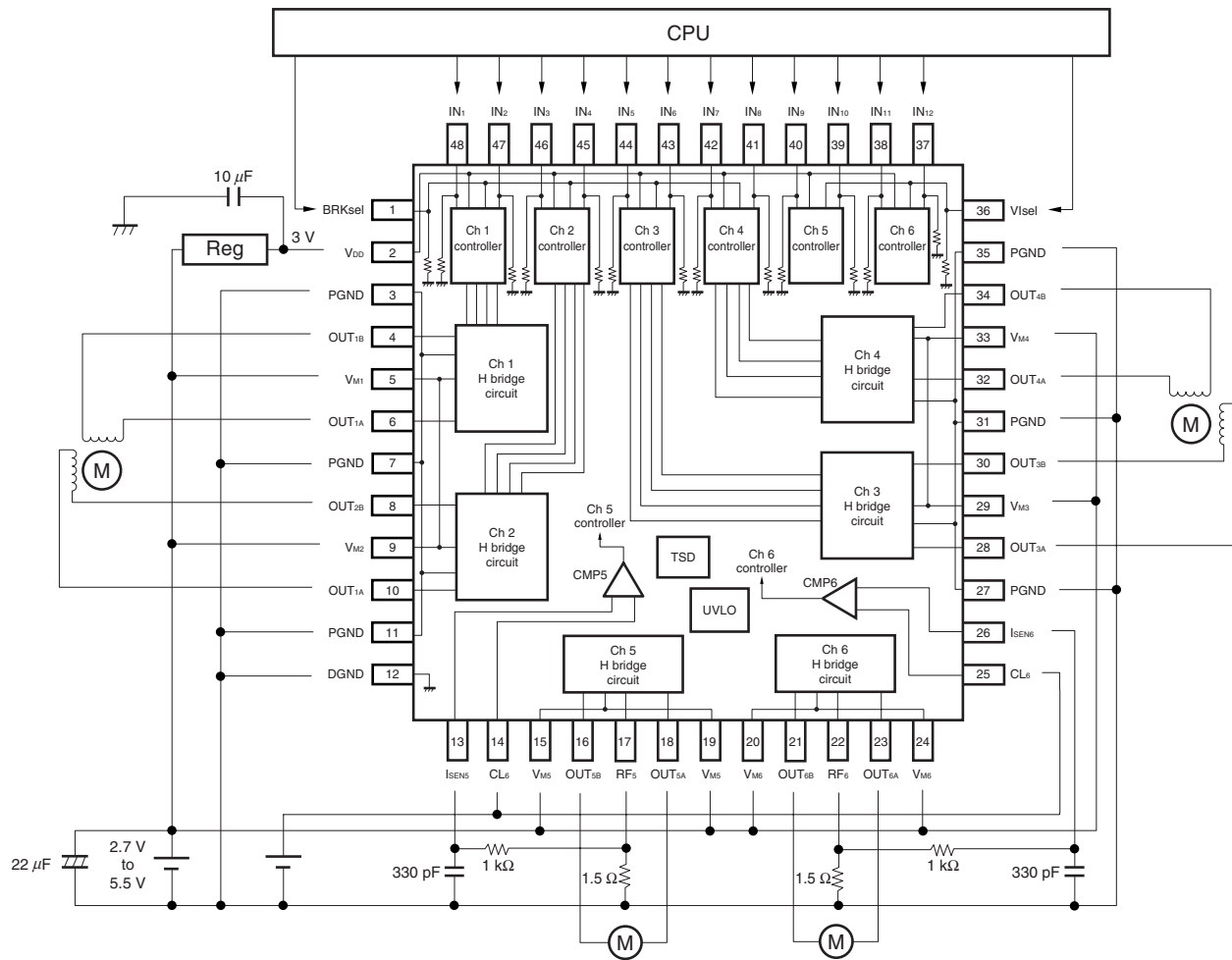
**Caution** Multiple pins with the same function must all be connected.

**BLOCK DIAGRAM**



**Caution** Multiple pins with the same function must all be connected. The motor power supply pins  $V_{M1}$  and  $V_{M2}$ , and  $V_{M3}$  and  $V_{M4}$  are internally connected, so be sure to apply the same potential to them.

EXAMPLE OF STANDARD CONNECTION



This circuit diagram is shown as an example of connection, and is not intended for mass production design.

**FUNCTION OPERATION TABLE**

The logic of each channel is shown in the table below.

**I/O Truth Table for Channels 1 to 6**

Input			Output		Output Status	Operating Mode of Ch 5 and Ch 6
VIsel	IN1, 3, 5, 7, 9, 11	IN2, 4, 6, 8, 10, 12	OUTA	OUTB		
L	L	L	Z	Z	Stopped (output open, standby)	Voltage control output
	L	H	L	H	Reverse (OUTB → OUTA)	
	H	L	H	L	Forward (OUTA → OUTB)	
	H	H	L	L	Stopped (short brake)	
H	L	L	Z	Z	Stopped (output open)	Constant current chopping
	L	H	L	H	Reverse (OUTB → OUTA)	
	H	L	H	L	Forward (OUTA → OUTB)	
	H	H	L	L	Stopped (short brake)	

H: High level, L: Low level, Z: High impedance

Constant current chopping is possible for channels 5 and 6.

When VIsel is set to high level, if the voltage becomes higher than the reference voltage (external input) and the current becomes higher than the current set by the feedback resistor, the output can be forcibly chopped.

When VIsel is set to low level, channels 5 and 6 function in the same way as channels 1 to 4.

**Standby function**

The μPD168102 realizes a standby function by combining the input signals.

By setting all the control input signals of channels 1 to 6 to low level, a standby mode in which the current consumption of the internal circuit is suppressed is entered. Note that the output status is high impedance (output open).

**BRKsel pin function**

By using the logic of BRKsel, whether the function that prevents the motor power supply rising in the Hi-Z output status (input L, L) is enabled or disabled can be selected. Refer to the truth table below.

**BRKsel Truth Table**

BRKsel	Function
L	Hi-Z status
H	Regenerates output current using an internal channel. An internal timer is incorporated, through which the regeneration period is set for approx. 1 ms, and then the Hi-Z status is entered.

**ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25°C: MOUNTED ON GLASS EPOXY BOARD 100 mm × 100 mm × 1 mm, COPPER FILM AREA: 15%)**

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V <sub>DD</sub>	Control block	-0.5 to +6.0	V
	V <sub>M</sub>	Motor block	-0.5 to +6.0	
Input voltage	V <sub>IN</sub>		-0.5 to V <sub>DD</sub> +0.5	V
Output pin voltage	V <sub>OUT</sub>	Ch 1 to ch 4	6.2	V
		Ch 5, ch 6	5.7	
DC output current 1 (ch 1 to ch 4)	I <sub>D(DC)1</sub>	DC	±0.3	A/ch
DC output current 2 (ch 5, ch 6)	I <sub>D(DC)2</sub>	DC	±0.5	A/ch
Instantaneous output current 1 (ch 1 to ch 4)	I <sub>D(pulse)1</sub>	PW < 10 ms, duty ≤ 20%	±0.6	A/ch
Instantaneous output current 2 (ch 5, ch 6)	I <sub>D(pulse)2</sub>	PW < 10 ms, duty ≤ 20%	±1.0	A/ch
Power consumption	P <sub>T</sub>		1.0	W
Peak junction temperature	T <sub>CH(MAX)</sub>		150	°C
Storage temperature	T <sub>stg</sub>		-55 to +150	°C

**RECOMMENDED OPERATING CONDITIONS (T<sub>A</sub> = 25°C: MOUNTED ON GLASS EPOXY BOARD 100 mm × 100 mm × 1 mm, COPPER FILM AREA: 15%)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	V <sub>DD</sub>	Control block	2.5		5.5	V
	V <sub>M</sub>	Motor block	2.7		5.5	V
Input voltage	V <sub>IN1</sub>		0		V <sub>DD</sub>	V
	V <sub>IN2</sub>	CL pin	0.1		0.5	V
DC output current 1 (ch 1 to ch 4)	I <sub>D(DC)1</sub>	DC	-0.2		+0.2	A/ch
DC output current 2 (ch 5, ch 6)	I <sub>D(DC)2</sub>	DC	-0.4		+0.4	A/ch
Instantaneous output current 1 (ch 1 to ch 4)	I <sub>D(pulse)1</sub>	PW < 10 ms, duty ≤ 20%	-0.4		+0.4	A/ch
Instantaneous output current 2 (ch 5, ch 6)	I <sub>D(pulse)2</sub>	PW < 10 ms, duty ≤ 20%	-0.8		+0.8	A/ch
Logic input frequency	f <sub>IN</sub>				100	kHz
Operating temperature range	T <sub>A</sub>		-10		85	°C
Peak junction temperature	T <sub>CH(MAX)</sub>				125	°C

**ELECTRICAL SPECIFICATIONS (Unless otherwise specified,  $V_{DD} = V_M = 3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ )**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$V_{DD}$ pin current in standby mode	$I_{DD(STB)}$				1.0	μA
$V_{DD}$ pin current when operating	$I_{DD(ACT)}$				1.0	mA
Input current, high	$I_{IH}$	$V_{IN} = V_{DD}$			60	μA
Input current, low	$I_{IL}$	$V_{IN} = 0$	-1.0			μA
Input pull-down resistor	$R_{IND}$		50		200	kΩ
Input voltage, high	$V_{IH}$	$2.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$0.7 \times V_{DD}$			V
Input voltage, low	$V_{IL}$	$2.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$0.3 \times V_{DD}$	V
H bridge on-resistance 1 (ch 1 to ch 4)	$R_{ON1}$	$I_M = 0.2\text{ A}$ , sum of the top and bottom stages		1.5	2.0	Ω
H bridge on-resistance 2 (ch 5, ch 6)	$R_{ON2}$	$I_M = 0.4\text{ A}$ , $R_{F5}, R_{F6} = 0\text{ V}$ , sum of the top and bottom stages		1.0	1.5	Ω
Output leakage current	$I_{M(OFF)}$	Per $V_M$ pin, $V_M = 5.5\text{ V}$ , all control pins are low level			10	μA
Current detection comparator offset voltage	$V_{CO}$	$V_{CL} = 0.1\text{ V}$	-10		10	mV
Detection voltage at low voltage	$V_{DDS}$				2.5	V
Output turn-on time	$t_{ON}$	$R_M = 20\ \Omega$ , see <b>Figure 1</b>		0.7	2.0	μs
Output turn-off time	$t_{OFF}$			0.2	0.5	μs
All-off time at mode change	$t_{HIZ}$		50			ns
Rise time	$t_r$	$R_M = 20\ \Omega$ , see <b>Figure 1</b>		0.3		μs
Fall time	$t_f$			0.1		μs
Current detection comparator operation delay time	$t_{CDL}$	$V_{CL} = 0.1\text{ V}$ , $V_{ISEN} = 0\text{ V} \longleftrightarrow 0.2\text{ V}$ , see <b>Figure 2</b>		0.4	1.0	μs

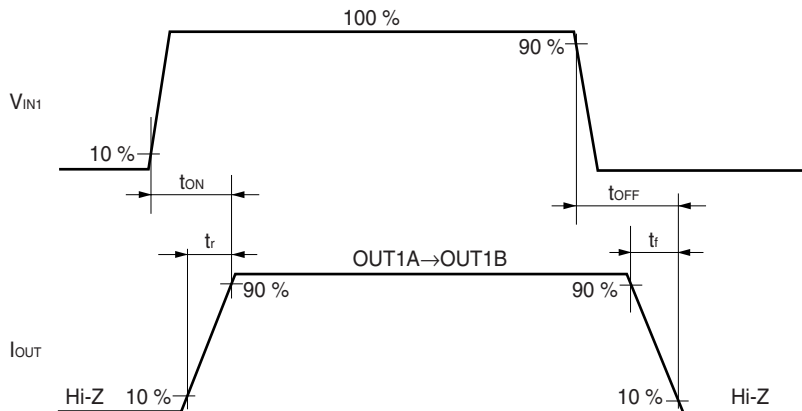
The overheat protection circuit operates at  $T_{ch} > 150^\circ\text{C}$ . In the overheat protected status, all outputs are high impedance.

In the standby mode, the overheat protection circuit and the low-voltage malfunction prevention circuit do not operate.

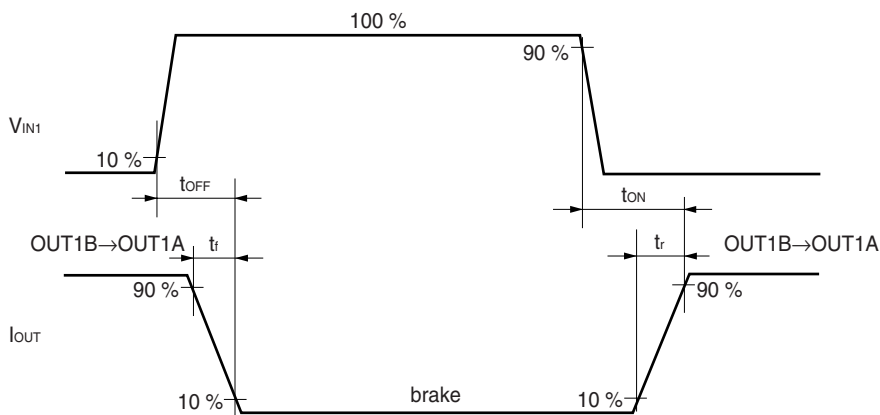
**SWITCHING CHARACTERISTICS WAVEFORMS**

**Figure 1. H Bridge Switching Waveform**

(1) IN2 = Low level

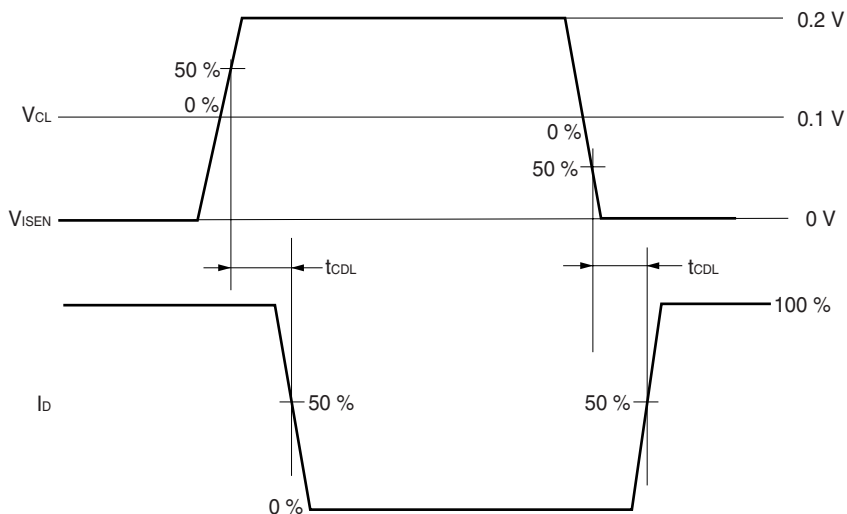


(2) IN2 = High level



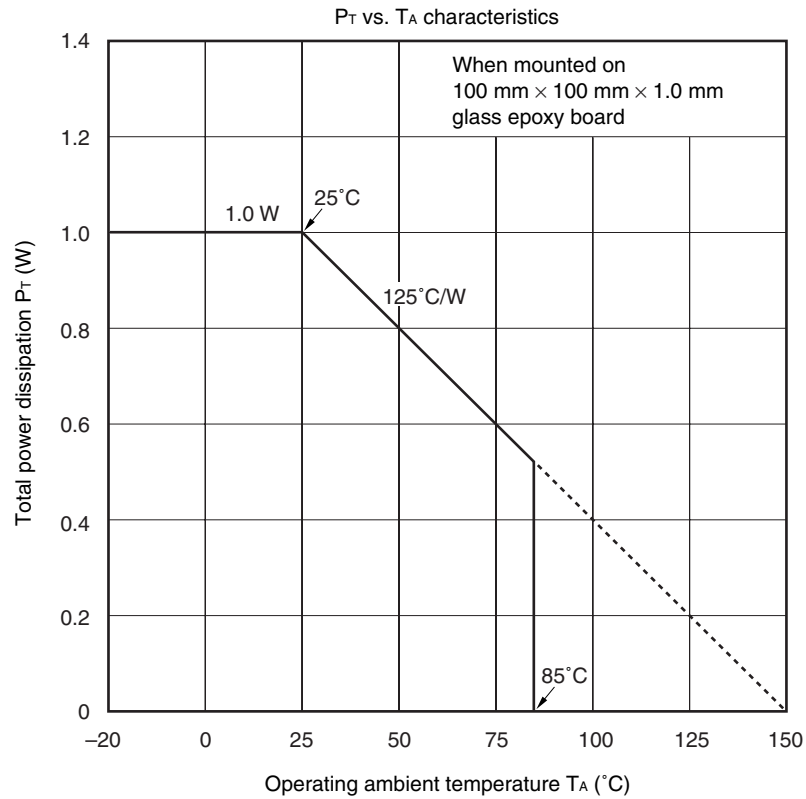
A high impedance period of approx. 50 ns is secured to prevent through current when switching the mode.

**Figure 2. Current Detection Comparator Switching Waveform**



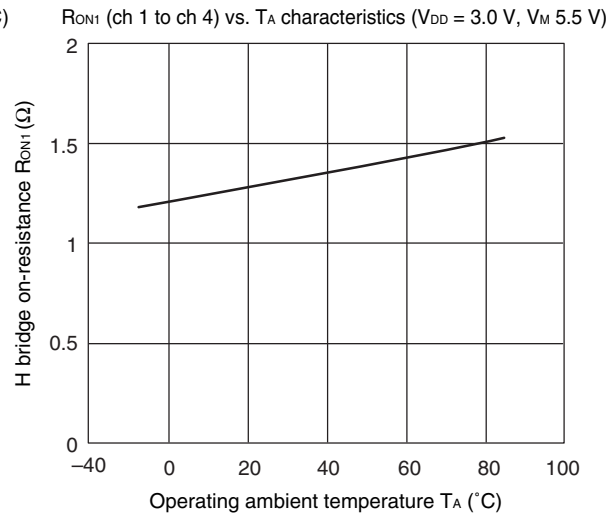
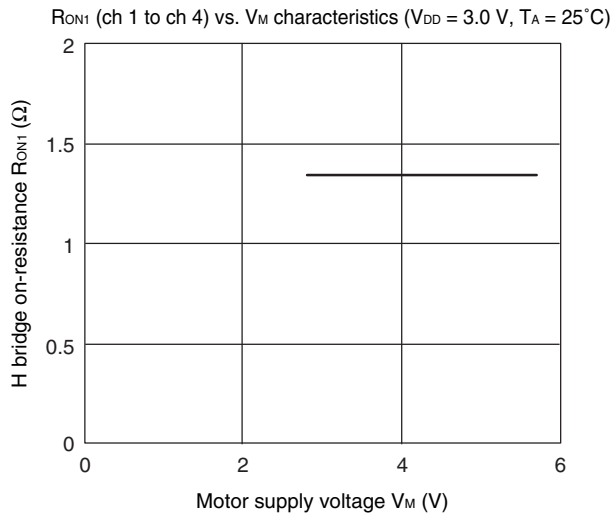
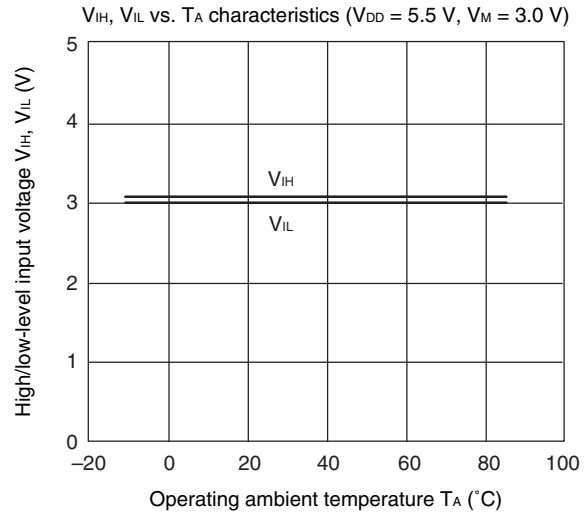
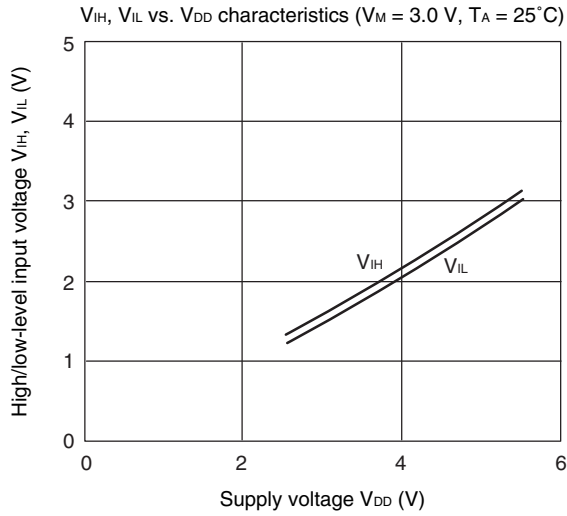
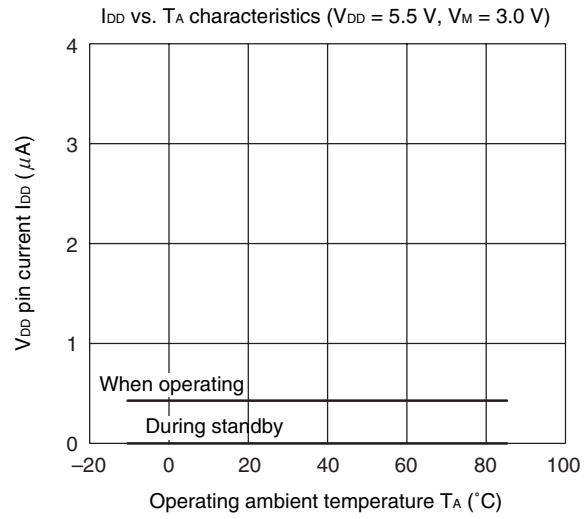
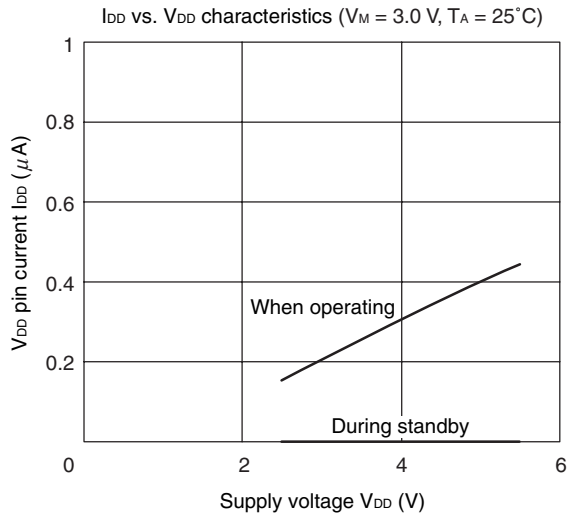


TOTAL POWER DISSIPATION AND OPERATING AMBIENT TEMPERATURE CHARACTERISTICS

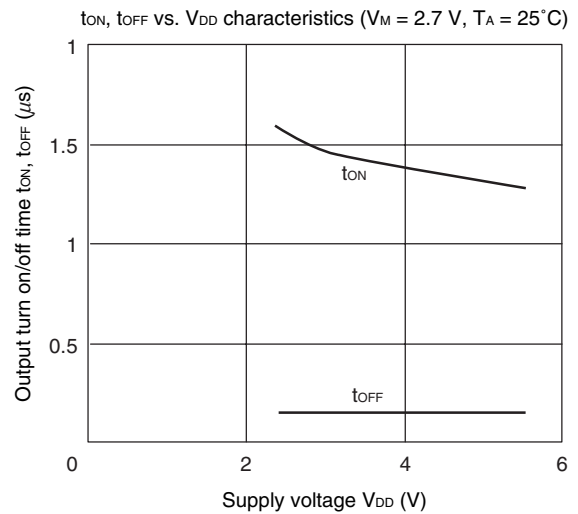
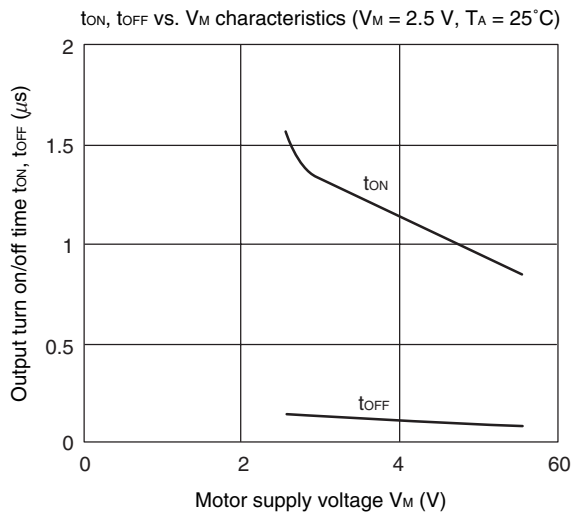
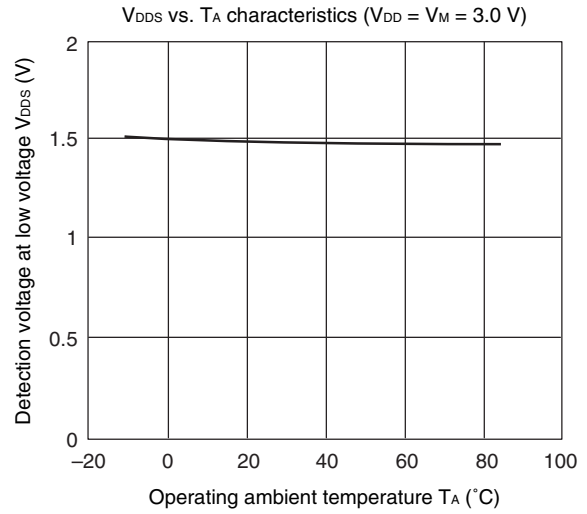
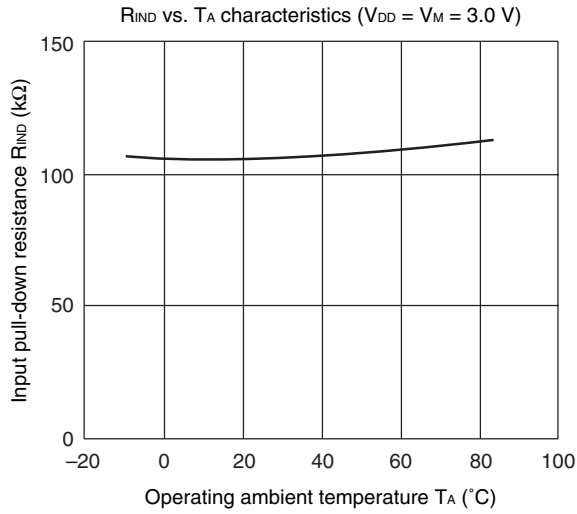
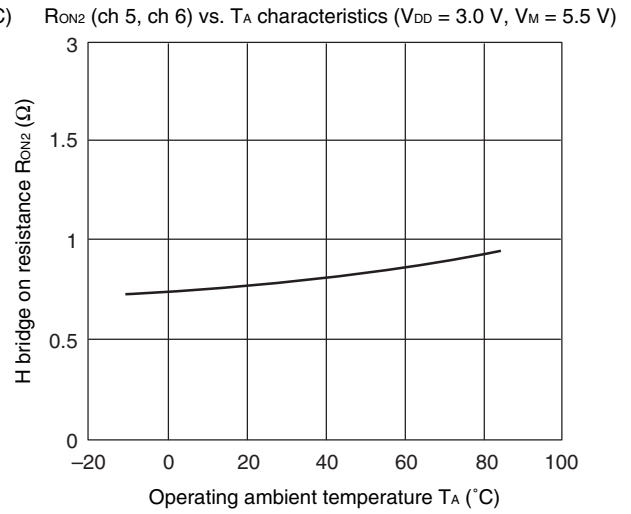
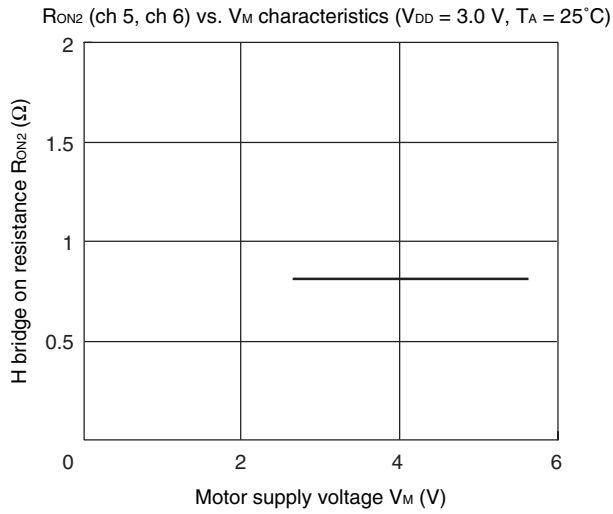


**Remark** When the operating ambient temperature is 25°C or lower, power application up to 1 W is possible. When the operating ambient temperature is higher than 25°C, perform derating in accordance with the above figure. In addition, when at 85°C (operating ambient temperature recommended condition), power application up to 0.52 W is possible.

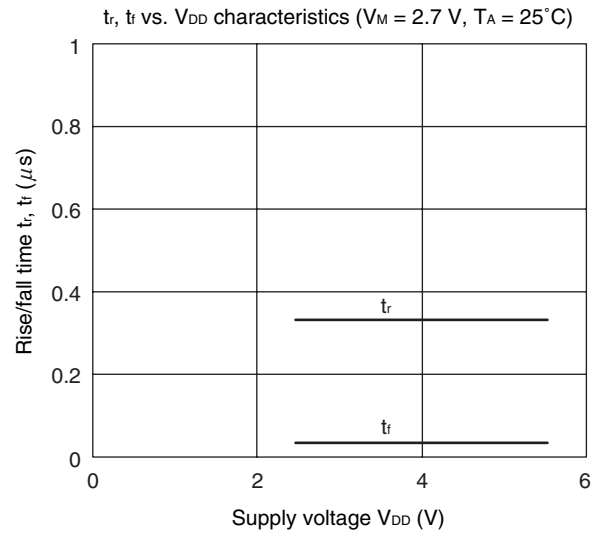
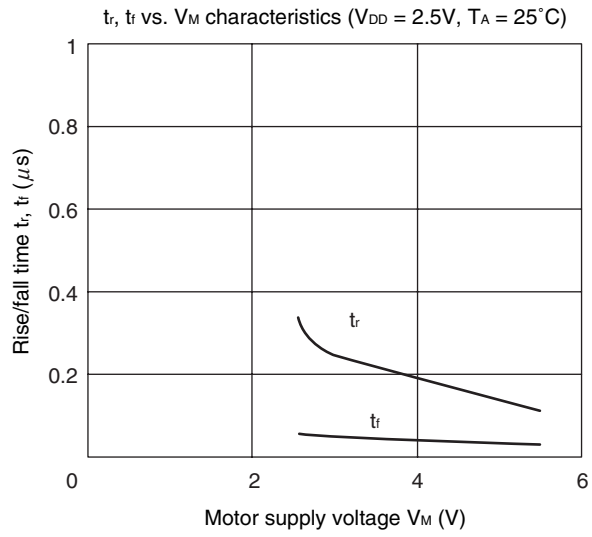
CHARACTERISTICS CURVES



CHARACTERISTICS CURVES

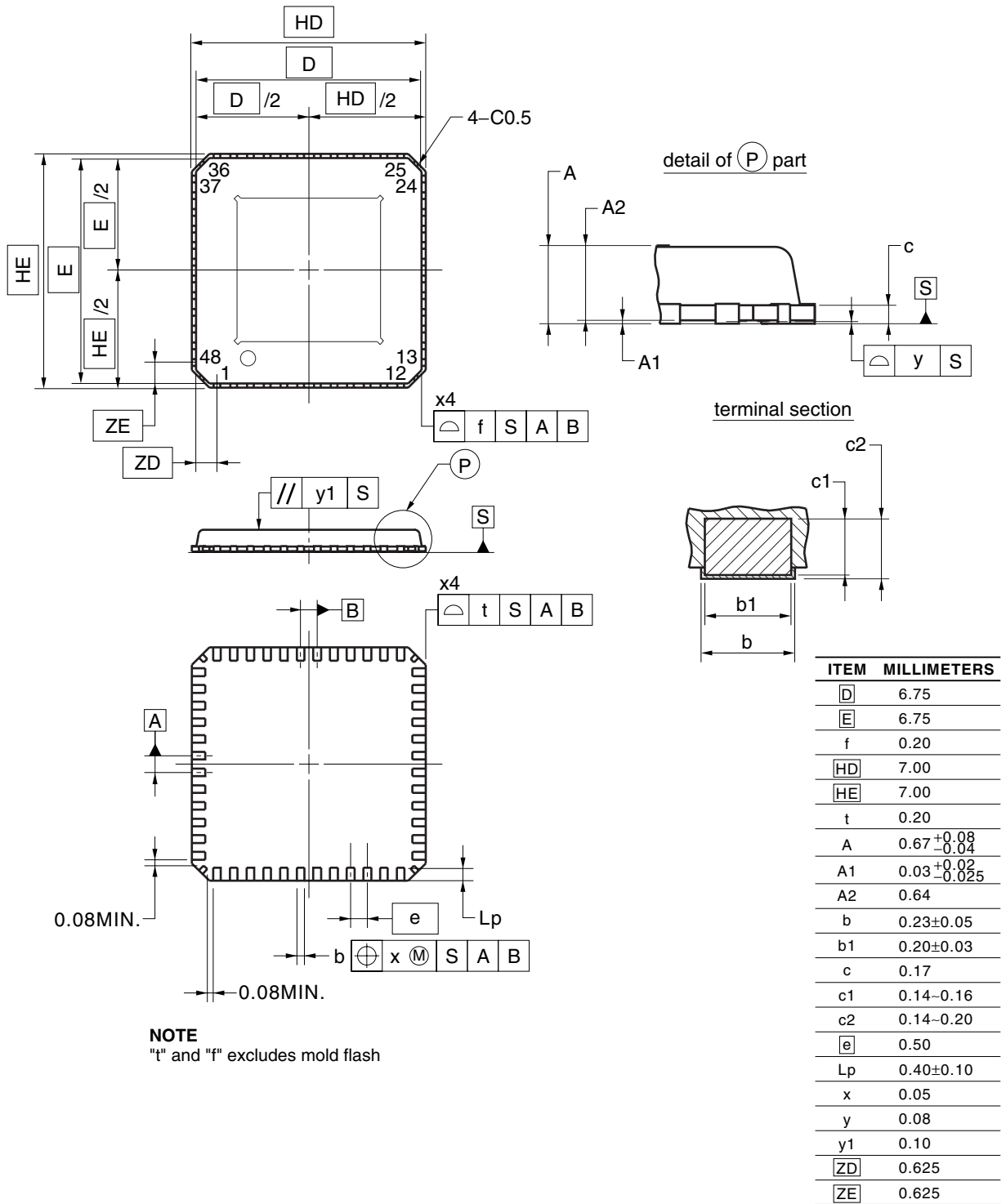


CHARACTERISTICS CURVES



PACKAGE DRAWING

48-PIN PLASTIC WQFN (7x7)



**NOTE**  
"t" and "f" excludes mold flash

P48K9-50-5B4

**RECOMMENDED SOLDERING CONDITIONS**

The μPD168102 should be soldered and mounted under the following recommended conditions.

For details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**. For soldering methods and conditions other than those recommended below, contact an NEC sales representative.

**Surface Mounting Type Soldering Conditions**

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 260°C, Time: 60 seconds max. (at 220°C or higher), Count: Three times or less, Exposure limit: 3 days <sup>Note</sup> (after that, prebake at 125°C for 10 hours), Flux: Rosin-based flux with low chlorine content (chlorine 0.2 Wt% or below) is recommended	IR60-103-3

**Note** After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

**Caution** Do not use different soldering methods together (except for partial heating).

## NOTES FOR CMOS DEVICES

**① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

**② HANDLING OF UNUSED INPUT PINS FOR CMOS**

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

**③ STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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