AKD7782-A

AK7782 Evaluation Board Rev.0

GENERAL DESCRIPTION

The AKD7782-A is an evaluation board for AK7782, which is a highly integrated audio processor including 5ch 24bit ADC, 4ch SRC and two audio DSP cores. This board is composed of a main board and a sub board. It is possible to control the setting of board via USB port. RCA connectors are used for the input and output of analog signal. This board also has digital interface and can achieve the interface with digital audio system via optical connector.

■ Ordering guide

AKD7782-A --- Evaluation board for AK7782
Control software is packed with this.

FUNCTION

- ☐ **Read/Write access to PRAM, CRAM, OFREG and control registers of AK7782**
- ☐ **Compatible with 2 types of digital audio interface**
  - **Optical input (x1) / Optical output (x1)**
  - **10pin header for interface with external data source (x2)**
- ☐ **ADC1/ADC2 18ch input, ADCM 1ch input, DAC 8ch output**
  (Note: There is no DAC within AK7782. 8ch DAC AK4359 is equipped.)
- ☐ **USB port for board control**

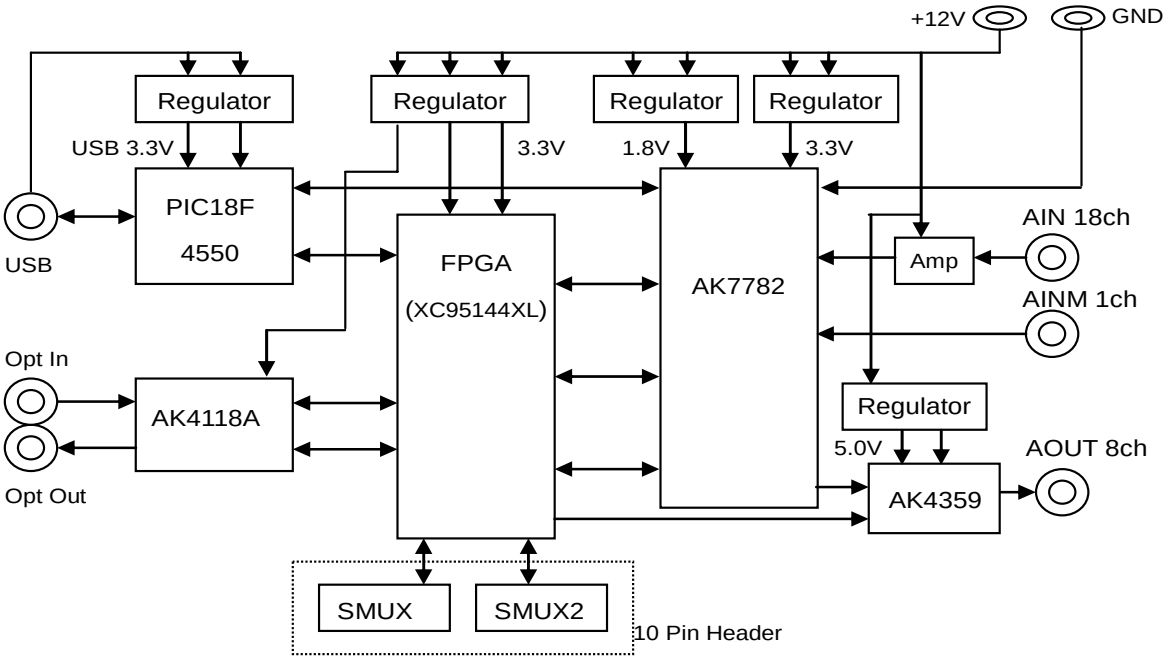


Figure 1. AKD7782-A Block Diagram

Evaluation Board Diagram

■ Board Diagram

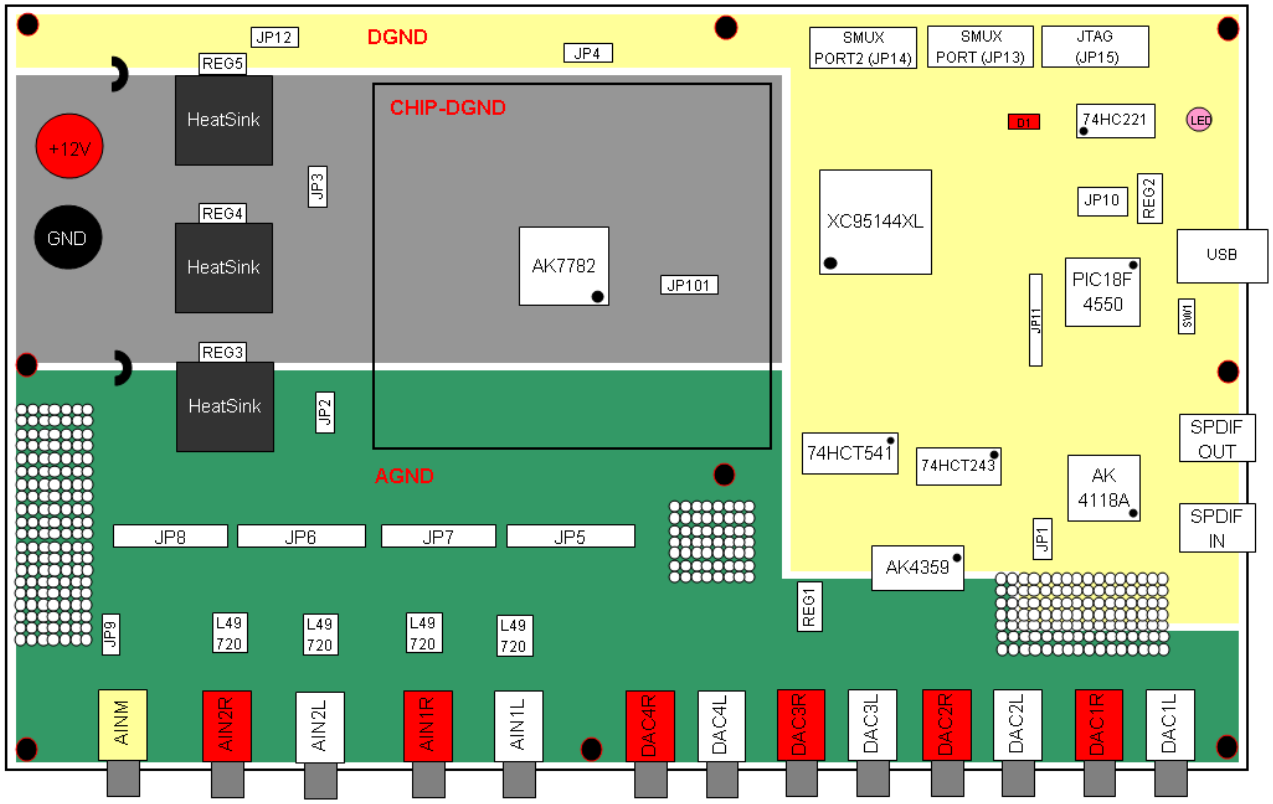


Figure 2. AKD7782-A Board Diagram

■ Description

(1) AIN/DAC (RCA Jack)
AIN: Analog input jacks. DAC: Analog output jacks.
The white jacks are used for left channel and the red ones are for right channel.

(2) AK4118A
AK4118A has DIR, DIT and X'tal oscillator. It transports digital data to AK7782 when working in master mode and outputs data from AK7782 when working in slave mode.

(3) SPDIF-IN/SPDIF-OUT (Optical Connector)
SPDIF-IN (input): It inputs optical digital signal to AK4118A and supports sampling frequencies from 8 to 96kHz.
SPDIF-OUT (output): It outputs optical digital signal from AK4118A and supports sampling frequencies from 8 to 96kHz.

(4) +12V/GND (Power supply)
Connect to +12V and GND according to the following operation sequence on page 4.

(5) PIC18F4550
USB control chip. It is possible to set up the registers of AK7782, FPGA and AK4118A from PC via USB port.

(6) SW1
Push type switch. It is used to initialize PIC18F4550. Please push down the button once when PC has trouble identifying the evaluation board.

(7) XC95144XL(Xilinx)
FPGA used for data path control. It is possible to run a variety of tests by way of controlling the data path via control software.

(8) SMUX PORT (PORT1/PORT2)
10 pin header for interface with external data source. Two ports are equipped and available to achieve with other audio system.

Pin	I/O	Function	pin	I/O	Function
1	I/O	MCLK	2	P	GND
3	I/O	BITCLK	4	P	GND
5	I/O	LRCLK	6	P	GND
7	I	SDTI	8	P	GND
9	P	VDD	10	O	SDTO

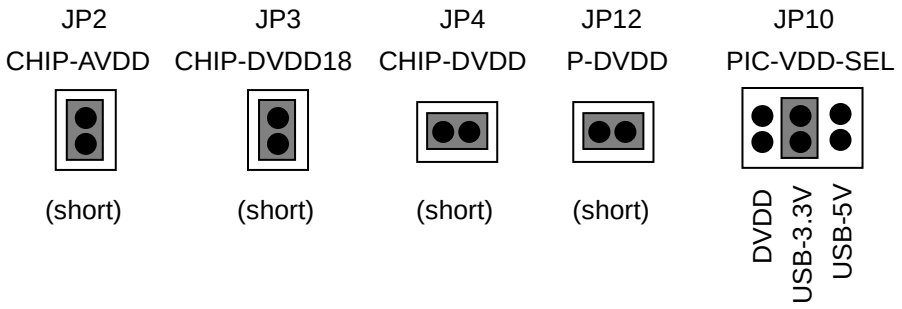
Table 1. Pin assignment of SMUX port

Evaluation Board Manual

■ Operation sequence

(1) Set up the power supply lines.

Setting of jumper pins



Connection of power supply lines (Each supply line should be distributed from the power supply unit.)

Name	Color	Voltage	Comment	Attention
+12V	Red	+9～+12V	Regulator, Power supply for op-amp	This jack is always needed.
GND	Black	0V	Ground	This jack is always needed.

Table 2. Power supply connection

(2) Set up the evaluation mode, jumper pins and connectors according to the follows.

(3) Connect the board to PC with the USB cable packed.

(4) Power On.

(5) Start the control soft and setup the registers.

■ Evaluation Mode

In case of AK7782 evaluation using AK4118A, it is necessary to correspond to audio interface format for AK7782 and AK4118A. About AK7782's audio interface format, please refer to datasheet of AK7782. About AK4118A's audio interface format, please refer to Table 11 in this manual.

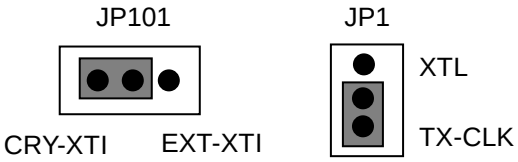
Applicable Evaluation Mode
(1) Evaluation mode of ADC using DIT of AK4118A: CKM Master Mode = 0
(2) Evaluation mode of DSP using DIR/DIT of AK4118A: CKM Slave Mode = 2/4/5
(3) Evaluation mode of SRC using DIR of AK4118A and SMUX port: CKM Master Mode = 0
(4) Evaluation mode of sound (tone) quality using DAC of AK4359

Please refer to the control software manual from page 12 and the datasheet of AK7782 to set up FPGA, AK4118A and AK7782 from PC.

(1) Evaluation mode of ADC using DIT of AK4118A : CKM Master Mode = 0

SPDIF-OUT is used. Set the clock mode of AK7782 to Master Mode 0 (12.288MHz).
AK7782 supplies MCLK, BICK, and LRCK to AK4118A and AK4118A outputs the data from ADC1, ADC2 and ADCM.

[Setting of jumper]

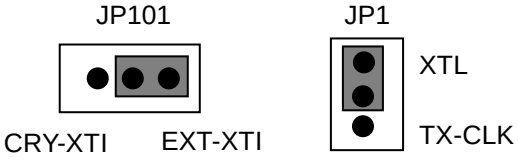


[Connection of other connectors]
For ADC1 and ADC2, RCA1/RCA2 or RCA3/RCA4 are available. Please refer to Table 5 for the setting of jumpers which used to select input channels.
For ADCM, RCA5(AINM) is available.

(2) Evaluation mode of DSP using DIR/DIT of AK4118A : CKM Slave Mode = 2/4/5

SPDIF-IN and SPDIF-OUT are used. Set the clock mode of AK7782 to Master Mode 2/4/5.
AK4118A supplies MCLK, BICK, LRCK and digital data to AK7782 and outputs data from AK7782.
(MCLK is needed when CKM Slave Mode = 2.)

[Setting of jumper]

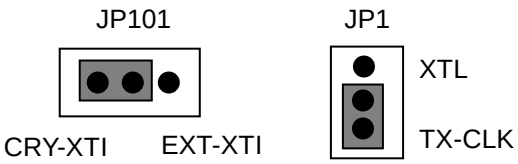


(JP101 is needed only when CKM Mode = 2)

(3) Evaluation mode of SRC using DIR of AK4118A and SMUX port : CKM Master Mode = 0

SPDIF-OUT and SMUX PORT are used. Set the clock mode of AK7782 to Master Mode 0 (12.288MHz).
SMUX PORT is used as input and supplies BICK, LRCK and digital data to SRC of AK7782.
AK7782 supplies MCLK, BICK, and LRCK to AK4118A and AK4118A outputs the data from SRC.

[Setting of jumper]



Crystal of 12.288MHz is equipped on the sub board for frequencies of 48kHz series. Please change the cystal to 11.2896MHz when using 44.1kHz series's frequencies.

[Connection of other connectors]
SMUX PORT 1 or PORT 2 is available. Please refer to Table 1 about the pin assignment of SMUX port.

(4) Evaluation mode of sound (tone) quality using DAC of AK4359

AK4359 is used. AK7782 supplies MCLK, BICK, LRCK and digital data to AK4359, which converts digital data to analog signal and output it.

[Connection of other connectors]
For analog output, RCA6 ~ RCA13 (DAC1-4) are available.

■ Board control

It is possible to control AKD7782-A via general USB port. Connect the USB port on the board to PC with the packed cable.

Control software is packed with this board and the software manual is included in this manual.

■ Indication for LED

[LED]: U12 When power is supplied, LED is lighted to red. It monitors PC-RQN signal and changes color when the board is communicating with PC.

[LED] D1: Monitor the status of INITRSTN pin of AK7782.
'L' → light up, 'H' → light out.

■ Setting of Jumper Pins

Main board:

Jumper	Setting (Default)	Note
JP1 (AK4118A Clock)	"XTL"	AK4118A Clock Source "XTL": Crystal Clock "TX-CLK": External Clock
JP2 (CHIP-AVDD)	Short	AK7782 AVDD
JP3 (CHIP-DVDD18)	Short	AK7782 DVDD18
JP4 (CHIP-DVDD)	Short	AK7782 DVDD
JP5 (AIN1L-SEL)	AINL+, AINL-	Input channel selector for ADC1/ADC2
JP6 (AIN1R-SEL)	AINR+, AINR-	
JP7 (AIN2L-SEL)	AINL2	
JP8 (AIN2R-SEL)	AINR2	
JP9 (AINM)	Short	Input for ADCM
JP10 (PIC-VDD-SEL)	"USB 3.3V"	USB chip power supply "USB-5V" : USB 5V "USB-3.3V" : USB 3.3V "DVDD" : Peripheral DVDD 3.3V
JP12 (P-DVDD)	Short	Peripheral DVDD 3.3V

Table 3. Setting of jumper pins on main board

Sub board:

Jumper	Setting (Default)	Note
JP101 (Clock)	"EXT-XTI"	AK7782 Clock Source "XTL": Crystal Clock "EXT": External Clock

Table 4. Setting of jumper pins on sub board

■ Analog Input Circuit

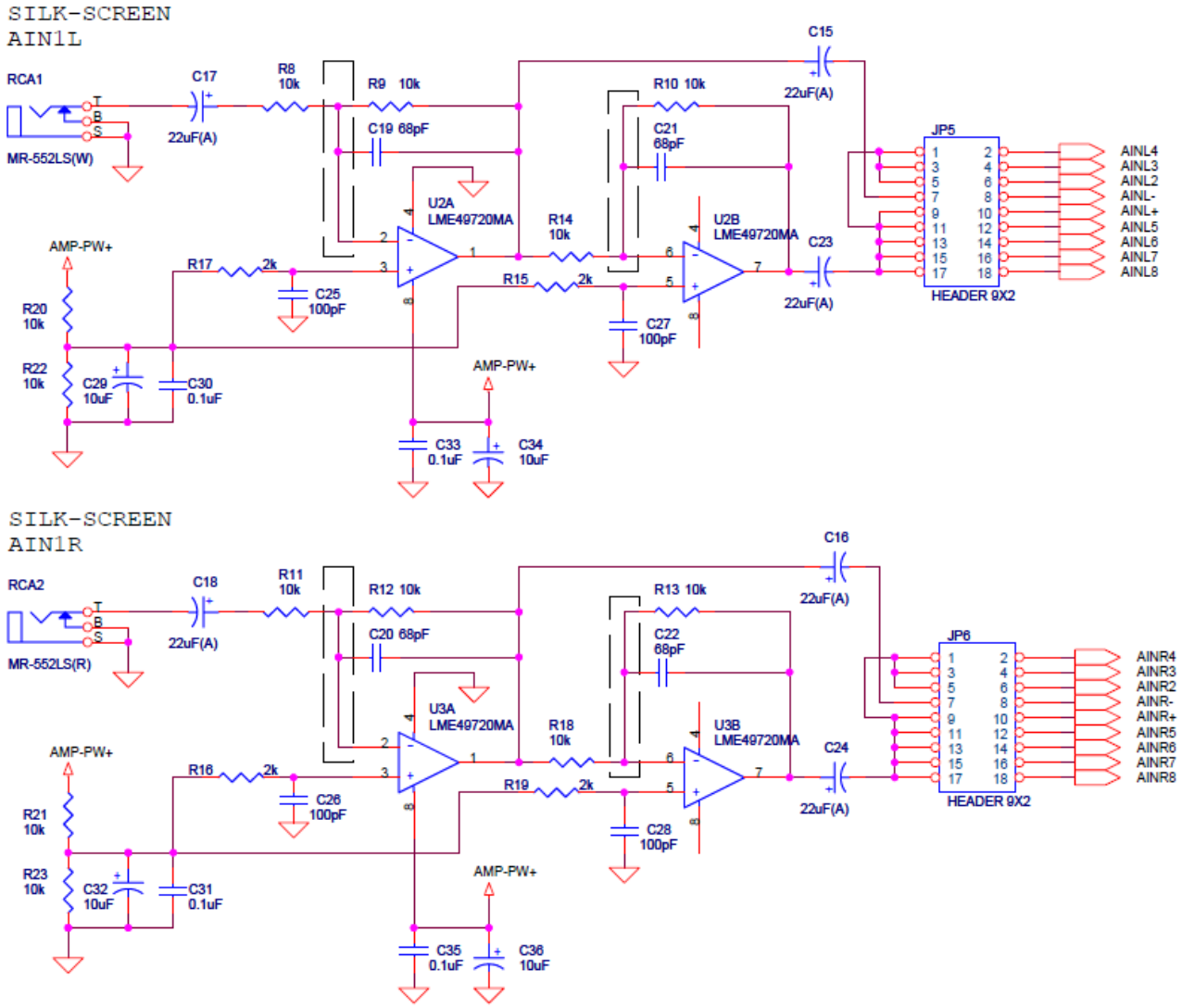


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Figure 3. Analog Input Circuit 1 for ADC1/ADC2

For ADC1/ADC2 analog differential input and single-end input, RCA1(AIN1L)、RCA2(AIN1R) are available.
The input range of each channel is 2.00Vpp@3.3V.

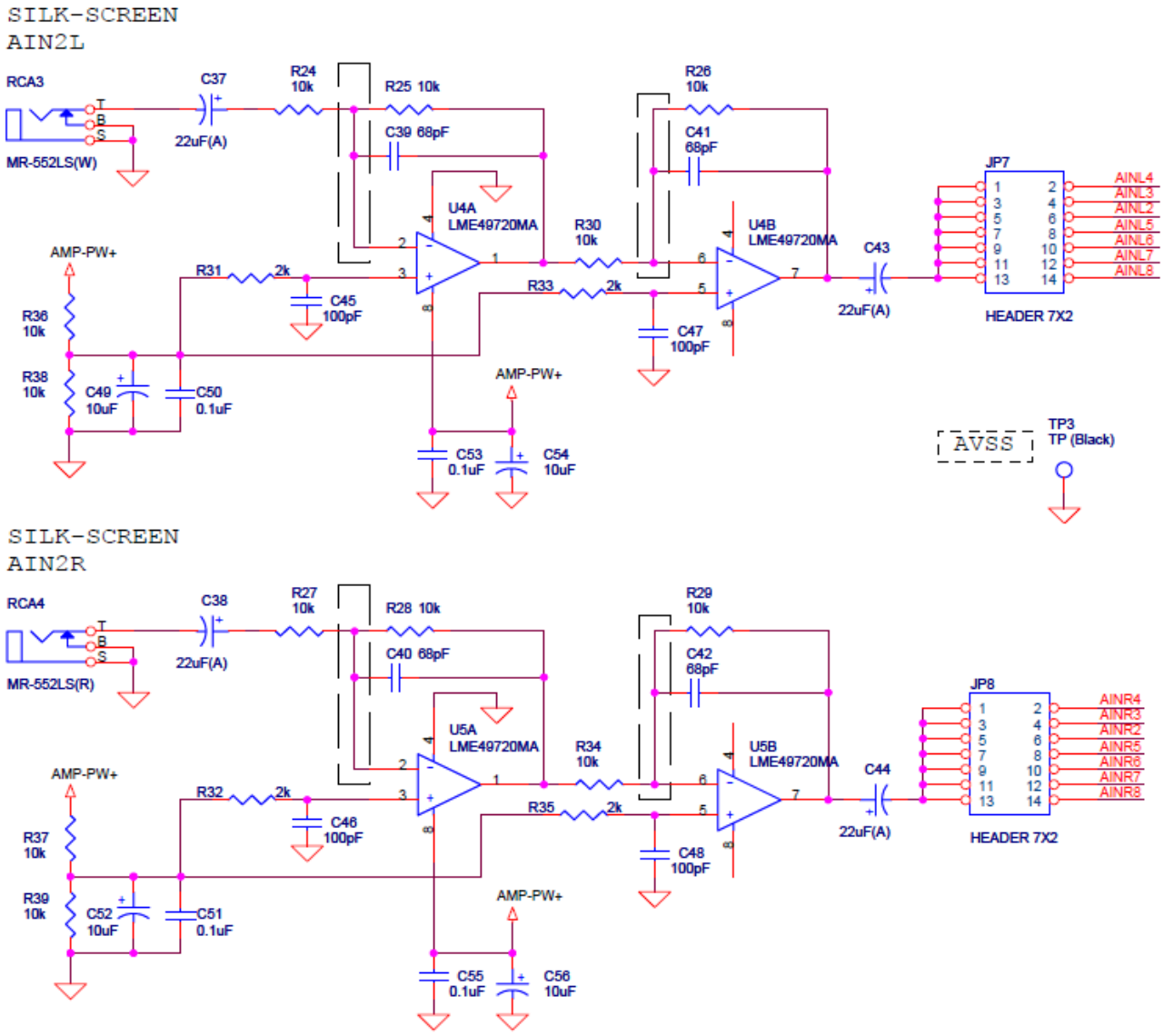


Figure 4. Analog Input Circuit 2 for ADC1/ADC2

For ADC1/ADC2 analog single-end input, RCA3(AIN2L)、RCA4(AIN2R) are available.
The input range of each channel is 2.00Vpp@3.3V.

Setting of JP5, JP6, JP7, JP8 for ADC1/ADC2 analog input:

Input Pin	Setting of JP5 and JP6 when using RCA1/RCA2	Setting of JP7 and JP8 when using RCA3/RCA4
AINL±/ AINR±	7-8 pin short 9-10 pin short	-
AINL2/ AINR2	5-6 pin short	5-6 pin short
AINL3/ AINR3	3-4 pin short	3-4 pin short
AINL4/ AINR4	1-2 pin short	1-2 pin short
AINL5/ AINR5	11-12 pin short	7-8 pin short
AINL6/ AINR6	13-14 pin short	9-10 pin short
AINL7/ AINR7	15-16 pin short	11-12 pin short
AINL8/ AINR8	17-18 pin short	13-14 pin short

Table 5. Setting of jumpers for ADC1/ADC2 analog input

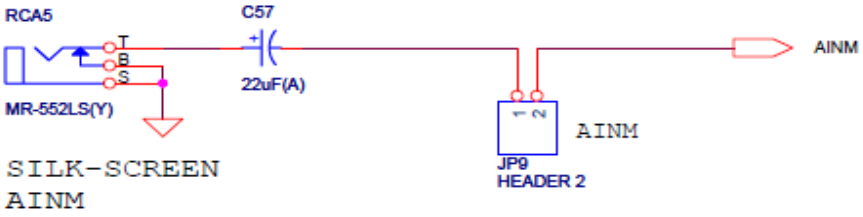


Figure 5. Analog Input Circuit for ADCM

For ADCM analog single-end input, RCA5(AINM) is available. The input range channel is 2.00Vpp@3.3V.

■ Analog Output Circuit

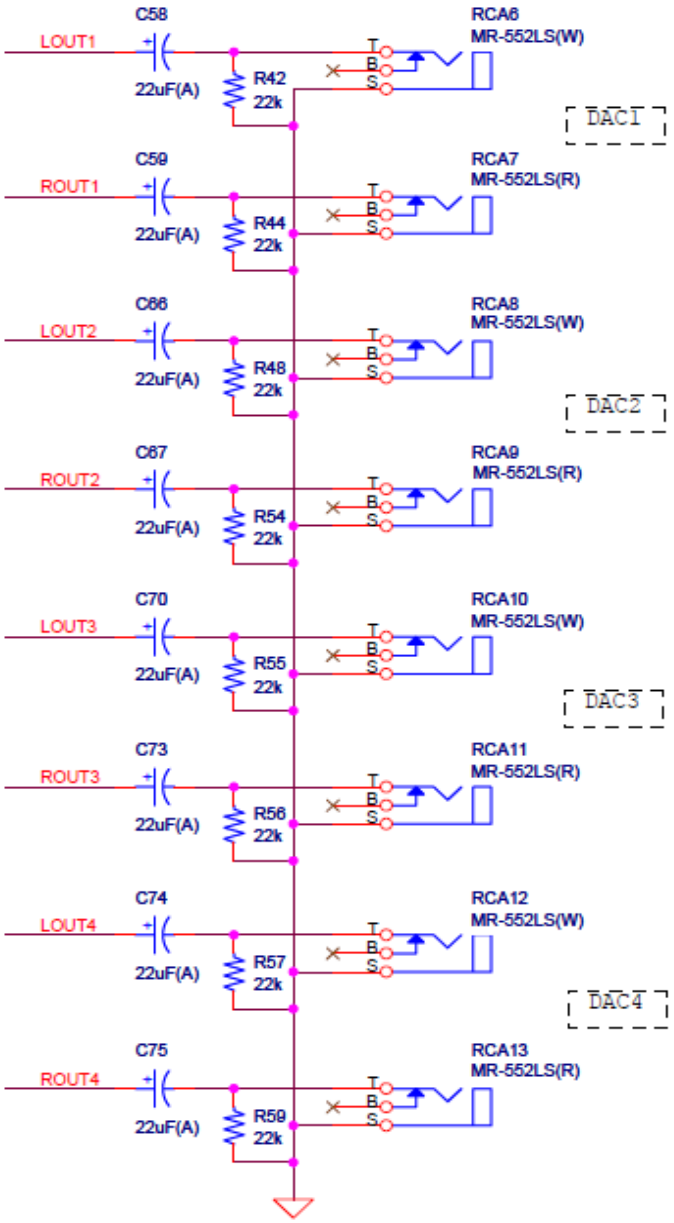


Figure 6. Analog Output Circuit for DAC

For DAC analog output, RCA6～RCA13(DAC1～DAC4) are available.
The output range of each channel is 3.4Vpp@5V.

■ Digital Input Circuit (DIR: PORT1)

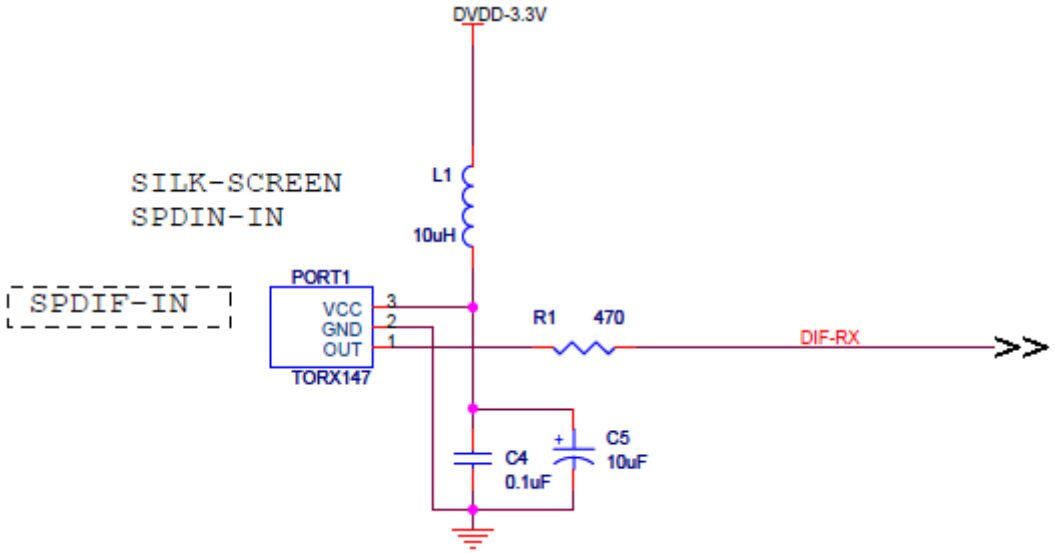


Figure 7. Digital Input Circuit

For digital input SPDIF-IN, optical connector PORT1 is available.

■ Digital Output Circuit (DIT: PORT2)

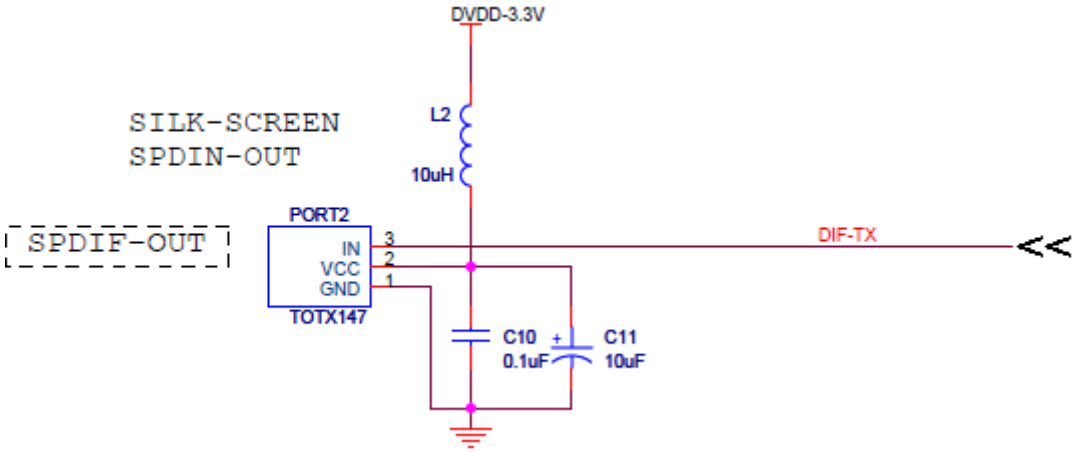


Figure 8. Digital output circuit

For digital output SPDIF-OUT, optical connector PORT2 is available.

Control Software Manual

■ Set-up of the evaluation board and control software

(1) Set up the AKD7782-A according to previous terms.

(2) Connect AKD7782-A to PC with the cable packed.

(3) Insert the CD-ROM labeled “AKD7782-A Evaluation Kit” into the CD-ROM drive.

(4) Access the CD-ROM drive and double-click the icon of “AK7782.exe” to start the control software.
AK7782.exe：Control Software for AK7782

(5) Then please evaluate according to the follows.

■ Operation flow

Keep the following flow

(1) Start the control software according to the explanation above.
(2) Select the needed dialogue to evaluate by modifying the setting. (If the USB cable is removed when control software is used, please close the software and start it again when operation is needed again.)

■ Description of Control Software

(1) Main Dialogue

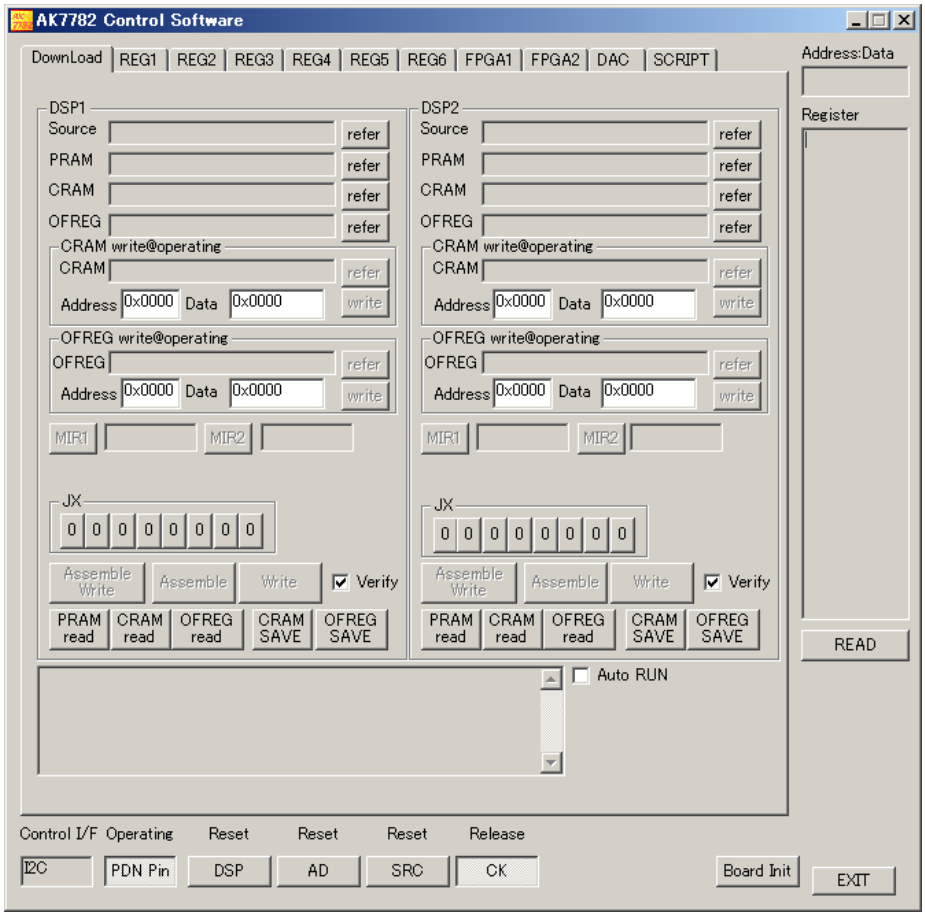


Figure 9. Main Dialogue of Control Software

Control software is used to download program, to set up the registers of AK7782 and FPGA and to process script file. These functions can be selected by the tab items above. The buttons of control signals which are frequently used and the initialization buttons are placed outside the tab dialogue. The control interface of the control software, "Serial (4 lines)" or "I2C", is displayed in the "Control I/F" column.

[PDN pin] : Initial Reset. It is used to initialize AK7782.
[DSP] : DSP Reset.
[AD] : AD Reset.
[SRC] : SRC Reset.
[CK]: Clock Reset. Clock Reset is required when changing the clock mode or the frequency of input clock without initial reset. The registers will not be initialized.
[Board Init]: Execute initial reset and then write the setting of AK7782's registers, FPGA and AK4118A on the software to the board again.
[READ]: Read back the setting of registers of AK7782 and display them in "Register" column.
[EXIT]: Close the control soft.

(2) “DownLoad” Dialogue

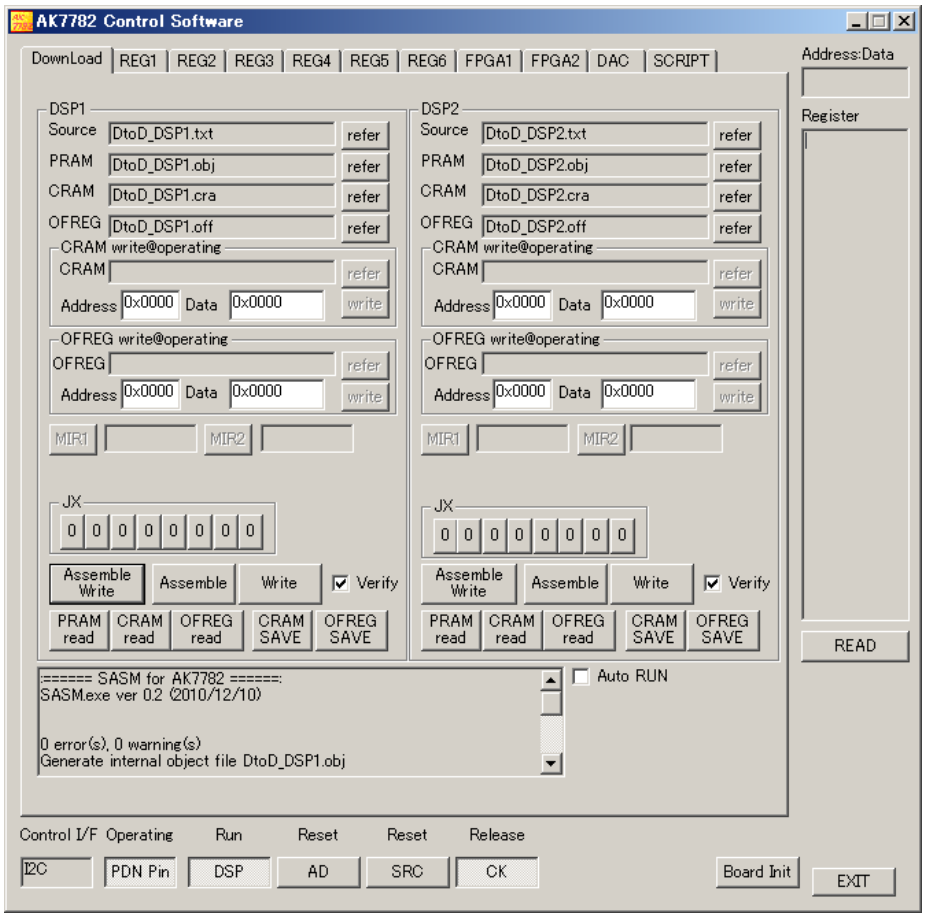


Figure 10. “DownLoad” Dialogue

Because AK7782 has two DSP cores, there are two sets of control buttons on the dialogue for DSP1 and DSP2, like program select columns, JX setup buttons and so on. The following descriptions are common to DSP1 and DSP2.

File of Source column, Program column, CRAM column or OFREG column can be selected by clicking the [refer] button of each column or by way of dropping or tracking files from desktop.

CRAM file or OFREG file can be selected and be written to CRAM or OFREG by clicking the [refer] button of CRAM write@operation column or OFREG write@operation column when system is running. The data will be written to specific address of CRAM or OFREG when the [write] button at right side is clicked.

[Assemble]: Compile the source file and the output file will be selected to the download file automatically.
[Write]: Download the program file to AK7782.
[Assemble Write]: Compile the source file and then download the program file to AK7782.
[PRAM read]: Read the data of PRAM to temporary file and then open the file.
[CRAM read]: Read the data of CRAM to temporary file and then open the file.
[OFREG read]: Read the data of OFREG to temporary file and then open the file.
[CRAM SAVE]: Read the data of CRAM and save to file.
[OFREG SAVE]: Read the data of OFREG and save to file.
[MIR1/MIR2]: Read the data of register MIR1/MIR2 when program is running and display the result.
[JX]: JX code setting column.
[Verify]: When it is checked, the verification of data will be done when downloading files to AK7782.
[Auto RUN]: When it is checked, DSP/AD/SRC will be released and AK7782 will be set to run mode automatically after downloading data to AK7782. Otherwise, AK7782 will be set to DSP reset mode after downloading.

(3) "REG" Dialogue

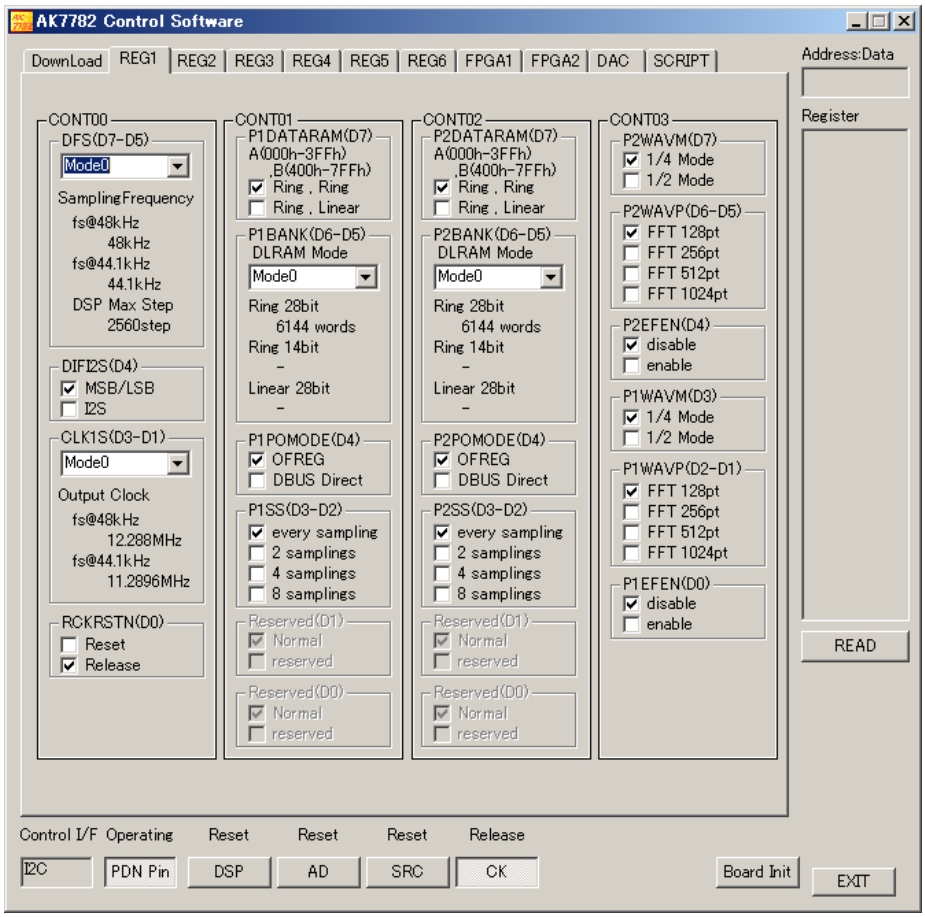


Figure 11. "REG1" Dialogue

Dialogues REG1~REG6 are used to set up the register of AK7782. (It is prohibited to modify test and reserved items.) As the checkbox is clicked, the data will be written to AK7782. Please set up the registers during system reset mode.

The reference pages of registers in datasheet are as follows:

Register	Reference Page		Register	Reference Page
CONT00	31		CONT0C	43
CONT01	32		CONT0D	44
CONT02	33		CONT0E	45
CONT03	34		CONT0F	46
CONT04	35		CONT10	47
CONT05	36		CONT11	48
CONT06	37		CONT12	49
CONT07	38		CONT13	50
CONT08	39		CONT14	51
CONT09	40		CONT15	52
CONT0A	41		CONT16	53
CONT0B	42			

Table 6. Reference page of registers

(4) “FPGA” Dialogue

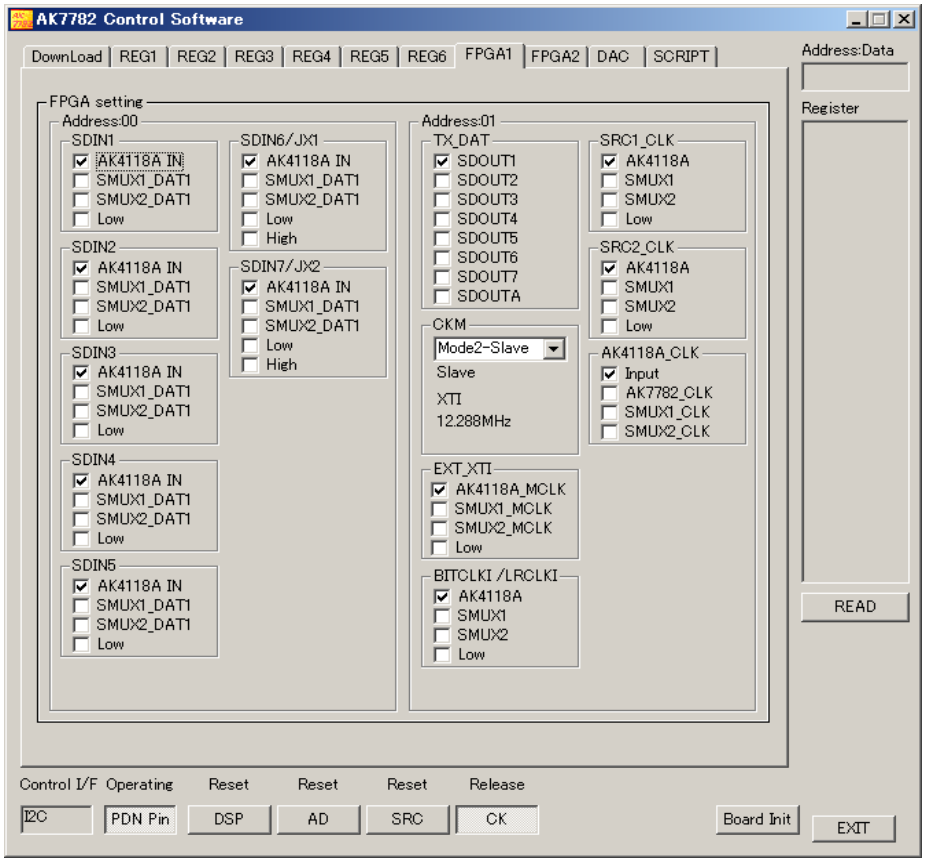


Figure 12. “FPGA1” Dialogue

FPGA1/FPGA2 dialogues are used to modify the data path and the setting of AK4118A.
(It is prohibited to modify test and reserved items.)

FPGA Setting Table： （Bold type items are the default setting.）

ADDRESS：00

Bit	Function	Description
D[15:14]	SDIN1	Input data source to SDIN1 pin of AK7782 **00 : AK4118A-IN** 01 : SMUX1-DAT1 10 : SMUX2-DAT1 11 : LOW
D[13:12]	SDIN2	Input data source to SDIN2 pin of AK7782 **00 : AK4118A-IN** 01 : SMUX1-DAT1 10 : SMUX2-DAT1 11 : LOW
D[11:10]	SDIN3	Input data source to SDIN3 pin of AK7782 **00 : AK4118A-IN** 01 : SMUX1-DAT1 10 : SMUX2-DAT1 11 : LOW
D[9:8]	SDIN4	Input data source to SDIN4 pin of AK7782 **00 : AK4118A-IN** 01 : SMUX1-DAT1 10 : SMUX2-DAT1 11 : LOW

D[7:6]	SDIN5	Input data source to SDIN5 pin of AK7782 **00 : AK4118A-IN** 01 : SMUX1-DAT1 10 : SMUX2-DAT1 11 : LOW
D[5:3]	SDIN6/JX1	Input data source to SDIN6/JX1 pin of AK7782 **000 : AK4118A-IN** 001 : SMUX1-DAT1 010 : SMUX2-DAT1 011 : LOW 100 : HIGH
D[2:0]	SDIN7/JX2	Input data source to SDIN7/JX2 pin of AK7782 **000 : AK4118A-IN** 001 : SMUX1-DAT1 010 : SMUX2-DAT1 011 : LOW 100 : HIGH

Table 7. FPGA Setting Table 1

ADDRESS : 01

Bit	Function	Description
D[15:13]	TX-DAT	Output data source to AK4118A **000 : SDOUT1** 001 : SDOUT2 010 : SDOUT3 011 : SDOUT4 100 : SDOUT5 101 : SDOUT6 110 : SDOUT7 111 : SDOUTA
D[12:10]	CKM Mode	High/Low setup of AK7782's CKM[2:0] pin 000 : CKM Mode 0 – Master 001 : CKM Mode 1 – Master **010 : CKM Mode 2 – Slave** 011 : CKM Mode 3 – Slave 100 : CKM Mode 4 – Slave 101 : CKM Mode 5 – Slave
D[9:8]	EXT-XTI	Input clock source to XTI pin of AK7782 **000 : AK4118A-MCLK** 001 : SMUX1-MCLK 010 : SMUX2-MCLK 011 : LOW
D[7:6]	BITCLKI/LRCLKI	Input clock source to BITCLKI/LRCLKI pin of AK7782 **00 : AK4118A** 01 : SMUX1 10 : SMUX2 11 : LOW
D[5:4]	SRC1-CLK	Input clock source to SRCBICK/SRCLRCK pin of AK7782 **00 : AK4118A** 01 : SMUX1 10 : SMUX2 11 : LOW
D[3:2]	SRC2-CLK	Input clock source to SRC2BICK/SRC2LRCK pin of AK7782 **00 : AK4118A** 01 : SMUX1 10 : SMUX2 11 : LOW

D[1:0]	AK4118A-CLK	I/O clock setup of AK4118A **00 : Input** 01 : AK7782-CLK 10 : SMUX1-CLK 11 : SMUX2-CLK

Table 8. FPGA Setting Table 2

ADDRESS : 02

Bit	Function	Description (Check Box only)
D[15]	AK4118A-PDN	High/Low setup of AK4118A's PDN pin **Default : H**
D[14]	DAC-PDN	High/Low setup of AK4359's PDN pin **Default : H**
D[13]	PADRSTN	High/Low setup of AK7782's PADRSTN pin **Default : L**
D[12]	PSRCRSTN	High/Low setup of AK7782's PSRCRSTN pin **Default : L**
D[11]	PDSPRSTN	High/Low setup of AK7782's PDSPRSTN pin **Default : L**
D[10]	PCKRSTN	High/Low setup of AK7782's PCKRSTN pin **Default : H**
D[9]	PSRCSMUTE	High/Low setup of AK7782's PSRCSMUTE pin **Default : L**
D[8]	TESTI1	High/Low setup of AK7782's TESTI1 pin **Default : L**
D[7]	TESTI2	High/Low setup of AK7782's TESTI2 pin **Default : L**
D[6]	JX0	High/Low setup of AK7782's JX0 pin **Default : L**
D[5:0]	Reserved	

Table 9. FPGA Setting Table 3

ADDRESS : 03

Bit	Function	Description
D[15:14]	SMUX1-CLK	I/O clock setup of SMUX1 00 : Input **01 : AK7782-CLK** 10 : AK4118A-CLK 11 : SMUX2-CLK
D[13:12]	SMUX2-CLK	I/O clock setup of SMUX2 00 : Input **01 : AK7782-CLK** 10 : AK4118A-CLK 11 : SMUX1-CLK
D[11:9]	SMUX1-DAT2	Output data source to DAT2 pin of SMUX PORT1 **000 : SDOUT1** 001 : SDOUT2 010 : SDOUT3 011 : SDOUT4 100 : SDOUT5 101 : SDOUT6 110 : SDOUT7 111 : SDOUTA
D[8:6]	SMUX2-DAT2	Output data source to DAT2 pin of SMUX PORT2 **000 : SDOUT1** 001 : SDOUT2 010 : SDOUT3

		011 : SDOUT4 100 : SDOUT5 101 : SDOUT6 110 : SDOUT7 111 : SDOUTA
D[5:4]	CAD[1:0]	High/Low setup of AK7782's CAD1,CAD0 pin **00 : Low, Low** 01 : Low, High 10 : High, Low 11 : High, High
D[3]	DAC-OUT1	Output data source to DAC1 **0 : SDOUT1** 1 : SDOUT5
D[2]	DAC-OUT2	Output data source to DAC2 **0 : SDOUT2** 1 : SDOUT6
D[1]	DAC-OUT3	Output data source to DAC3 **0 : SDOUT3** 1 : SDOUT7
D[0]	DAC-OUT4	Output data source to DAC4 **0 : SDOUT4** 1 : SDOUTA

Table 10. FPGA Setting Table 4

AK4118A Setting Table:

Function	Description
MCLK	Frequency of main clock output from AK4118A **00: 265fs** 01: 256fs 10: 512fs 11: 128fs
CM	Master clock operation mode of AK4118A 00: CM = 00 01: CM = 01 **10: CM = 10** 11: CM = 11
DIF	Audio I/O format of AK4118A 000: 16bit Right(O) 001: 18bit Right(O) 010: 20bit Right(O) 011: 24bit Right(O) **100: 24bit Left(O)** 101: 24bit I2S(O) 110: 24bit Left(I) 111: 24bit I2S(I)

Table 11. AK4118A Setting Table

(5) “SCRIPT” Dialogue

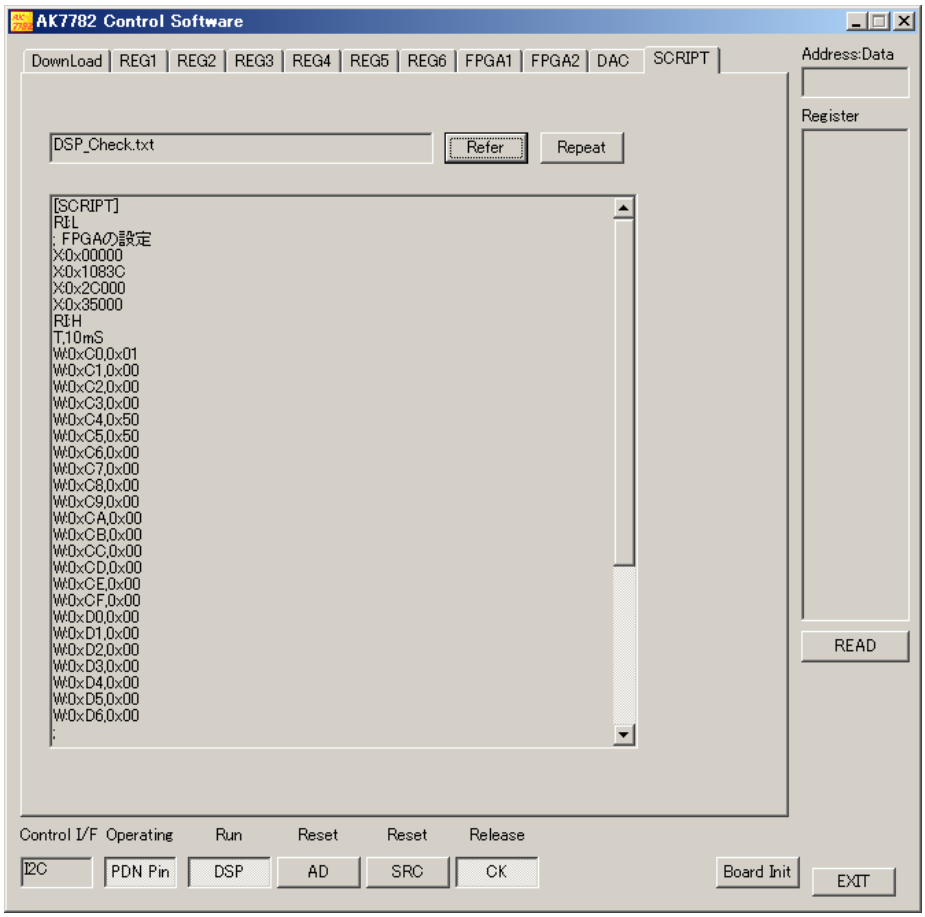


Figure 13. “SCRIPT” Dialogue

As the script file is selected, it will be executed directly. If [Repeat] button is clicked, the selected script file will be executed once again.

Command	Description
[SCRIPT]	Header of script file. The script file will be compiled to error without this header.
;注釈	The content after semicolon is ignored as comment.
W,<address>,<data> W,0xC0,0x00	Write data to register. Both address and data must be BYTE (8bit).
WL,<command>,<address>,<data>,… WL,0x82,0x0022,0x4000,0x4000,0x4000	Write data continuously. It can be used when CRAM is running. The command must be BYTE (8bit) and the data below must be WORD (16bit).
WS,<command>,<address>,<data>,… WS,0x81,0x00,0x22,0x40,0x00,0x40,0x00	Write data continuously. It can be used when CRAM is running. The command, address and data must be BYTE (8bit).
RI : H / RI : L RA : H / RA : L RD : H / RD : L RR : H / RR : L RC : H / RC : L	Init Reset ADC Reset DSP Reset SRC Reset CK Reset
D,<address>,<data>	Write data to AK4118A.
X,<address>,<data>	Write data to the registers of FPGA.
A,<address>,<data>	Write data to the registers of AK4359.
P,<message>	Show message and pause the processing of script.
T,<wait> T,50mS	Wait some milliseconds. When actual operation, it is possible to wait longer than this.
LP1:<filename> / LP2:<filename>	Download program file to DSP1/DSP2.
LC1:<filename> / LC2:<filename>	Download CRAM file to DSP1/DSP2.
LO1:<filename> / LO2:<filename>	Download OFREG file to DSP/DSP2.

Table 12. Script Command Table

Measurement Results

[Measurement condition]

- Measurement unit : Audio Precision, System two Cascade
- MCKI : 12.288MHz
- BICK : 64fs
- fs : 48kHz, 96kHz
- Bit : 24bit
- Measurement Mode : CKM Mode 0, Master Mode
- Power Supply : +12V, GND
- Input Frequency : 1kHz
- Measurement Frequency : 20 ~ 20kHz@48kHz, 20Hz ~ 40kHz@96kHz
- Temperature : Room

[Measurement Results]

1. ADC1

		Result		Unit
		Lch	Rch	
ADC1 : AIN1(Differential) => ADC1 => SDOUTA1				
S/(N+D)	fs = 48kHz (-1dBFS)	90.4	90.3	dB
	fs = 96kHz (-1dBFS)	87.5	87.4	
DR	fs = 48kHz (-60dBFS, A-Weighted)	96.1	96.1	dB
	fs = 96kHz (-60dBFS)	92.3	92.2	
S/N	fs = 48kHz (A-weighted)	96.2	96.1	dB
	fs = 96kHz	92.3	92.3	

2. ADC2

		Result		Unit
		Lch	Rch	
ADC2 : AIN1(Differential) => ADC2 => SDOUTA1				
S/(N+D)	fs = 48kHz (-1dBFS)	90.2	90.2	dB
	fs = 96kHz (-1dBFS)	87.3	87.3	
DR	fs = 48kHz (-60dBFS, A-Weighted)	96.0	96.1	dB
	fs = 96kHz (-60dBFS)	92.3	92.4	
S/N	fs = 48kHz (A-weighted)	96.2	96.2	dB
	fs = 96kHz	92.4	92.4	

3. ADCM

		Result	Unit
ADCM : ADCM => ADCM => SDOUT7			
S/(N+D)	fs = 48kHz (-1dBFS)	88.5	dB
	fs = 96kHz (-1dBFS)	87.0	
DR	fs = 48kHz (-60dBFS, A-Weighted)	95.5	dB
	fs = 96kHz (-60dBFS)	91.5	
S/N	fs = 48kHz (A-weighted)	95.6	dB
	fs = 96kHz	91.6	

[Plot Data]

1. ADC1 (fs=48kHz)

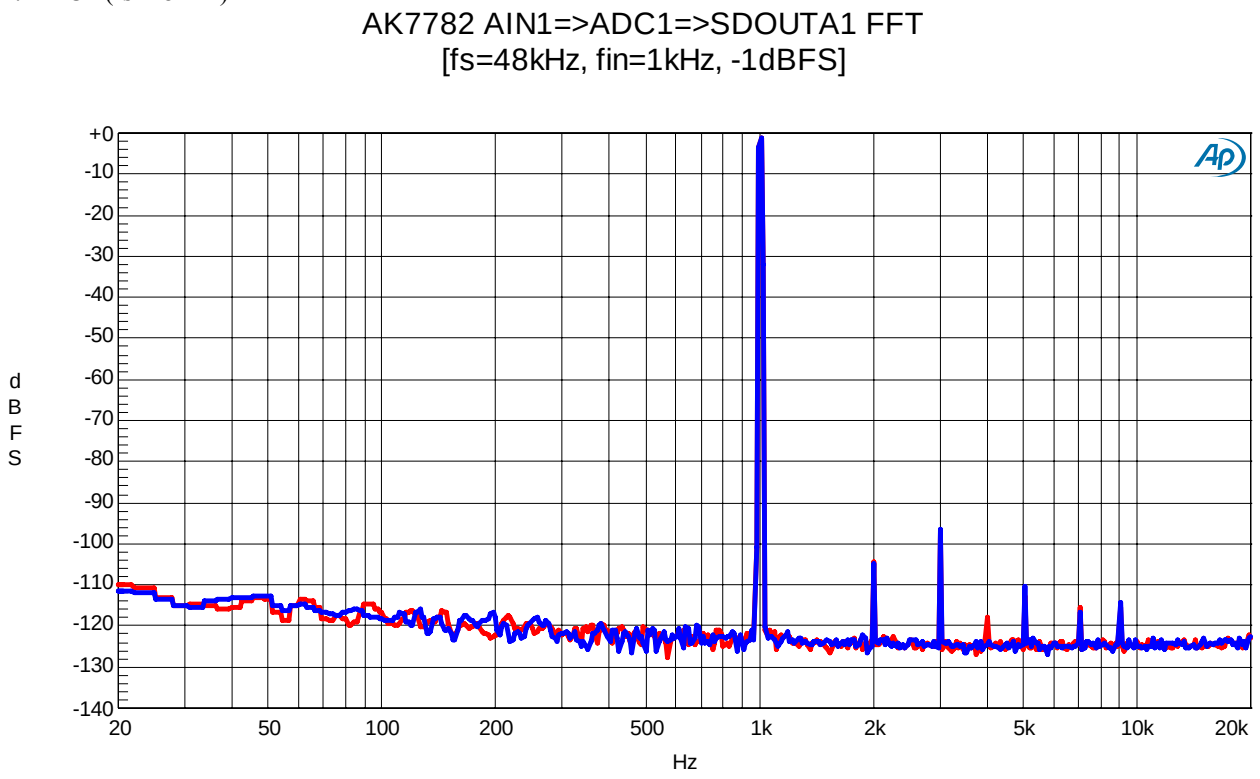


Figure 14. ADC1 – FFT (-1dBFS) [fs=48kHz]

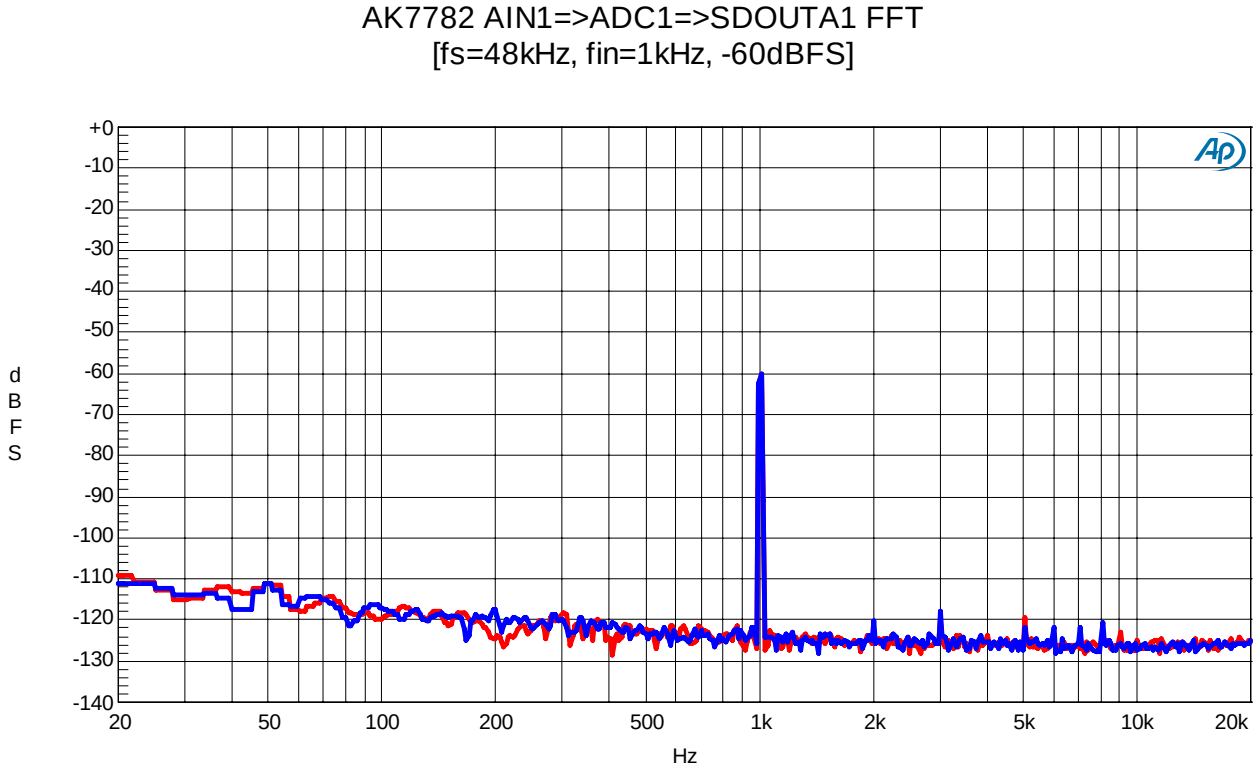


Figure 15. ADC1 – FFT (-60dBFS) [fs=48kHz]

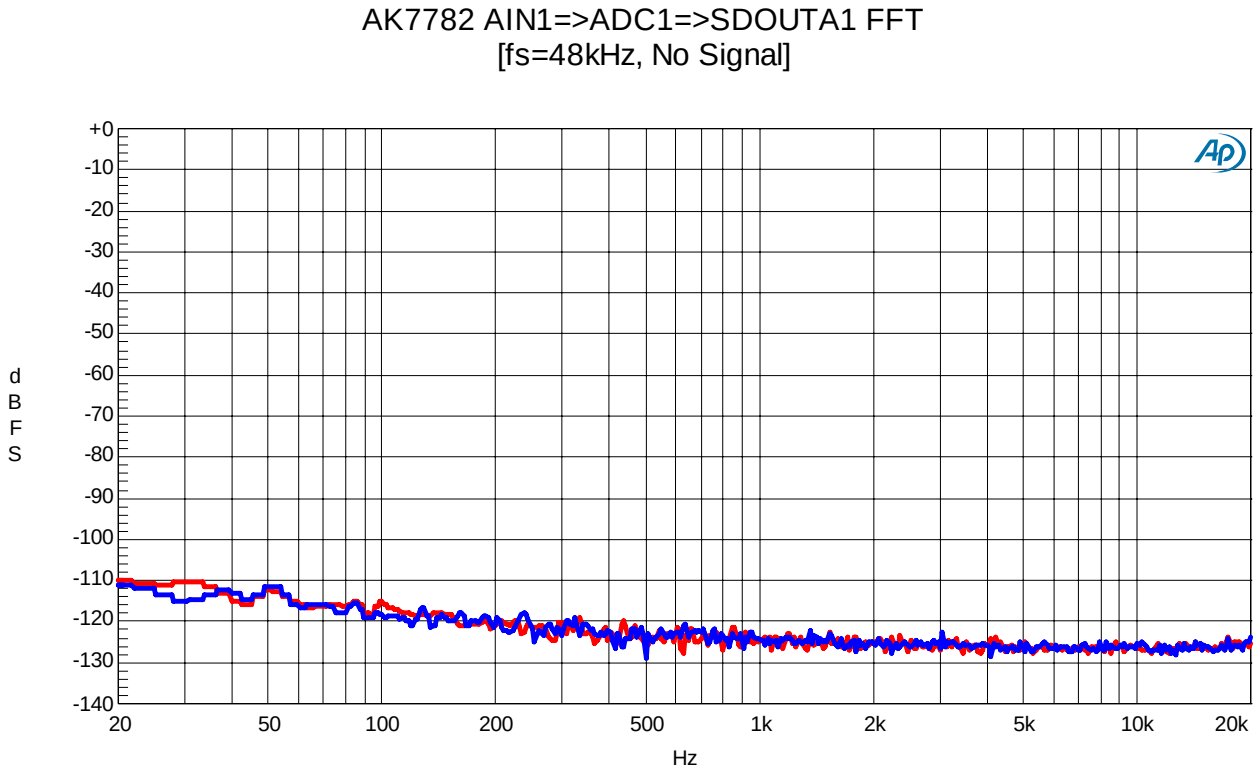


Figure 16. ADC1 – FFT (No Signal) [fs=48kHz]

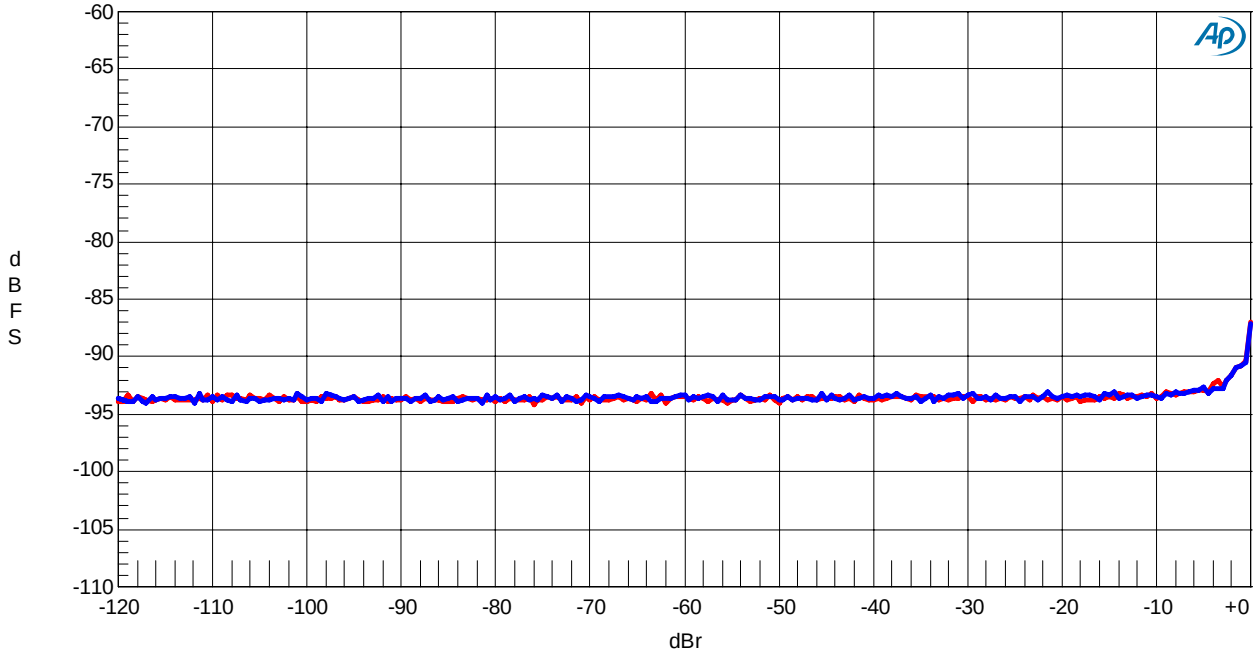


Figure 17. ADC1 – THD+N vs. InputLevel [fs=48kHz]

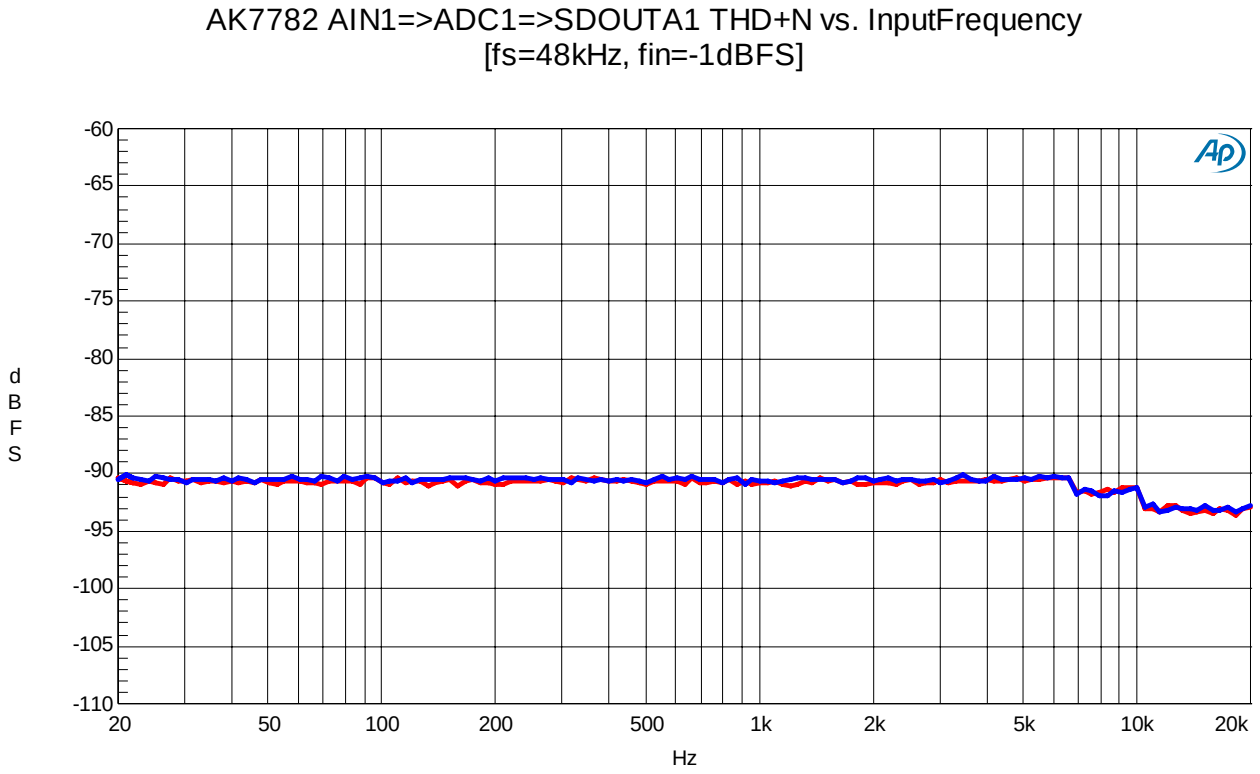


Figure 18. ADC1 – THD+N vs. InputFrequency [fs=48kHz]

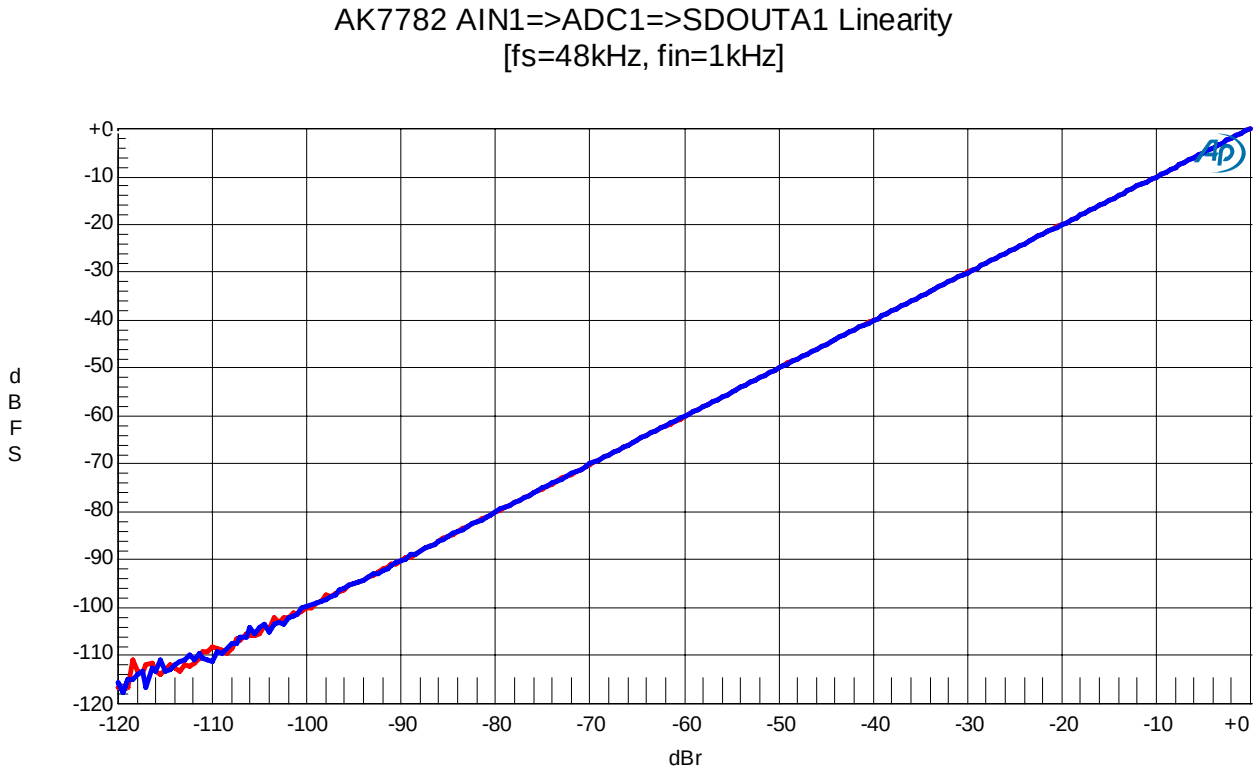


Figure 19. ADC1 – Linearity [fs=48kHz]

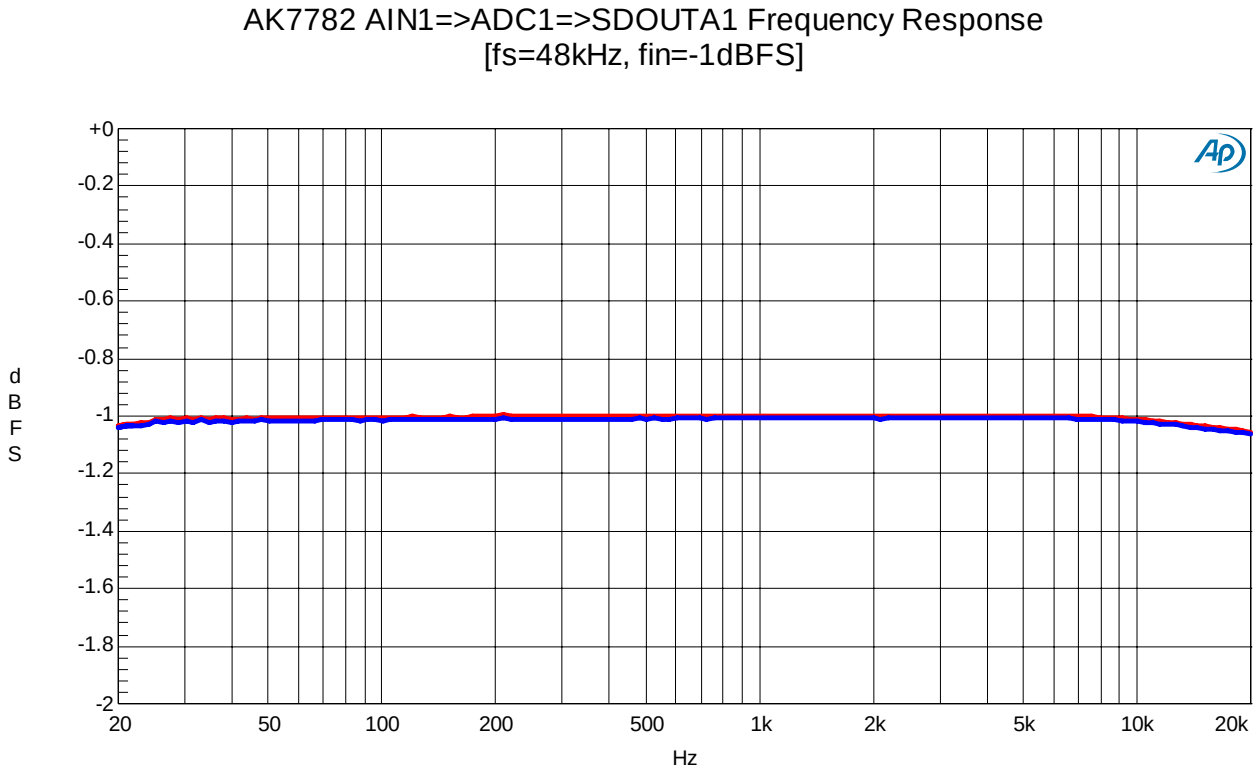


Figure 20. ADC1 – Frequency Response [fs=48kHz]

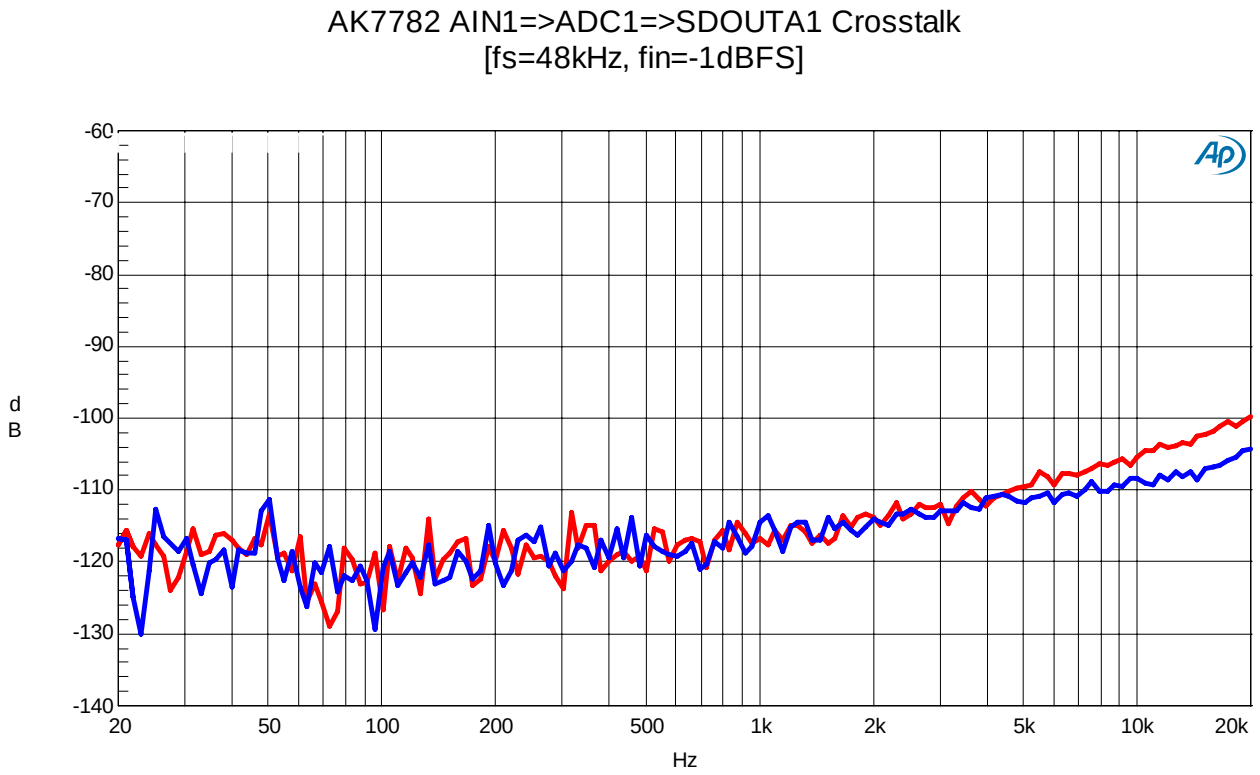


Figure 21. ADC1 – Crosstalk [fs=48kHz]

2. ADC1 (fs=96kHz)

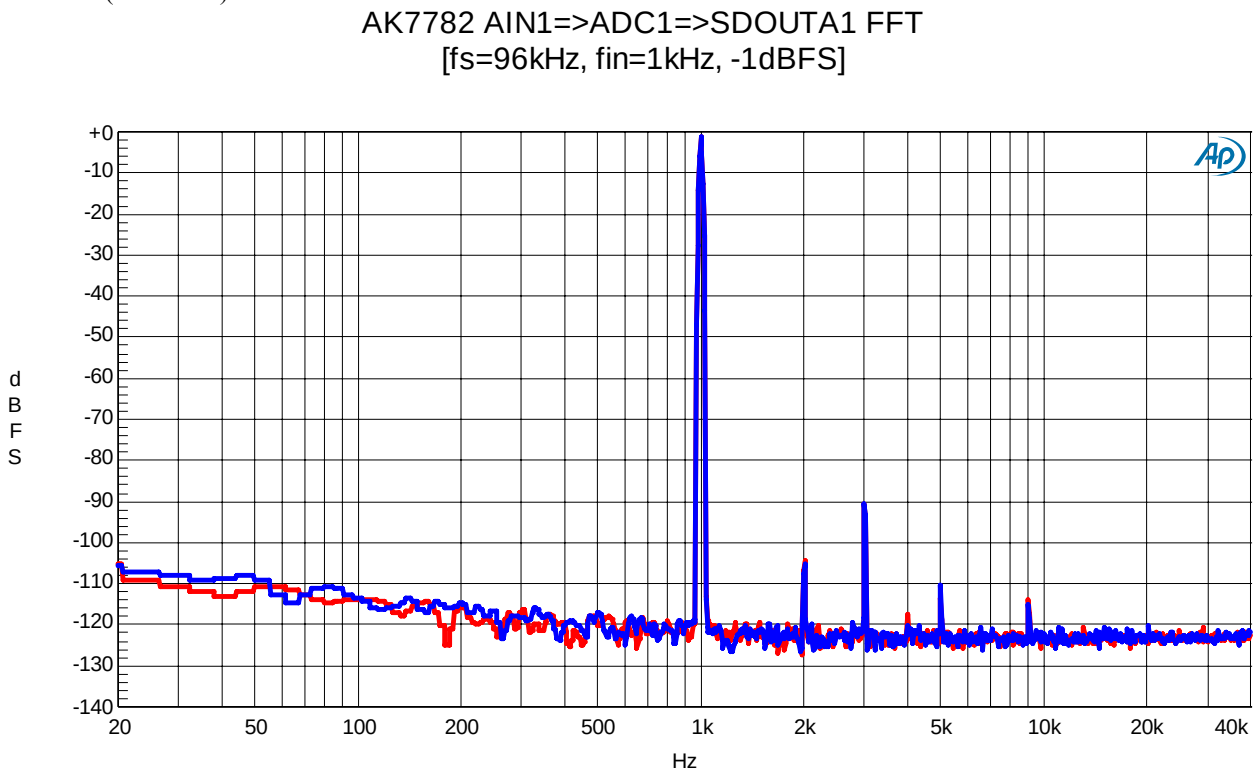


Figure 22. ADC1 – FFT (-1dBFS) [fs=96kHz]

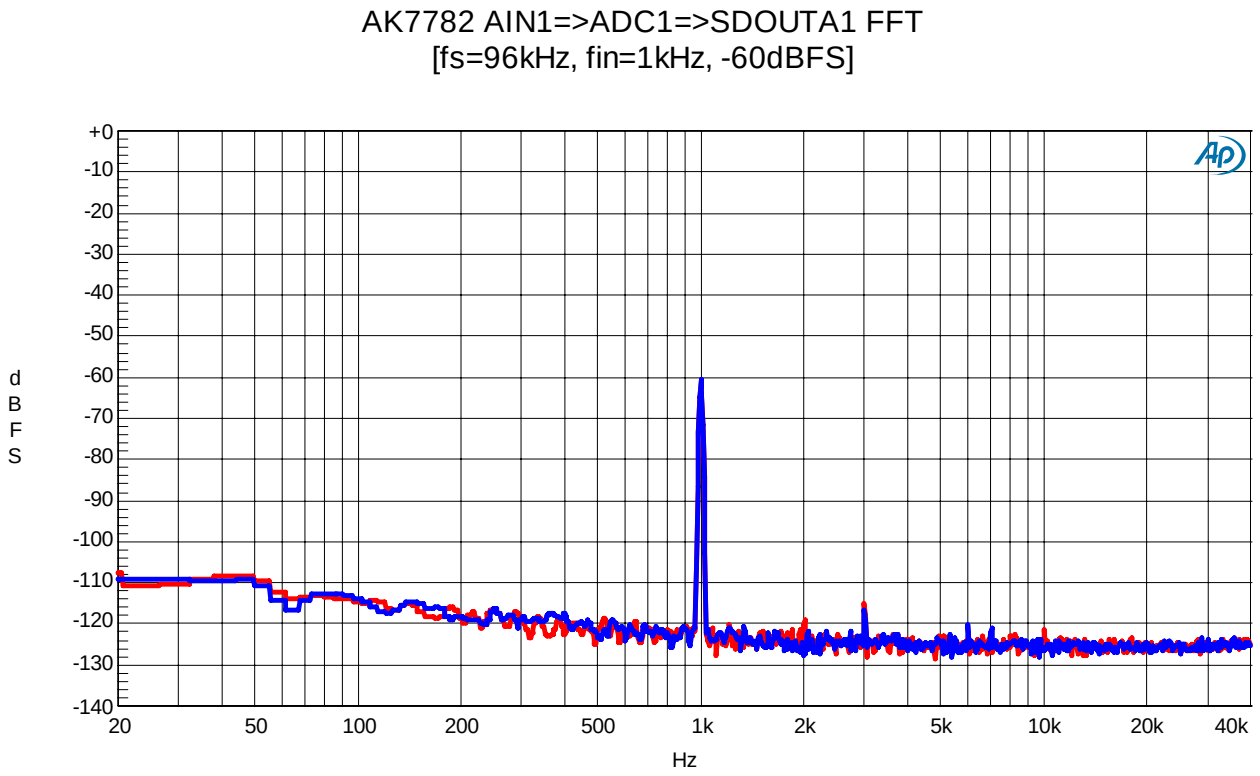


Figure 23. ADC1 – FFT (-60dBFS) [fs=96kHz]

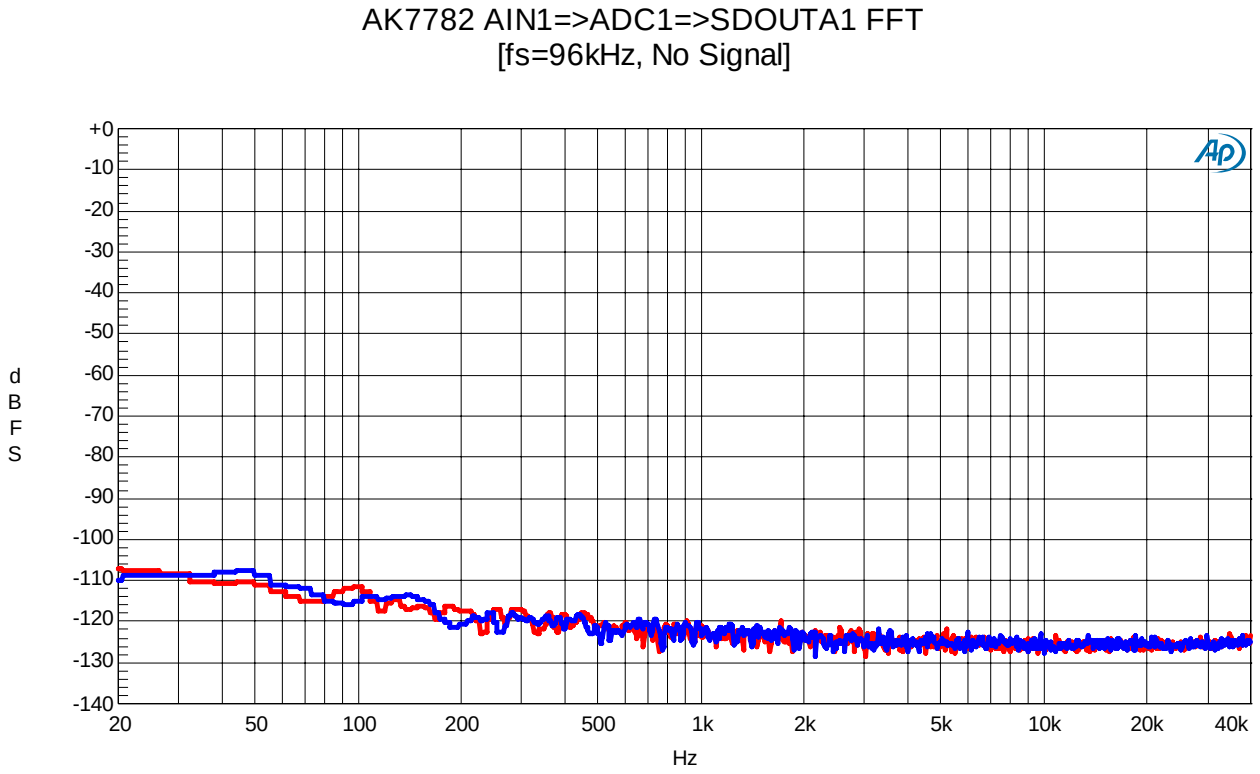


Figure 24. ADC1 – FFT (No Signal) [fs=96kHz]

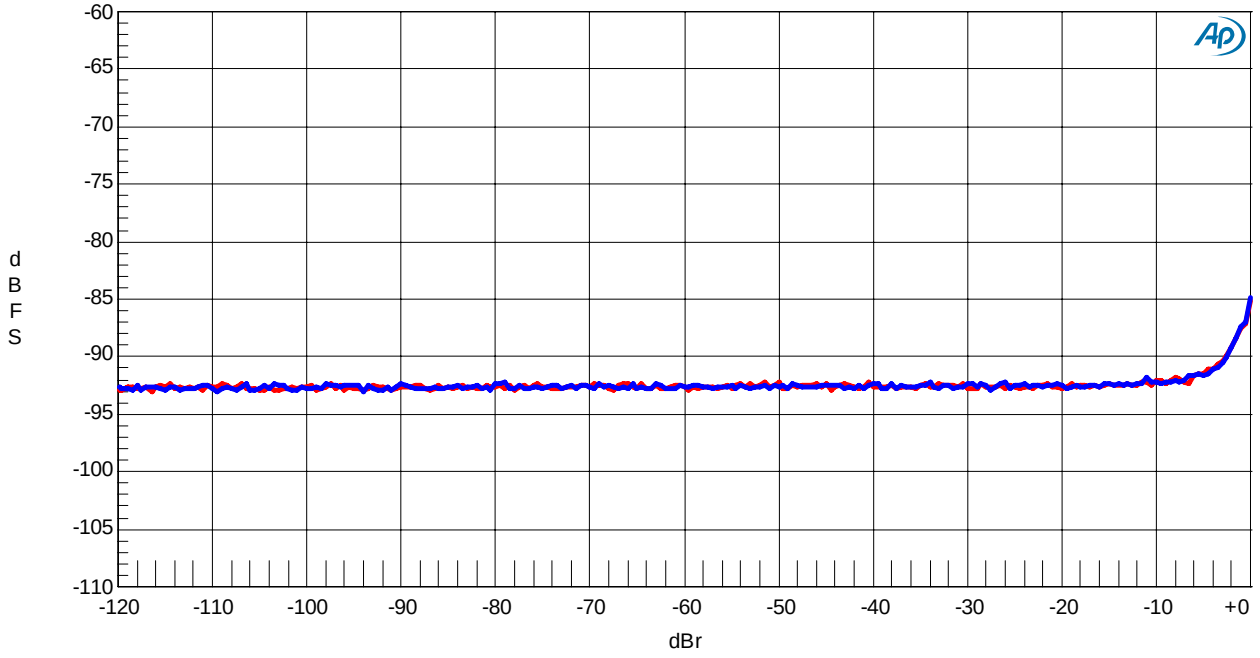


Figure 25. ADC1 – THD+N vs. InputLevel [fs=96kHz]

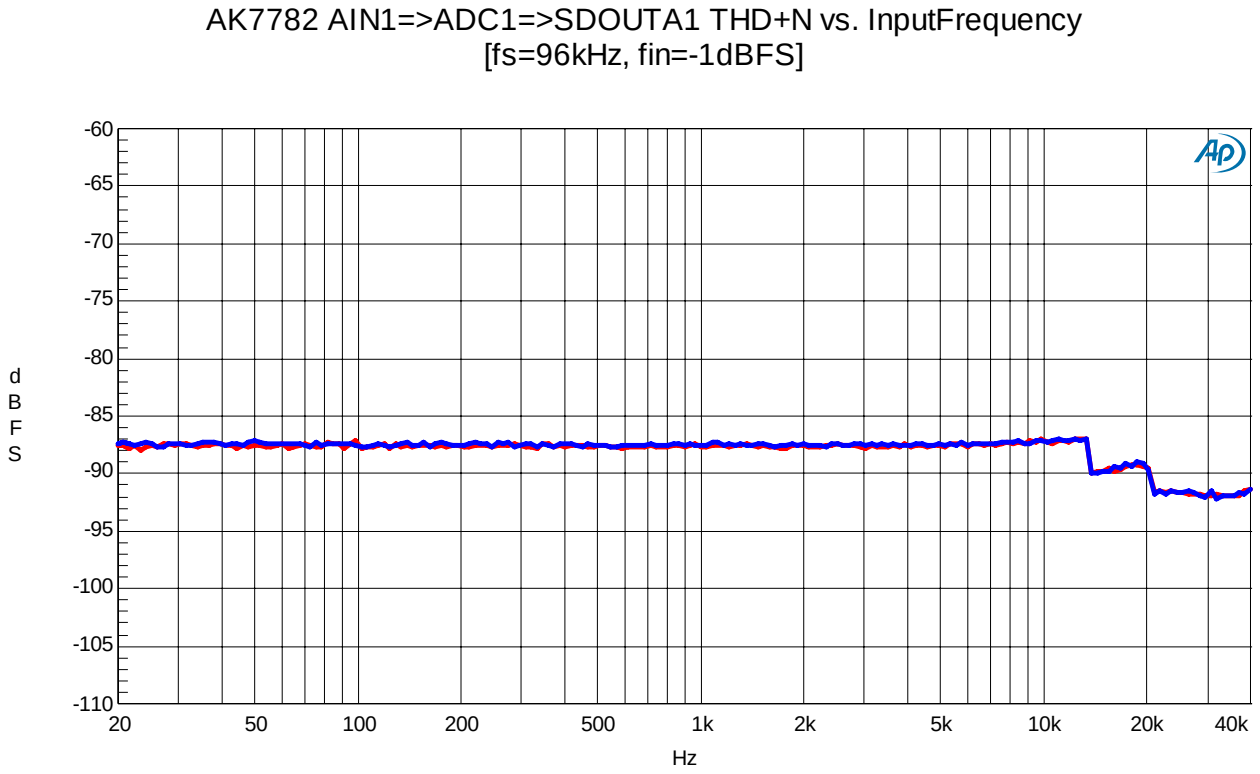


Figure 26. ADC1 – THD+N vs. InputFrequency [fs=96kHz]

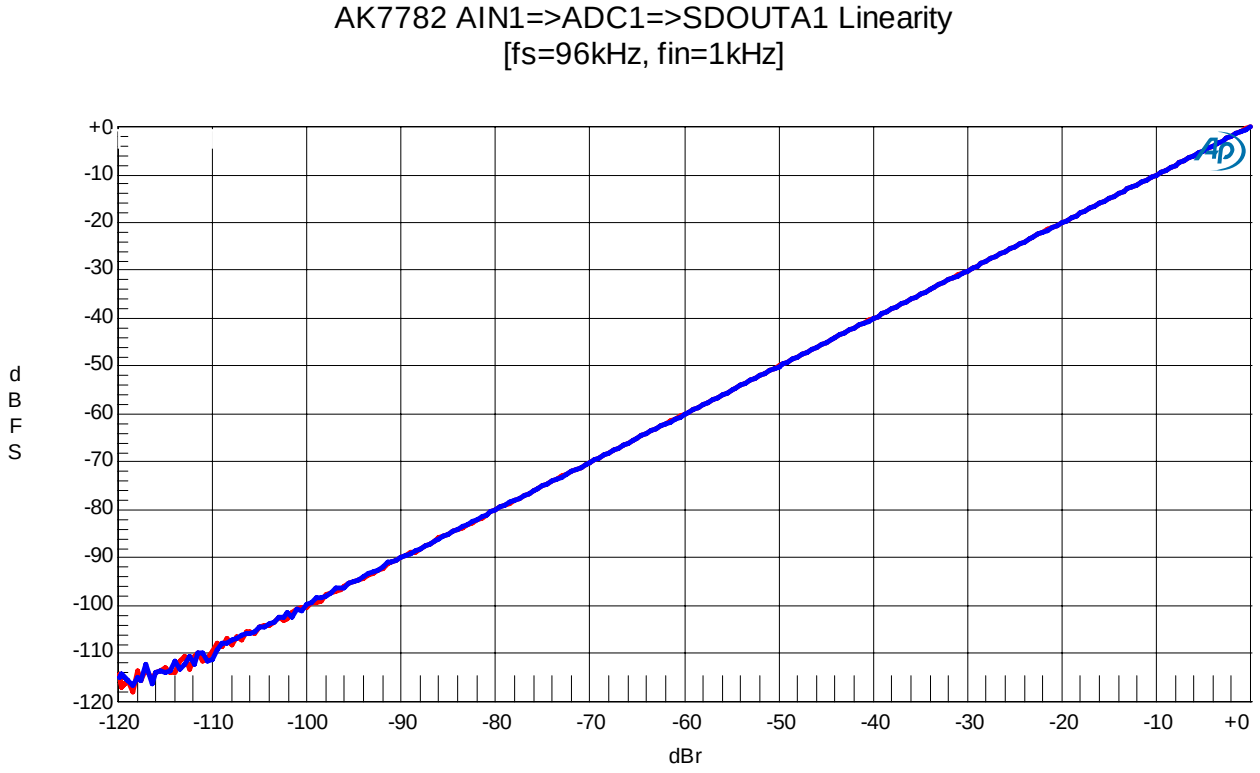


Figure 27. ADC1 – Linearity [fs=96kHz]

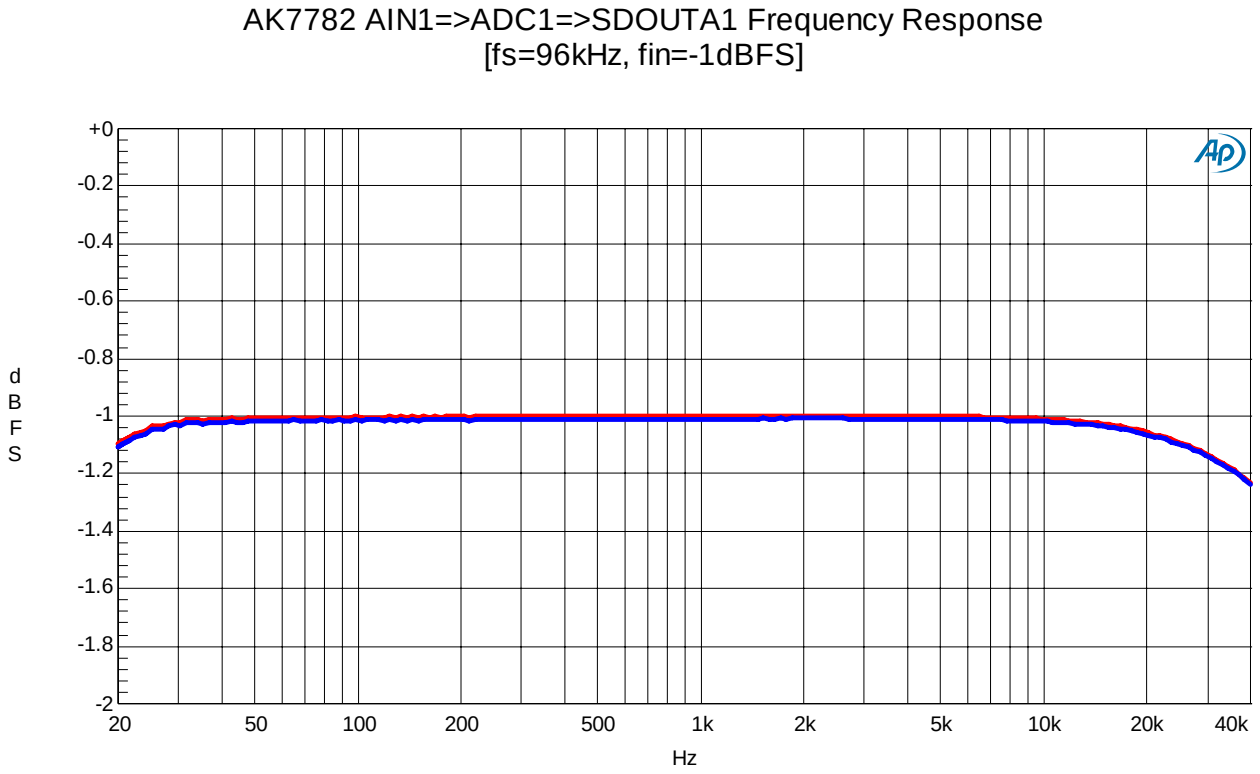


Figure 28. ADC1 – Frequency Response [fs=96kHz]

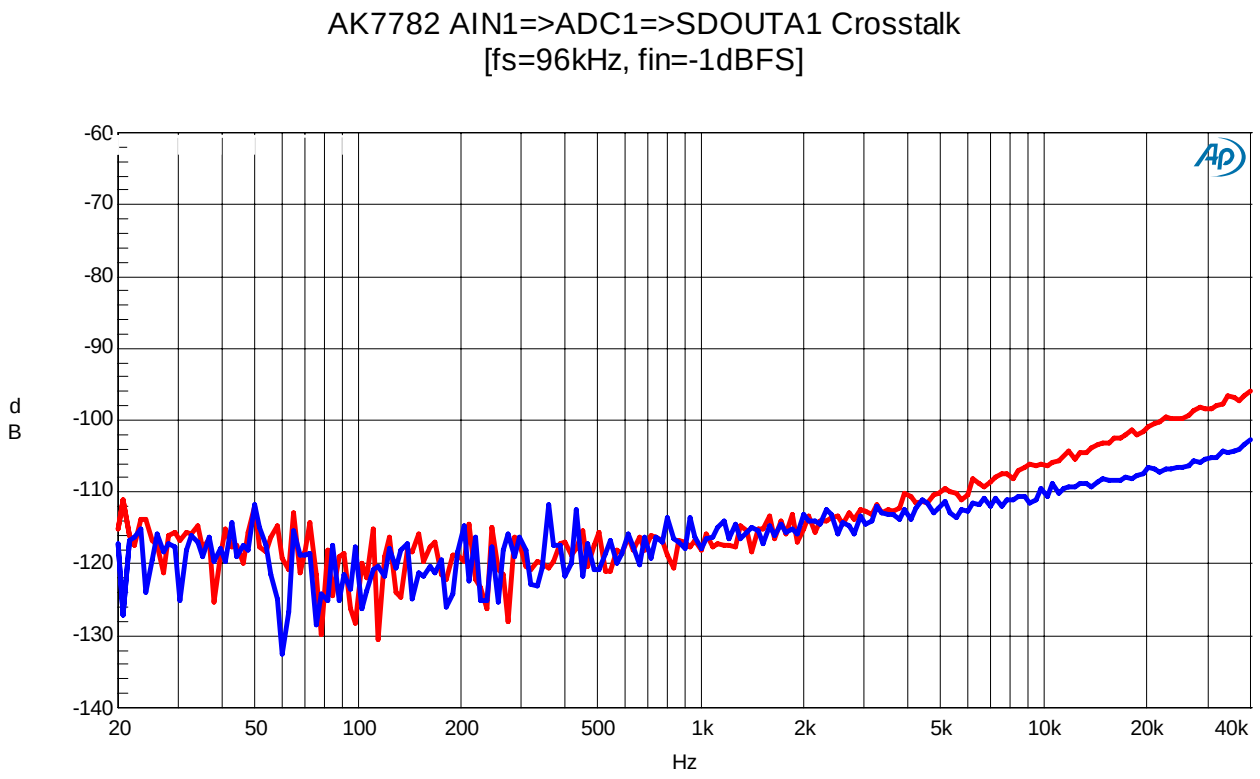


Figure 29. ADC1 – Crosstalk [fs=96kHz]

3. ADC2 (fs=48kHz)

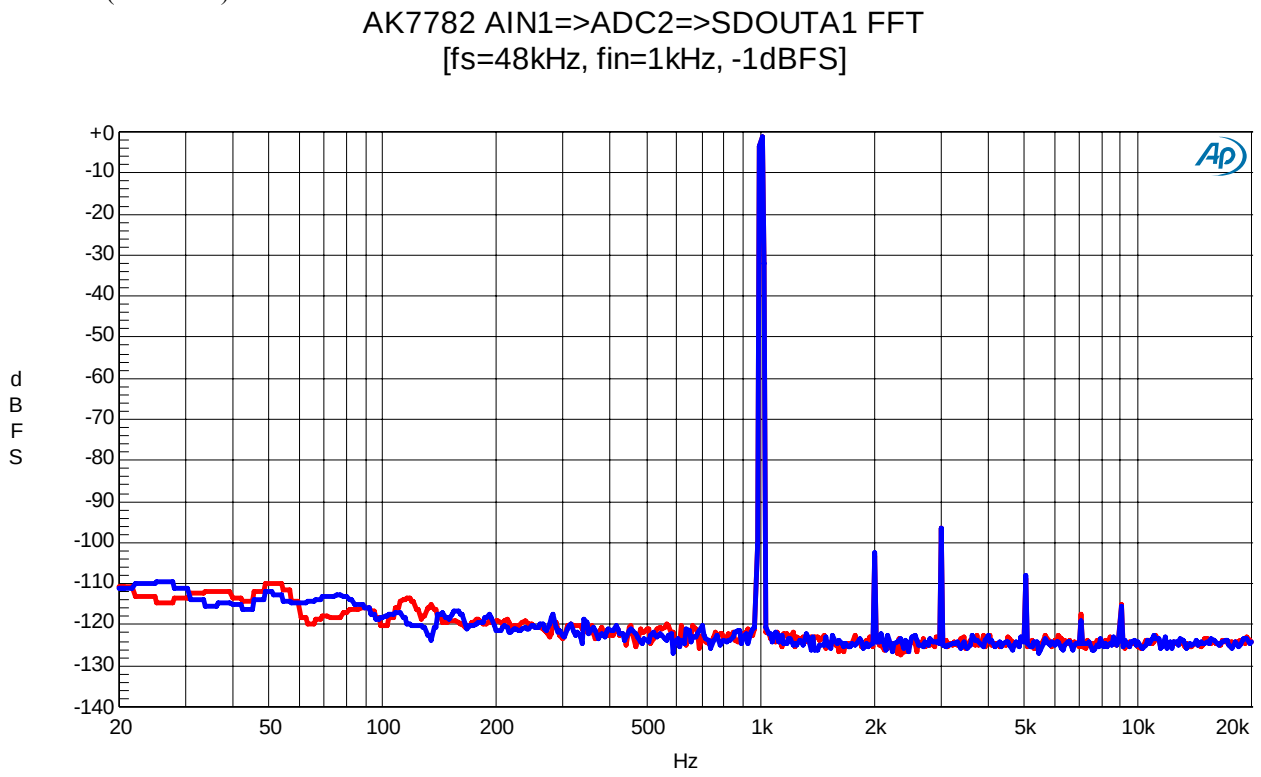


Figure 30. ADC2 – FFT (-1dBFS) [fs=48kHz]

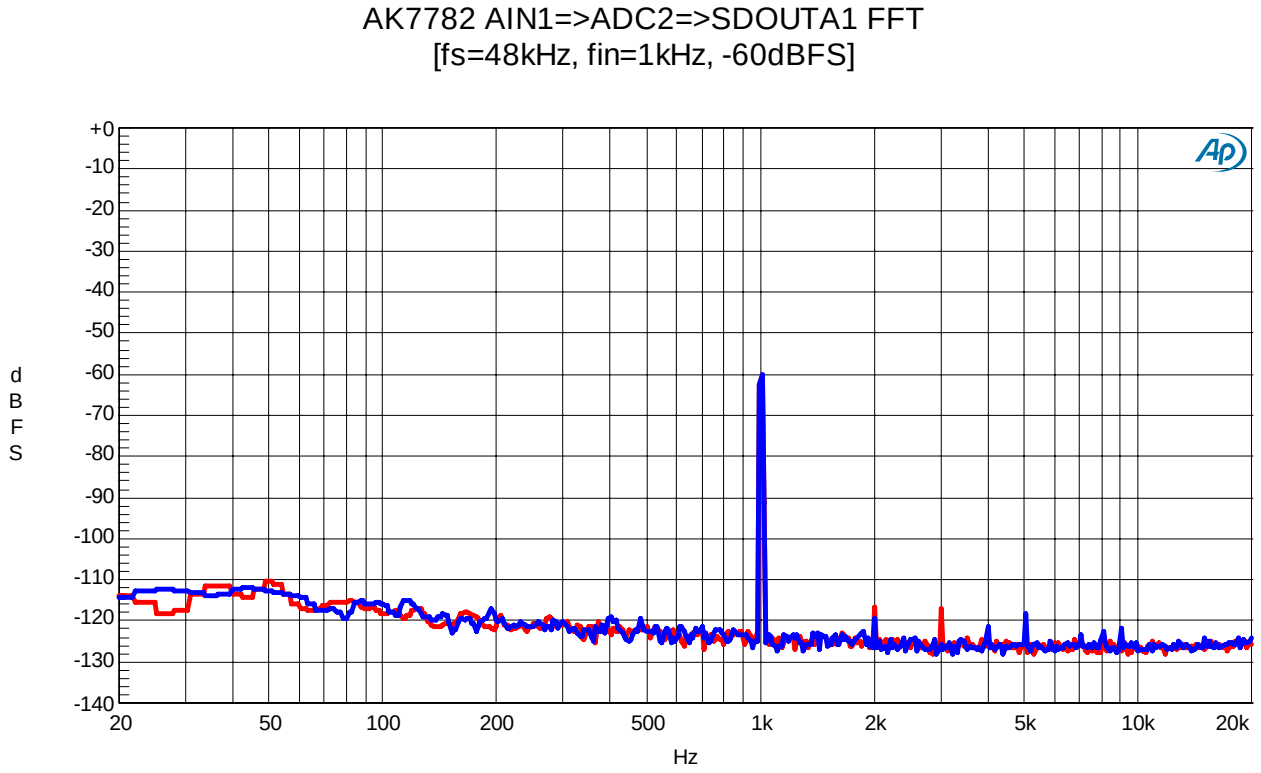


Figure 31. ADC2 – FFT (-60dBFS) [fs=48kHz]

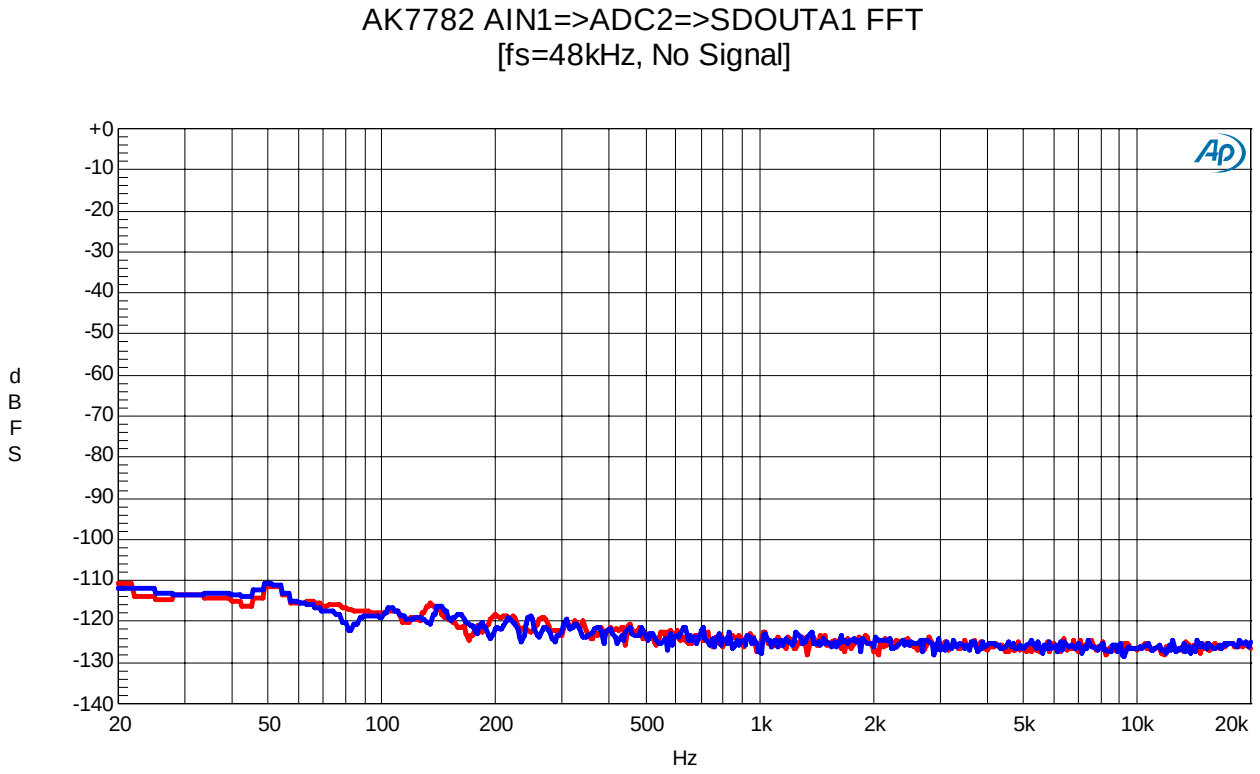


Figure 32. ADC2 – FFT (No Signal) [fs=48kHz]

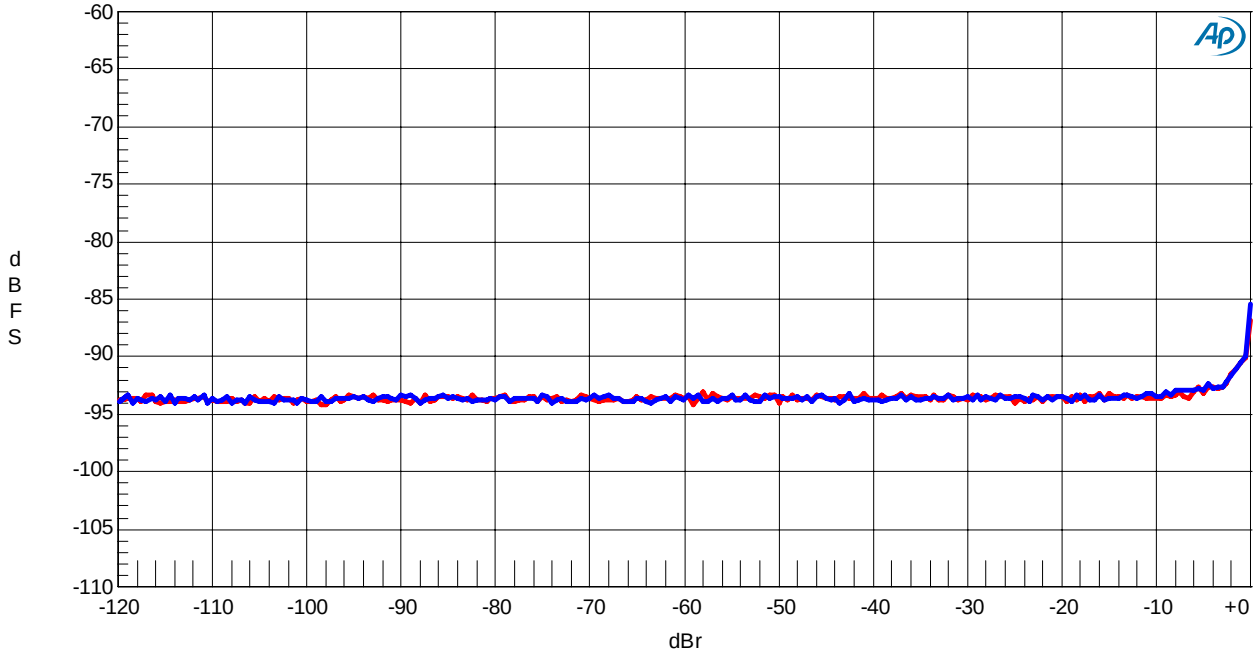


Figure 33. ADC2 – THD+N vs. InputLevel [fs=48kHz]

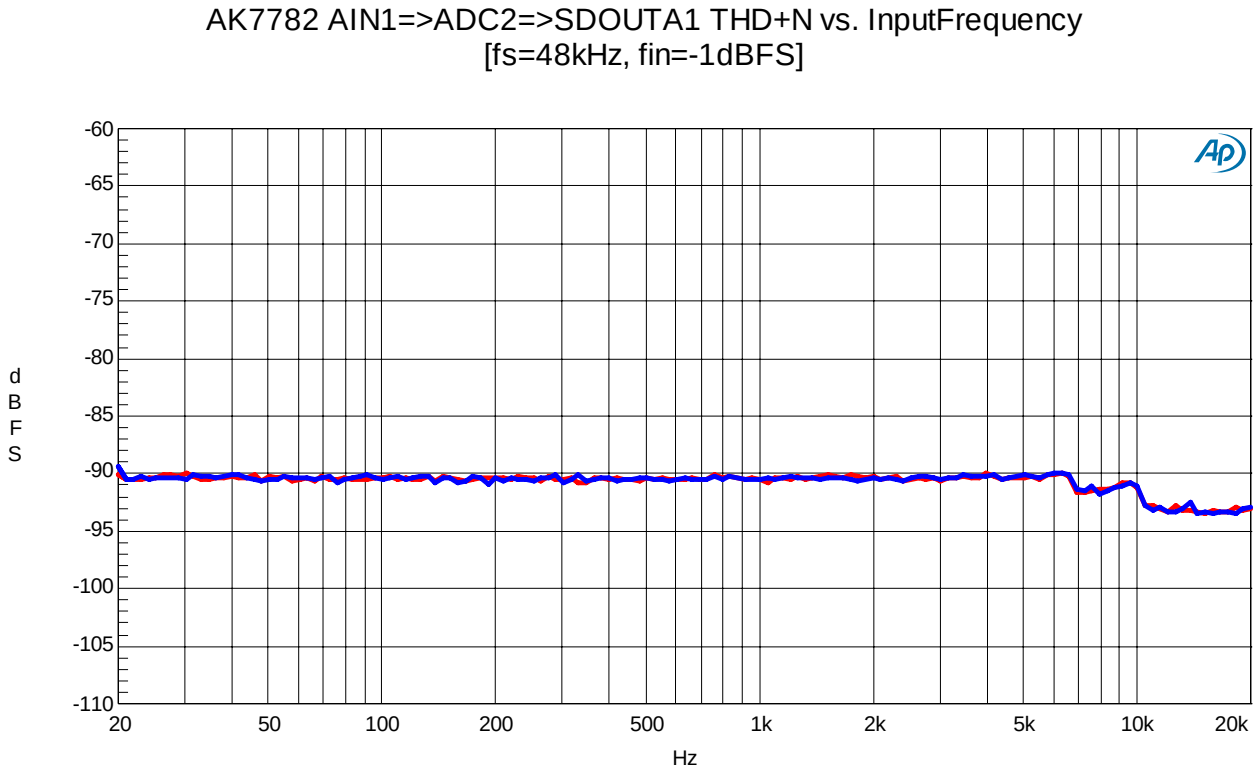


Figure 34. ADC2 – THD+N vs. InputFrequency [fs=48kHz]

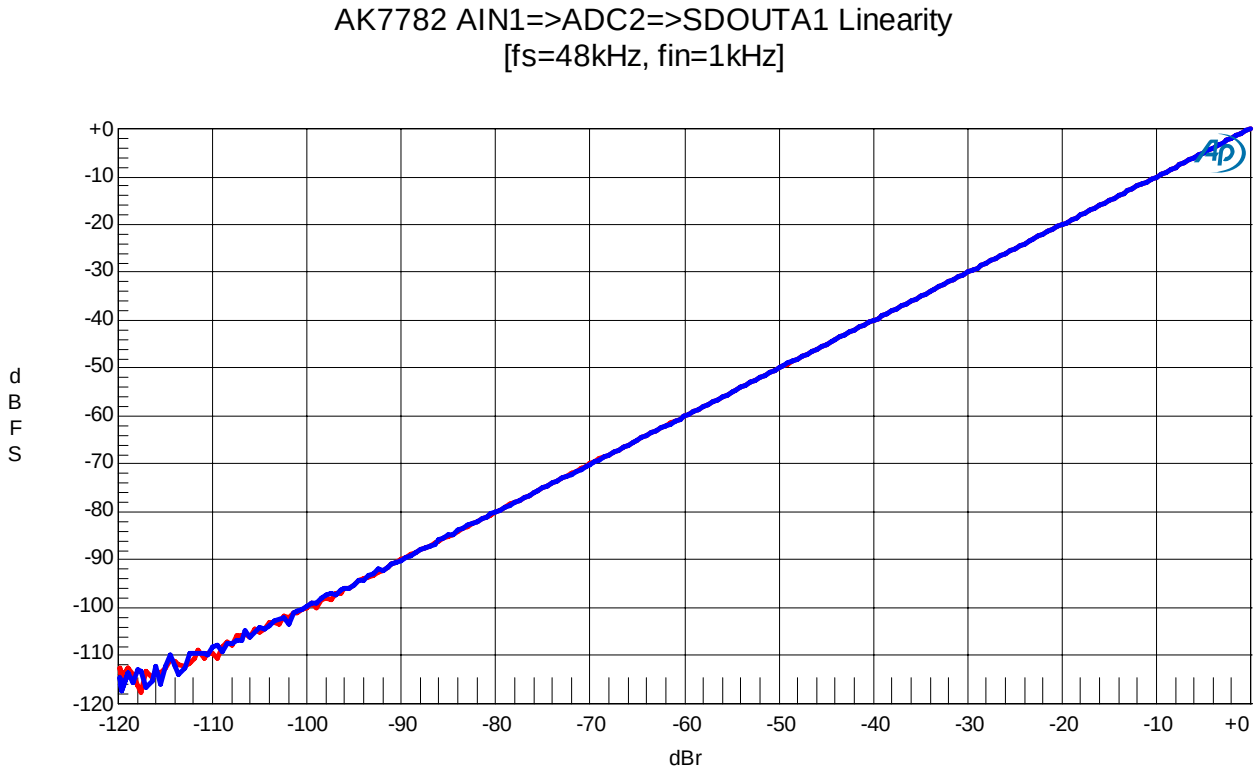


Figure 35. ADC2 – Linearity [fs=48kHz]

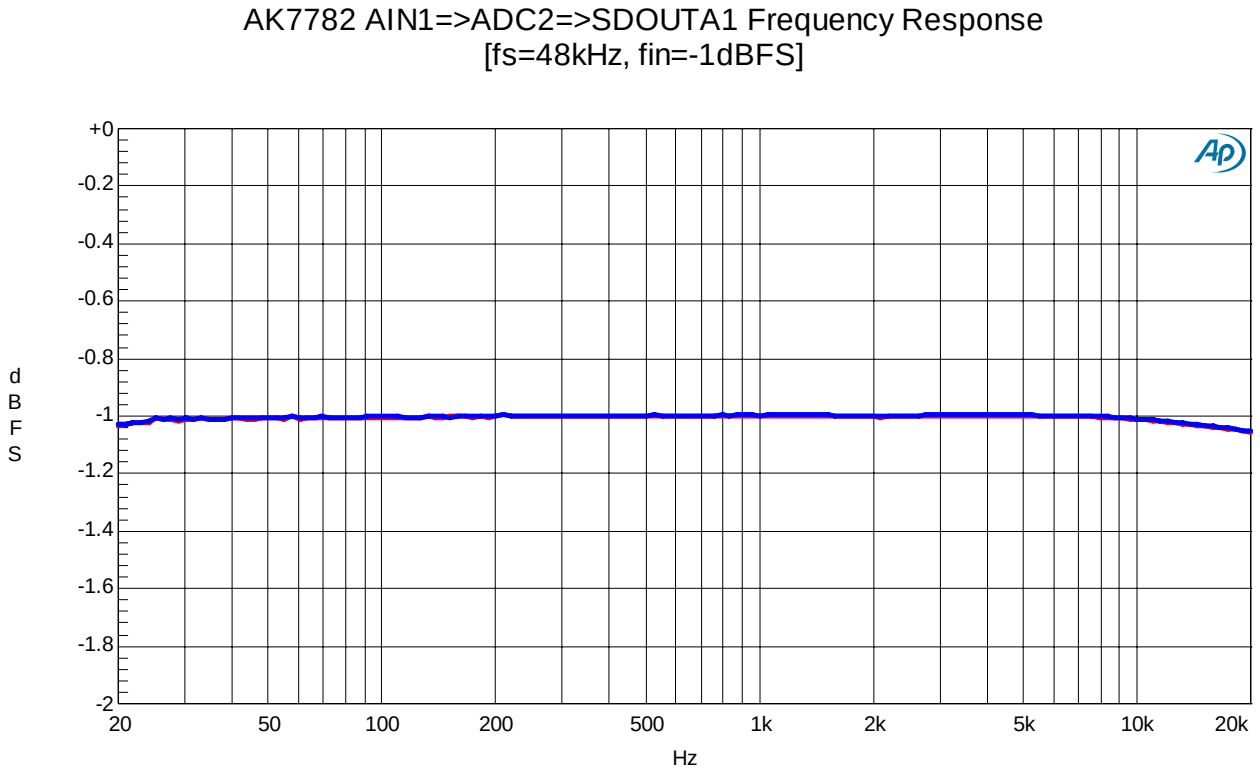


Figure 36. ADC2 – Frequency Response [fs=48kHz]

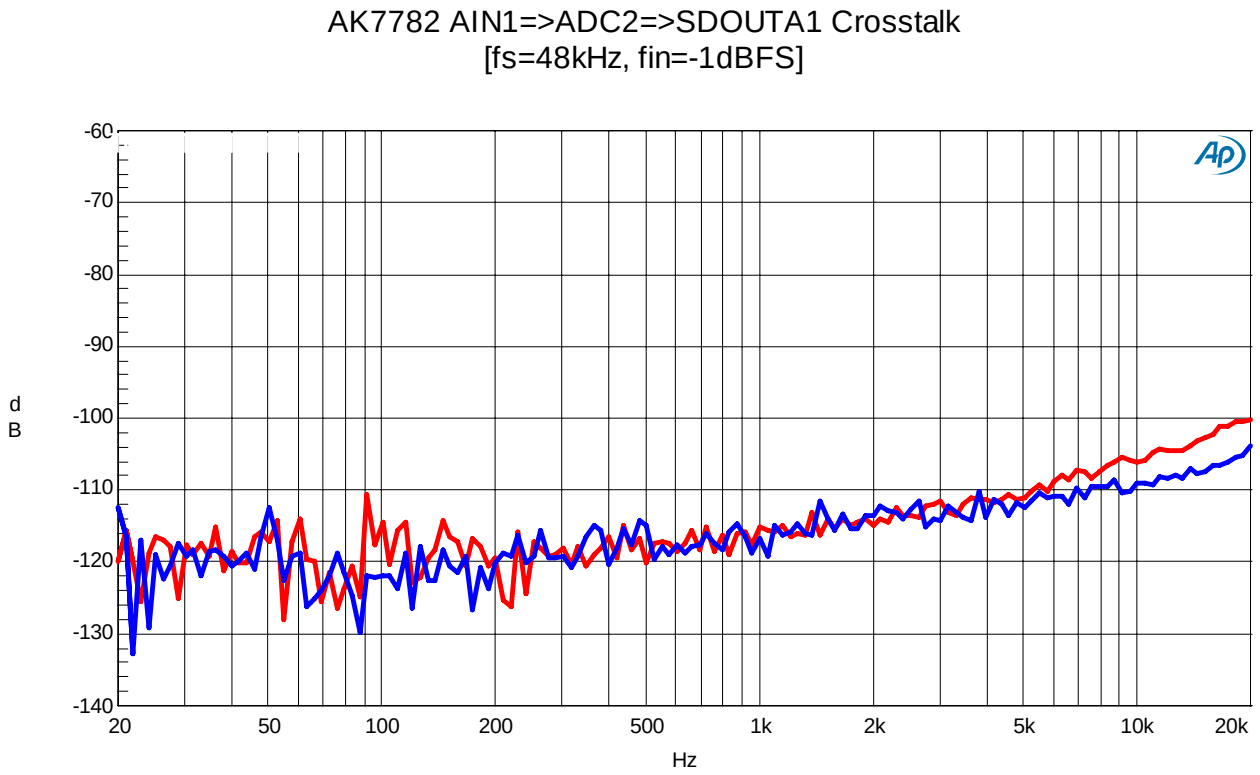


Figure 37. ADC2 – Crosstalk [fs=48kHz]

4. ADC2 (fs=96kHz)

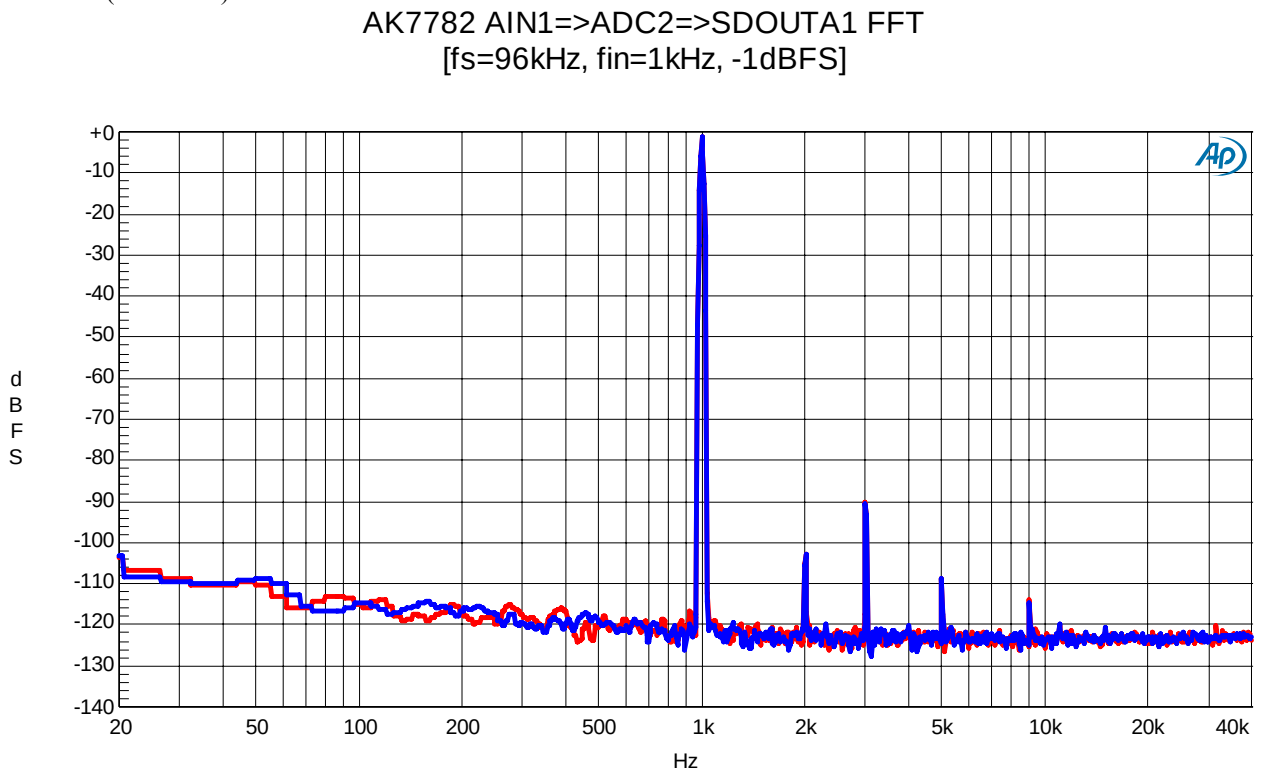


Figure 38. ADC2 – FFT (-1dBFS) [fs=96kHz]

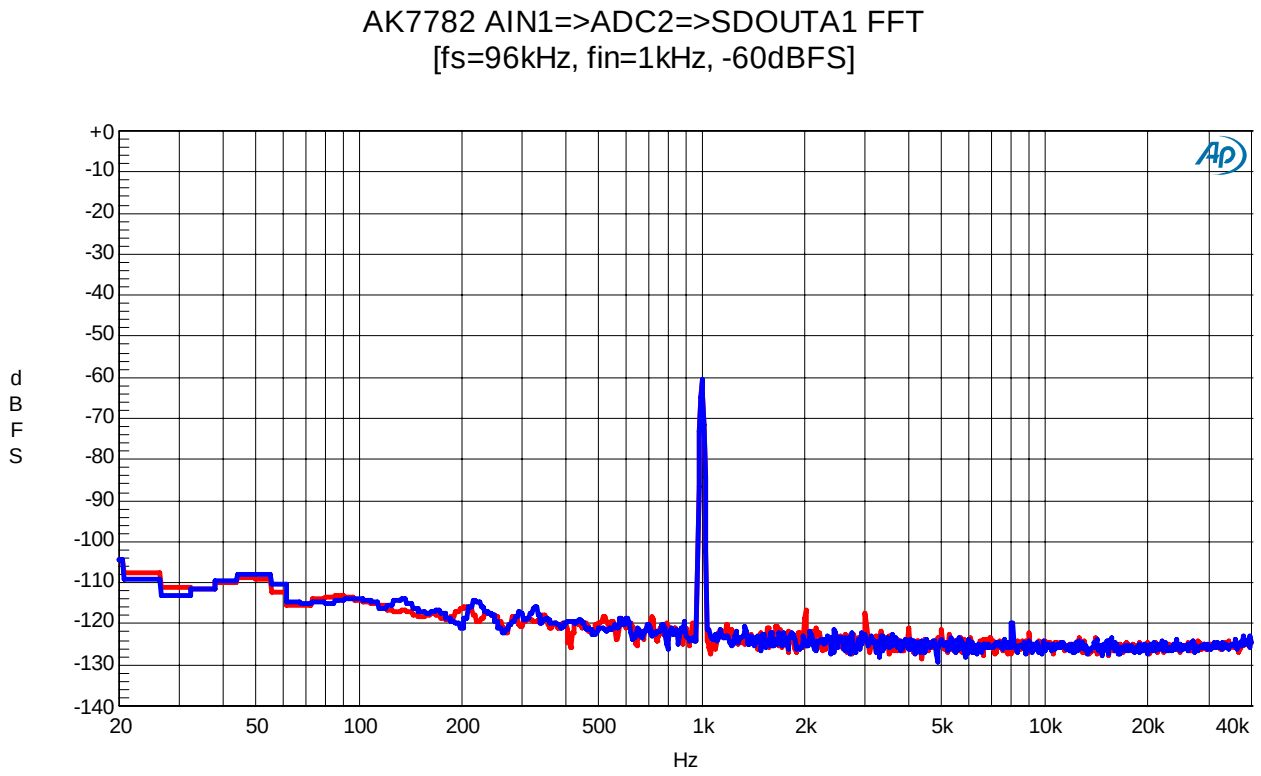


Figure 39. ADC2 – FFT (-60dBFS) [fs=96kHz]

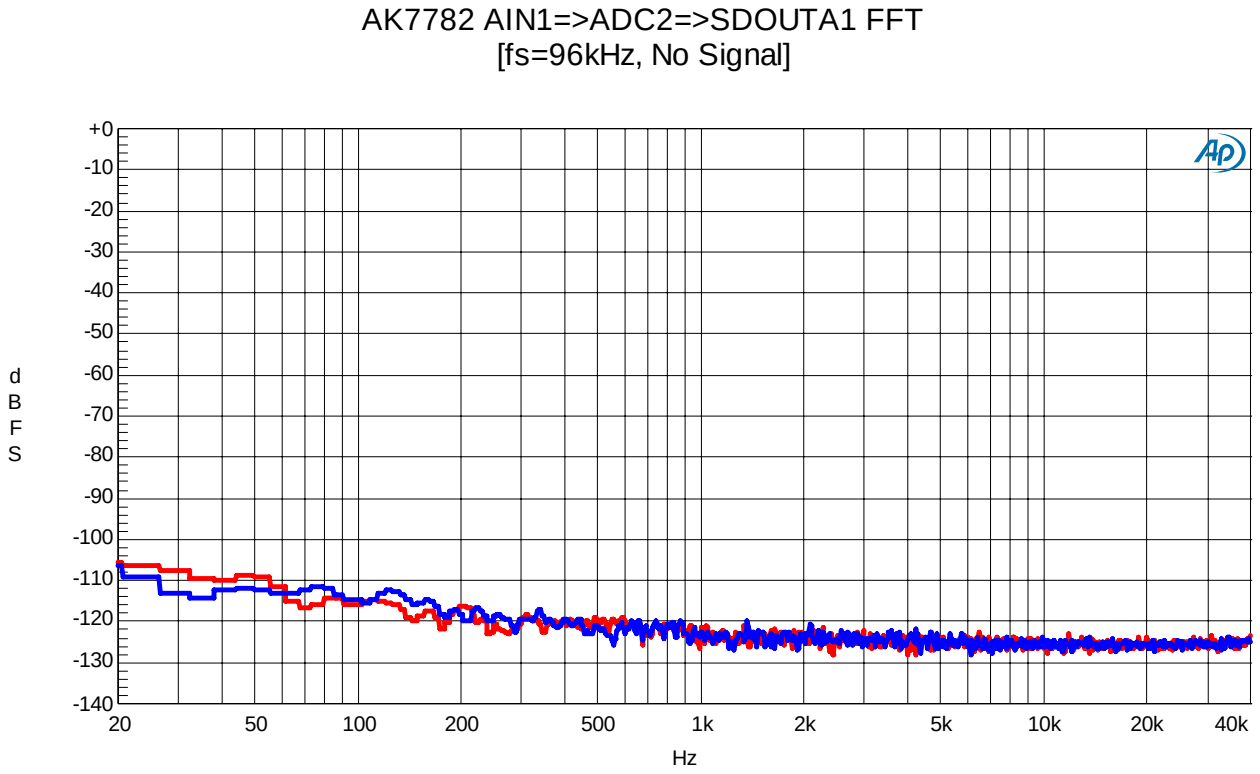


Figure 40. ADC2 – FFT (No Signal) [fs=96kHz]

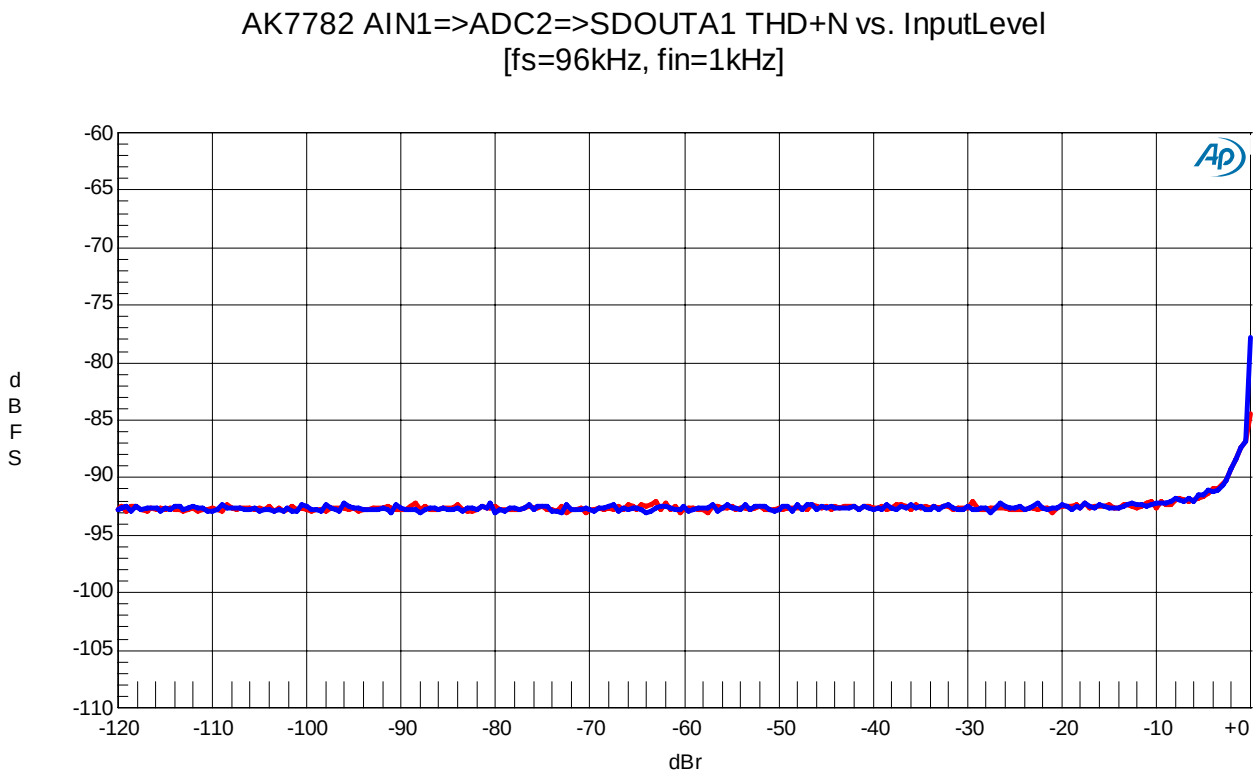


Figure 41. ADC2 – THD+N vs. InputLevel [fs=96kHz]

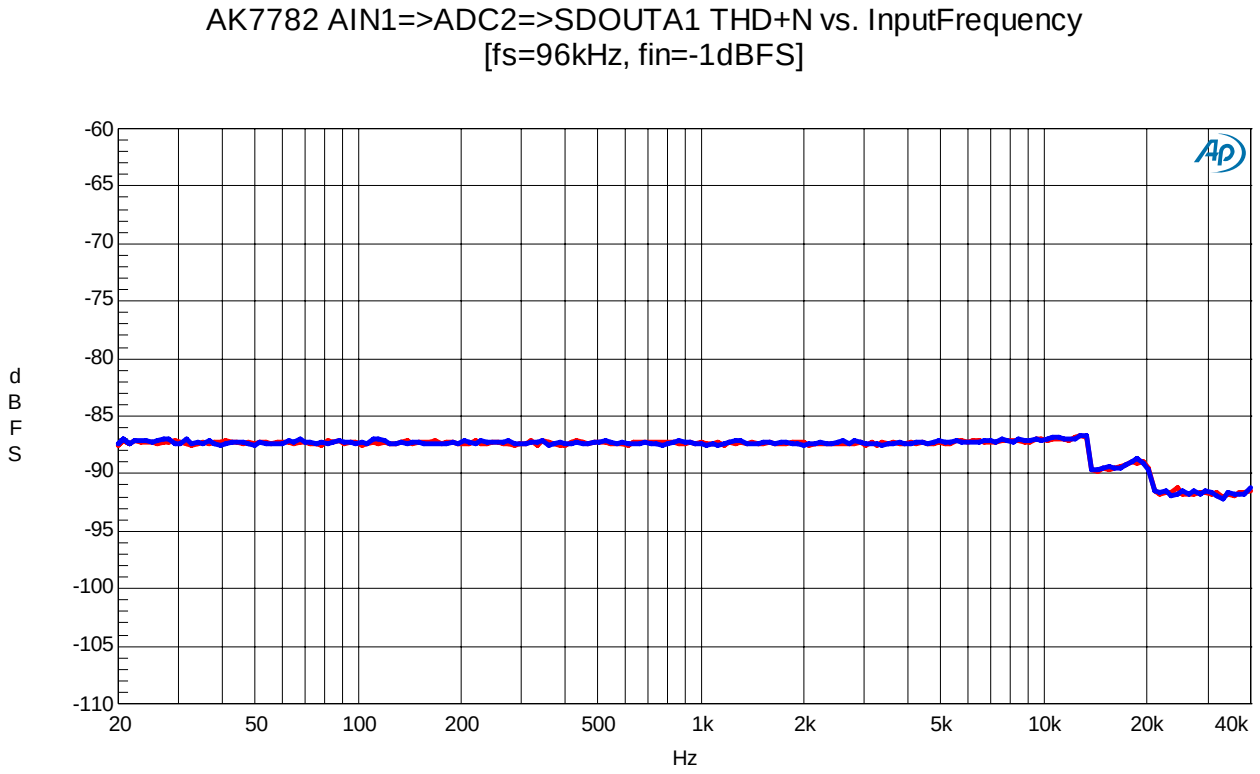


Figure 42. ADC2 – THD+N vs. InputFrequency [fs=96kHz]

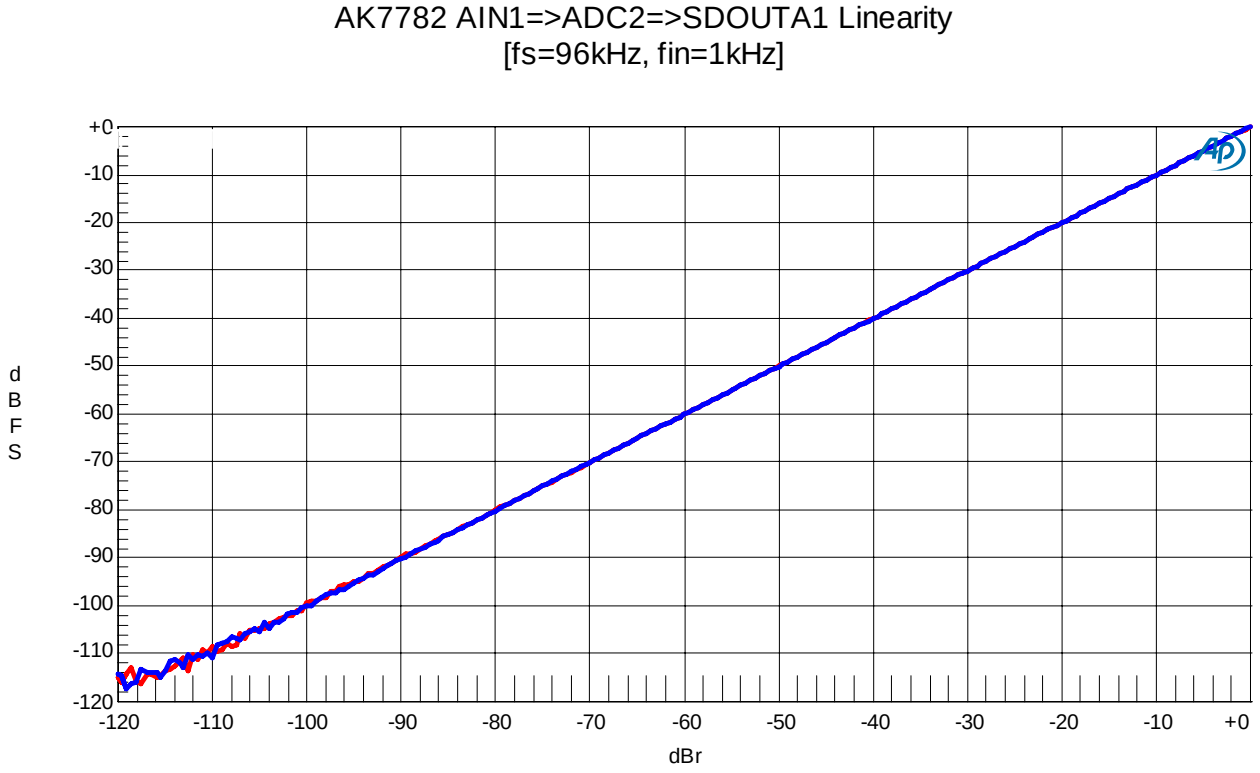


Figure 43. ADC2 – Linearity [fs=96kHz]

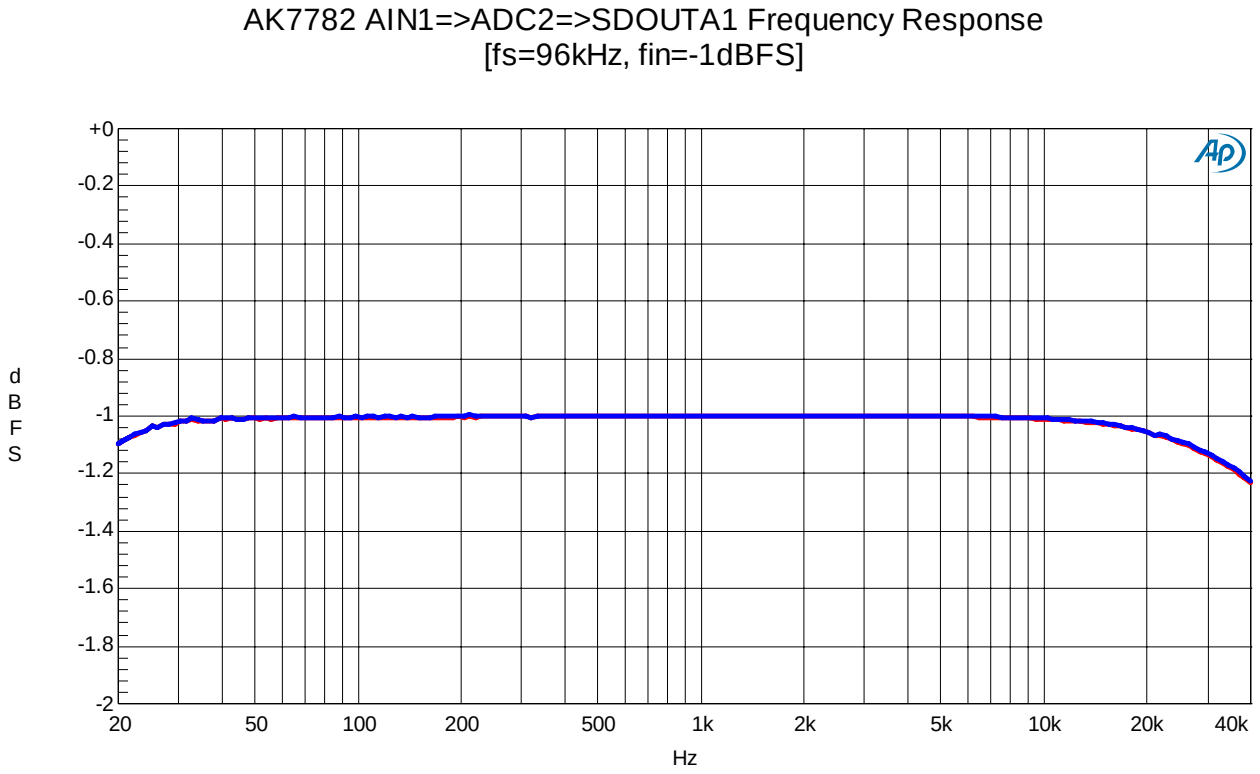


Figure 44. ADC2 – Frequency Response [fs=96kHz]

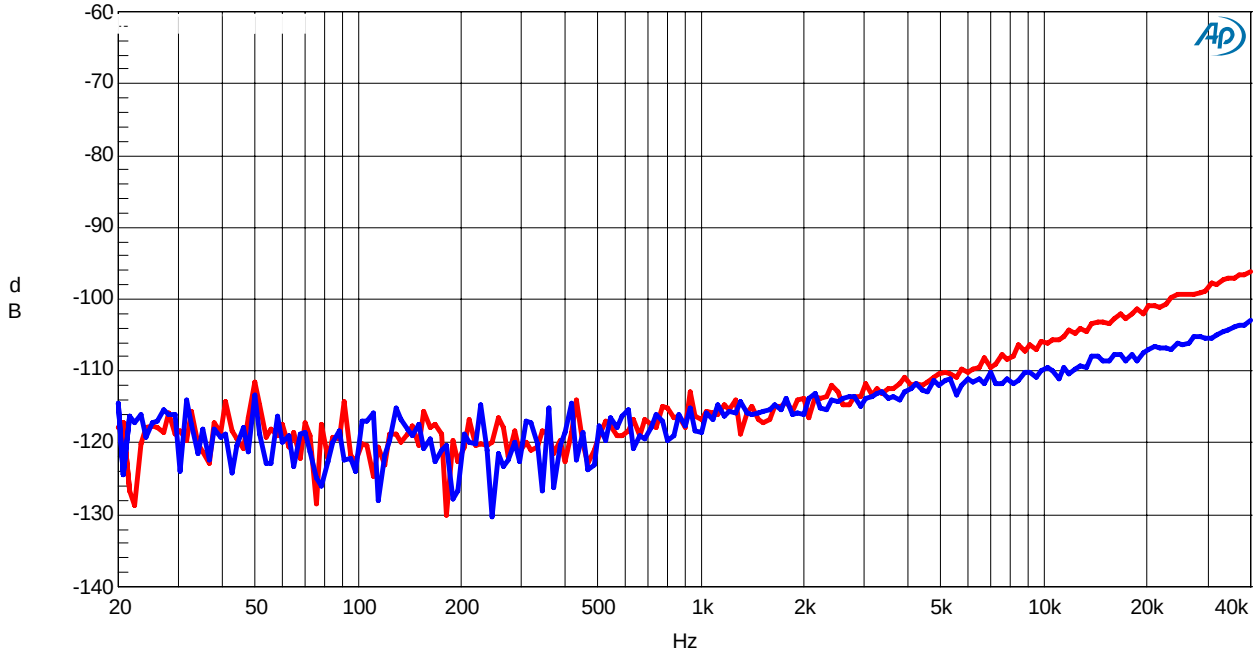


Figure 45. ADC2 – Crosstalk [fs=96kHz]

5. ADCM (fs=48kHz)

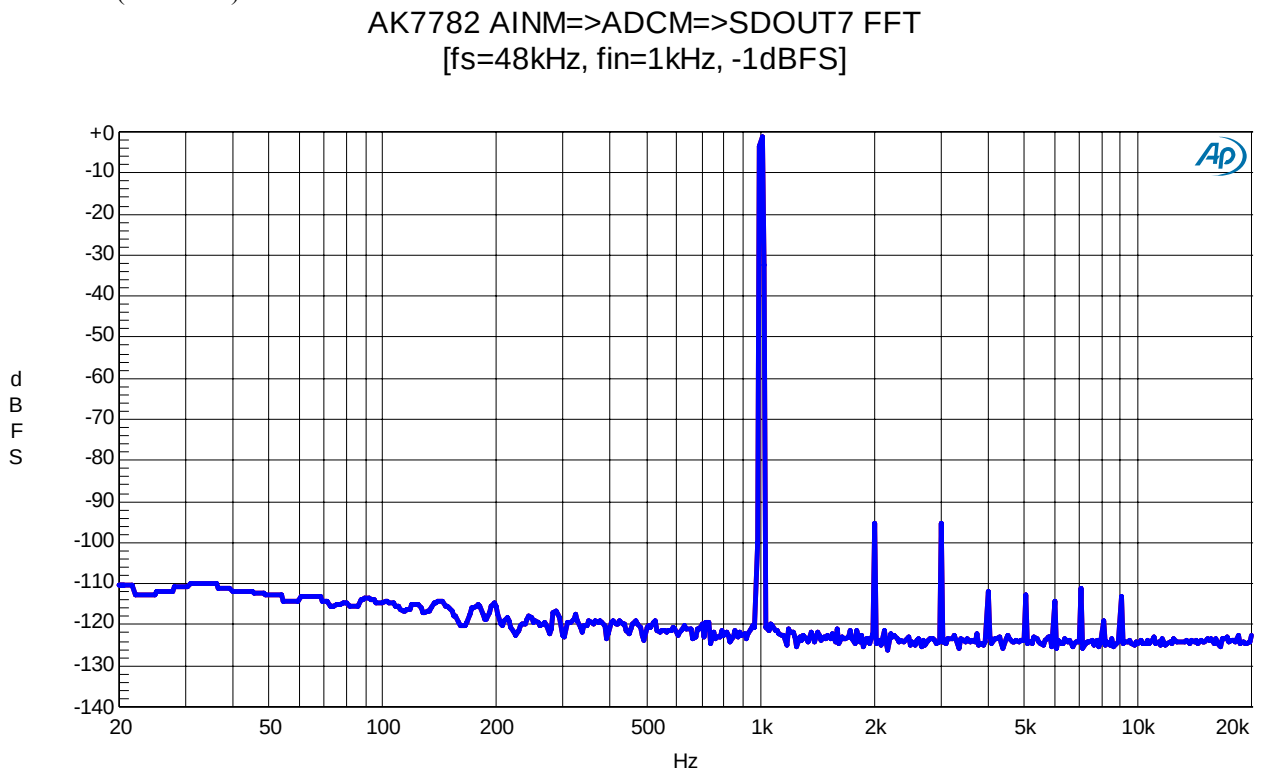


Figure 46. ADCM – FFT (-1dBFS) [fs=48kHz]

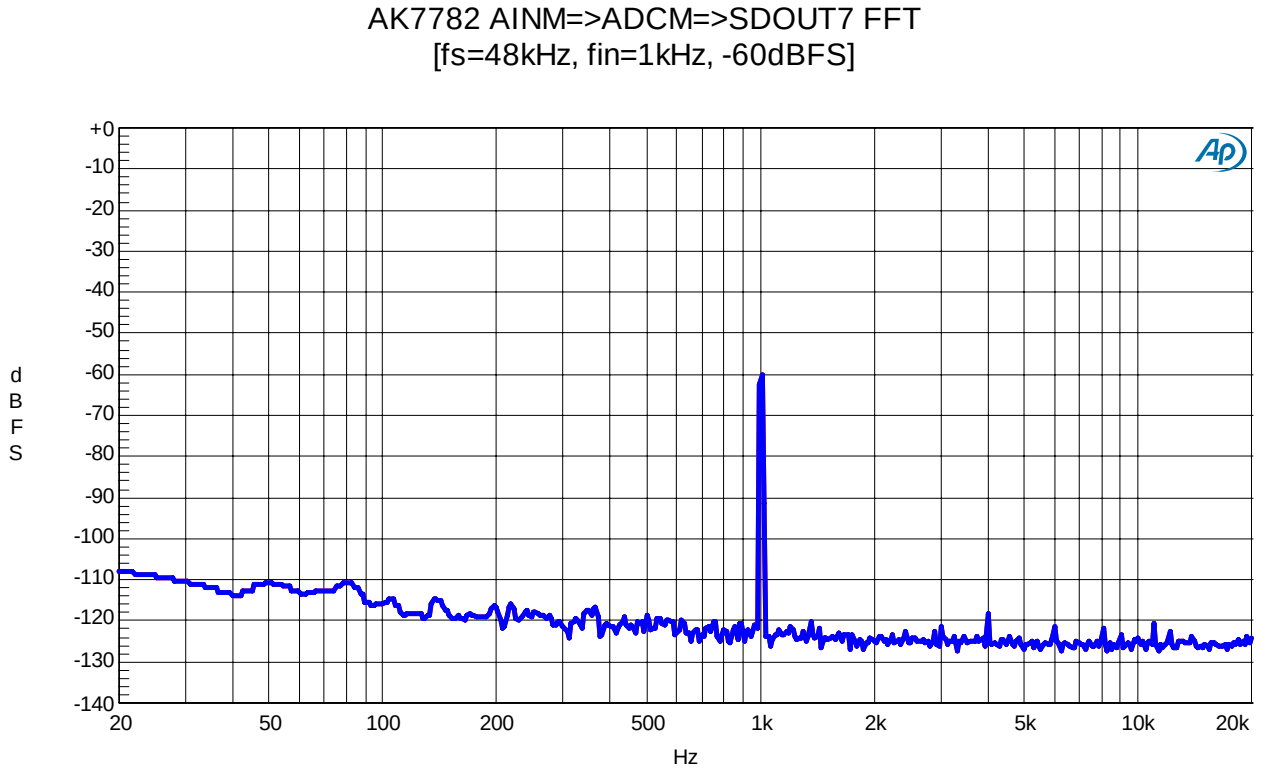


Figure 47. ADCM – FFT (-60dBFS) [fs=48kHz]

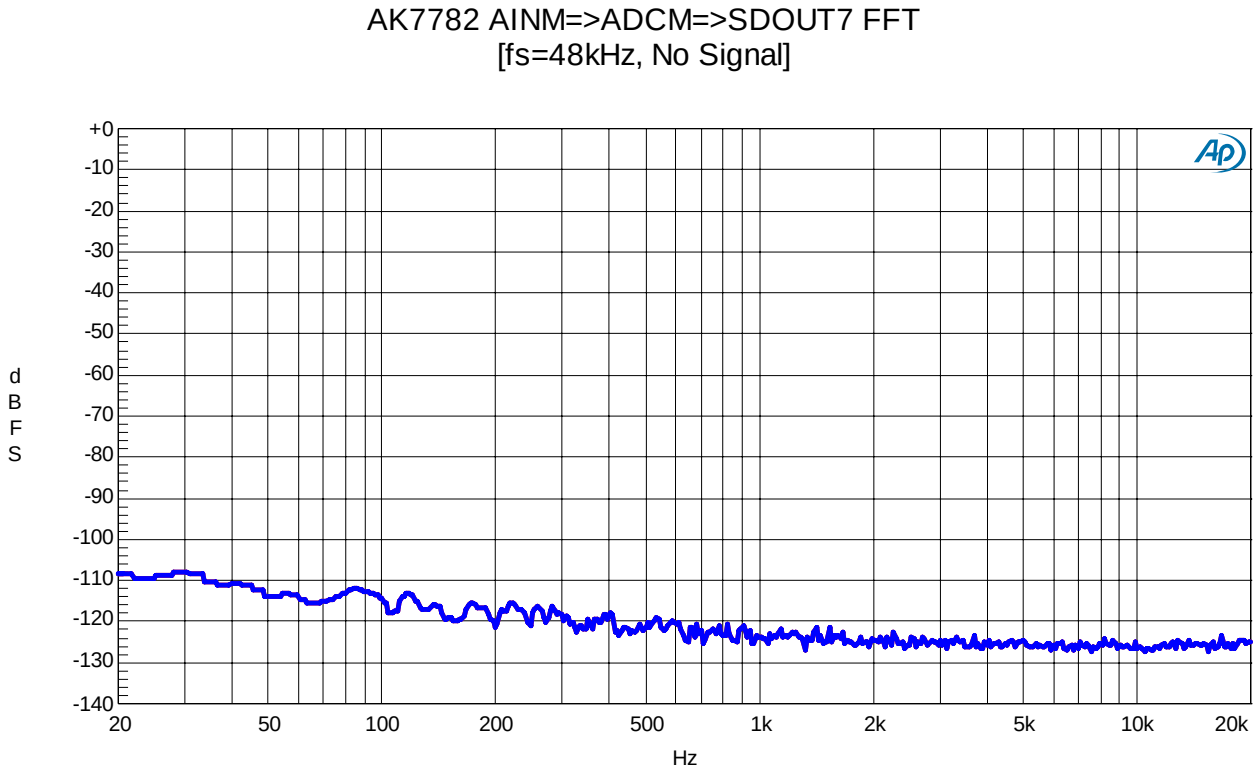


Figure 48. ADCM – FFT (No Signal) [fs=48kHz]

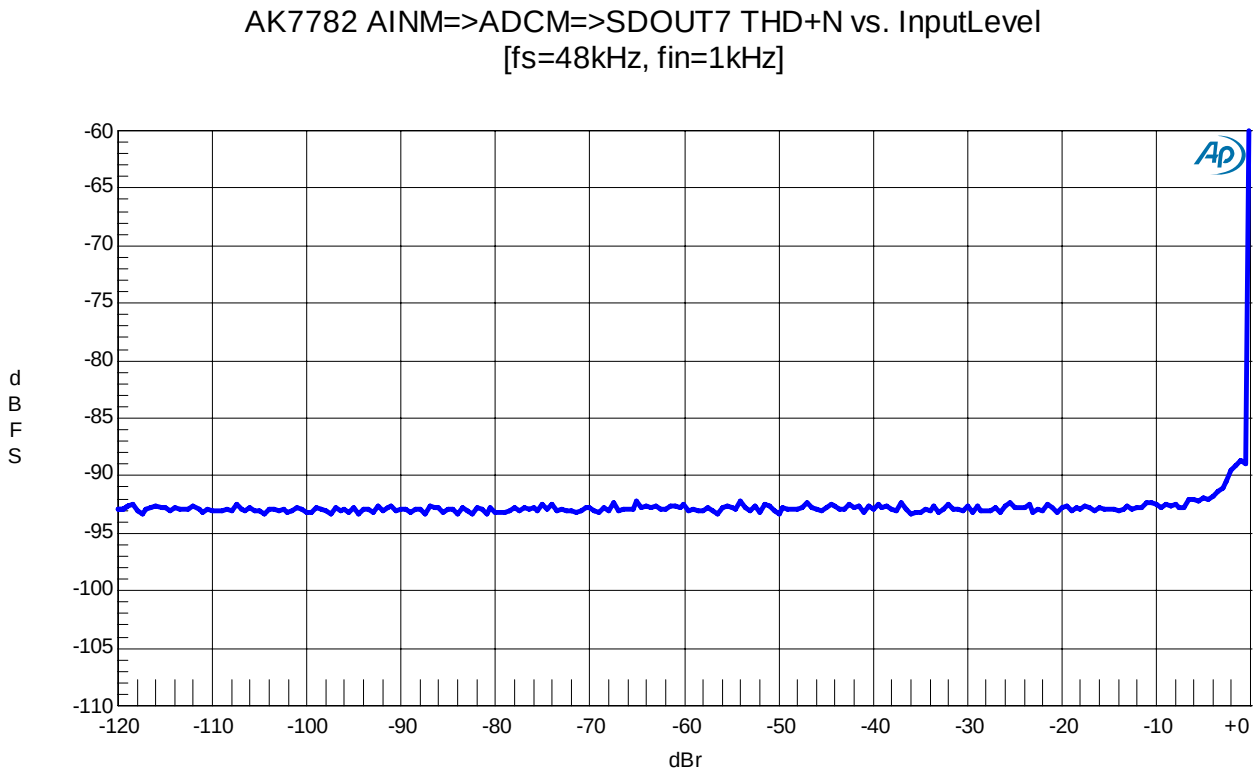


Figure 49. ADCM – THD+N vs. InputLevel [fs=48kHz]

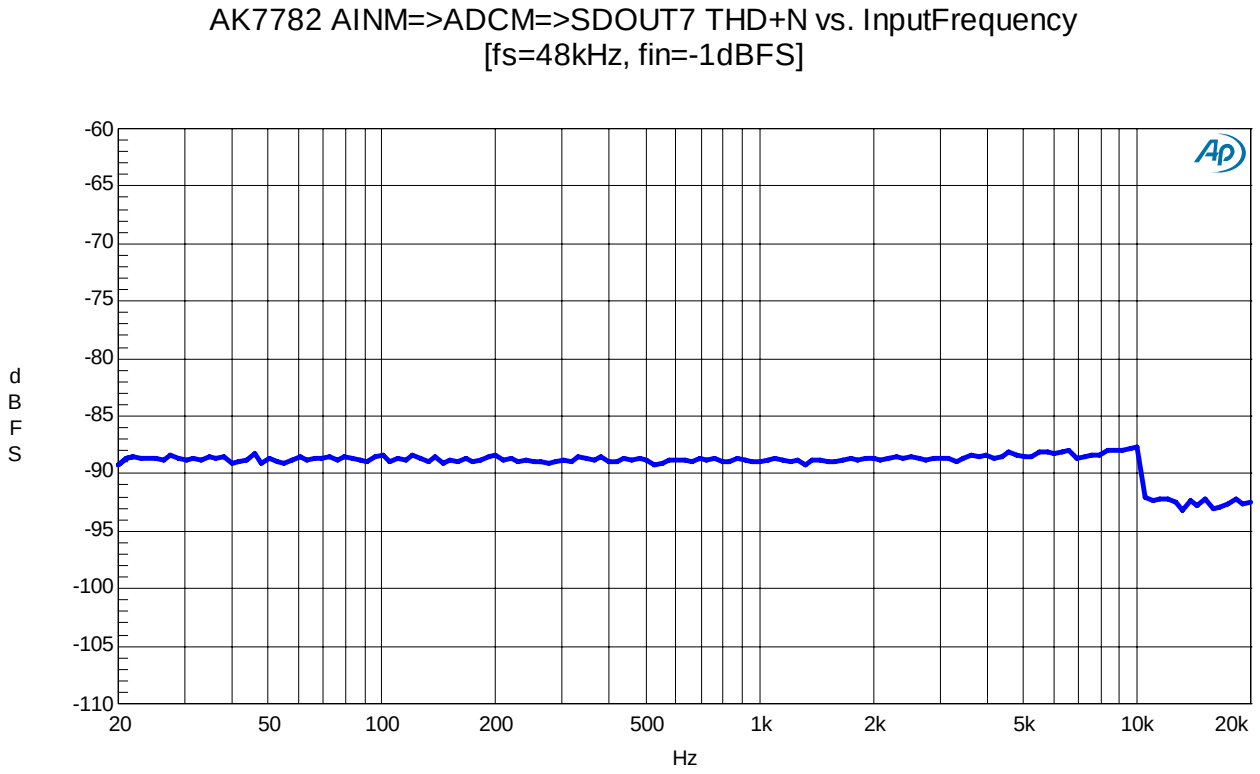


Figure 50. ADCM – THD+N vs. InputFrequency [fs=48kHz]

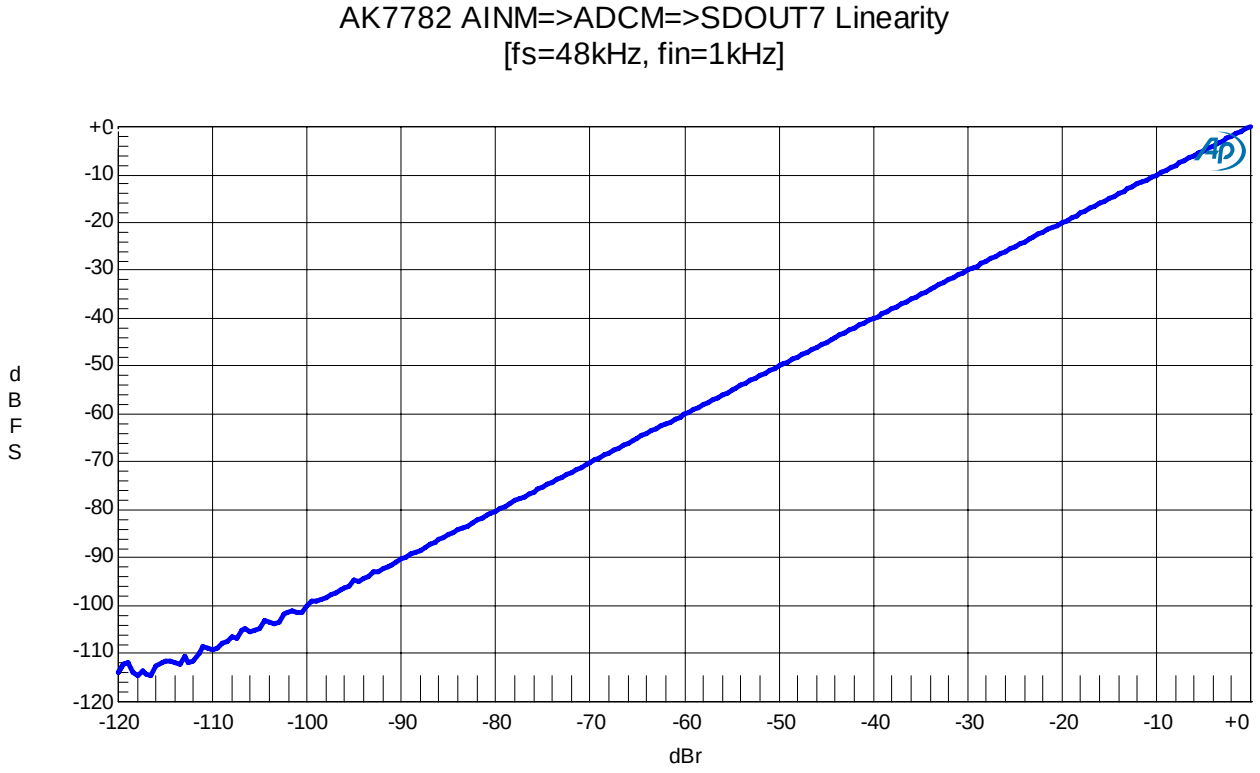


Figure 51. ADCM – Linearity [fs=48kHz]

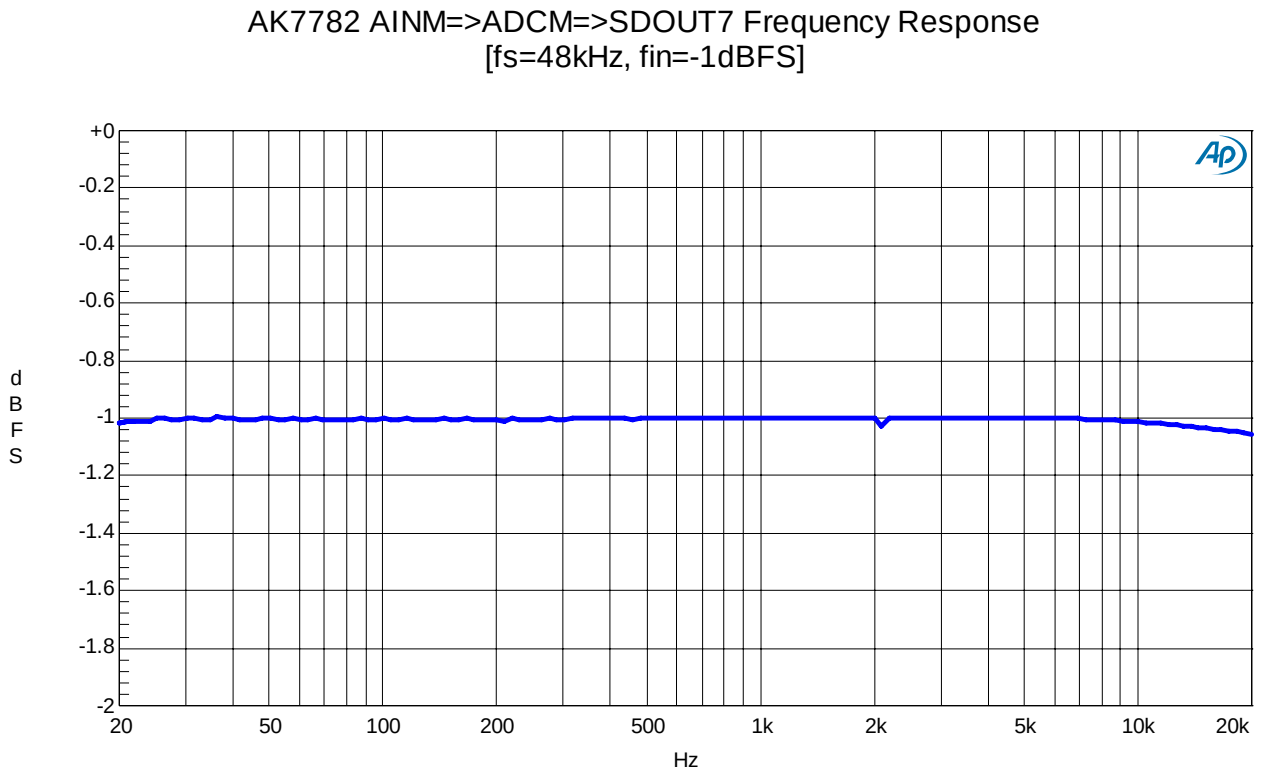


Figure 52. ADCM – Frequency Response [fs=48kHz]

6. ADCM (fs=96kHz)

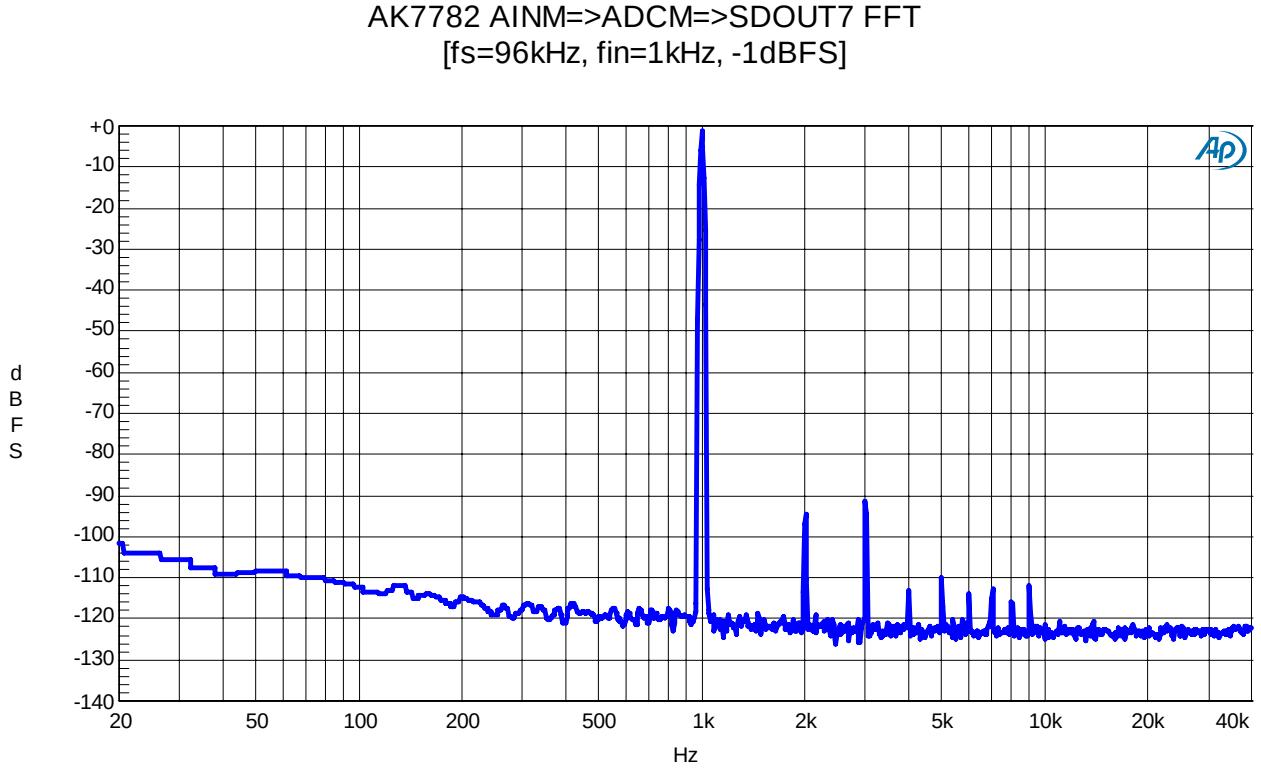


Figure 53. ADCM – FFT (-1dBFS) [fs=96kHz]

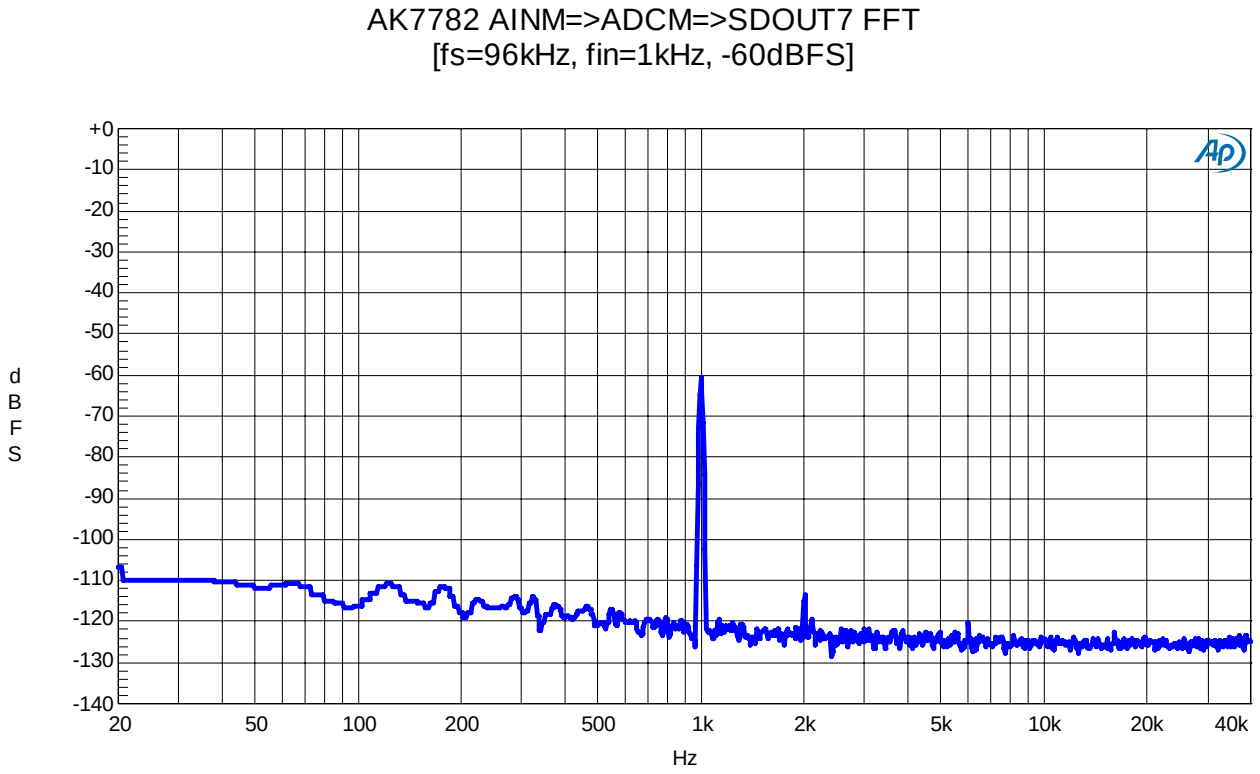


Figure 54. ADCM – FFT (-60dBFS) [fs=96kHz]

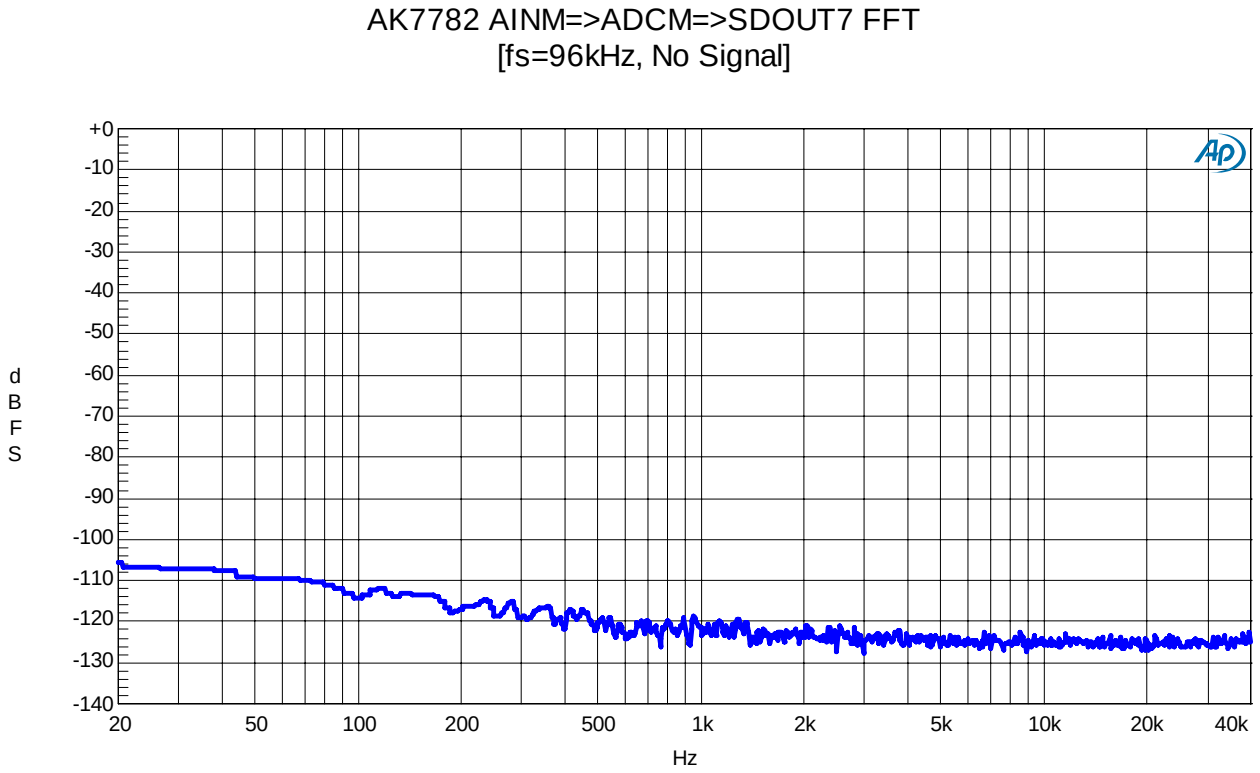


Figure 55. ADCM – FFT (No Signal) [fs=96kHz]

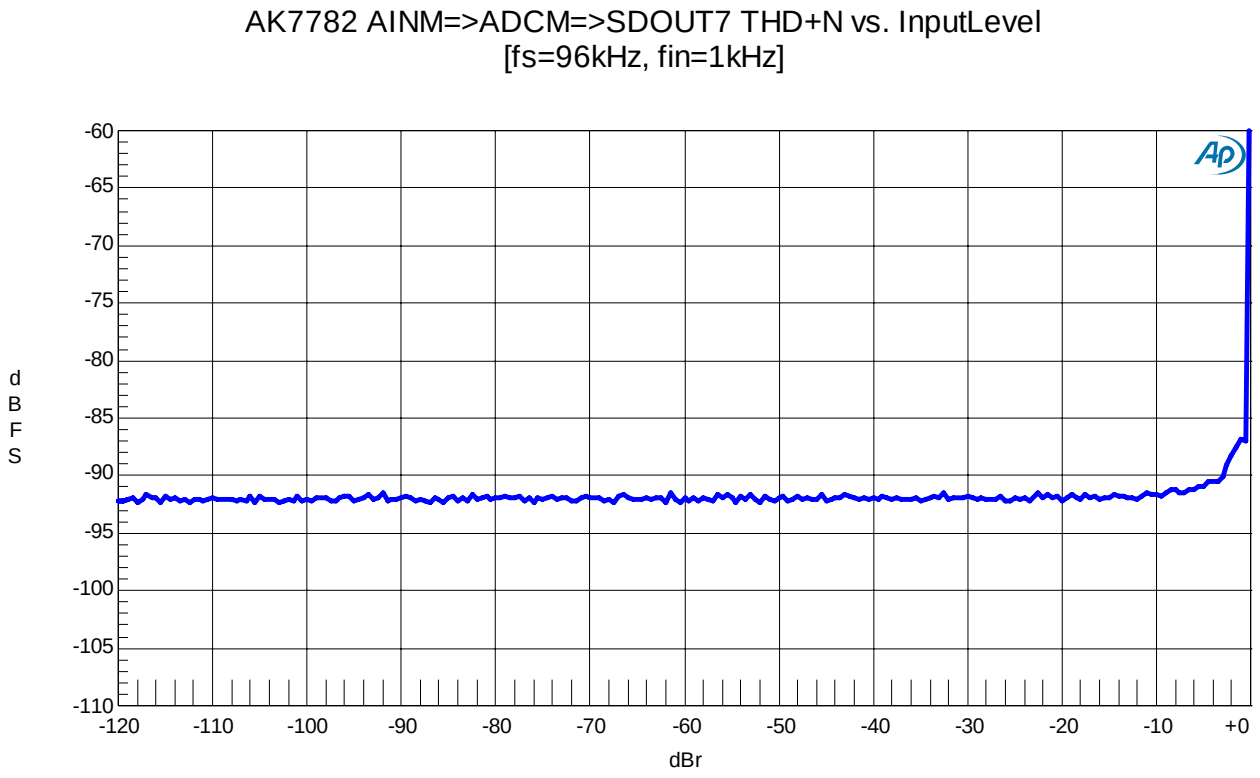


Figure 56. ADCM – THD+N vs. InputLevel [fs=96kHz]

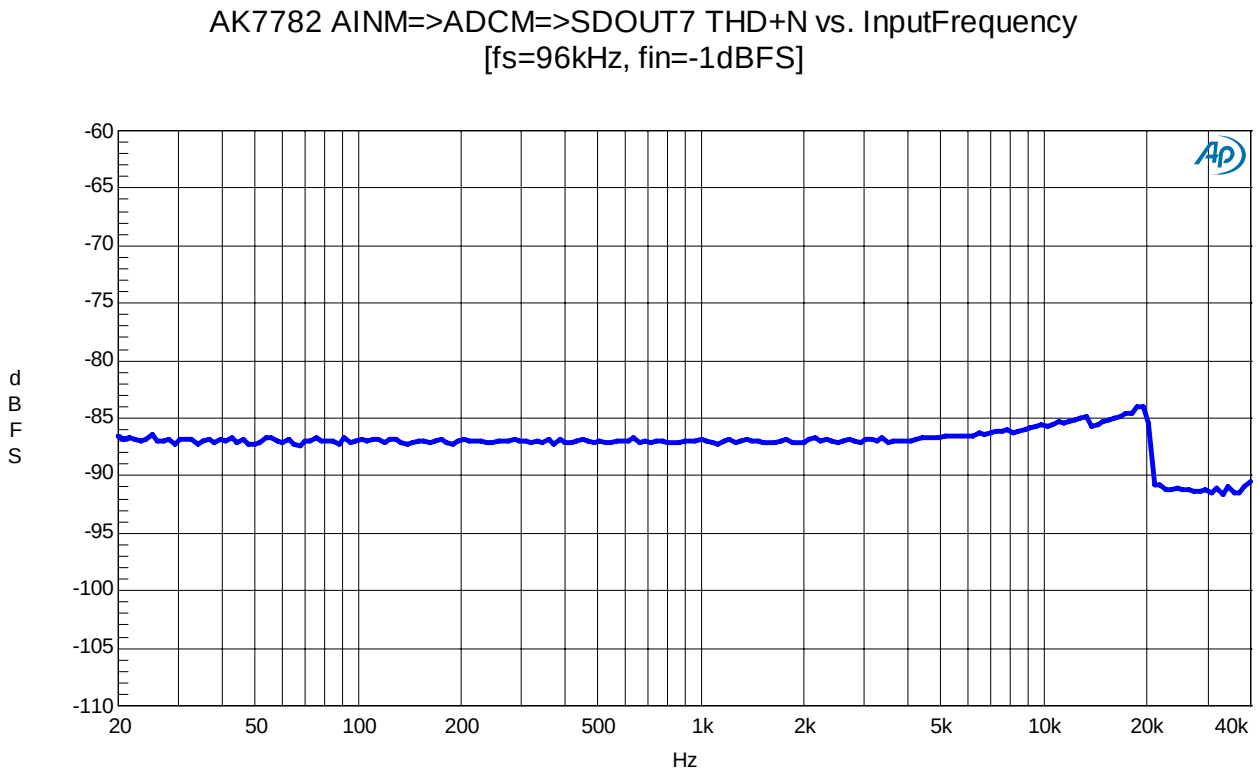


Figure 57. ADCM – THD+N vs. InputFrequency [fs=96kHz]

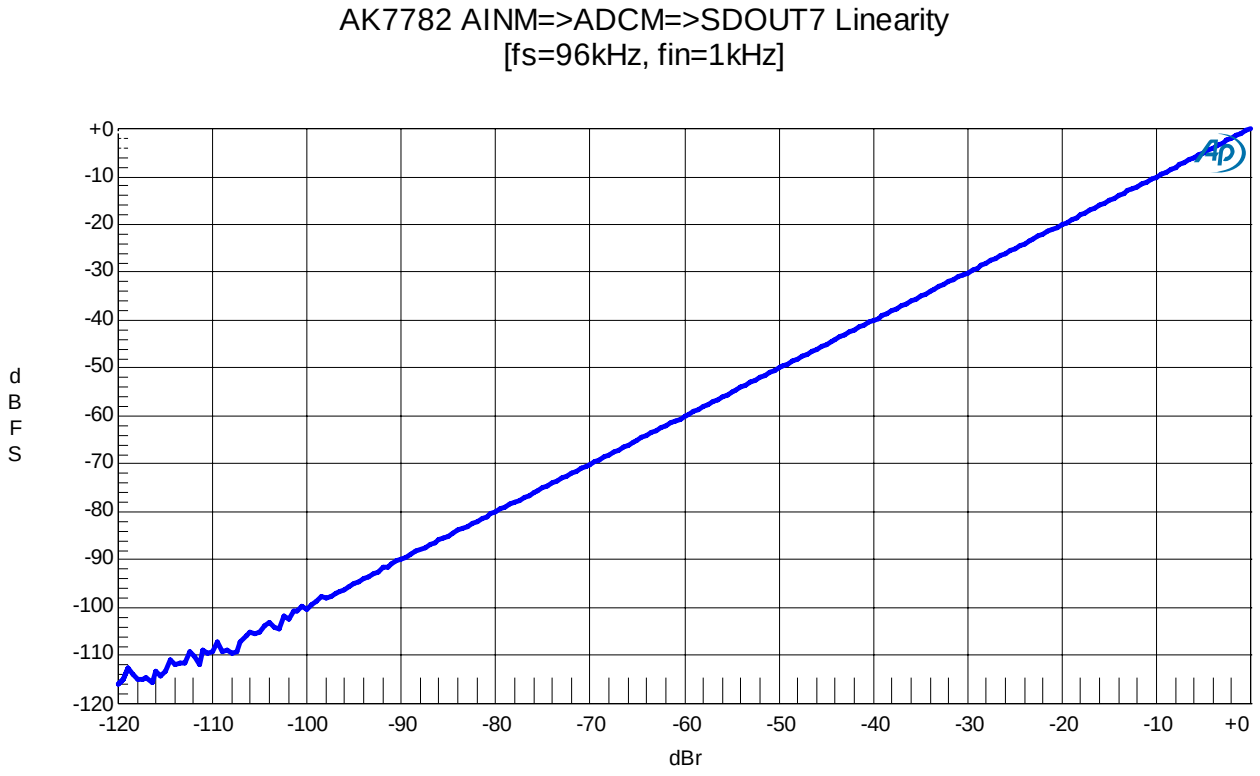


Figure 58. ADCM – Linearity [fs=96kHz]

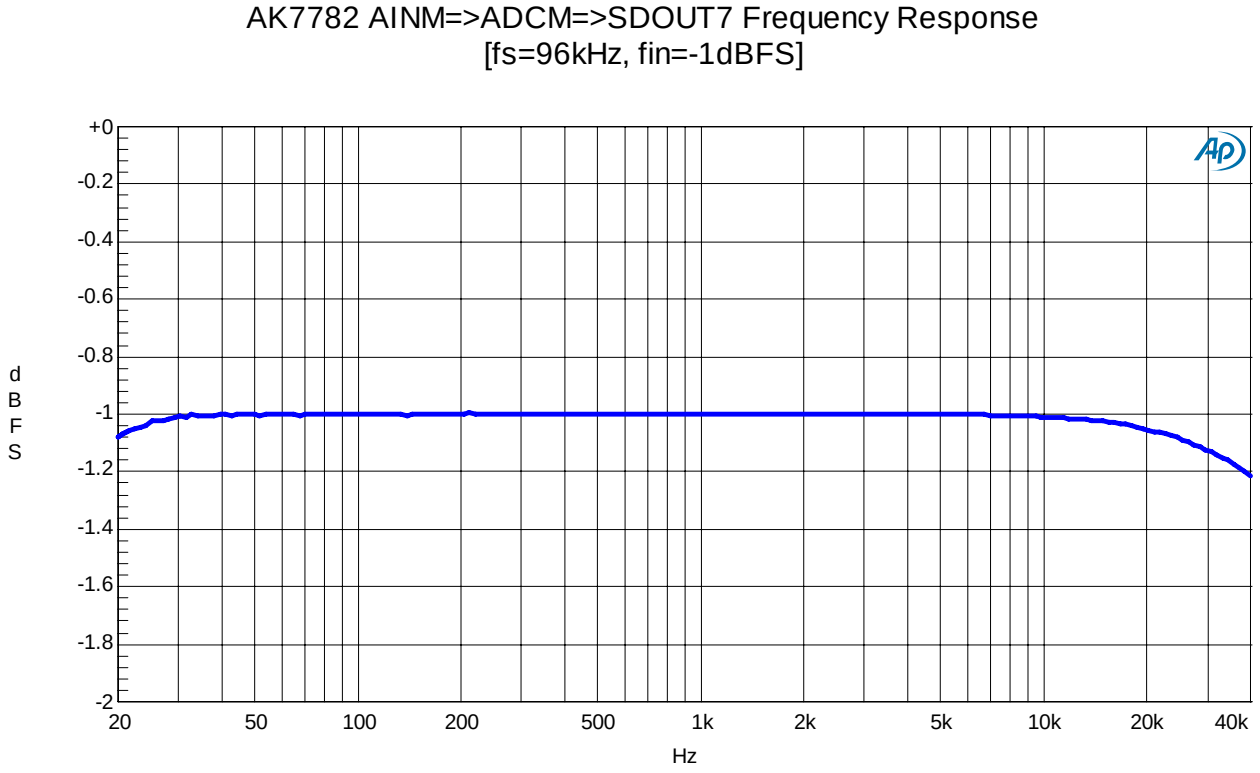
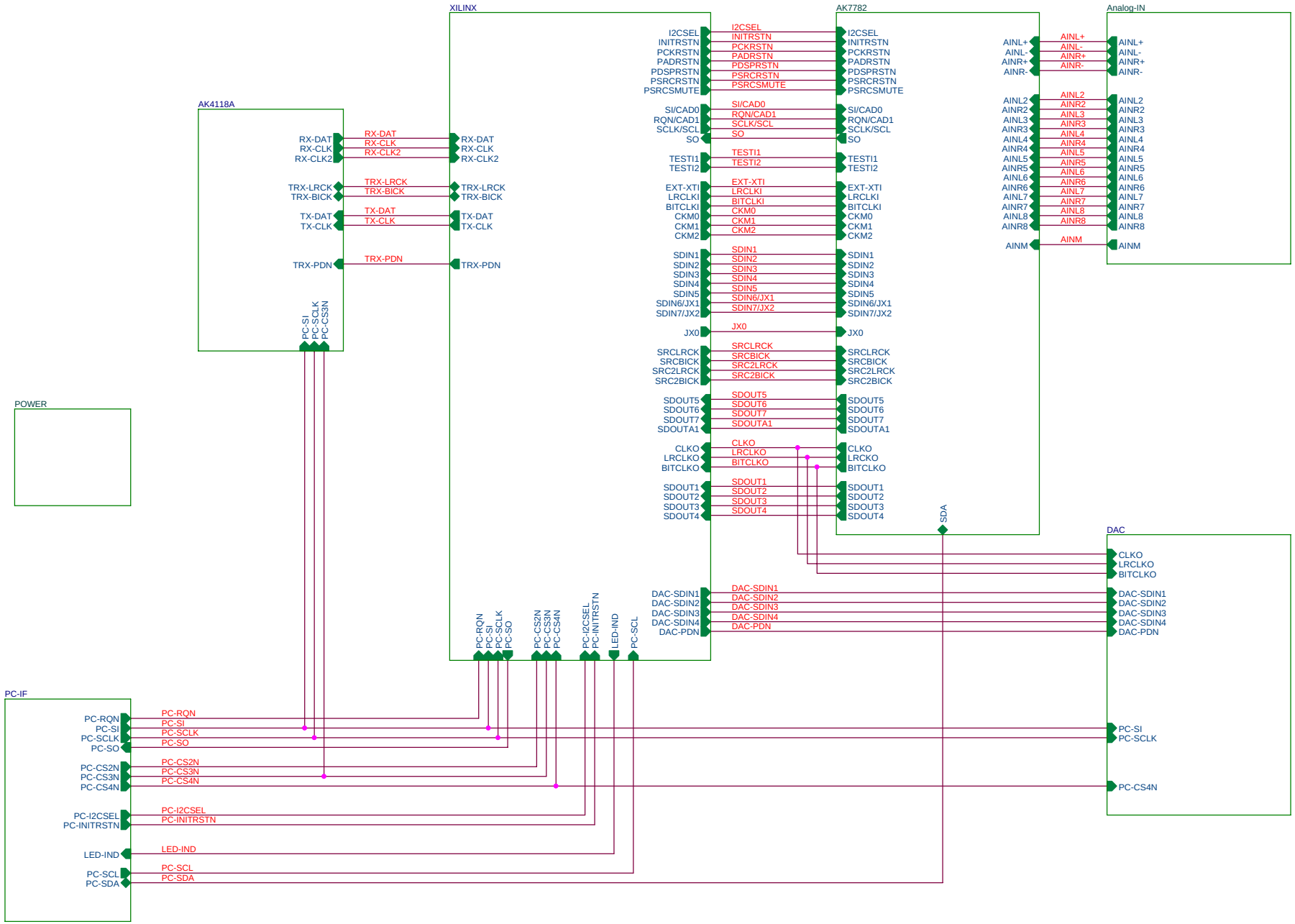


Figure 59. ADCM – Frequency Response [fs=96kHz]

REVISION HISTORY

Date (yy/mm/dd)	Manual Revision	Board Revision	Reason	Page	Contents
11/03/25	KM106200	0	First edition		



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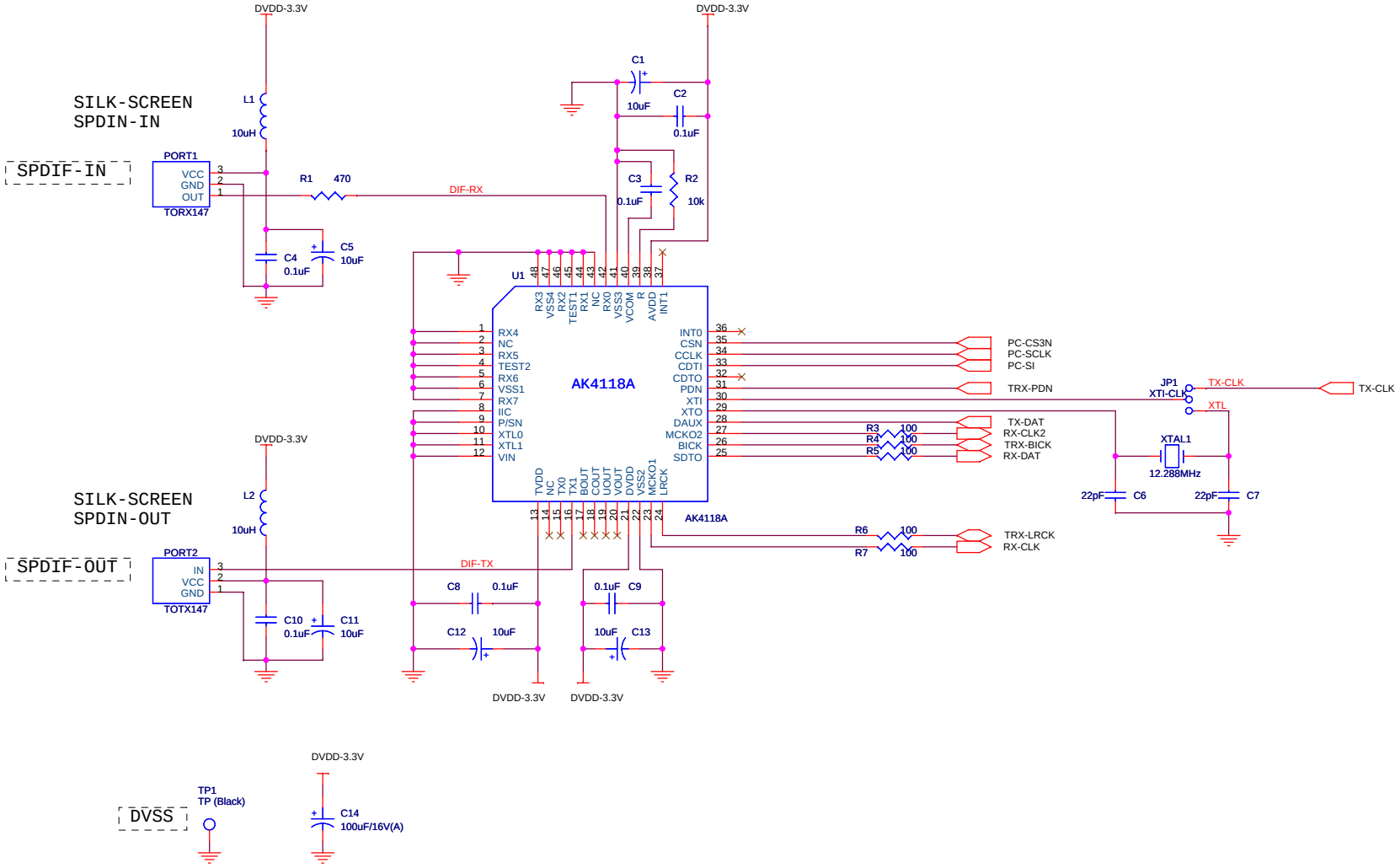
Date: Wednesday, January 12, 2011	Sheet 1 of 8	



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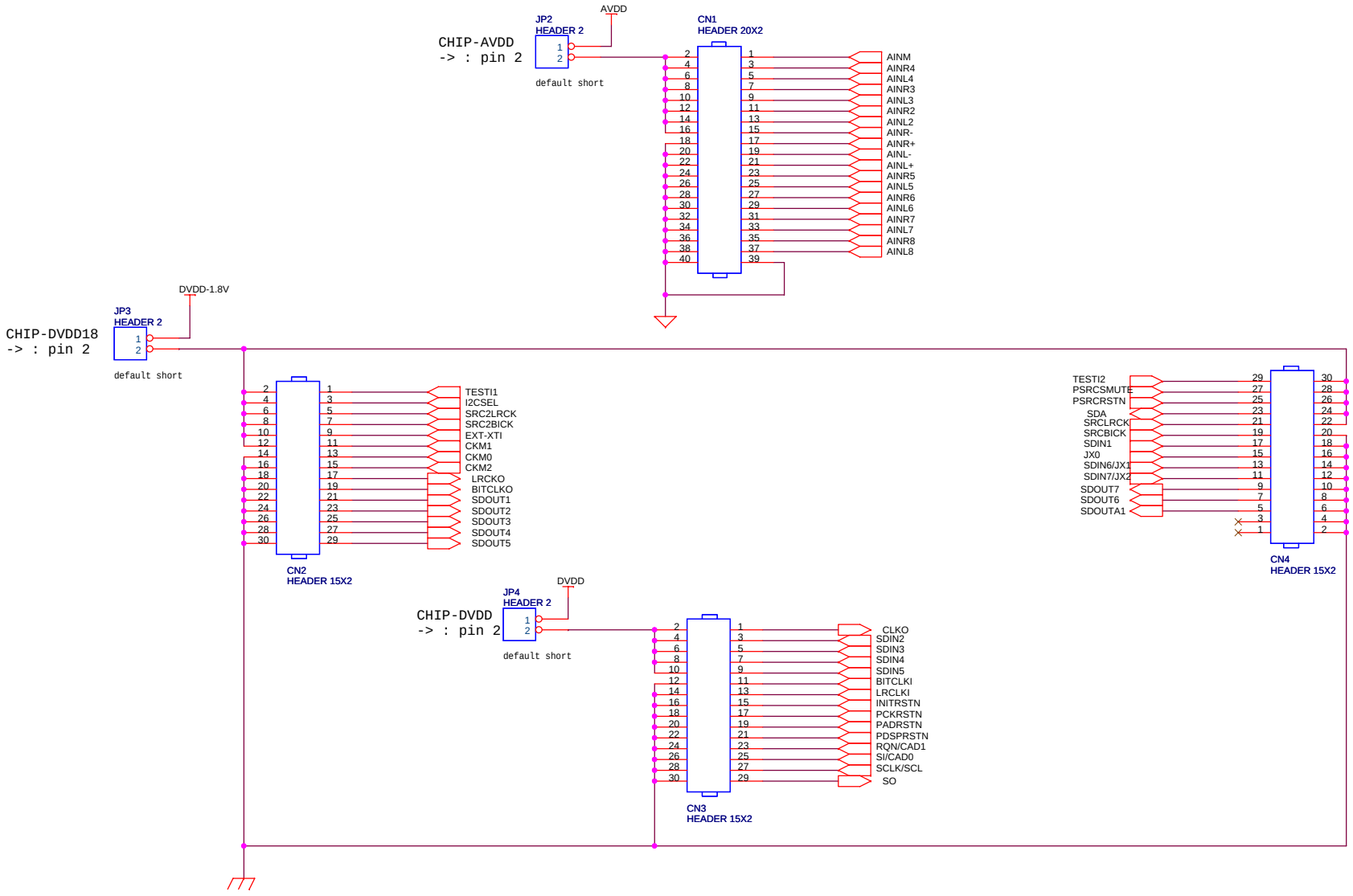

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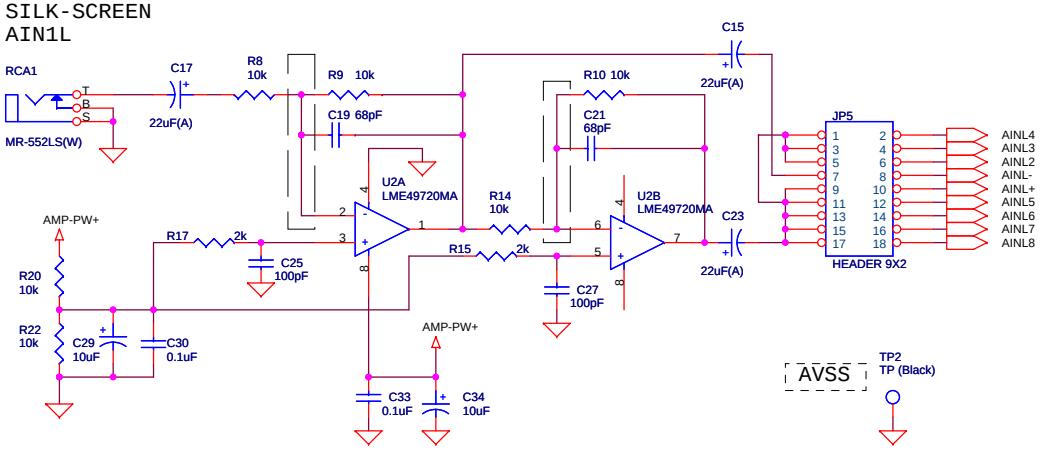
RCA: WHITE

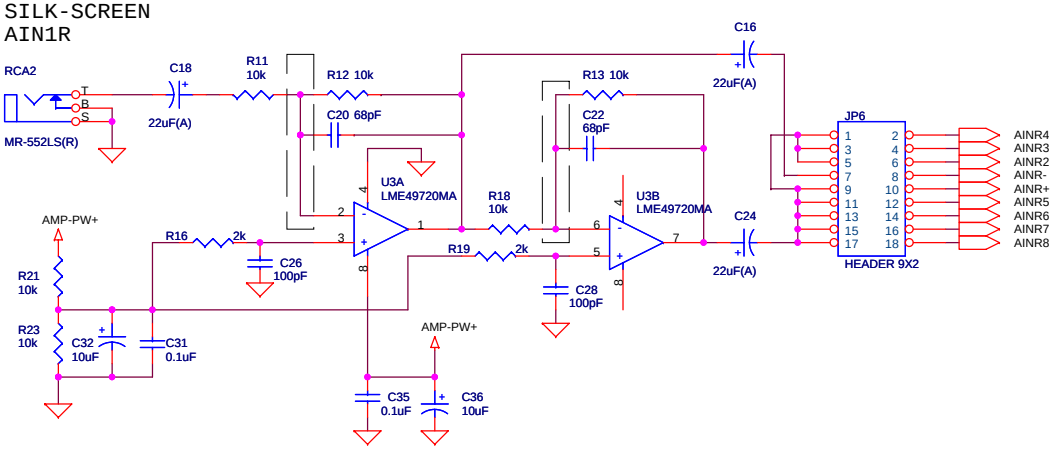
AREA : SHORTEST WIRING

RCA: RED

SILK-SCREEN
AIN1L



SILK-SCREEN
AIN1R



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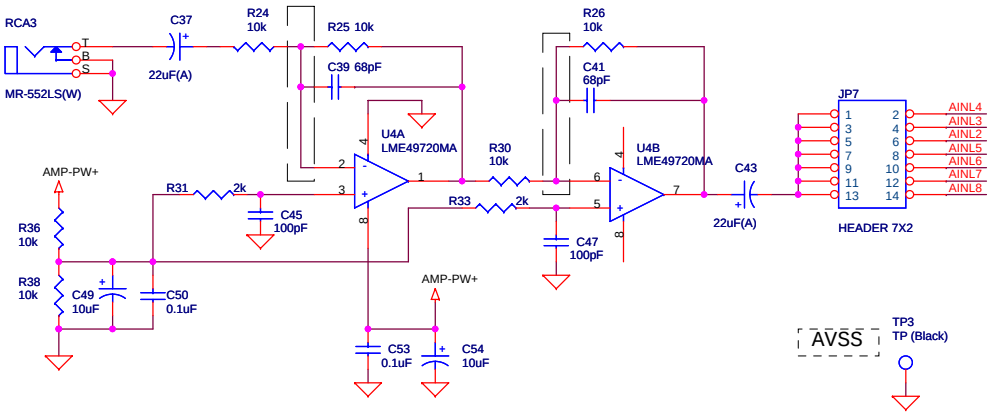
AIN2L



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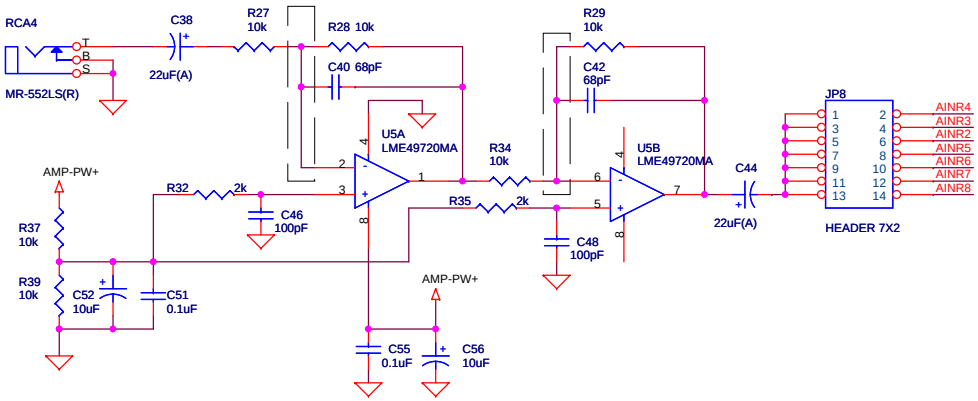
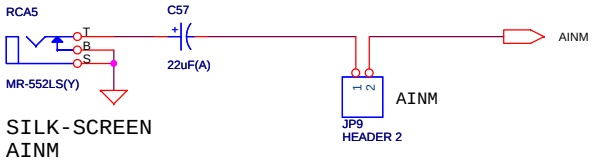


RCA: YELLOW



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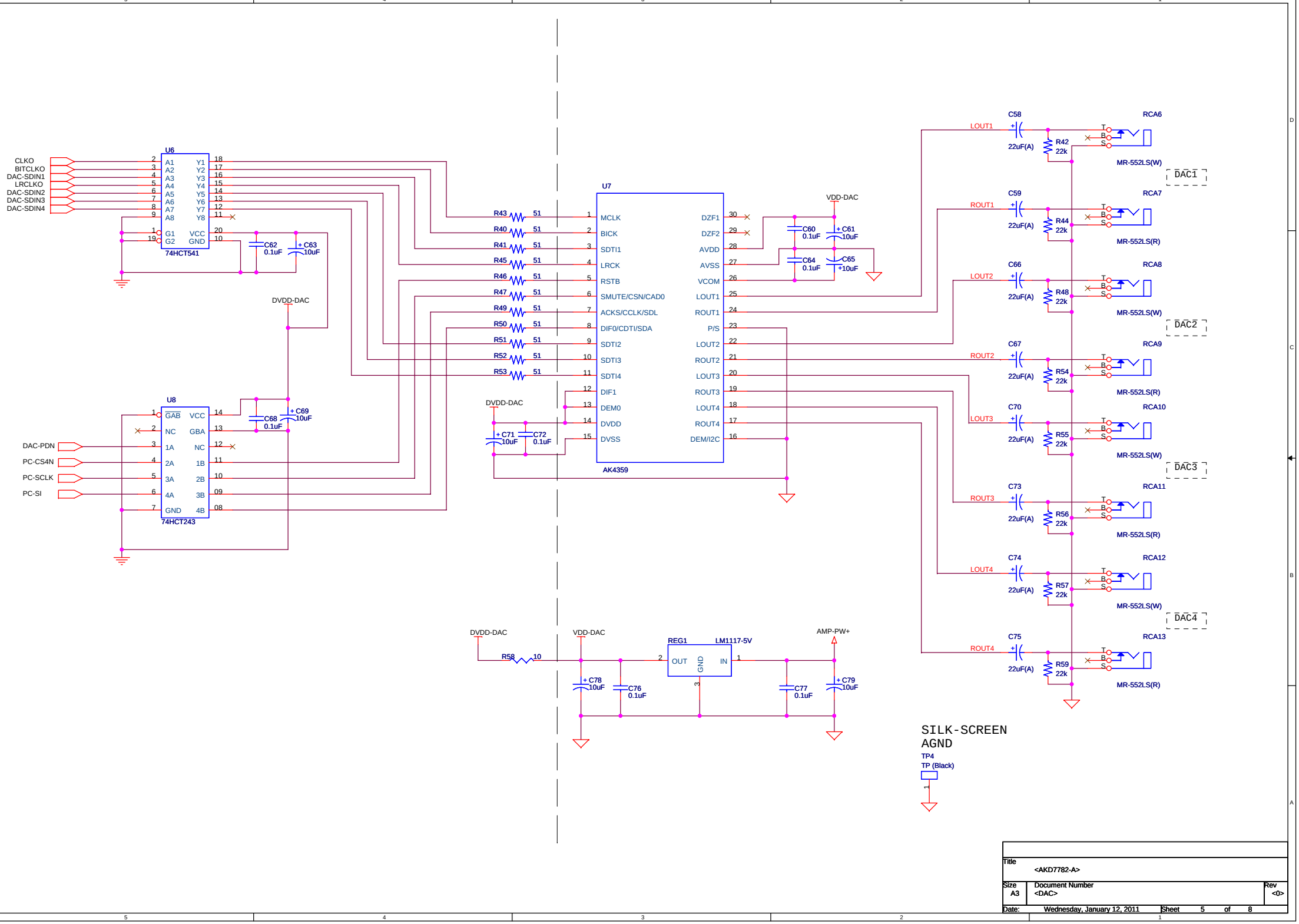

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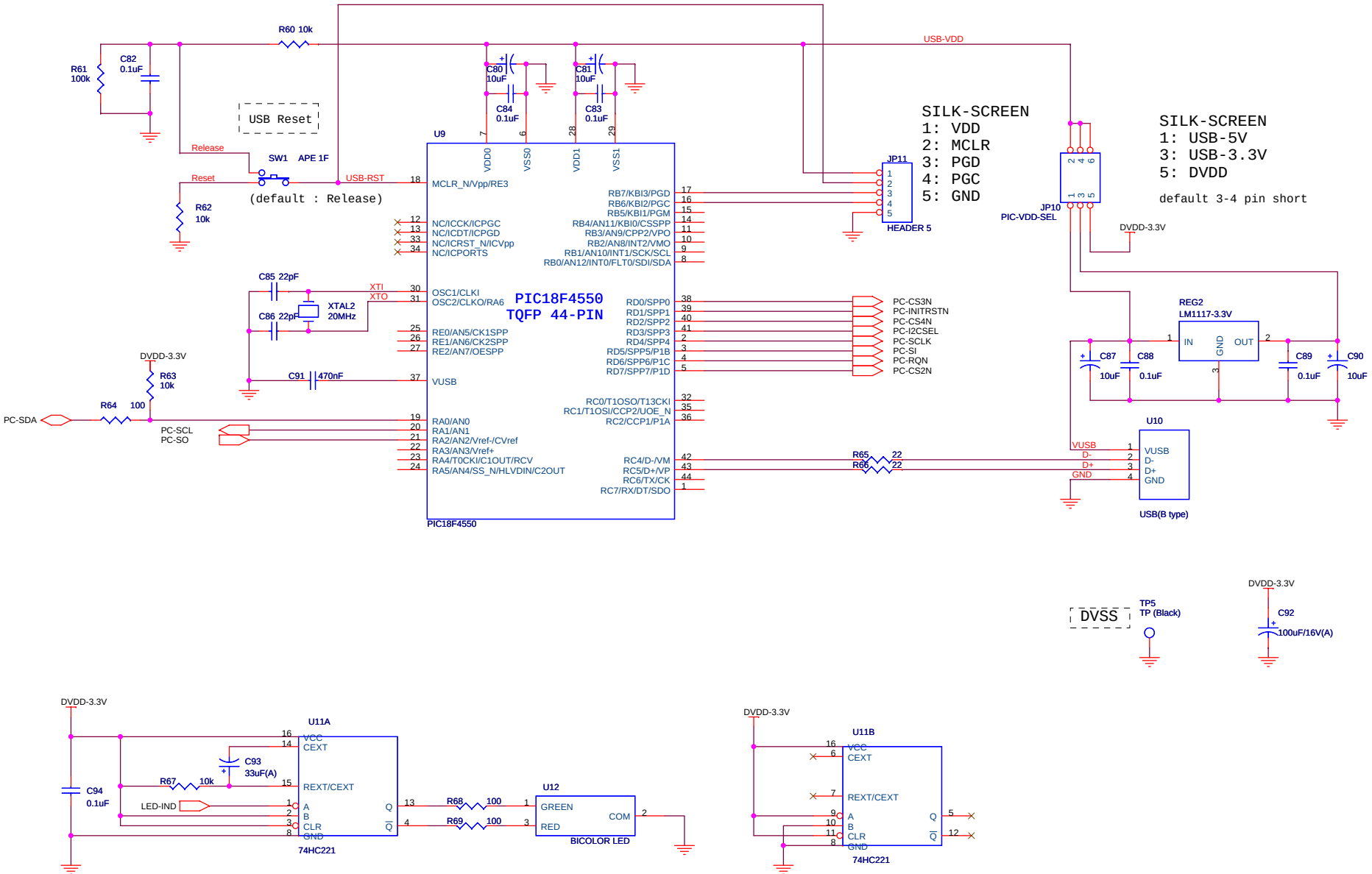

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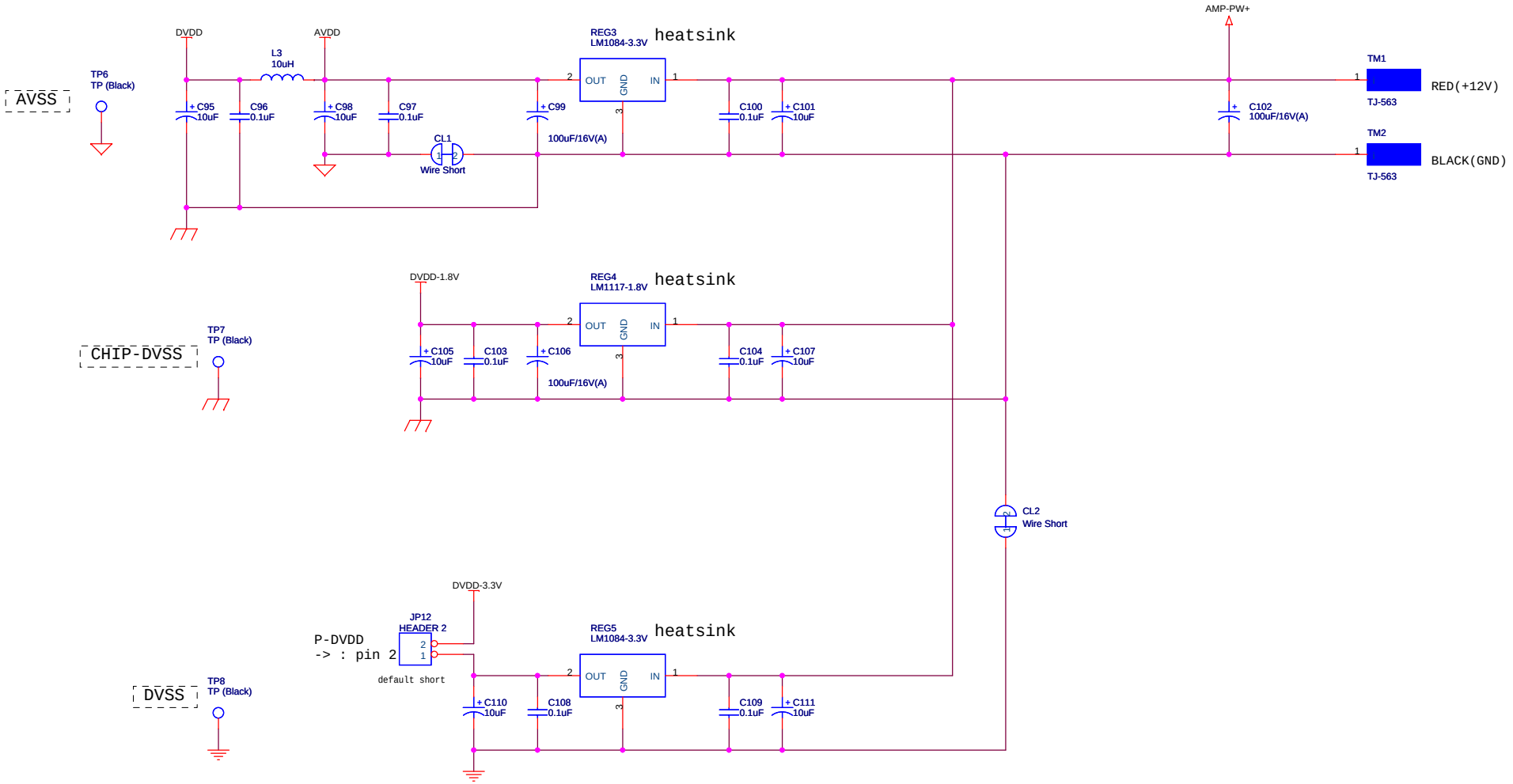

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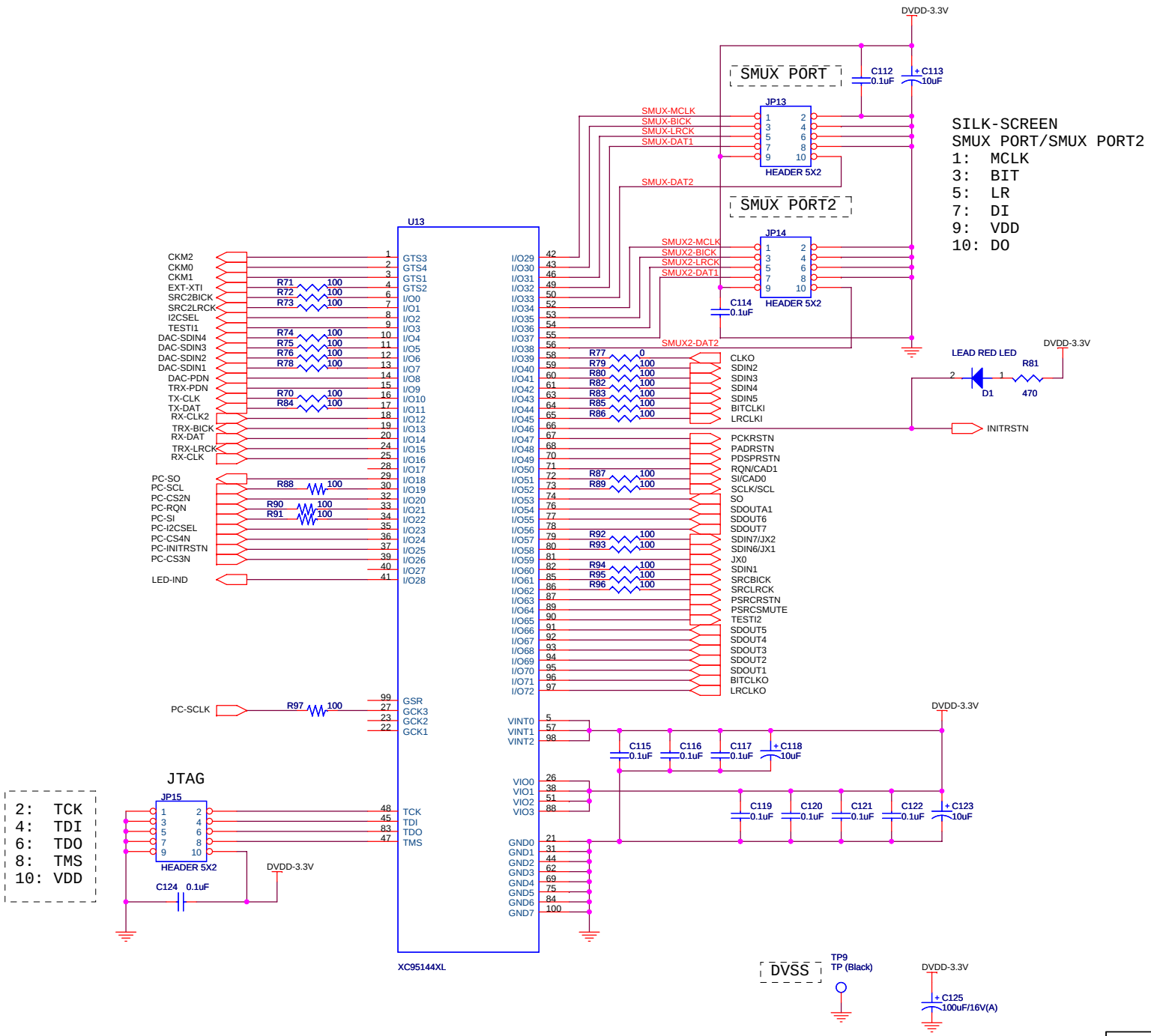
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HEADER 5X2
SMUX-MCLK
SMUX-BICK
SMUX-LRCK
SMUX-DAT1
SMUX-DAT2
SMUX PORT2
JP14
HEADER 5X2
SMUX2-MCLK
SMUX2-BICK
SMUX2-LRCK
SMUX2-DAT1
SMUX2-DAT2
C112 0.1uF
C113 10uF
C114 0.1uF
DVDD-3.3V
SILK-SCREEN
SMUX PORT/SMUX PORT2
1: MCLK
3: BIT
5: LR
7: DI
9: VDD
10: DO
LEAD RED LED
R81 470
D1
INITRSTN
U13
XC95144XL
CKM2
CKM0
CKM1
EXT-XTI
SRC2BICK
SRC2LRCK
I2CSEL
TESTI1
DAC-SDIN4
DAC-SDIN3
DAC-SDIN2
DAC-SDIN1
DAC-PDN
TRX-PDN
TX-CLK
TX-DAT
RX-CLK2
TRX-BICK
RX-DAT
TRX-LRCK
RX-CLK
PC-SO
PC-SCL
PC-CS2N
PC-RQN
PC-SI
PC-I2CSEL
PC-CS4N
PC-INITRSTN
PC-CS3N
LED-IND
PC-SCLK
CLKO
SDIN2
SDIN3
SDIN4
SDIN5
BITCLKI
LRCLKI
PCKRSTN
PADRSTN
PDSPRSTN
RQN/CAD1
SI/CAD0
SCLK/SCL
SO
SDOUTA1
SDOUT6
SDOUT7
SDIN7/JX2
SDIN6/JX1
JX0
SDIN1
SRCBICK
SRCLRCK
PSRCRSTN
PSRCSMUTE
TESTI2
SDOUT5
SDOUT4
SDOUT3
SDOUT2
SDOUT1
BITCLKO
LRCLKO
JTAG
JP15
HEADER 5X2
2: TCK
4: TDI
6: TDO
8: TMS
10: VDD
C124 0.1uF
TCK
TDI
TDO
TMS
C115 0.1uF
C116 0.1uF
C117 0.1uF
C118 10uF
C119 0.1uF
C120 0.1uF
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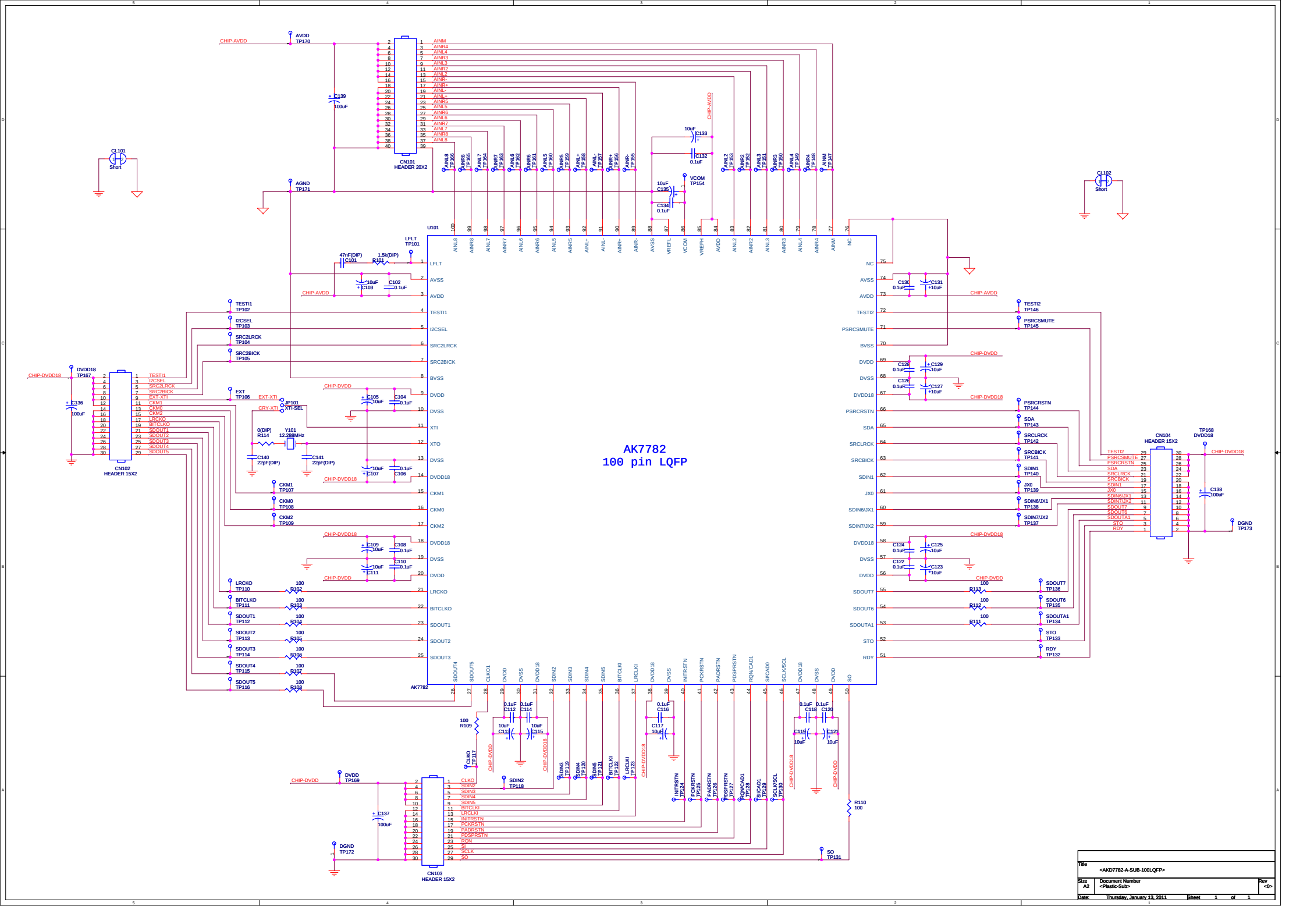

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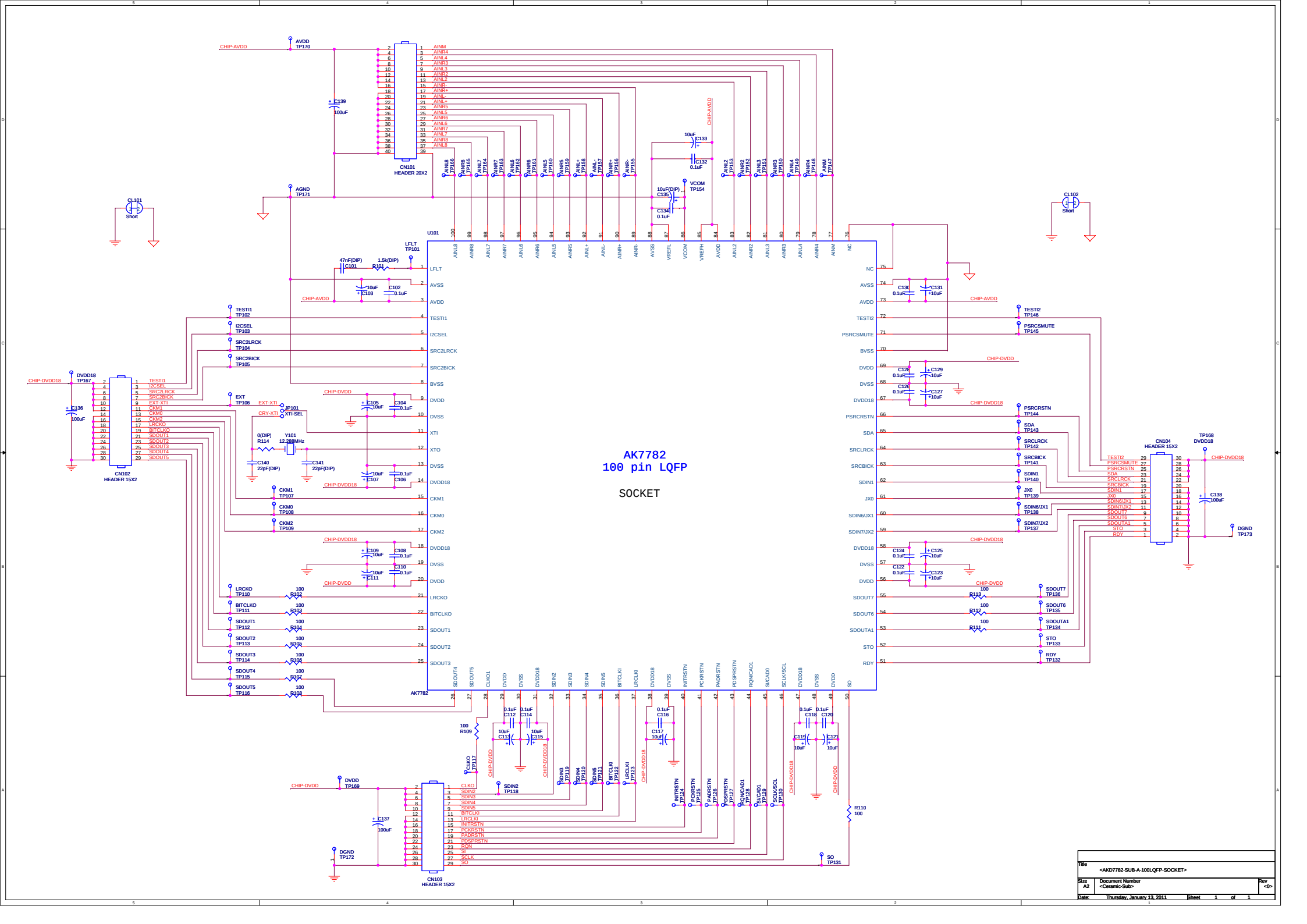
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U101
AK7782
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CN102
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CN103
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CN104
HEADER 15X2
CL101
Short
CL102
Short
AVDD
TP170
AGND
TP171
CHIP-AVDD
CHIP-DVDD
CHIP-DVDD18
VCOM
TP154
LFLT
TP101
TESTI1
TP102
I2CSEL
TP103
SRC2LRCK
TP104
SRC2BICK
TP105
EXT
TP106
JP101
XTI-SEL
CKM1
TP107
CKM0
TP108
CKM2
TP109
LRCKO
TP110
BITCLKO
TP111
SDOUT1
TP112
SDOUT2
TP113
SDOUT3
TP114
SDOUT4
TP115
SDOUT5
TP116
CLKO
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SDIN3
TP119
SDIN4
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SDIN5
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TP123
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TP124
PCKRSTN
TP125
PADRSTN
TP126
PDSPRSTN
TP127
RQN/CAD1
TP128
SI/CAD0
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SCLK/SCL
TP130
SDA
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SRCLRCK
TP142
SRCBICK
TP141
SDIN1
TP140
JX0
TP139
SDIN6/JX1
TP138
SDIN7/JX2
TP137
SDOUT7
TP136
SDOUT6
TP135
SDOUTA1
TP134
STO
TP133
RDY
TP132
PSRCSMUTE
TP145
PSRCRSTN
TP144
TESTI2
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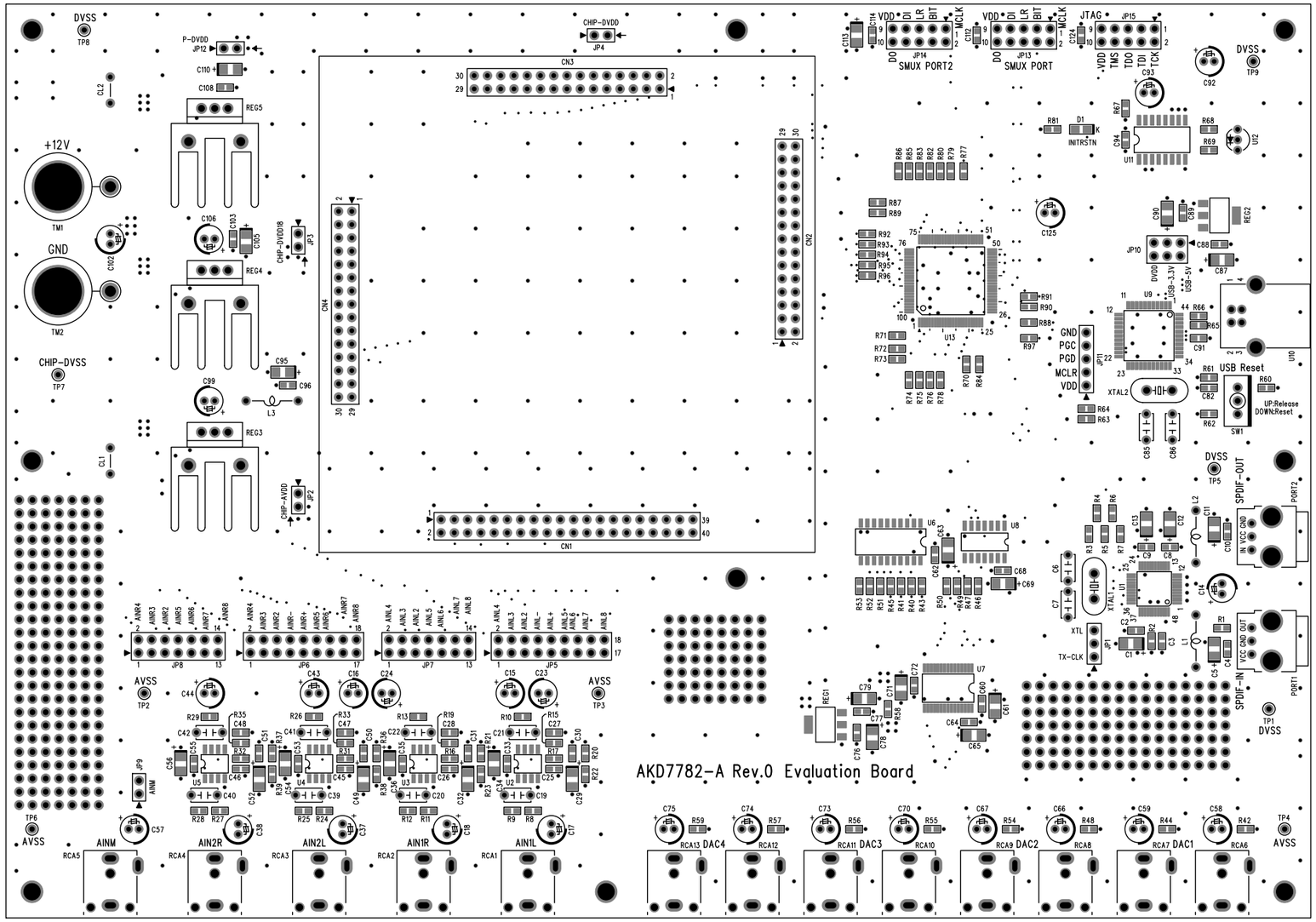

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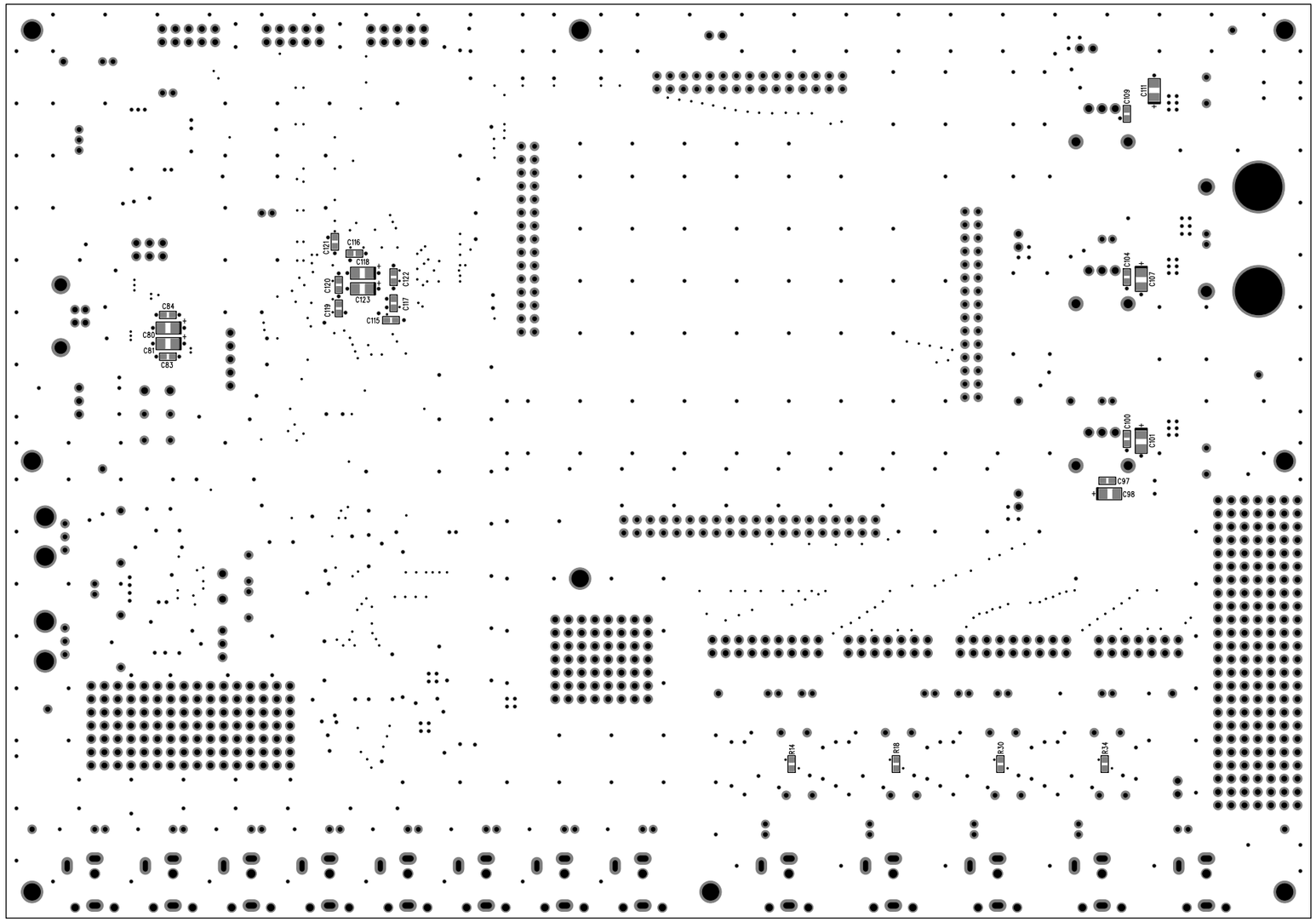
2011.2.16



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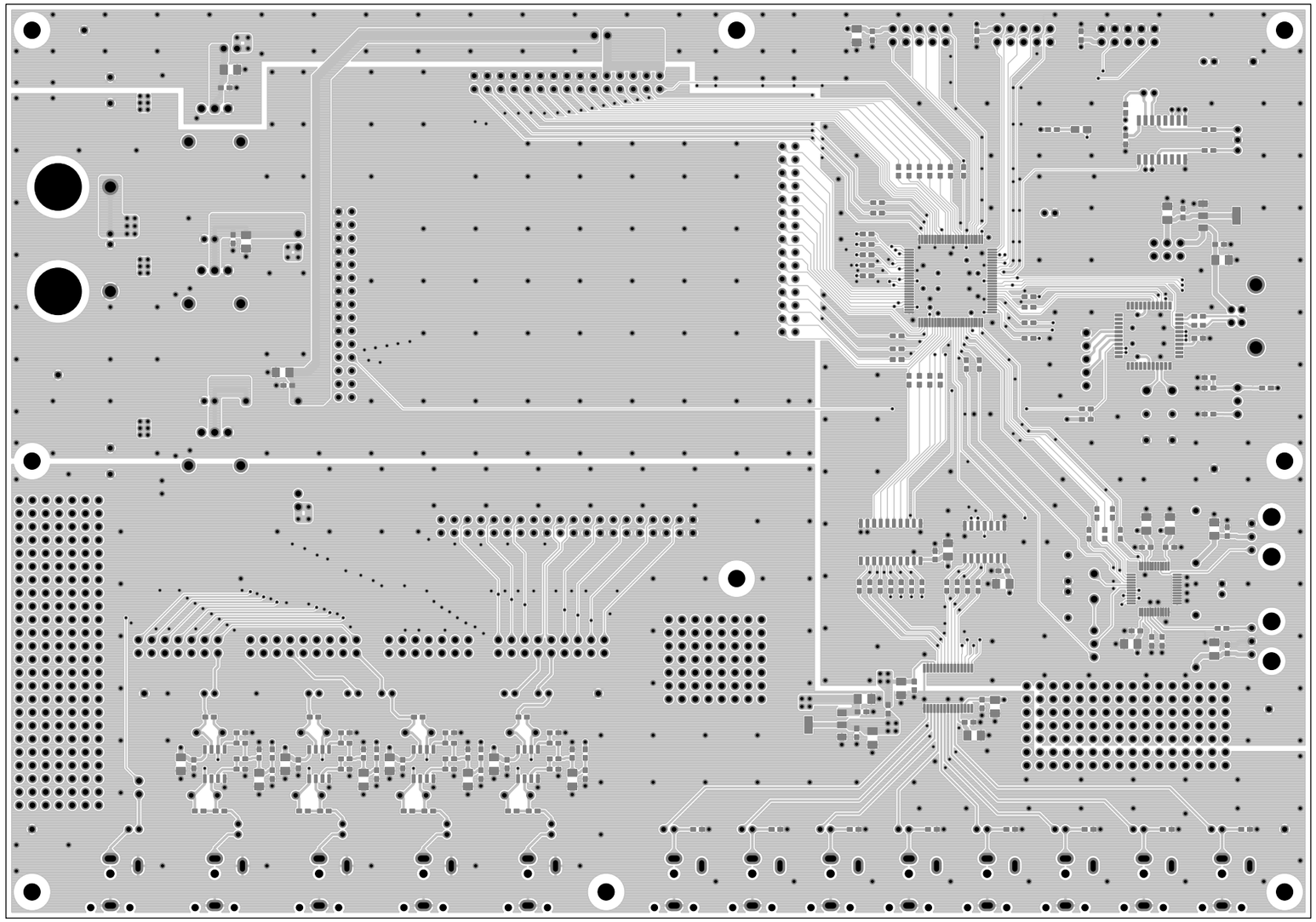

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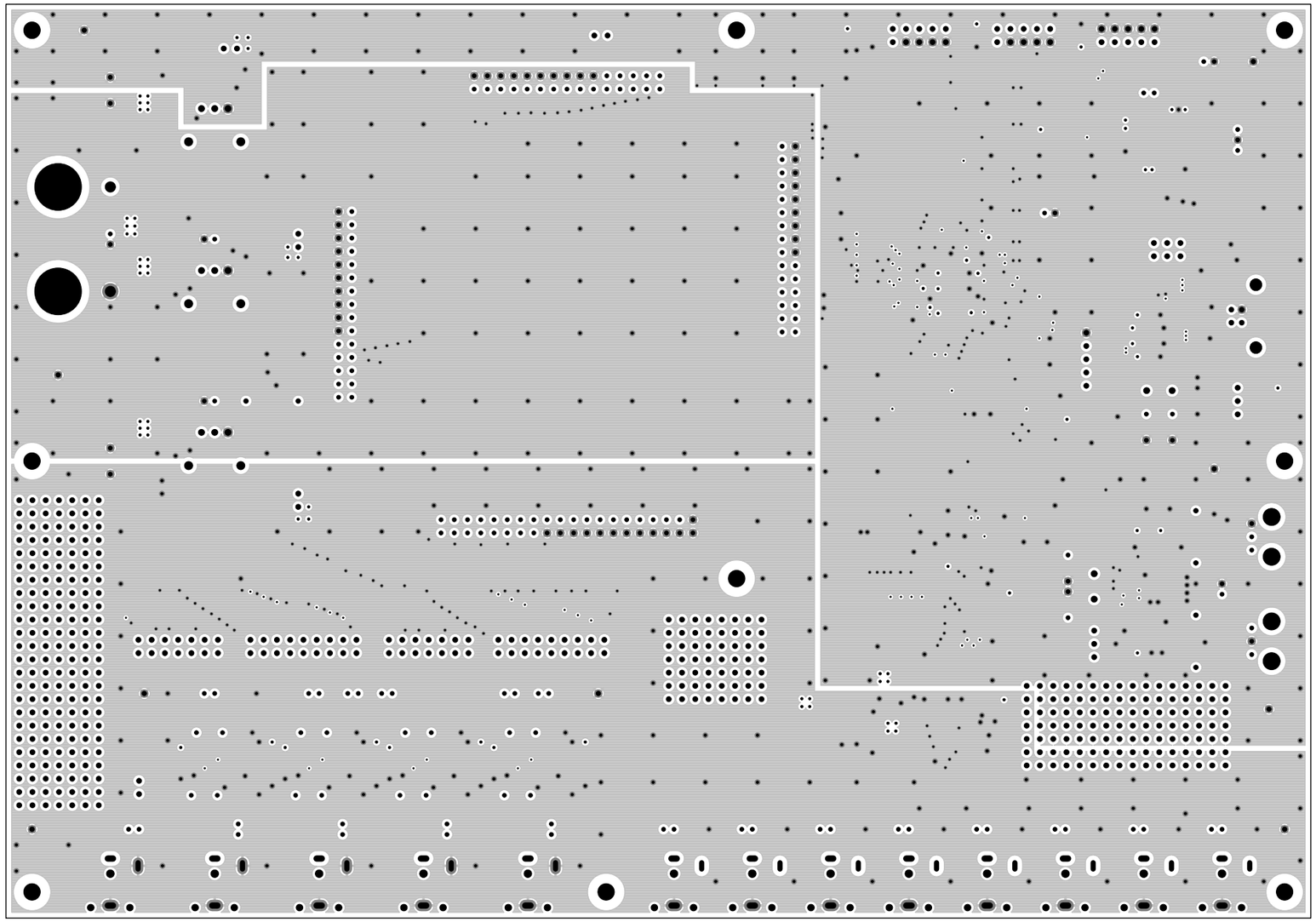

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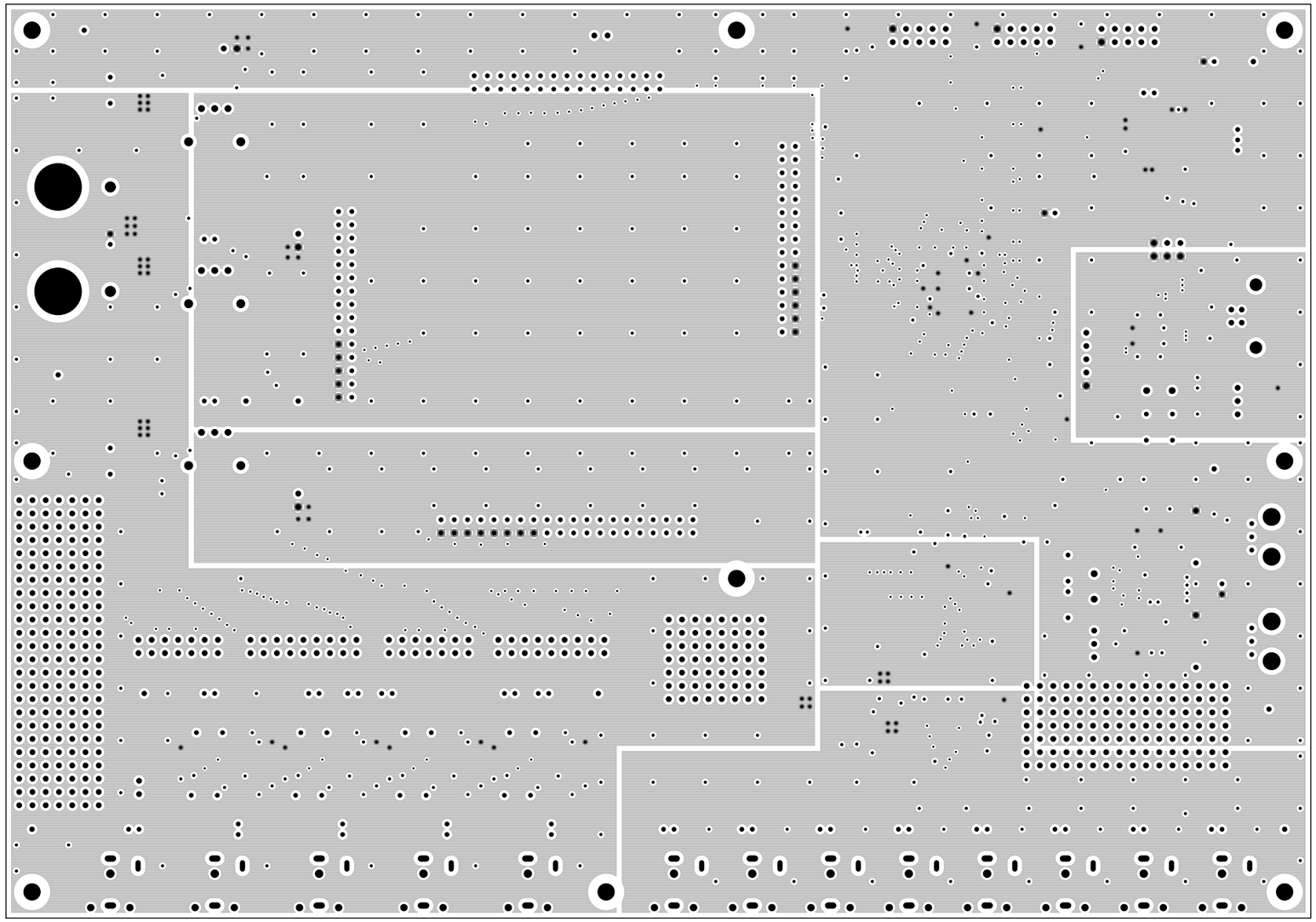

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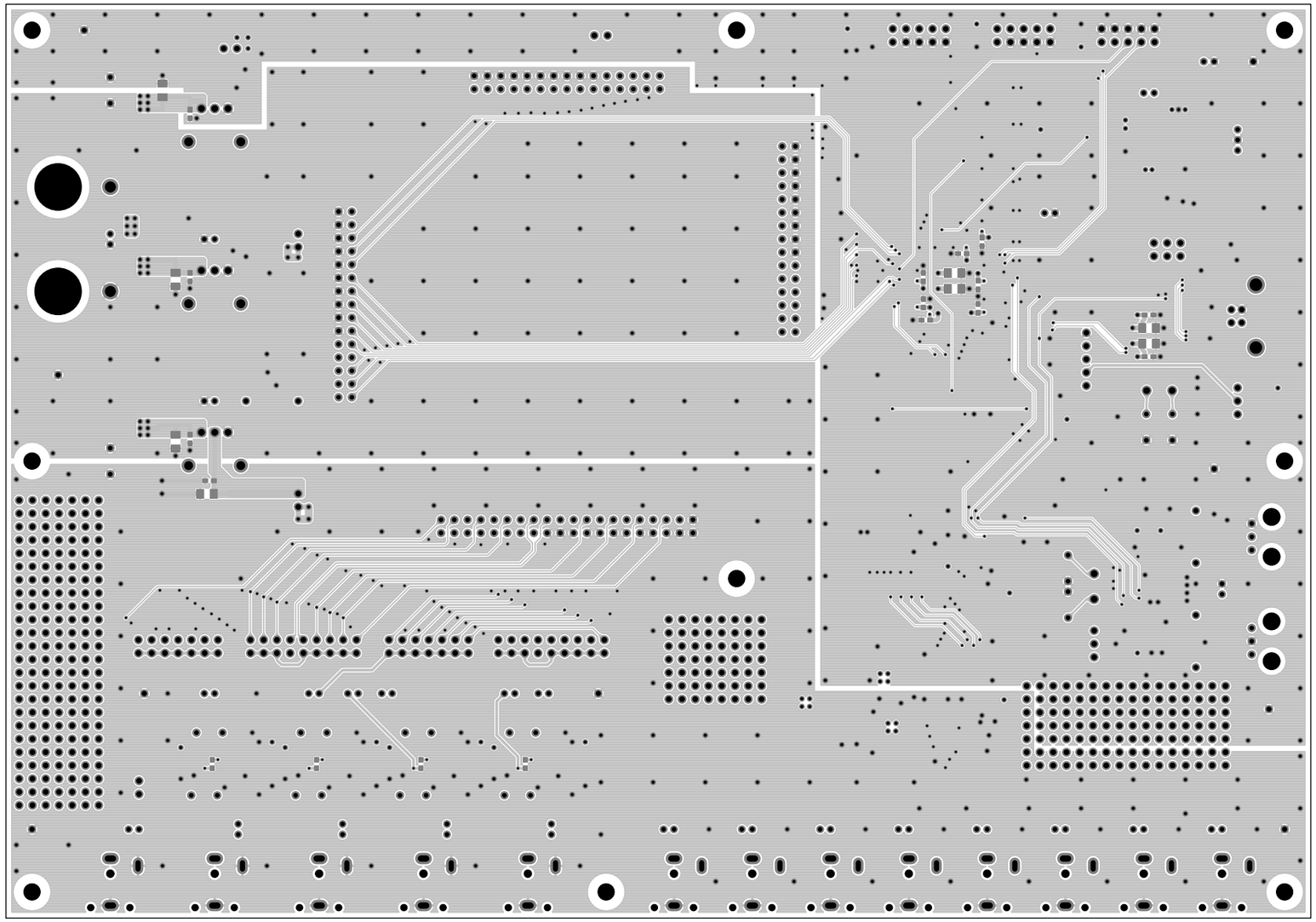

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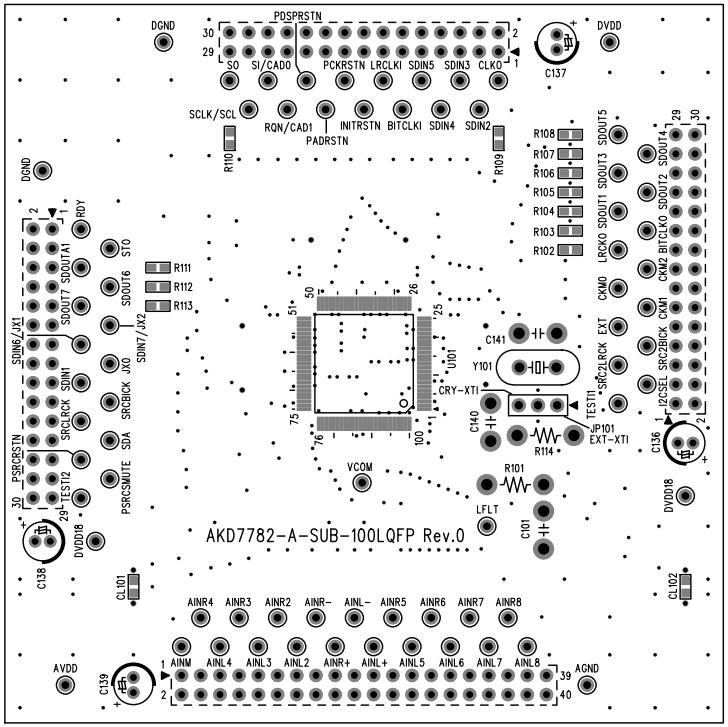

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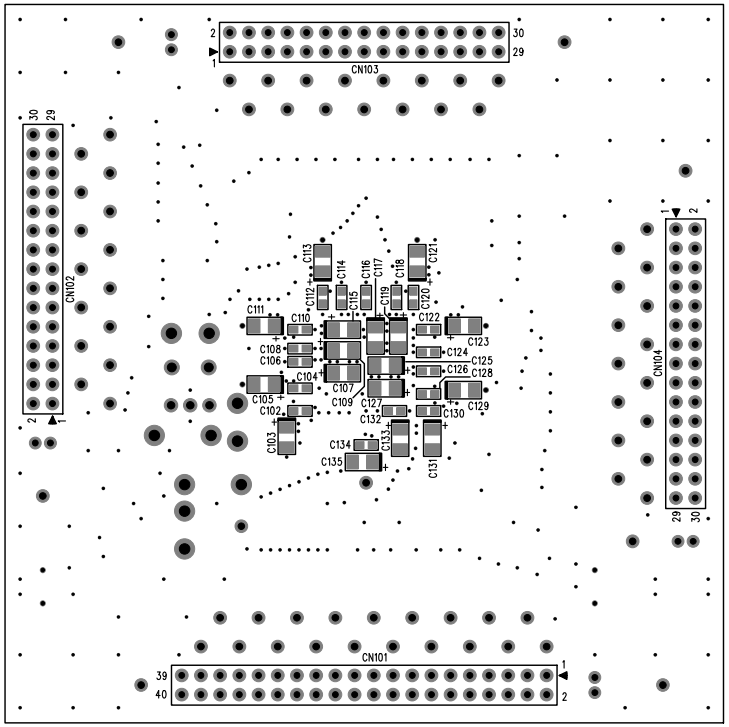

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AKD7782-A-SUB-100L0F0
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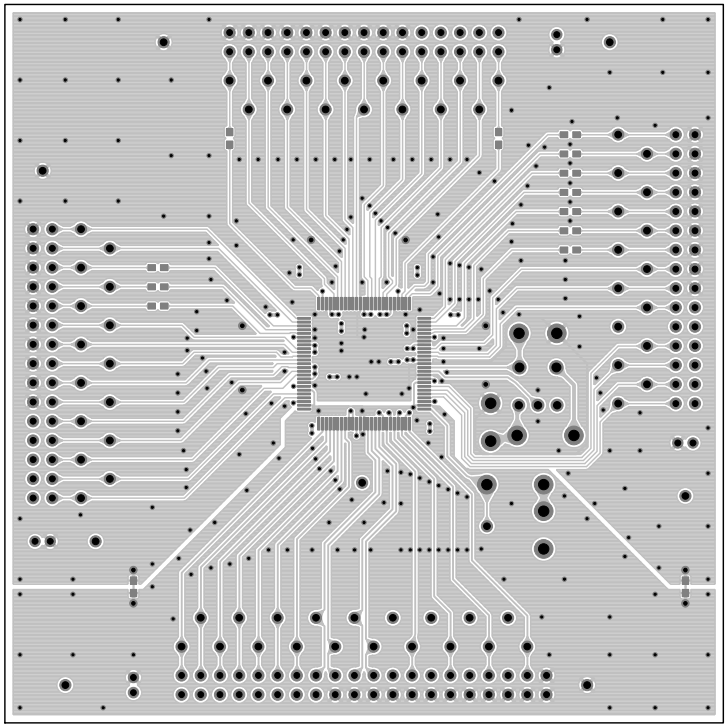

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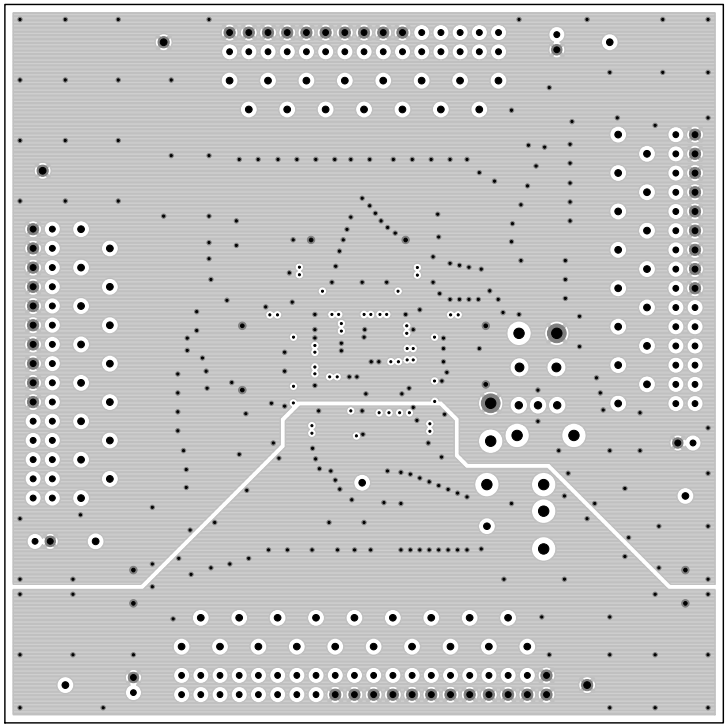

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AKD7782-A-SUB-100LQFP
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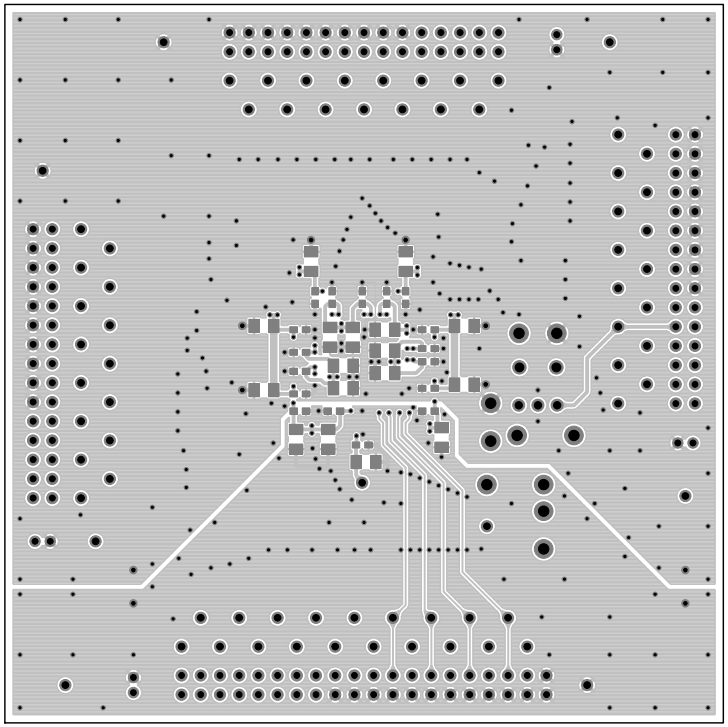

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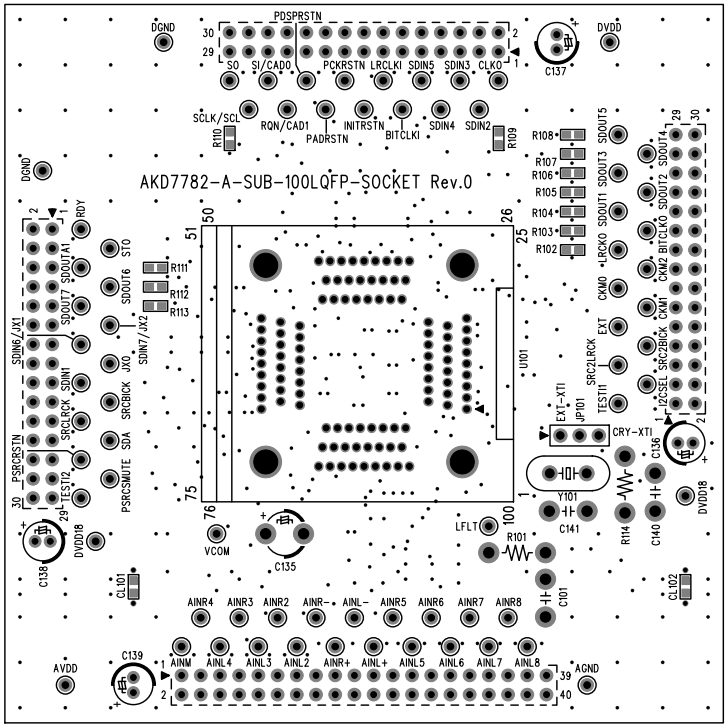

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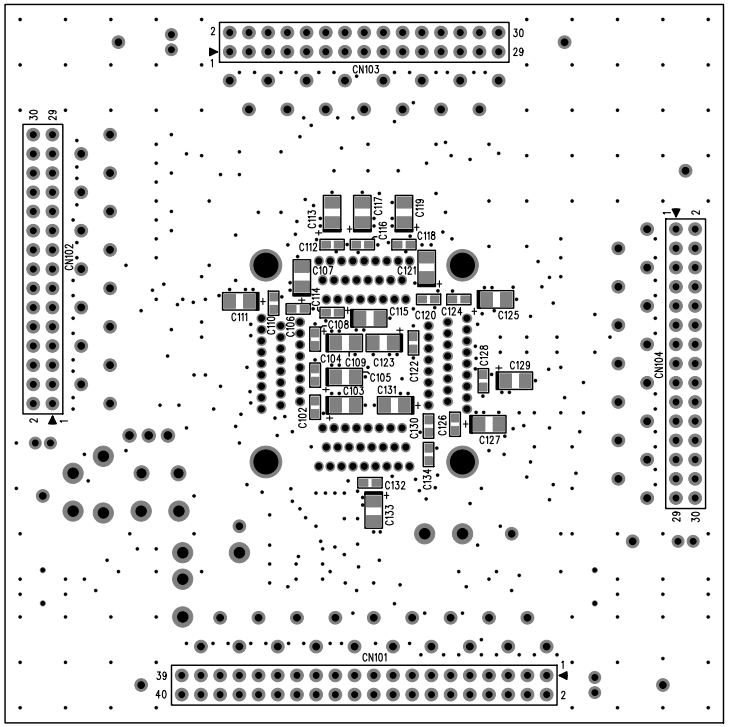

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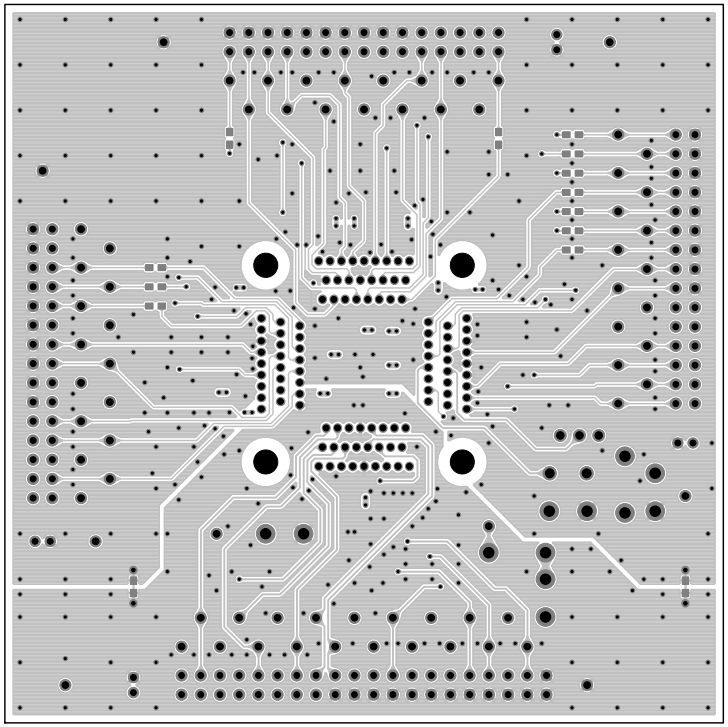

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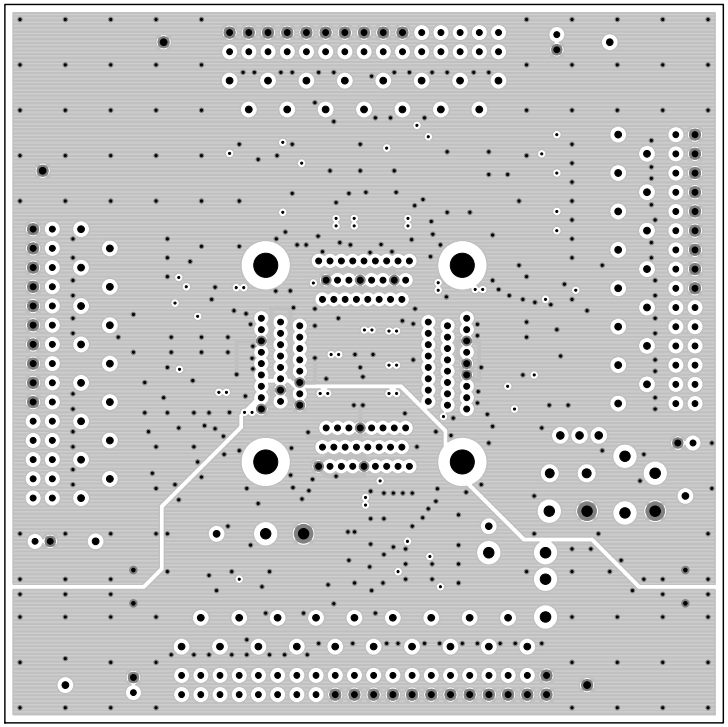

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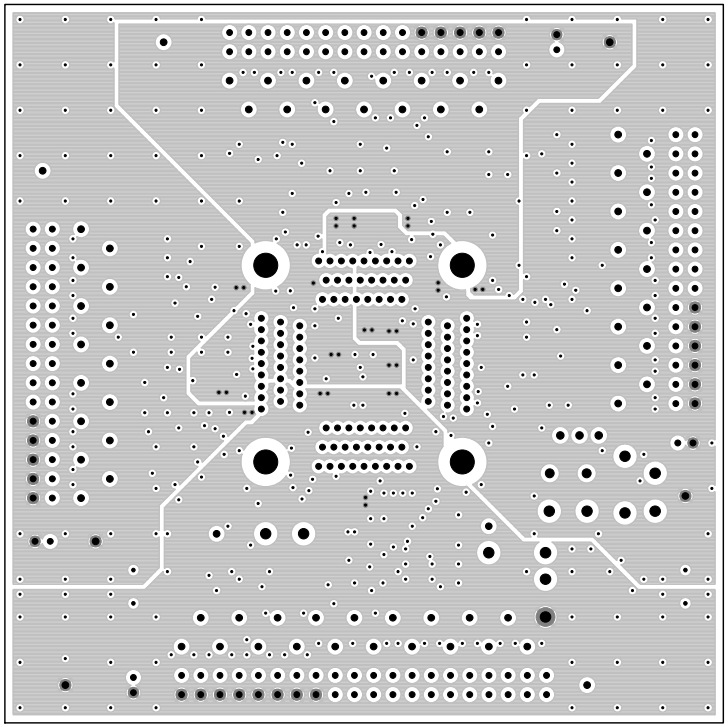

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AKD7782-A-SUB-100LQFP-SOCKET Layout
2011.2.14