CHRONTEL

Dual Graphics Clock Generator

Features

- Generates 16 preset video clock frequencies and 16 preset memory clock frequencies
- Supports output frequencies up to 130 MHz
- Draws less than 1 μA in power down mode for "Green PC" applications
- Requires only four external components: one 14.318 MHz crystal and three 0.1 μF capacitors
- Proprietary VCO design for low phase jitter
- Supports graphics standards such as EGA, VGA, Super-VGA, XGA™, and 8514
- Backward pin compatible with CH920x series and ICS1394
- CMOS technology in 20-pin PDIP and SOIC
- 5V or 3.3V supply. For specific details on the 3.3V version, please consult Chrontel.

Description

CH9204 is a dual PLL clock generator designed for low power, high performance applications, such as graphics systems based on VGA, Super-VGA, XGA™, and 8514 formats.

Since CH9204's power down feature typically draws less than 1 μA of supply current, it is ideal for notebook, palmtop, and other portable applications. It is also well-suited for applications requiring multiple clocks, such as disk drives, CD-ROM systems, and modems.

CH9203 provides separate memory (MCLK) and video (VCLK) clocks. The minimum and maximum frequencies of both clock outputs can be as low as 8 MHz, and as high as 130 MHz. The reference frequency is 14.318 MHz, which is derived from either a crystal or an external reference frequency. Other input frequencies can be used to obtain different output frequencies.
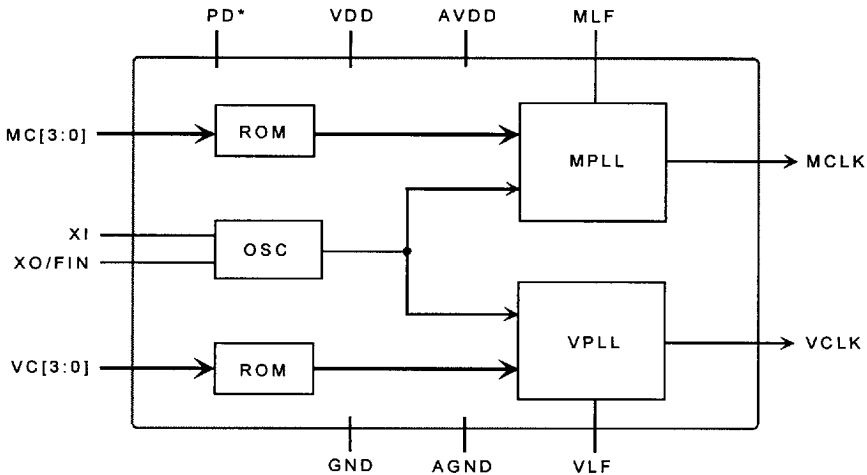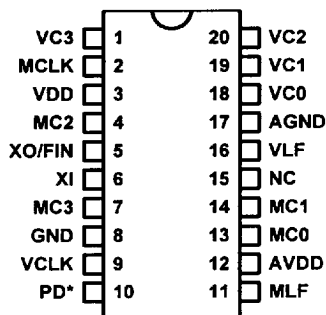
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Figure 1: Block Diagram

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        VC3  ⌷ 1      20 ⌷  VC2
       MCLK  ⌷ 2      19 ⌷  VC1
        VDD  ⌷ 3      18 ⌷  VC0
        MC2  ⌷ 4      17 ⌷  AGND
      XO/FIN ⌷ 5      16 ⌷  VLF
         XI  ⌷ 6      15 ⌷  NC
        MC3  ⌷ 7      14 ⌷  MC1
        GND  ⌷ 8      13 ⌷  MC0
       VCLK  ⌷ 9      12 ⌷  AVDD
        PD*  ⌷ 10     11 ⌷  MLF
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Figure 2: CH9204B and L

Table 1 • Pin Description CH9204B and L

Pin	Type	Symbol	Description
1, 18, 19, 20	In	VC3, VC0, VC1, VC2	Video clock select (internal pull-up)
2	Out	MCLK	Memory clock output
3	Power	VDD	5V supply
4, 7, 13, 14	In	MC2, MC3, MC0, MC1	Memory clock select (internal pull-up)
5	Out / In	XO / FIN	Crystal output or external FREF input
6	In	XI	Crystal input
8	Power	GND	Ground
9	Out	VCLK	Video clock output
10	In	PD*	Power down input (active low)
11	In	MLF	Memory loop filter
12	Power	AVDD	Analog 5V supply
15	–	NC	No connect, **MUST BE LEFT OPEN**
16	In	VLF	Video loop filter
17	Power	AGND	Analog ground

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Table 2 • Frequencies for CH9204B and L (in MHz)

Video Clock

Frequency Select (FS)				VCLK	
FS3	FS2	FS1	FS0	Ver B	Ver L
0	0	0	0	25.175	25.175
0	0	0	1	28.322	28.322
0	0	1	0	32.514	40.0
0	0	1	1	36.0	72.0
0	1	0	0	40.0	50.0
0	1	0	1	44.9	77.0
0	1	1	0	50.35	36.0
0	1	1	1	65.0	44.9
1	0	0	0	78.0	90.0
1	0	0	1	56.644	120.0
1	0	1	0	63.0	80.0
1	0	1	1	75.0	31.5
1	1	0	0	80.0	110.0
1	1	0	1	89.8	65.0
1	1	1	0	100.7	75.0
1	1	1	1	31.5 (default)	94.5 (default)

Memory Clock

Memory Select (MS)				MCLK	
MS3	MS2	MS1	MS0	Ver B	Ver L
0	0	0	0	80.0	80.0
0	0	0	1	78.0	78.0
0	0	1	0	75.0	75.0
0	0	1	1	72.0	72.0
0	1	0	0	70.0	70.0
0	1	0	1	68.0	68.0
0	1	1	0	66.0	66.0
0	1	1	1	63.0	63.0
1	0	0	0	60.0	60.0
1	0	0	1	58.0	58.0
1	0	1	0	50.0	50.0
1	0	1	1	45.0	45.0
1	1	0	0	55.0	55.0
1	1	0	1	48.0	48.0
1	1	1	0	60.0	60.0
1	1	1	1	40.0 (default)	40.0 (default)

Power Down Mode

When power down is active (logic low), CH9204 is placed in standby mode, drawing less than 1 µA of current. All outputs are tristated and both internal PLLs are disabled to minimize power consumption. After power up, CH9204 typically requires 40 ms for the PLLs to stabilize.

Variable Output Drive Current

For output frequencies less than 50 MHz, the output source current is typically 4.0 mA and the sink current is 6.0 mA. When the output frequency is higher than 50 MHz, the output source and sink currents automatically increase to 6.0 mA and 8.0 mA, respectively. This feature adjusts the output rise and fall times for different applications. In some cases, fast rise and fall times may cause excessive electromagnetic interference.

CH9204 Advantages and Compatibility

The pinout diagrams of Chrontel's CH920x-series are based on those of CH9201 and ICS1394. If a board was originally designed for CH9201 or ICS1394, only the following minor changes are required in the board layout to upgrade to CH9204:

1. Instead of using a separate oscillator for the VGA controller memory clock (MCLK), CH9204 provides the MCLK output at pin 2.

2. By connecting the CH9204 AVDD directly to the 5V supply, the zener diode necessary for CH9201 and ICS1394 designs is eliminated and further power consumption is reduced.

3. MC0 – MC3 jumpers may be required for proper MCLK frequency selection. The MCLK frequency defaults to 40 MHz if MC0-MC3 are left open (internal pull-up).

4. Two 0.1 µF capacitors are needed: one between pins 11 and 12 for the memory loop filter, and the other between pins 16 and 12 for the video loop filter.

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Table 3 • Absolute Maximum Ratings

Symbol	Description	Value	Unit
VDD	Power supply voltage with respect to GND	−0.5 to +7.0	V
VIN	Input voltage on any pins with respect to GND	−0.5 to VDD +0.5	V
TSTOR	Storage temperature	−55 to +150	°C

Note: Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the normal operating conditions is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 4 • DC Specifications (Operating Conditions: $T_A = 0°C - 70°C$, $V_{DD} = 5V \pm 5\%$)

Symbol	Description	Test Condition @TA = 25°C	Min	Typ	Max	Unit
VOH	Output high voltage	VDD = 4.75V, IOH = 4mA	2.4			V
VOL	Output low voltage	VDD = 4.75V, IOL = 8mA			0.4	V
VIH	Input high voltage		2.0			V
VIL	Input low voltage				0.8	V
IPU	Input pull-up current			5	20	µA
ILK	Input leakage current		−10		10	µA
ISTBY	Standby current	PD* = Low		1	10	µA
IDD	Operating current	VDD = 5V VCLK = 50MHz MCLK = 55MHz		45		mA

Table 5 • AC Specifications (Operating Conditions: $T_A = 0°C - 70°C$, $V_{DD} = 5V \pm 5\%$)

Symbol	Description	Test Condition @TA = 25°C	Min	Typ	Max	Unit
FIN	Crystal / FREF input			14.318		MHz
VCLK	Video clock frequency		8		130	MHz *
MCLK	Memory clock frequency		8		130	MHz *
TR	Output clock rise time	CL = 25pF, VOL − VOH		2		ns
TF	Output clock fall time	CL = 25pF, VOL − VOH		2		ns
TDC	Output clock duty cycle	VDD = 5V @VDD / 2	40	50	60	%

Note: * Output levels are guaranteed up to 90 MHz. Please consult Chrontel for suggested circuit implementations for frequencies higher than 90 MHz.
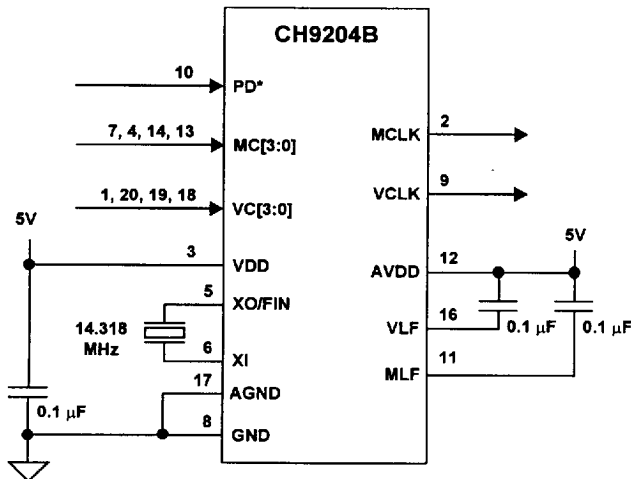
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CH9204B

Pin	Signal
10	PD*
7, 4, 14, 13	MC[3:0]
1, 20, 19, 18	VC[3:0]
3	VDD
5	XO/FIN
6	XI
17	AGND
8	GND
2	MCLK
9	VCLK
12	AVDD
16	VLF
11	MLF

5V

14.318 MHz

0.1 µF

5V

0.1 µF   0.1 µF

Figure 3: Application Schematic

ORDERING INFORMATION			
Part number	Package type	Number of pins	Voltage supply
CH9204Cx-NC	300 mil PDIP	20	5V
CH9204Cx-SC	300 mil SOIC	20	5V
Note: x = frequency table version			

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