

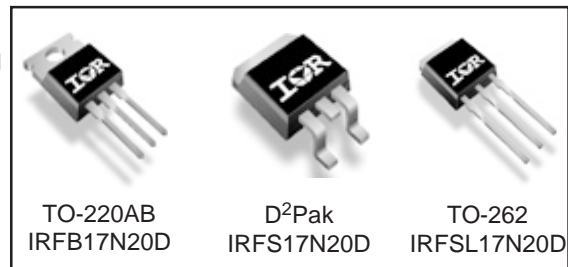
Applications

- High frequency DC-DC converters

V_{DSS}	R_{DS(on)} max	I_D
200V	0.17Ω	16A

Benefits

- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C_{OSS} to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current



Absolute Maximum Ratings

	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	16	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V	12	
I _{DM}	Pulsed Drain Current ①	64	
P _D @ T _A = 25°C	Power Dissipation ②	3.8	W
P _D @ T _C = 25°C	Power Dissipation	140	
	Linear Derating Factor	0.90	W/°C
V _{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③	2.7	V/ns
T _J	Operating Junction and	-55 to + 175	°C
T _{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw④	10 lbf•in (1.1N•m)	

Typical SMPS Topologies

- Telecom 48V input Forward Converter

Notes ① through ⑤ are on page 11

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Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	200	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.25	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$ ⑥
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.17	Ω	$V_{GS} = 10V, I_D = 9.8A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.5	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 200V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 160V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 30V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -30V$

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	5.3	—	—	S	$V_{DS} = 50V, I_D = 9.8A$
Q_g	Total Gate Charge	—	33	50	nC	$I_D = 9.8A$ $V_{DS} = 160V$ $V_{GS} = 10V, \text{④⑥}$
Q_{gs}	Gate-to-Source Charge	—	8.4	13		
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	16	24		
$t_{d(on)}$	Turn-On Delay Time	—	11	—	ns	$V_{DD} = 100V$ $I_D = 9.8A$ $R_G = 5.1\Omega$ $V_{GS} = 10V$ ④
t_r	Rise Time	—	19	—		
$t_{d(off)}$	Turn-Off Delay Time	—	18	—		
t_f	Fall Time	—	6.6	—		
C_{iss}	Input Capacitance	—	1100	—	pF	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1.0\text{MHz}$ ⑥
C_{oss}	Output Capacitance	—	190	—		
C_{rss}	Reverse Transfer Capacitance	—	44	—		
C_{oss}	Output Capacitance	—	1340	—		
C_{oss}	Output Capacitance	—	76	—		
$C_{oss \text{ eff.}}$	Effective Output Capacitance	—	130	—		

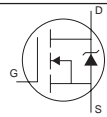
Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy ②⑥	—	240	mJ
I_{AR}	Avalanche Current ①	—	9.8	A
E_{AR}	Repetitive Avalanche Energy ①	—	14	mJ

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.1	$^\circ\text{C}/\text{W}$
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface ⑥	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient ⑥	—	62	
$R_{\theta JA}$	Junction-to-Ambient ⑦	—	40	

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	16	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①⑥	—	—	64		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 9.8A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	160	240	ns	$T_J = 25^\circ\text{C}, I_F = 9.8A$
Q_{rr}	Reverse Recovery Charge	—	900	1350	nC	$di/dt = 100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

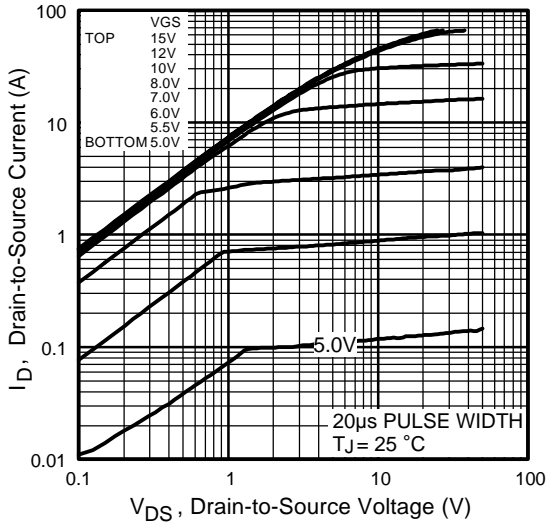


Fig 1. Typical Output Characteristics

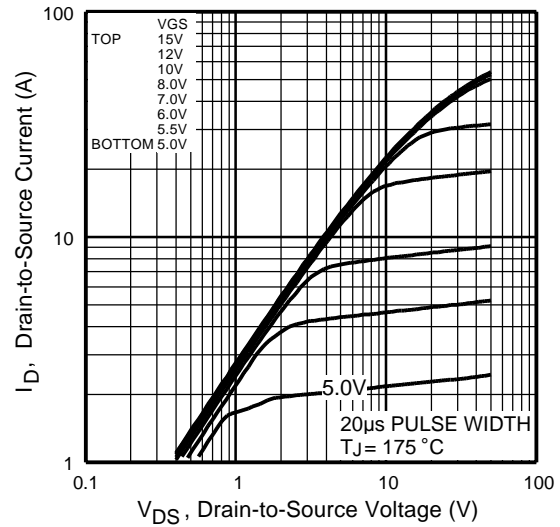


Fig 2. Typical Output Characteristics

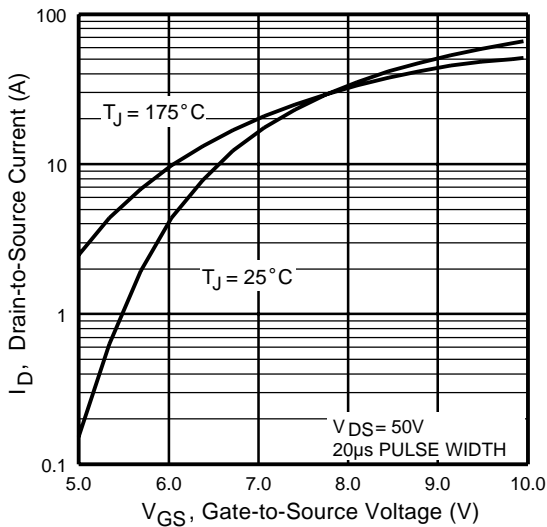


Fig 3. Typical Transfer Characteristics

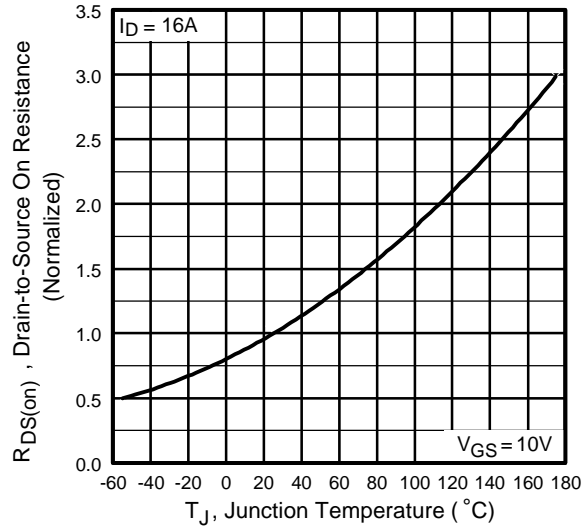


Fig 4. Normalized On-Resistance Vs. Temperature

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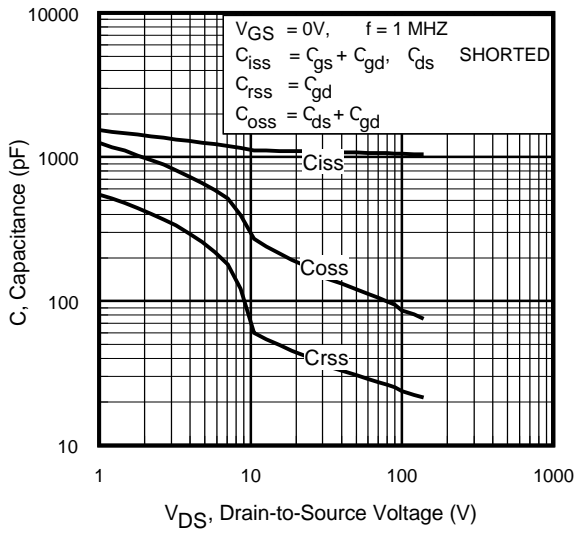


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

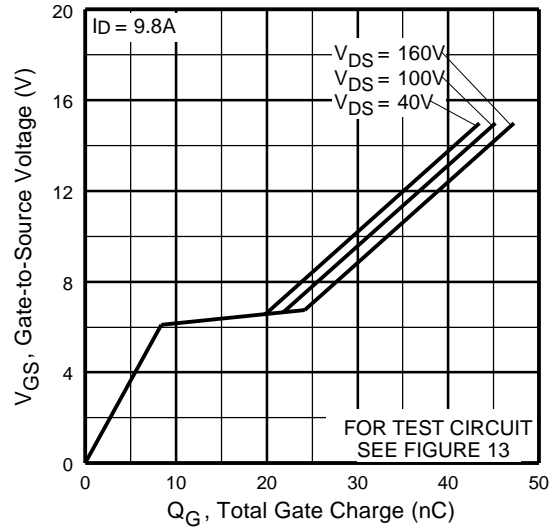


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

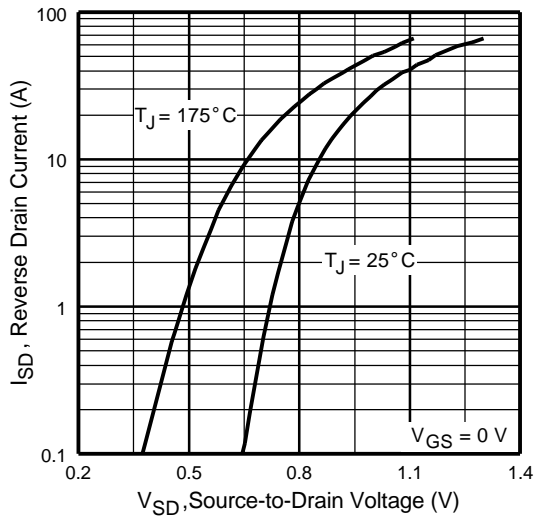


Fig 7. Typical Source-Drain Diode Forward Voltage

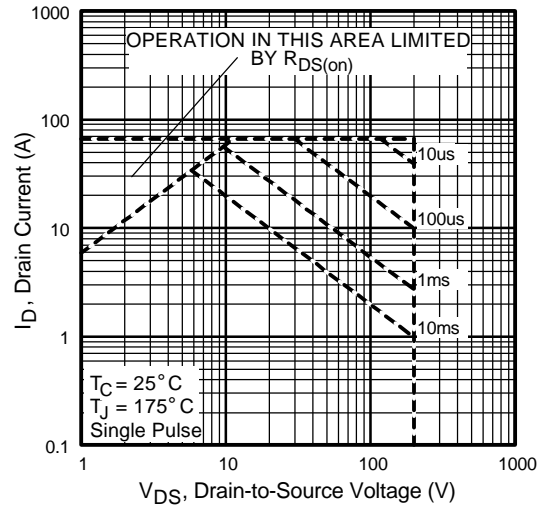


Fig 8. Maximum Safe Operating Area

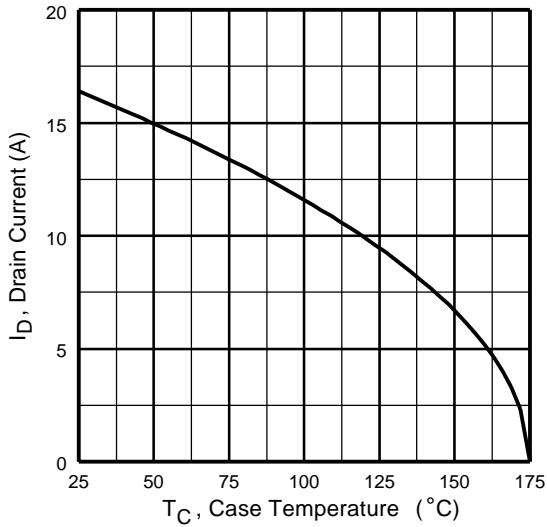


Fig 9. Maximum Drain Current Vs. Case Temperature

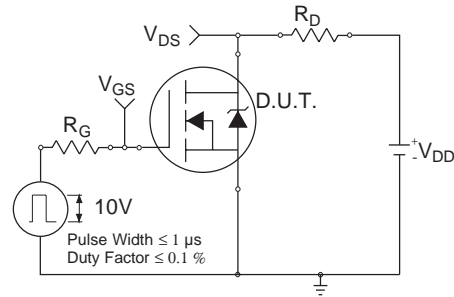


Fig 10a. Switching Time Test Circuit

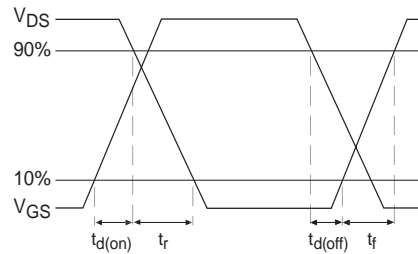


Fig 10b. Switching Time Waveforms

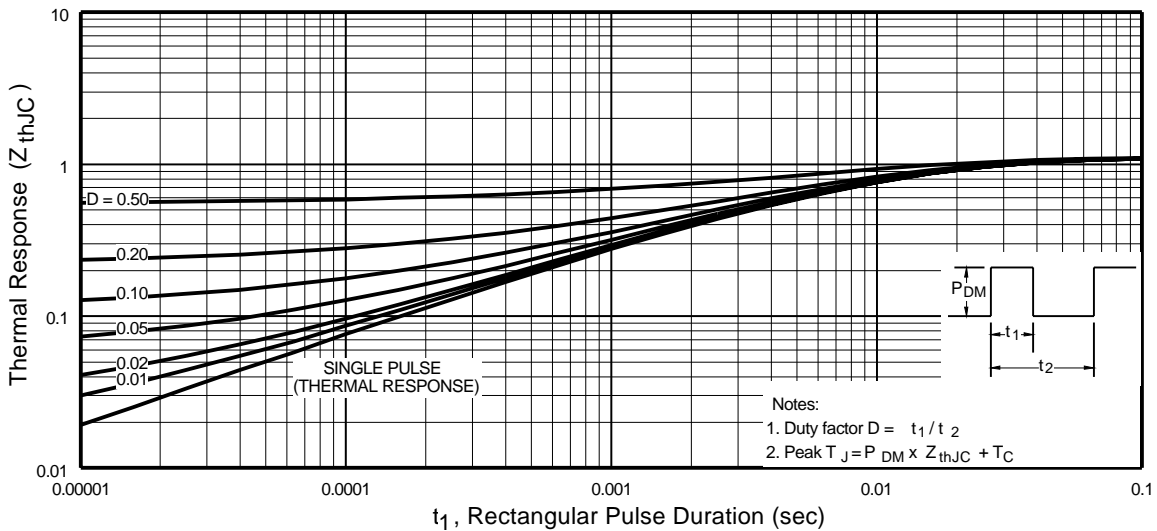


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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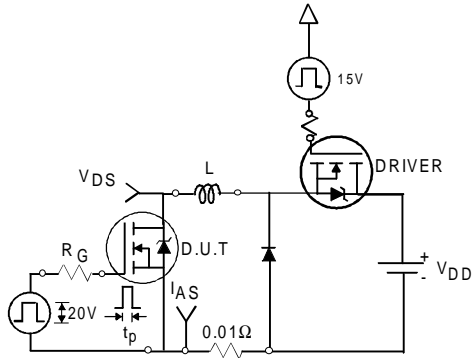


Fig 12a. Unclamped Inductive Test Circuit

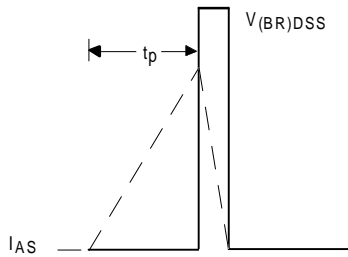


Fig 12b. Unclamped Inductive Waveforms

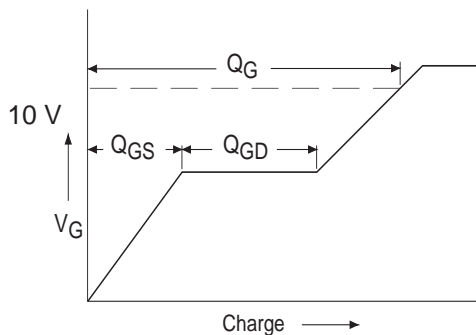


Fig 13a. Basic Gate Charge Waveform

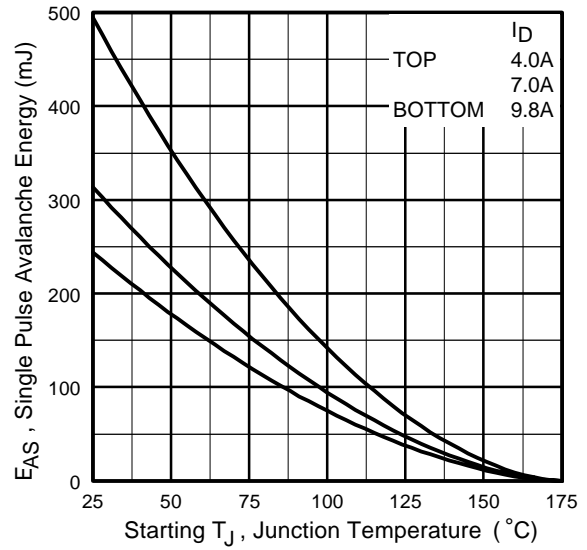


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

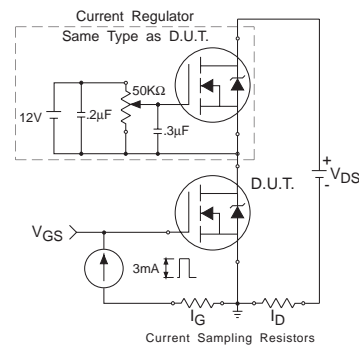
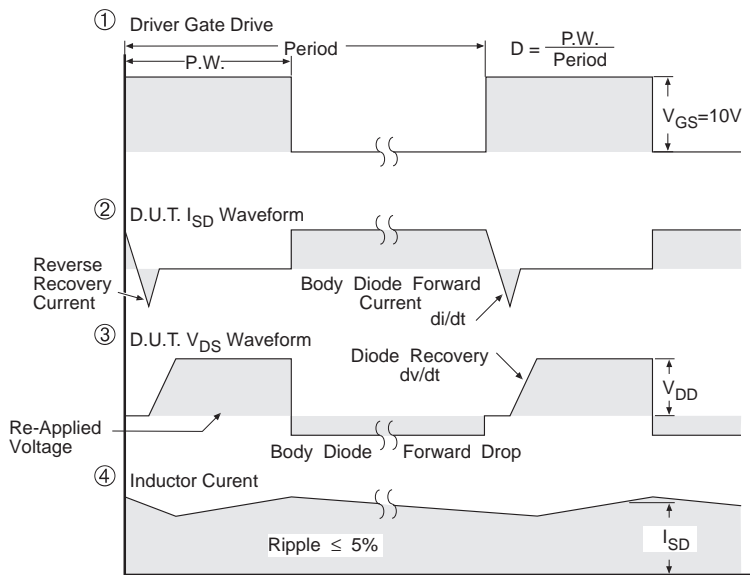
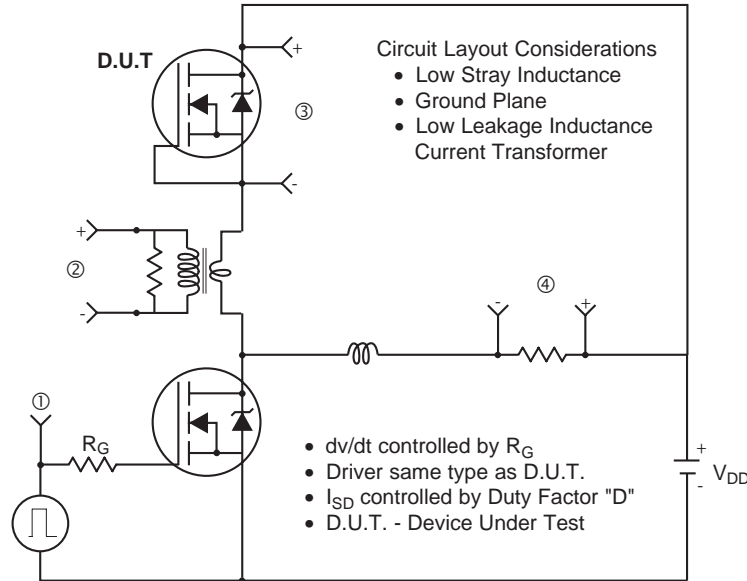


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

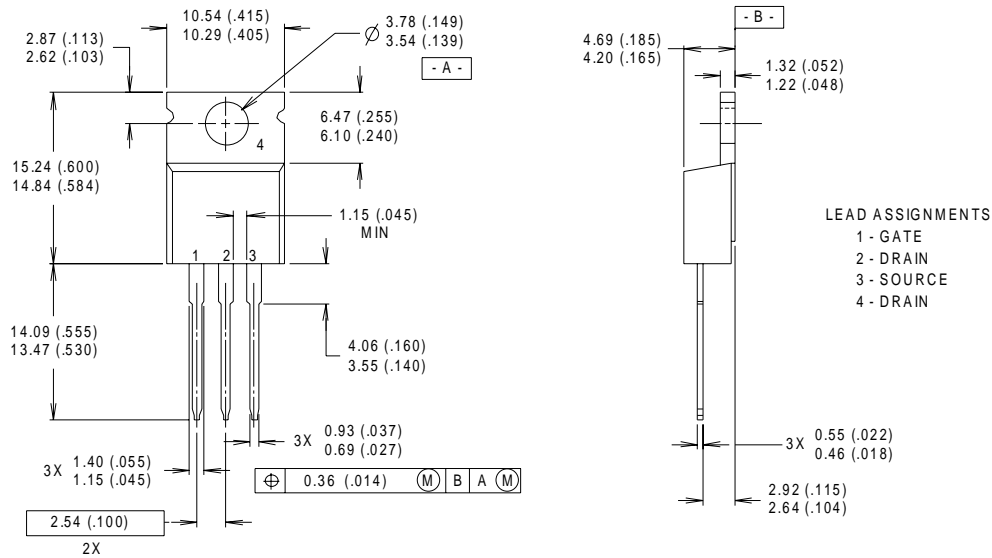
Fig 14. For N-Channel HEXFET® Power MOSFETs

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TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



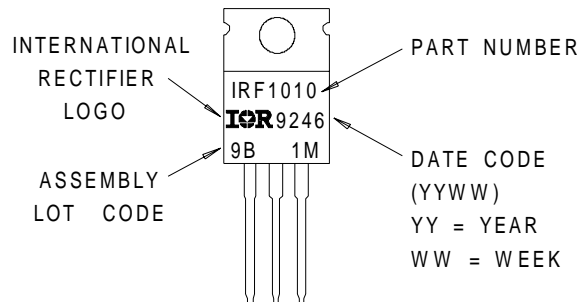
NOTES:

- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH

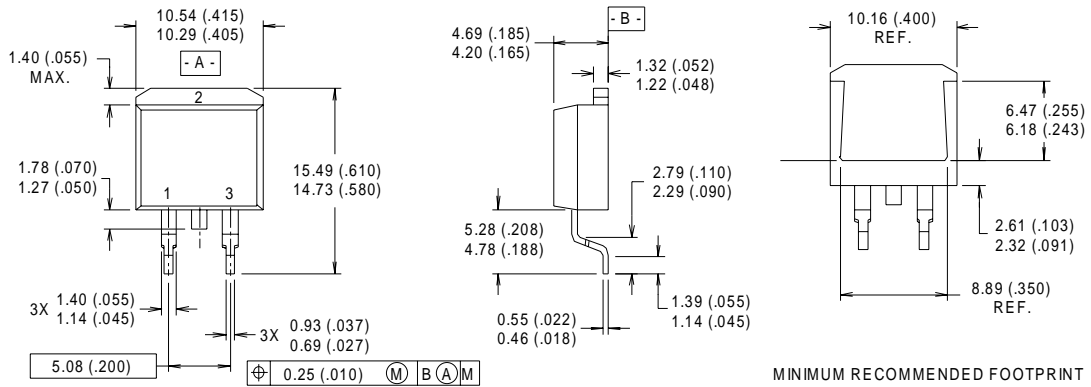
- 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
- 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

TO-220AB Part Marking Information

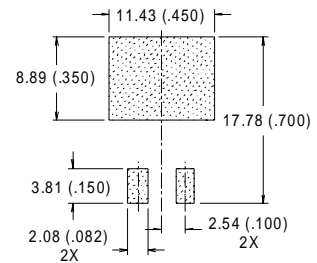
EXAMPLE : THIS IS AN IRF1010
WITH ASSEMBLY
LOT CODE 9B1M



D²Pak Package Outline



MINIMUM RECOMMENDED FOOTPRINT



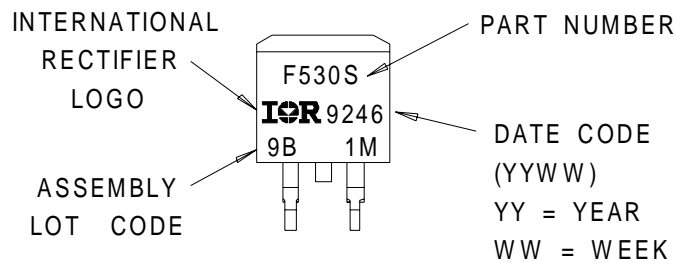
NOTES:

- 1 DIMENSIONS AFTER SOLDER DIP.
- 2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 3 CONTROLLING DIMENSION : INCH.
- 4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

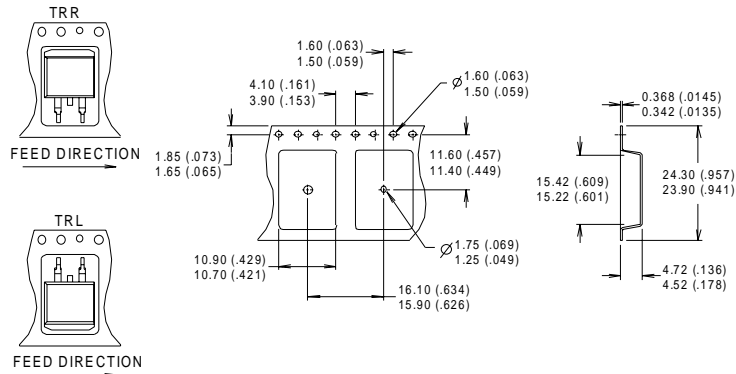
LEAD ASSIGNMENTS

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE

D²Pak Part Marking Information



D²Pak Tape & Reel Information



- NOTES :
1. CONFORMS TO EIA-418.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION MEASURED @ HUB.
 4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 5.0\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 9.8\text{A}$.
- ③ $I_{SD} \leq 9.8\text{A}$, $di/dt \leq 110\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 175^\circ\text{C}$
- ④ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑤ C_{OSS} eff. is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS}
- ⑥ This is only applied to TO-220AB package
- ⑦ This is applied to D²Pak, when mounted on 1" square PCB (FR-4 or G-10 Material).
 For recommended footprint and soldering techniques refer to application note #AN-994.