OnChip Systems

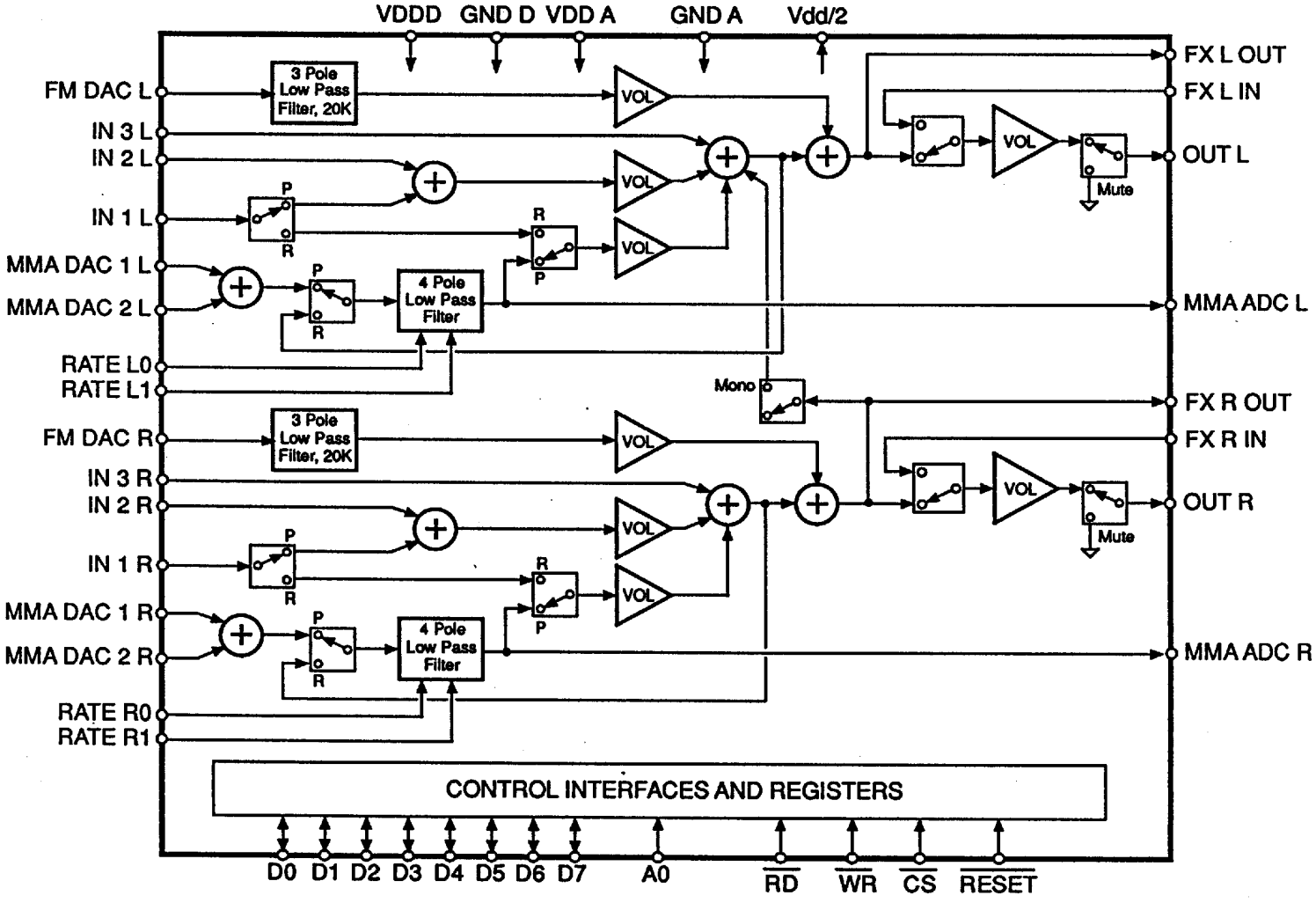
PMM 542

PRELIMINARY PRODUCT SPECIFICATION

Multimedia Audio Mixer/Filter

Features:

- One chip solution for most analog functions
- System cost reduction; replaces numerous ICs, resistors, and capacitors
- Easy design-in for multimedia sound systems
- Compatible with Yamaha Multimedia chipset
- Logarithmic gain cells; not linear - more useful resolution with fewer levels
- Continuous-time filters; not switched capacitor - no clock noise
- Wafer trimmed filters for optimum accuracy
- Few external components
- +5 volt only



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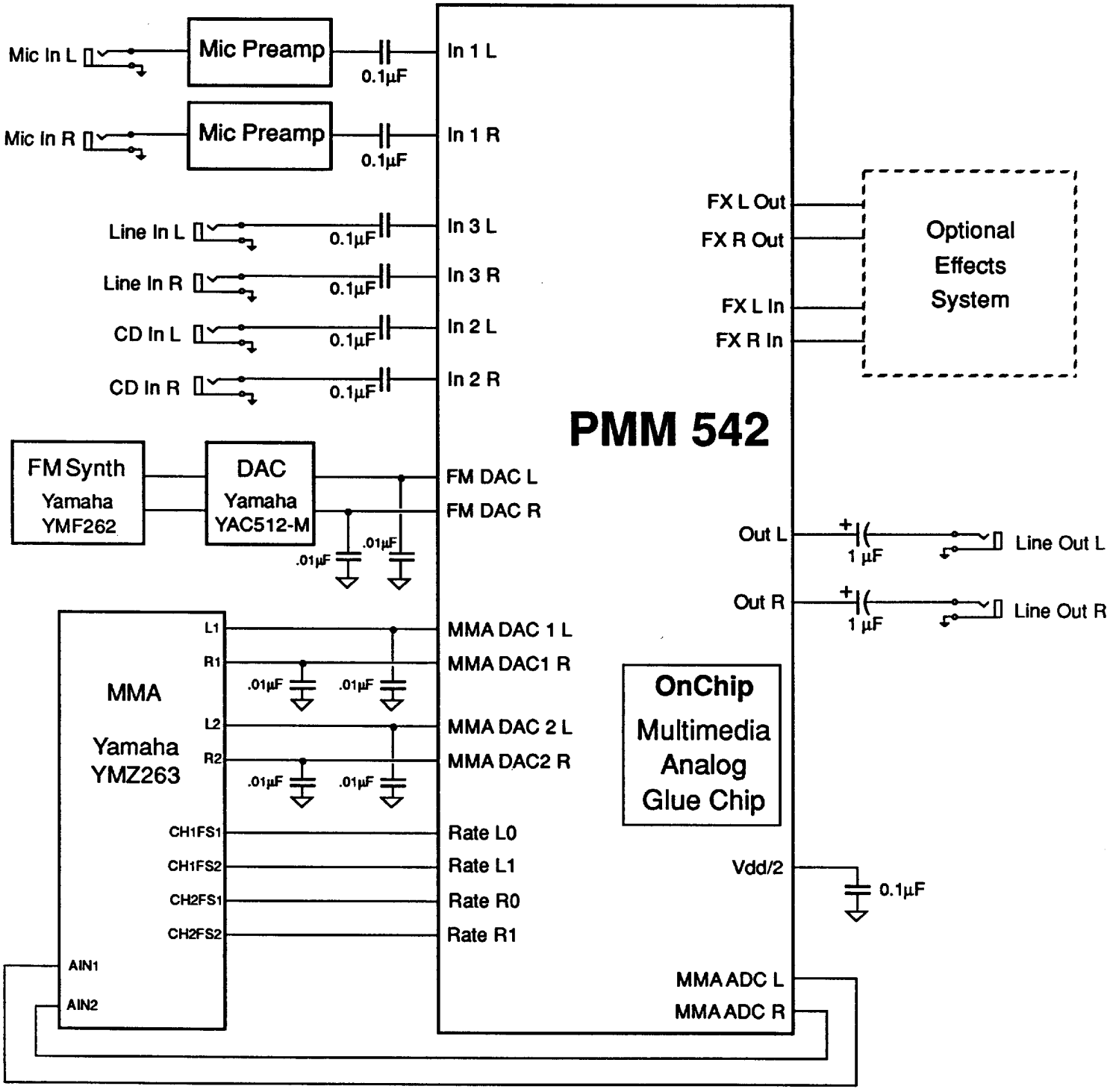
TYPICAL SYSTEM

T-74-05-01



Note: Digital control signals and power supply connections not shown.

Pinout (44 PIN PLCC)

REVISED 10/01/92

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NAME	PIN #	I/O	FUNCTION
DO	40	I/O	CPU Data Bus LSB
D1	41	I/O	CPU Data Bus
D2	42	I/O	CPU Data Bus
D3	43	I/O	CPU Data Bus
D4	3	I/O	CPU Data Bus
D5	4	I/O	CPU Data Bus
D6	5	I/O	CPU Data Bus
D7	6	I/O	CPU Data Bus MSB
A0	8	I	CPU Address
RD	2	I	CPU Read enable
WR	1	I	CPU Write enable
CS	44	I	CPU chip select
RESET	38	I	Chip reset
RATE L0	20	I	Lowpass filter rate select, left, bit 0
RATE L1	21	I	Lowpass filter rate select, left, bit 1
RATE R0	26	I	Lowpass filter rate select, right, bit 0
RATE R1	25	I	Lowpass filter rate select, right, bit 1
FMDAC L	13	I	FM DAC input, left
FMDAC R	33	I	FM DAC input, right
MMA DAC 1L	18	I	MMA DAC input 1, left
MMA DAC 1R	28	I	MMA DAC input 1, right
MMA DAC 2L	19	I	MMA DAC input 2 left
MMA DAC 2R	27	I	MMA DAC input 2 right
IN 1 L	14	I	Input 1, left
IN 1 R	32	I	Input 1, right
IN 2 L	15	I	Input 2, left
IN 2 R	31	I	Input 2, right
IN 3 L	16	I	Input 3, left
IN 3 R	30	I	Input 3, right
FX IN L	11	I	Effects Input, left
FX IN R	35	I	Effects Input, right
OUT L	10	O	Main output, left
OUT R	36	O	Main output, right
FX OUT L	12	O	Effects output, left
FX OUT R	34	O	Effects output, right
MMA ADC L	22	O	MMA ADC output, left
MMA ADC R	24	O	MMA ADC output, right
VDD D	7	-	+5 power supply, digital
VDD A	17	-	+5 power supply, analog
GND D	39	-	Ground, digital
GND A	29	-	Ground, analog
VR	9	O	Internal reference

PRELIMINARY ELECTRICAL SPECIFICATIONS

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Parameter	Min	Typ	Max	Units
Input Levels (note 1)				
In 1	---	---	1.0	Vrms
In 2,3	---	---	0.5	Vrms
MMA DAC 1,2	---	---	4.8	V p-p
FM DAC	---	---	2.5	V p-p
Effects	---	---	4.8	V p-p
Input Gainls (note 3)				
In 1	---	---	0	dB
In 2,3	---	---	+6	dB
MMA DAC 1,2	---	---	0	dB
FM DAC	---	---	0	dB
Effects	---	---	-4.5	dB
Input Impedance				
In 1	40K	50K	65K	ohms
In 2, 3	20K	25K	32K	ohms
MMA DAC 1,2	200K	250K	325K	ohms
FM DAC	80K	100K	125K	ohms
Effects	40K	50K	65K	ohms
Output Levels (note 1)				
Line	---	---	1.0	Vrms
MMA ADC	---	---	4.8	V p-p
Effects	---	---	1.0	Vrms
Output Impedance				
All outputs	---	---	100	ohms
Output Drive Load				
All outputs	10K	---	---	ohms
Digitally Controlled Attenuators				
Gain Error (note 2)	---	±0.15	±0.4	dB
Step Size	1.2	1.5	1.8	dB
MMA Filters (4th order)				
Cutoff Frequencies	4.3	5.0	5.7	Khz
	8.5	10.0	11.5	Khz
	17.0	20.0	23.0	Khz
Passband Ripple	---	1.0	2.0	dB
2xF Attenuation	30	35	---	dB
FM Filters (3rd order)				
Cutoff Frequency	17.0	20.0	23.0	Khz
Passband Ripple	---	1.0	2.0	dB
2xF Attenuation	18	23	---	dB
Output Noise (note 3)				
Line	---	100	300	µV rms
MMA ADC	---	100	300	µV rms
System THD (note 4)	---	0.5	2	%
Internal Reference	Vdd/2.1	Vdd/2	Vdd/1.9	V
Supply Current	---	10	15	mA

Note 1: All inputs referenced to Vdd/2 for direct connection to ICs with analog I/O referenced to Vdd/2.
Note 2: Deviation of each step from ideal from 0 to -48 dB.
Note 3: All gains at maximum (volume registers programmed to FF).
Note 4: Any input to any output.

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AC Characteristics

Item	Symbol	Minimum	Maximum	Units
Address setup time	t_{AS}	10	-	nsec
Address hold time	t_{AH}	10	-	nsec
Chip select write pulse width	t_{CSW}	50	-	nsec
Chip select read pulse width	t_{CSR}	250	-	nsec
Write pulse width	t_{WW}	50	-	nsec
Write data setup time	t_{WDS}	20	-	nsec
Write data hold time	t_{WD}	20	-	nsec
Read pulse width	t_{RW}	250	-	nsec
Read data access time	t_{ACC}	-	250	nsec
Read data hold time	t_{RDH}	0	-	nsec
Reset pulse width	t_{RSTW}	50	-	nsec

DC Characteristics

Item	Symbol	Minimum	Maximum	Units
High logic level (note 5)	V_{IHA}	2.2	-	volts
Low logic level (note 5)	V_{ILA}	-	0.8	volts
High logic level (note 6)	V_{IHB}	3.5	-	volts
Low logic level (note 6)	V_{ILB}	-	1.0	volts
Output voltage high @ 80 µA	V_{OH}	V_{DD}-1.0	-	volts
Output voltage low @ - 2mA	V_{OL}	-	0.4	volts
Output current	I_{OZ}	-	±10	µA

Note 5: $\overline{WR}$, $\overline{RD}$, $\overline{CS}$, A0, D0-D7
Note 6: Rate selects, $\overline{RESET}$

Timing Diagrams

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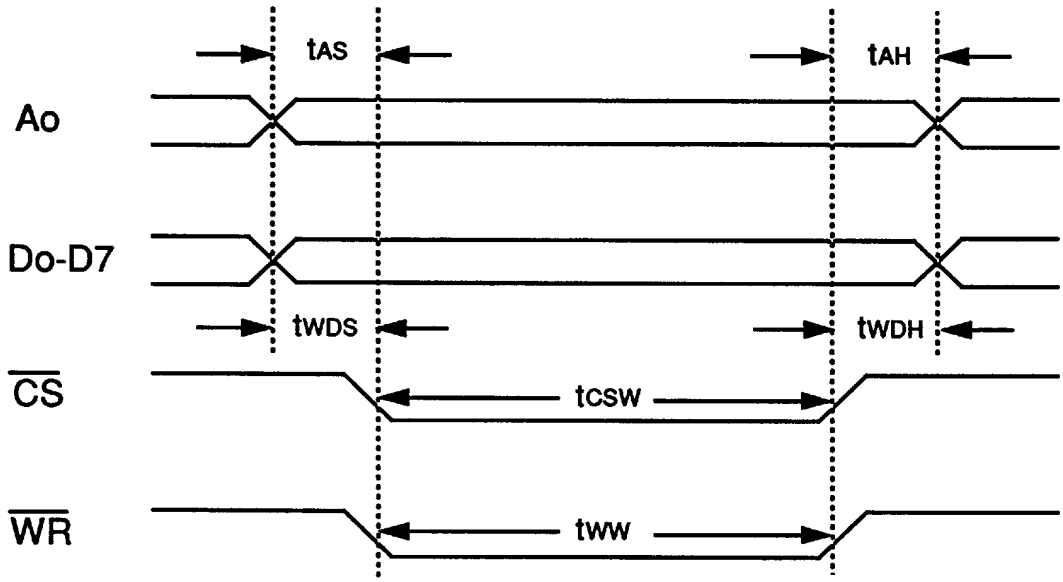
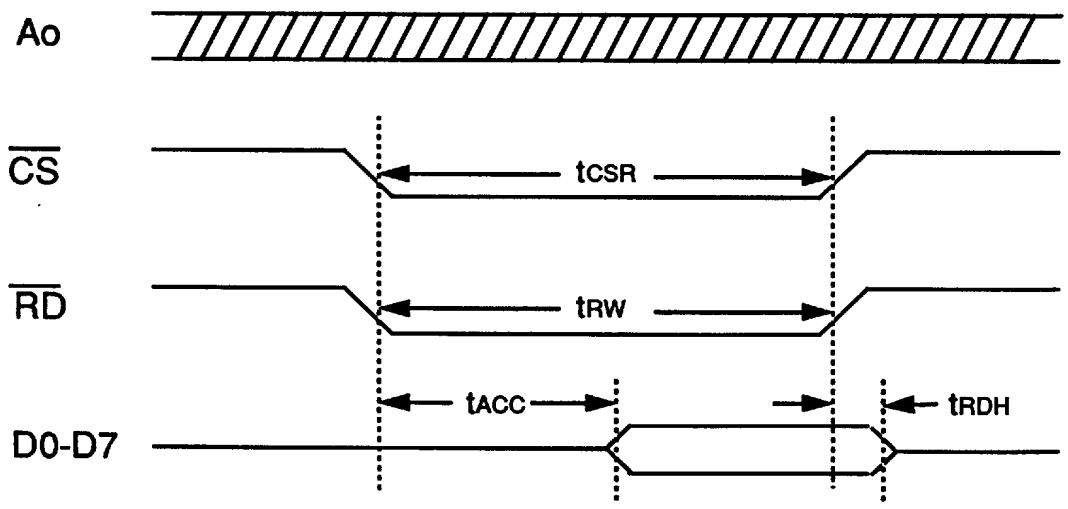
Write



Read (Must be preceded by a write with A0 = 0)



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Rate select pins:

RATE 1	RATE 2	Sample Rate	Cutoff
L	L	44.1 Khz	20 Khz
L	H	22.05 Khz	10 Khz
H	L	11.025 Khz	5 Khz
H	H	7.35 Khz	5 Khz

Register Reference

All registers are read/write registers for controlling functions on the chip, and allow the current status or value of the register to read back. All read or write operations are done in two operations; the first writes the desired register address to the chip by holding the A0 pin low during the write. The second operation, with A0 high, performs the read or write to the register specified in the proceeding operation.

04 / 05 Left (4) / Right (5) Output Volume

Read / Write

X	X	Vol 5	Vol 4	Vol 3	Vol 2	Vol 1	X

These are the final mixed output volume level controls for the left and right channels. The volume level steps logarithmically in 32 equal 1.5 db steps, with 00 value equal to volume off.

08 Output Mode

Read / Write

X	X	Mute	X	X	Left Output Select	Right Output Select	X

Bits 1 and 2 are used to select the individual left and right channel's output signals. When set = 0, the normal mixer output is sent to the gain cell; when set = 1, the external effects input is routed to the gain cell.

Bit 5 is used to mute both channel's outputs when set = 1. The mute bit is set on chip reset to prevent power-on audio spikes on the main line outputs. This bit should be cleared only after the entire audio system had been initialized. Note that reset does not clear any registers.

09 / 0A Left (9) / Right (A) Channel FM Volume

Read / Write

1	Vol 6	Vol 5	Vol 4	Vol 3	Vol 2	X	X

These registers set the volume level for the FM inputs; the volume level steps logarithmically in 32 equal 1.5 db steps, with 00 value equal to volume off.

0B / 0C Left (B) / Right (C) Channel In 1 Volume (Record) Read / Write
Left (B) / Right (C) Channel MMA DAC Volume (Playback) Read / Write

1	Vol 6	Vol 5	Vol 4	Vol 3	Vol 2	X	X

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These registers set the volume level for the MMA DAC inputs; the volume level steps logarithmically in 32 equal 1.5 db steps, with 00 value equal to volume off.

0D / 0E Left (D) / Right (E) Channel In 2 Volume (Record) Read / Write
Left (D) / Right (E) Channel In1+In2 Volume (Playback) Read / Write

1	Vol 6	Vol 5	Vol 4	Vol 3	Vol 2	X	X

These registers set the volume level for the AUX inputs; the volume level steps logarithmically in 32 equal 1.5 db steps, with 00 value equal to volume off.

11 Audio Selection Read / Write

X	X	X	X	X	Mono Input	Left Record Mode	Right Record MOde

Bits 0 and 1 are used to select Record Mode; set = 0 for playback, set = 1 for recording. As can be seen in the schematic, during record mode, the selectable anti-aliasing filter is used for the MMA ADC output. Also during record, In 1 and In 2 have separate gain controls since the MMA DAC input is not used. During playback mode, the filter is used on the MMA DAC input. Also, In 1 and In 2 are added and routed to a single gain control, and the MMA uses the last gain cell.

Bit 2, when set = 1, mixes the summed left and right channels, and routes the sum to the left channel input, for monophonic recording; when set = 0, normal stereo recording is performed.