

General Description

The AAT7361 is a low threshold dual P-channel MOSFET designed for the battery, cell phone, and PDA markets. Using AnalogicTech's ultra-high-density MOSFET process and space-saving, small-outline, J-lead package, performance superior to that normally found in a larger footprint has been squeezed into the footprint of a TSOPJW8 package.

Applications

- Battery Packs
- Battery-Powered Portable Equipment
- Cellular and Cordless Telephones

Absolute Maximum Ratings

 $T_A = 25^{\circ}C$, unless otherwise noted.

Symbol	Description		Value	Units
V _{DS}	Drain-Source Voltage www.DataSheet4U.com Gate-Source Voltage		-20	V
V _{GS}			±12	V
	Continuous Drain Current @ T _J = 150°C ¹	$T_A = 25^{\circ}C$	±3.0	
I _D		$T_A = 70^{\circ}C$	±2.4	А
I _{DM}	Pulsed Drain Current ²	±9	A	
ا _s	Continuous Source Current (Source-Drain Diode) ¹	-1.0		
TJ	Operating Junction Temperature Range	-55 to 150	°C	
T _{STG}	Storage Temperature Range	-55 to 150	°C	

Thermal Characteristics¹

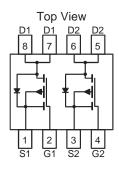
Symbol	Description		Тур	Мах	Units	
R _{θJA}	Junction-to-Ambient Steady State, One FET On		124	155	°C/W	
R _{0JA2}	Junction-to-Ambient t<5 Seconds		74	90	°C/W	
R _{0JF}	Junction-to-Foot		66	80	°C/W	
р	P _D Maximum Power Dissipation	T _A = 25°C	1.4		W	
ΓD		$T_A = 70^{\circ}C$	0.9		vv	

1. Based on thermal dissipation from junction to ambient while mounted on a 1" x 1" PCB with optimized layout. A 5-second pulse on a 1" x 1" PCB approximates testing a device mounted on a large multi-layer PCB as in most applications. $R_{\theta JF} + R_{\theta FA} = R_{\theta JA}$ where the foot thermal reference is defined as the normal solder mounting surface of the device's leads. $R_{\theta JF}$ is guaranteed by design; however, $R_{\theta CA}$ is determined by the PCB design. Actual maximum continuous current is limited by the application's design.

2. Pulse test: Pulse Width = 300μ s.

- Drain-Source Voltage (max): -20V
- Continuous Drain Current¹ (max) -3.0A @ 25°C
- Low On-Resistance:
 - 100mΩ @ V_{GS} = -4.5V
 - 175m $\Omega @ V_{GS} = -2.5V$

Dual TSOPJW-8 Package





AAT7361 20V P-Channel Power MOSFET

Electrical Characteristics

 $T_{\rm J} = 25^{\circ}$ C, unless otherwise noted.

Symbol	Description	Conditions	Min	Тур	Max	Units		
DC Charao	DC Characteristics							
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_{D} = -250\mu A$	-20			V		
R _{DS(ON)}	Drain-Source On-Resistance ¹	$V_{GS} = -4.5V, I_{D} = -3.0A$		80	100	- mΩ		
		$V_{GS} = -2.5V, I_{D} = -2.3A$		140	175			
I _{D(ON)}	On-State Drain Current ¹	V_{GS} = -4.5V, V_{DS} = -5V (pulsed)	-9			А		
V _{GS(th)}	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = -250 \mu A$	-0.6			V		
I _{GSS}	Gate-Body Leakage Current	$V_{GS} = \pm 12V, V_{DS} = 0V$			±100	nA		
1	Drain Source Leakage Current	$V_{GS} = 0V, V_{DS} = -20V$			-1	μA		
I _{DSS}		$V_{GS} = 0V, V_{DS} = -16V, T_{J} = 70^{\circ}C^{2}$			-5			
9 _{fs}	Forward Transconductance ¹	$V_{DS} = -5V, I_{D} = -3.0A$		5		S		
Dynamic (Characteristics ²							
Q _G	Total Gate Charge	$V_{DS} = -10V, R_{D} = 3.3\Omega, V_{GS} = -4.5V$		6				
Q _{GS}	Gate-Source Charge	$V_{DS} = -10V, R_{D} = 3.3\Omega, V_{GS} = -4.5V$		1.3		nC		
Q_{GD}	Gate-Drain Charge	$V_{DS} = -10V, R_{D} = 3.3\Omega, V_{GS} = -4.5V$		1.7				
t _{D(ON)}	Turn-On Delay	V_{DS} = -10V, R_D = 3.3 Ω , V_{GS} = -4.5V, R_G = 6 Ω		7				
t _R	Turn-On Rise Time	V_{DS} = -10V, R_D = 3.3 Ω , V_{GS} = -4.5V, R_G = 6 Ω		13		ns		
t _{D(OFF)}	Turn-Off Delay	$V_{DS} = -10V, R_{D} = 3.3\Omega, V_{GS} = -4.5V, R_{G} = 6\Omega$		15				
t _F	Turn-Off Fall Time	V_{DS} = -10V, R_D = 3.3 Ω , V_{GS} = -4.5V, R_G = 6 Ω		20				
Source-Dr	Source-Drain Diode Characteristics							
V_{SD}	Source-Drain Forward Voltage ¹	$V_{GS} = 0, I_{S} = -3.0A$			-1.3	V		
۱ _s	Continuous Diode Current ³				-1.0	А		

1. Pulse test: Pulse Width = 300µs.

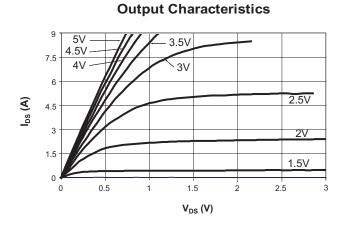
2. Guaranteed by design. Not subject to production testing.

^{3.} Based on thermal dissipation from junction to ambient while mounted on a 1" x 1" PCB with optimized layout. A 5-second pulse on a 1" x 1" PCB approximates testing a device mounted on a large multi-layer PCB as in most applications. $R_{\theta JF} + R_{\theta FA} = R_{\theta JA}$ where the foot thermal reference is defined as the normal solder mounting surface of the device's leads. $R_{\theta JF}$ is guaranteed by design; however, $R_{\theta CA}$ is determined by the PCB design. Actual maximum continuous current is limited by the application's design.

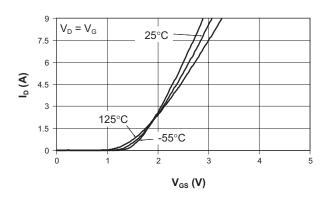


Typical Characteristics

 $T_J = 25^{\circ}C$, unless otherwise noted.



Transfer Characteristics



On-Resistance vs. Drain Current



0.4

0.32

0.24

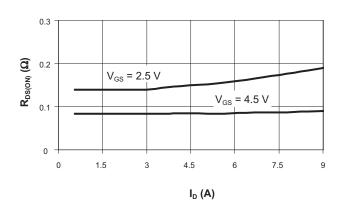
0.16

0.08

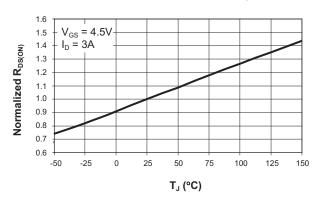
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 $R_{DS(ON)}$ (Ω)

I_D = 3A



On-Resistance vs. Junction Temperature



V_{GS} (V)

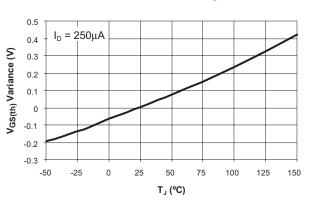
3

4

5

2

1



Threshold Voltage



AAT7361 20V P-Channel Power MOSFET

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700

600

500

400

300

200

100

0 -

0

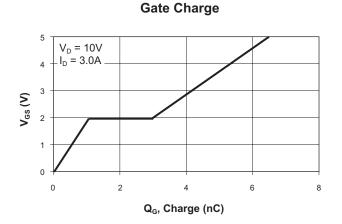
Ciss

C

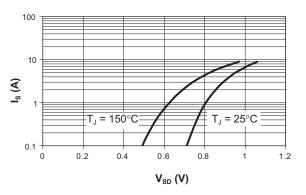
 C_{rss}

5

Capacitance (pF)



Source-Drain Diode Forward Voltage



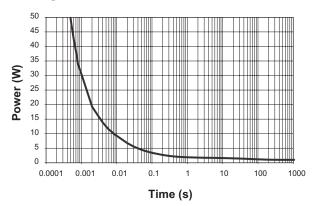
Capacitance

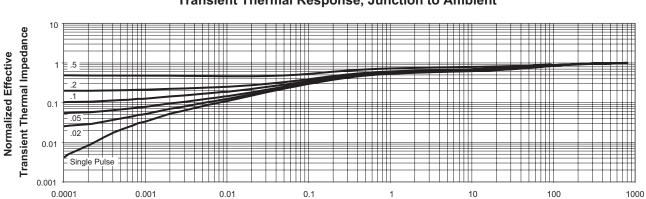
10

V_{DS} (V)

15

Single Pulse Power, Junction To Ambient







20

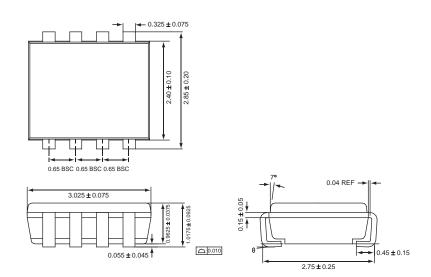


Ordering Information

Package	Marking ¹	Part Number (Tape and Reel) ²
TSOPJW-8	JYXYY	AAT7361ITS-T1

Package Information

TSOPJW-8



All dimensions in millimeters.

^{1.} XYY = assembly and date code.

^{2.} Sample stock is generally held on part numbers listed in BOLD.



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