IMISG502 SYSTEM CLOCK CHIP

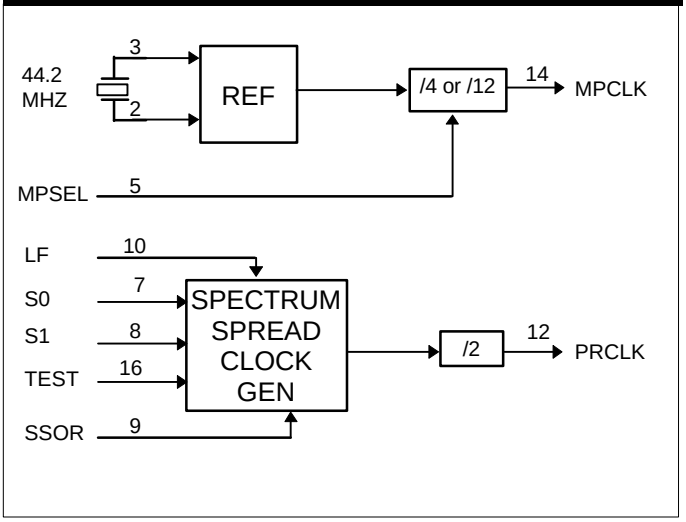
April 1996

CMOS LSI
SPECTRUM SPREAD CLOCK

PRODUCT FEATURES

- Generates CPU Clock Signals for Microprocessor Systems
- Reduces Measured EMI by 10 db nominal
- 4V to 7V Operating Supply Range
- Supports 80286-, 80386-, 80486-, Pentium™- and 29000-Based Designs
- Wide Range of Selectable Output Frequencies including 40, 33.3, 16.7
- Single, Low Cost Crystal Used as Reference Frequency
- Glitch-Free Switching
- 50% Duty Cycle
- Power Down Mode for Low Power Consumption
- TTL or CMOS Compatible Outputs with 6 mA Drive Capability
- Low, Short and Long Term Jitter (cycle-to-cycle jitter less than 50 ps)
- 16 PIN PDIP and 16 PIN SOIC (300 mil body) package options

BLOCK DIAGRAM

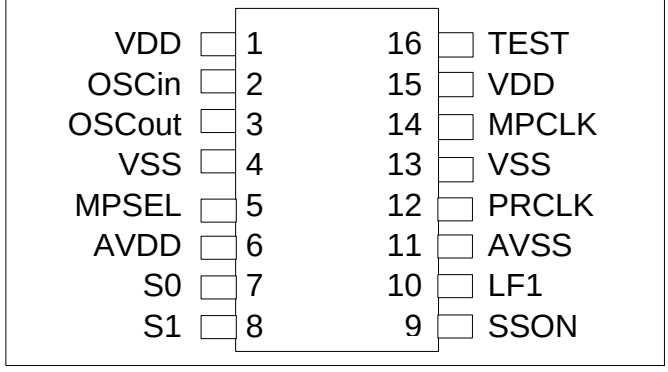


PRODUCT DESCRIPTION

The IMISG502 is a spectrum spread clock generator specially designed for personal computers, laser printers and other digital systems. IMISG502 uses a patented concept to generate popular clock frequencies that are intentionally broadbanded to reduce electromagnetic interference. The IMISG502 attenuates the radiated emission amplitudes from products associated with either the clock harmonics or any signals derived from the clock signals nominally 10 dB and could significantly reduce the cost of complying with the regulatory requirements.

PRCLK is the broadbanded output and can be programmed to generate 40, 33.3, 16.7 and 12 MHz with S0 and S1 pins. A single, low cost external crystal is required as reference frequency for the synthesizer. Output modulation function can be turned off with the SSON pin. Several power down modes add the flexibility to operate the device in a completely static mode to reduce standby currents and simplify system board tests.

P-DIP/SOIC DIAGRAM



APPLICATIONS

The IMISG502 eliminates the need for multiple oscillators and generates the CPU clock signals for personal computers, laser printers and other digital systems. Supports 8086-, 80286-, 80386-, 80486-, Pentium™- and 29000-based designs. IMISG502 can be used with laptop or notebook computers to save power by running the system slower than normal CPU speeds or completely disabling the clocks in standby mode.

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PIN DESCRIPTION

OSCin OSCout- These pins form an on-chip reference oscillator when connected to terminals of an external 44.2 Mhz third overtone parallel resonant crystal. OSCin may also serve as an input for an externally generated CMOS level or AC coupled reference signal.

S0 and S1- Standard frequency select inputs. These inputs control the PRCLK frequency selection. S0-S1 inputs control the CPU clock frequencies. All these inputs have internal pull-downs.

Table 1 shows the output frequency selection conditions.

TEST- Controls power down and Test Mode selection. When high, S0-S1 and MPSEL controls the mode selection as shown on Table 1 and Table 2. When low, the device operates in normal mode. This pin has an internal pull-down.

MPSEL - Controls MPCLK output frequency selections. Table 2 shows the selected frequencies for MPCLK. This input has an internal pull-up.

SSON - This is the control output for the clock generator. It is a single-ended, tri-state output. Component connections are shown in Figure 1.

LF1- Loop filter, phase detector outputs for the clock generators. It is a single-ended tristate output for use as a loop error signal. See figure 1 for circuit.

PRCLK FREQUENCY SELECTION			
INPUTS			OUTPUT
TEST	S1	S0	PRCLK
0	0	0	N/A
0	0	1	16.7 Mhz
0	1	0	33.3 Mhz
0	1	1	40.0 Mhz
1	0	0	0; Power Down
1	0	1	1; Power Down
1	1	0	TEST
1	1	1	Hi-Z

TABLE 1: When Power Down address is selected, the VCO is turned off and the device goes into standby.

MPCLK - This is a non modulated output. This output can be programmed to be 3.7 Mhz or 11.06 Mhz. The selection of these frequencies is controlled by the MPSEL pin shown in Table 1**.**

PRCLK - Output from the spectrum spread clock generator. Frequency selection is shown on Table 1. When the SSON pin is high, outputs are not modulated. When SSON is low, sprectrum spread function is enabled.

VSS- Circuit ground.

VDD- Positive power supply.

AVDD- Analog positive power supply.

AVSS- Analog circuit ground.

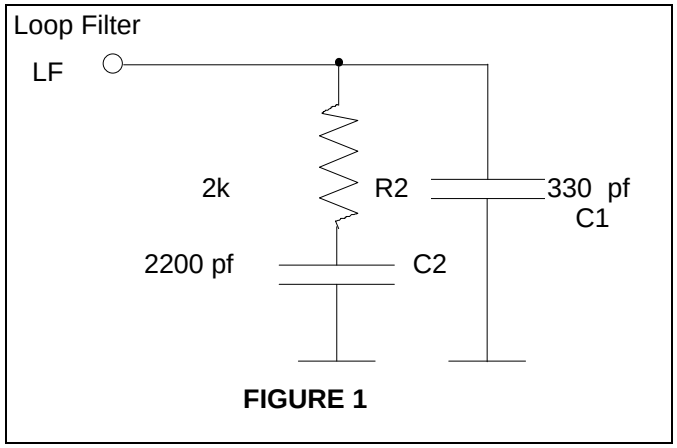

FIGURE 1

MPCLK FREQUENCY SELECTION				
INPUTS				OUTPUT
TEST	MPSEL	S1	S0	MPCLK
0	0	X	X	3.7 Mhz
0	1	X	X	11.06 Mhz
1	X	0	0	0; Power Down
1	X	0	1	1; Power Down
1	X	1	0	TEST
1	X	1	1	Hi-Z

TABLE 2: When Power Down address is slected, the VCO is turned off and the device goes to standy mode. Phase detector is in tri-state mode.

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MAXIMUM RATINGS

Voltage Relative to VSS	-0.3
Voltage Relative to VDD	0.3V
Storage Temperature:	-65° to +150°C
Ambient Temperature:	-0°C to + 70°C
Maximum supply voltage:	7.0V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)< VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units
Input Low Voltage	VIL	-	-	0.8	Vdc
Input High Voltage	VIH	2.0	-	-	Vdc
Input Low Current with Pull-up/ Pull-down	I_{IH}/I_{IL}	-	-	10/100	µA
Output Low Voltage IOL = 6mA	VOL	-	-	0.4	Vdc
Output High Voltage IOH=6mA	VOH	2.5	-	-	Vdc
Tri-State Leakage Current	IOZ	-	-	10	µA
Static Supply Current	IDD	-	-	250	µA
Dynamic Supply Current	ICC	-	25	30	mA
Short Circuit Current	ISC	25	-	-	mA

VDD = 5V ± 10%, TA = 0°C to +70°C

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SWITCHING CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units
Output Rise and Fall Time Measured at 10% - 90% of V_{DD}	**t**TLH, **t**THL	-	-	5	ns
Output Rise and Fall Time Measured at 0.8V - 2.0V	**t**TLH, **t**THL	-	-	3	ns
Output Duty Cycles	**TsymF1**	-	-	45/55	%
Jitter One Sigma	Tj1s	-	-	2	% of Fout

VDD = 5V ± 10%, TA = 0°C to 70°C, CL = 15 pF

OSCILLATOR CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Transconductance	g_m	20	80	180	millimhos	@ 44.2 MHz
Output Impedance	Z_o	-	200	800	ohms	@ 44.2 MHz
Input Capacitance	C_i	8	13	18	pf	
Output Capacitance	Co	3	6	9	pf	
DC Bias Voltage	V_B	1.5	VDD/2	3.5	Volt	
Start-up Time	t_s	-	-	2	ms	@ VDD = 4.5V
Duty Cycle	TsymF1	-	-	45/55	%	
Input Rise Time OSCIN	ICLKr	-	-	20	ns	

VCO CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
VCO Gain	Ko	35	55	65	MHz/volt	ΔF/ΔV Measured with VCO Control at 2V - 3V
Phase Detector Gain	Kd	100	145	200	μA	

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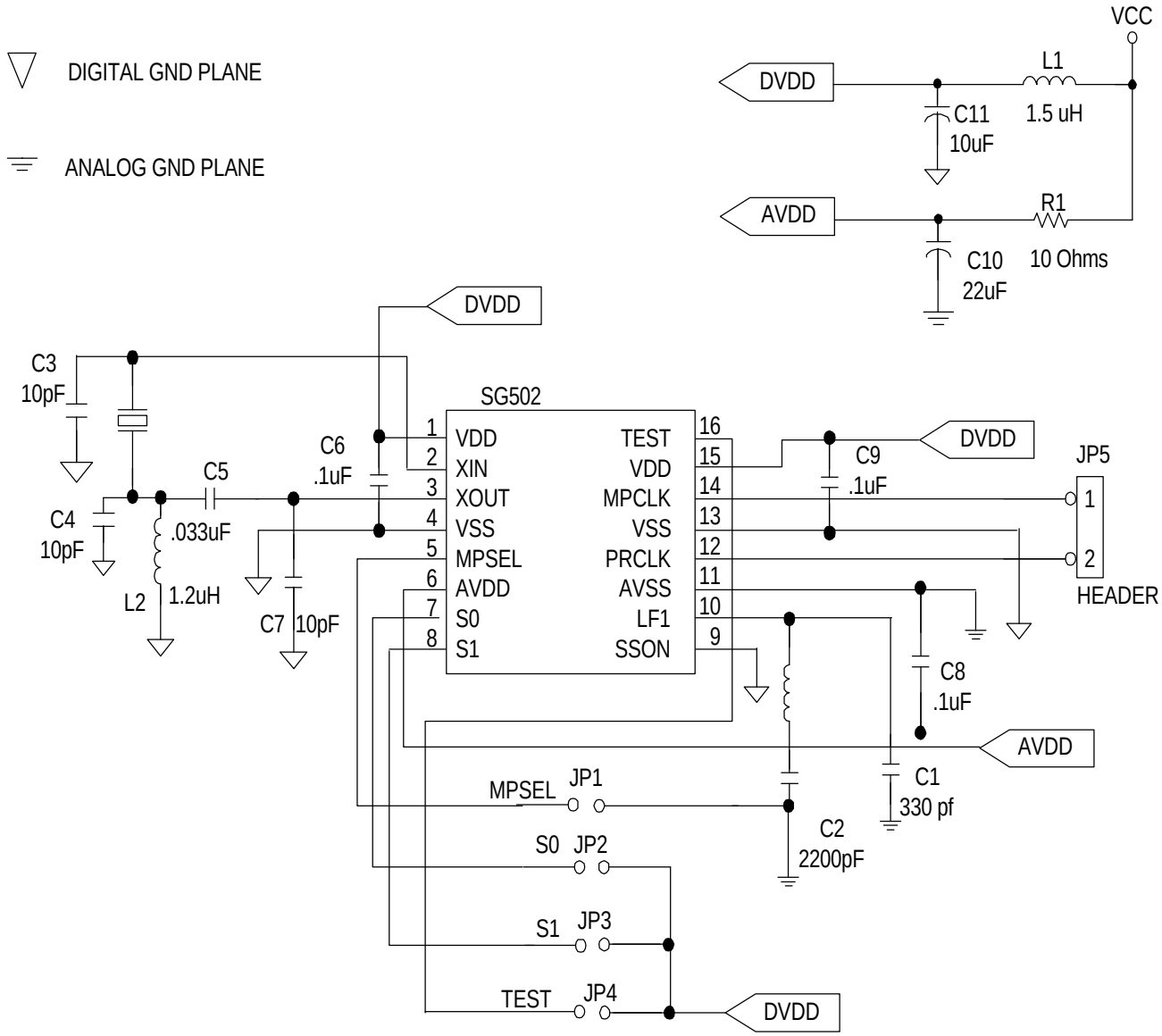
EXTERNAL CONNECTIONS



NOTE1: KEEP C3, C4, C5, C6 CLOSE TO THEIR PINS (4,11,13,10,9 RESPECTIVELY)

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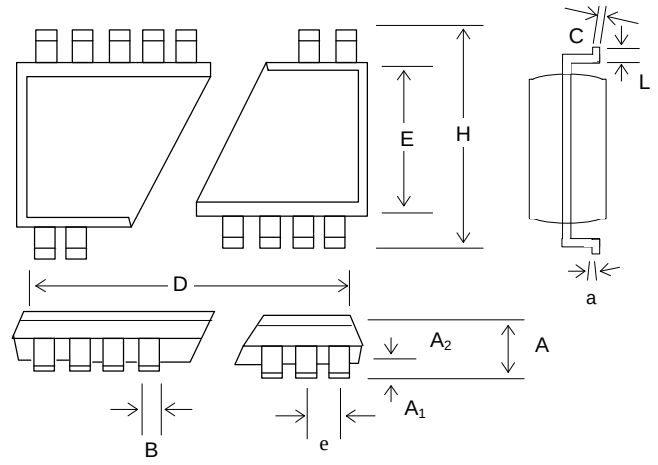
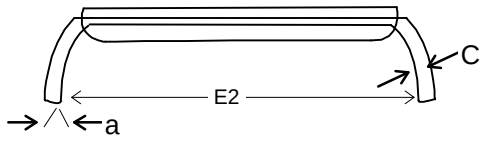
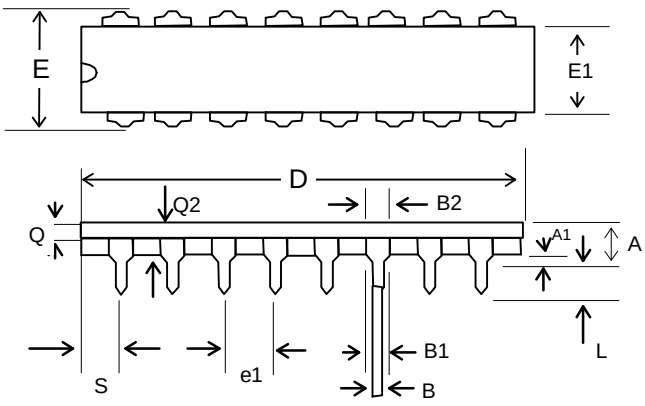
PACKAGE DRAWING AND DIMENSIONS







16 PIN SOIC OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.097	0.101	0.104	2.46	2.56	2.64
A_1	0.0020	0.009	0.0015	0.060	0.22	0.38
A2	0.090	0.092	0.111	2.29	2.34	2.39
B	0.014	0.016	0.019	0.35	0.41	0.48
C	0.0091	0.010	0.0125	0.23	0.25	0.32
D	.399	.407	.412	10.13	10.34	10.46
E	0.285	0.296	0.299	7.24	7.52	7.59
e	0.050 BSC			1.27 BSC		
H	0.400	0.406	0.40	10.16	10.31	10.41
a	0	5	10	0	5	10
L	0.24	0.032	0.040	0.61	0.81	1.02

16-PIN PLASTIC DIP DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.150	0.160	0.170	3.81	4.06	4.318
A_1	0.015	-	-	0.381	-	-
B	0.016	0.018	0.020	0.40	0.45	0.50
B_1	0.056	0.059	0.062	1.47	1.52	1.57
B_2	0.046	0.049	0.052	1.17	1.24	1.32
C	0.008	0.010	0.012	0.20	0.25	0.30
D	0.748	0.750	0.752	19.00	19.05	19.10
E	0.300	0.312	0.325	7.62	7.924	8.255
E_1	0.240	0.252	0.260	6.096	6.49	6.604
E_2	0.335	0.345	0.355	8.51	8.76	9.01
e_1	0.100 BSC			2.54 BSC		
L	0.25	0.230	0.135	3.175	3.30	3.429
a	0°	7°	15°	0°	7°	15°
Q_1	0.059	0.060	0.061	1.50	1.53	1.55
Q_2	0.128	0.130	0.132	3.25	3.30	3.35
S	0.073	0.075	0.077	1.85	1.90	1.95

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ORDERING INFORMATION

Part Number	Package Type	Production Flow
IMISG502xPB	28 Pin Plastic Dip	Commercial, 0°C to + 70°C
IMISG502xXB	28 Pin SOIC	Commercial, 0°C to + 70°C

Note: The "x" following the IMI Device Number denotes the device revision. The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: IMISG502
xPB
Date Code, Lot #

IMISG502xPB

Flow
B = Commercial, 0°C to + 70°C

Package
P = Plastic Dip
X = Small Outline

Revision

IMI Device Number

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