National Semiconductor

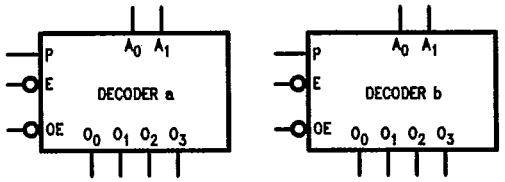
54F/74F539
Dual 1-of-4 Decoder with TRI-STATE® Outputs

General Description

The 'F539 contains two independent decoders. Each accepts two Address (A_0, A_1) input signals and decodes them to select one of four mutually exclusive outputs. A polarity control input (P) determines whether the outputs are active HIGH (P = L) or active LOW (P = H). An active LOW input Enable ($\overline{E}$) is available for data demultiplexing; data is routed to the selected output in non-inverted form in the active LOW mode or in inverted form in the active HIGH mode. A HIGH signal on the active LOW Output Enable ($\overline{OE}$) input forces the TRI-STATE outputs to the high impedance state.

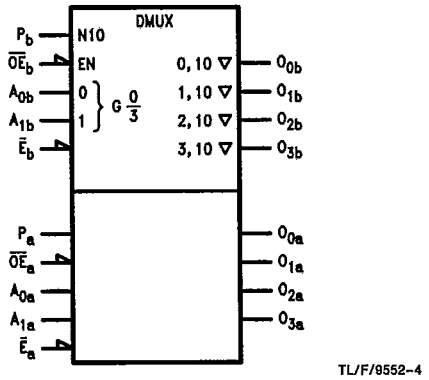
Ordering Code: See Section 5

Logic Symbols



TL/F/9552–1

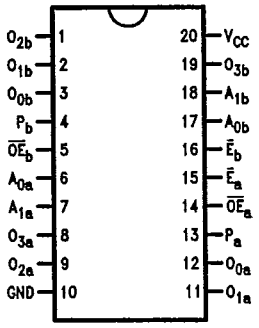
IEEE/IEC



TL/F/9552–4

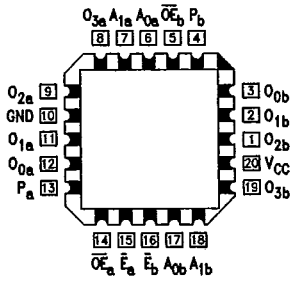
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



TL/F/9552–2

Pin Assignment for LCC and PCC



TL/F/9552–3

Unit Loading/Fan Out: See Section 2 for U.L. definitions

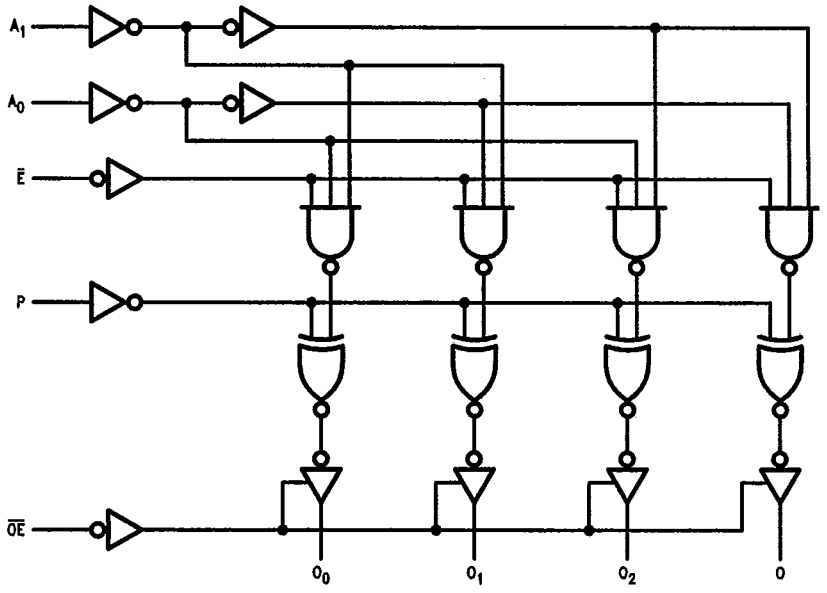
Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
A_{0a}–A_{1a}	Side A Address Inputs	1.0/1.0	20 μA/−0.6 mA
A_{0b}–A_{1b}	Side B Address Inputs	1.0/1.0	20 μA/−0.6 mA
$\overline{E}_a$, $\overline{E}_b$	Enable Inputs (Active LOW)	1.0/1.0	20 μA/−0.6 mA
$\overline{OE}_a$, $\overline{OE}_b$	Output Enable Inputs (Active LOW)	1.0/1.0	20 μA/−0.6 mA
P_a, P_b	Polarity Control Inputs	1.0/1.0	20 μA/−0.6 mA
O_{0a}–O_{3a}	Side A TRI-STATE Outputs	150/40 (33.3)	−3 mA/24 mA (20 mA)
O_{0b}–O_{3b}	Side B TRI-STATE Outputs	150/40 (33.3)	−3 mA/24 mA (20 mA)

Truth Table (each half)

Function	Inputs				Outputs			
	$\overline{OE}$	$\overline{E}$	A_1	A_0	O_0	O_1	O_2	O_3
High Impedance	H	X	X	X	Z	Z	Z	Z
Disable	L	H	X	X	$O_n = P$			
Active HIGH Output (P = L)	L	L	L	L	H	L	L	L
	L	L	L	H	L	H	L	L
	L	L	H	L	L	L	H	L
	L	L	H	H	L	L	L	H
Active LOW Output (P = H)	L	L	L	L	L	H	H	H
	L	L	L	H	H	L	H	H
	L	L	H	L	H	H	L	H
	L	L	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram (one half shown)



TL/F/9552–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

4

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	54F/74F Min	54F/74F Typ	54F/74F Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage 54F 10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA
	54F 10% V_{CC}	2.4					I_{OH} = −3 mA
	74F 10% V_{CC}	2.5					I_{OH} = −1 mA
	74F 10% V_{CC}	2.4					I_{OH} = −3 mA
	74F 5% V_{CC}	2.7					I_{OH} = −1 mA
	74F 5% V_{CC}	2.7					I_{OH} = −3 mA
V_{OL}	Output LOW Voltage 54F 10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA
	74F 10% V_{CC}			0.5			I_{OL} = 24 mA
I_{IH}	Input HIGH Current			20	μA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test			100	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current			−0.6	mA	Max	V_{IN} = 0.5V
I_{OZH}	Output Leakage Current			50	μA	Max	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current			−50	μA	Max	V_{OUT} = 0.5V
I_{OS}	Output Short-Circuit Current	−60		−150	mA	Max	V_{OUT} = 0V
I_{CEX}	Output HIGH Leakage Current			250	μA	Max	V_{OUT} = V_{CC}
I_{ZZ}	Bus Drainage Test			500	μA	0.0V	V_{OUT} = V_{CC}
I_{CCH}	Power Supply Current		28	45	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current		40	60	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current		40	60	mA	Max	V_O = HIGH Z

T-66-21-55

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			54F T_A, V_{CC} = Mil, $C_L = 50$ pF		74F T_A, V_{CC} = Com, $C_L = 50$ pF		Units	Fig No
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	4.0	14.5	18.5			3.5	19.5	ns	2-3
t_{PHL}	A_n to O_n	4.0	9.5	12.0			4.0	13.0		
t_{PLH}	Propagation Delay	5.0	12.0	16.0			5.5	17.0	ns	2-3
t_{PHL}	$\overline{E}$ to O_n	4.0	7.5	9.5			4.0	10.5		
t_{PLH}	Propagation Delay	7.5	14.5	21.5			4.5	22.5	ns	2-3
t_{PHL}	P to O_n	5.0	11.0	16.5			4.5	17.5		
t_{PZH}	Output Enable Time	4.5	8.0	10.5			4.0	11.5	ns	2-5
t_{PZL}	$\overline{OE}$ to O_n	5.5	10.0	13.0			5.0	14.0		
t_{PHZ}	Output Disable Time	2.0	4.5	6.5			2.0	7.0		
t_{PLZ}	$\overline{OE}$ to O_n	3.0	6.5	8.5			3.0	9.5		