REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R275-94.	94-09-14	K. A. Cottongim
B	Changes in accordance with NOR 5962-R365-97.	97-06-19	K. A. Cottongim
C	Add device types 03, 04, and CAGE code 88379. Correct note 1 in table I.	98-01-15	K. A. Cottongim
D	Corrections to tables I and II.	98-05-14	K. A. Cottongim

REV																			
SHEET																			
REV	D	D	D	D	D														
SHEET	15	16	17	18	19														

REV STATUS OF SHEETS	REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
91-11-25

REVISION LEVEL
D

DEFENSE SUPPLY CENTER COLUMBUS
P. O. BOX 3990
COLUMBUS, OHIO 43216-5000

MICROCIRCUIT, HYBRID, LINEAR, DUAL REDUNDANT REMOTE TERMINAL UNIT (RTU)

SIZE	CAGE CODE	5962-89798
A	67268	

SHEET 1 OF 19

DSCC FORM 2233
APR 97

5962-E309-98

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

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1. SCOPE

1.1 Scope. This drawing describes device requirements for class H hybrid microcircuits to be processed in accordance with MIL-PRF-38534.

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

5962-89798	01	X	X
Drawing number	Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device types	Generic number	Circuit function
01	BUS-65142, BUS-65144,	Dual redundant remote terminal unit (RTU)
02	BUS-65143, BUS-65145,	Dual redundant remote terminal unit (RTU)
03	CT2542, CT2542-FP	Dual redundant remote terminal unit (RTU)
04	CT2543, CT2543-FP	Dual redundant remote terminal unit (RTU)

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	78	Hybrid package
Y	See figure 1	82	Flat package

1.2.3 Lead finish. The lead finish shall be as specified in MIL-PRF-38534.

1.3 Absolute maximum ratings. 1/

Logic supply voltage (V_L)	5.5 V dc
Negative supply voltage (V_{EE})	-18.0 V dc
Storage temperature range	-65°C to +150°C
Thermal rise, case to junction (ΔT_J)	13.9°C
Lead soldering temperature (10 seconds)	+300°C
Power dissipation (T_C = +125°C)	Duty cycle dependent (see table I power supplies)

1.4 Recommended operating conditions.

Logic supply voltage (V_L)	+4.5 V dc to +5.5 V dc
Negative supply voltage (V_{EE}):	
Device types 01 and 03	-14.25 V dc to -15.75 V dc
Device types 02 and 04	-11.4 V dc to -12.6 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Maximum differential input voltage	40 Vp-p

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbook. The following specification, standards, and handbook form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1553 - Aircraft Internal Time Division Command/Response Multiplex Bus.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOK

DEPARTMENT OF DEFENSE

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbook are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item performance requirements shall be in accordance with MIL-PRF-38534. Compliance with MIL-PRF-38534 may include the performance of all tests herein or as designated in the device manufacturer's Quality Management (QM) plan or as designated for applicable device class. Therefore, the tests and inspections herein may not be performed for applicable device class (see MIL-PRF-38534). Futhermore, the manufacturers may take exceptions or use alternate methods to the tests and inspections herein and not perform them. However, the performance requirements as defined in MIL-PRF-38534 shall be met for the applicable device class. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38534 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 and figure 1 herein.

3.2.2 Terminal connections and pin functions. The terminal connections and pin functions shall be as specified on figure 2.

3.2.3 Block diagram. Block diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking of device(s). Marking of device(s) shall be in accordance with MIL-PRF-38534. The device shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's vendor similar PIN may also be marked as listed in QML-38534.

3.6 Data. In addition to the general performance requirements of MIL-PRF-38534, the manufacturer of the device described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, for each device type listed herein. Also, the data should include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DSCC-VA) upon request.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance (original copy) submitted to DSCC-VA shall affirm that the manufacturer's product meets the performance requirements of MIL-PRF-38534 and herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38534 shall be provided with each lot of microcircuits delivered to this drawing.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38534 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38534. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Receiver							
Differential input impedance	Z_{IN} diff	DC to 1 MHz 2/	1, 2, 3	All	4		kΩ
Differential input voltage	V_{IN} diff	2/	1, 2, 3	All		40	Vp-p
Input threshold	V_{TH}	Direct coupled (across 35Ω load)	4, 5, 6	All		1.2	Vp-p
		Transformer coupled (across 70Ω load)				0.86	
Common mode rejection ratio	CMRR	DC to 2 MHz 2/ 3/	1, 2, 3	All	40		dB
Common mode voltage	CMV	DC to 2 MHz 2/ 3/	1, 2, 3	All	-10	+10	V
Transmitter							
Differential output voltage	V_{OUT} diff	Direct coupled (across 35Ω load)	4, 5, 6	All	6.0	9.0	Vp-p
		Transformer coupled (across 70Ω load)			18.0	27.0	
Output rise and fall time	t_r, t_f	Transformer coupled (across 70Ω load) 10 to 90 percent of full waveform peak to peak. In accordance with MIL-STD-1553.	9, 10, 11	All	100	300	ns
Output noise	N_{OUT}	2/ 3/	4, 5, 6	All		14	mVp-p
Logic							
High level input voltage	V_{IH}	V_L = 5.5 V	1, 2, 3	All	2.4		V

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Device types	Limits		Unit
						Min	Max	
Logic - Continued.								
Low level input voltage	V_{IL}	$V_L = 5.5$ V		1, 2, 3	All		0.7	V
High level input current 4/	I_{IH}	$V_L = 5.5$ V $V_{IH} = 2.7$ V		1, 2, 3	All	-0.04	-0.2	mA
High level input current	I_{IH}	$V_L = 5.5$ V $V_{IH} = 2.7$ V	5/	1, 2, 3	All	-20	+20	µA
			6/			-0.02	-0.2	mA
Low level input current 4/	I_{IL}	$V_L = 5.5$ V $V_{IL} = 0.4$ V		1, 2, 3	All	-0.08	-0.4	mA
Low level input current	I_{IL}	$V_L = 5.5$ V $V_{IL} = 0.4$ V	5/	1, 2, 3	All	-20	+20	µA
			6/			-0.04	-0.4	mA
High level output voltage	V_{OH}	$V_L = 4.5$ V $I_{OH} = -0.4$ mA		1, 2, 3	All	2.7		V
Low level output voltage 7/	V_{OL}	$V_L = 4.5$ V $I_{OH} = 2.0$ mA		1, 2, 3	All		0.4	V
Low level output voltage 6/	V_{OL}	$V_L = 4.5$ V $I_{OL} = 4.0$ mA		1, 2, 3	All		0.4	V
Functional test 8/				7, 8	All			pass/ fail
Input capacitance	C_I	f = 1 MHz, see 4. 3. 1b		4	All		50	pF

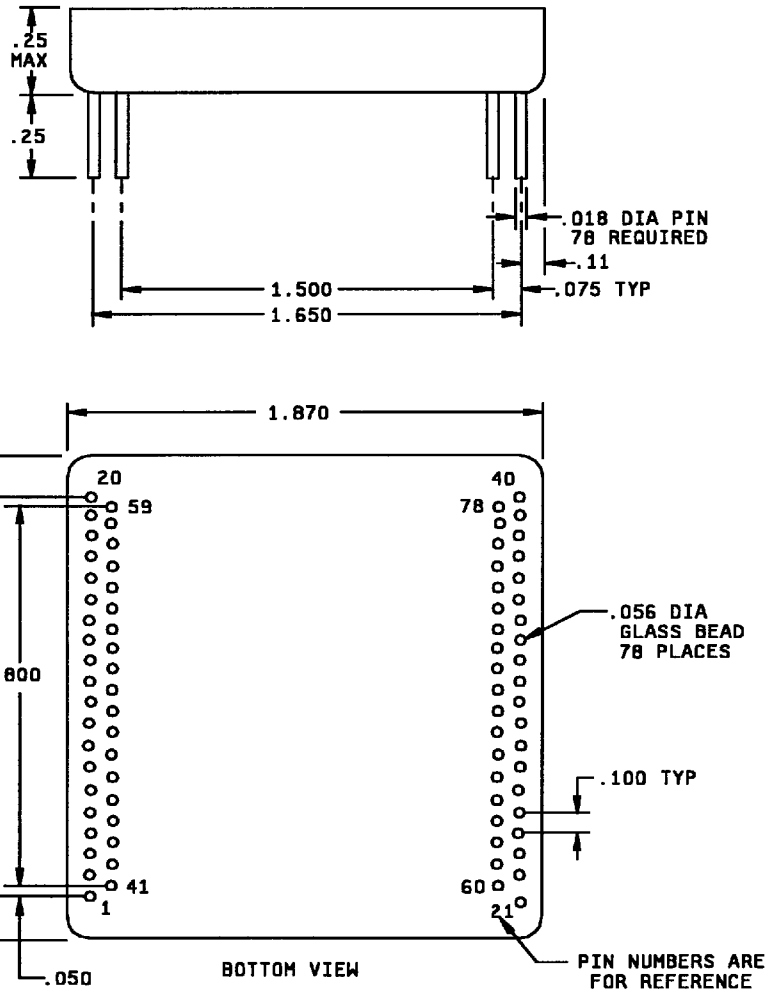
See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Input/output capacitance 6/	C_{IO}	f = 1 MHz, see 4. 3. 1b	4	All		50	pF
Power supplies							
+5 V dc current drain	I_L	V_L = 5.5 V dc Inputs = 0 V dc, except 12 MHz. Clock input active. All outputs open.	1, 2, 3	All		115	mA
-15 V dc current drain	I_{EE}	V_{EE} = -15.75 V dc					mA
- idle			1, 2, 3	01, 03		70	
- 50% transmit						175	
- 100% transmit						270	
-12 V dc current drain 9/	I_{EE}	V_{EE} = -12.6 V dc					mA
- idle			1, 2, 3	02, 04		70	
- 50% transmit						185	
- 100% transmit						305	

1/ V_{EE} = -15 V for device types 01 and 03. V_{EE} = -12.0 V for device types 02 and 04. V_L = +5 V unless otherwise specified.
2/ Parameter shall be tested as part of device characterization and after design and process changes and therefore shall be guaranteed to the limits specified in table I.
3/ Receiver and transmitter parameters are specified with transformer.
4/ I_{IH} and I_{IL} for input pins BRO ENA, ADDRE, ADDRC, ADDRA, ADDRD, ADDRB, and ADDRP. (These inputs have internal pull up resistors connected.)
5/ I_{IH} and I_{IL} for all input pins other than in note 4 and 6.
6/ I_O parameters for pins DB0 through DB15.
7/ V_{OH} for all output pins other than in note 6.
8/ Functional tests performed to verify functionally to MIL-STD-1553 RTU protocol.
9/ The dc current drain is only tested at 50% duty cycle with a maximum limit of 130 mA.

Case outline X.

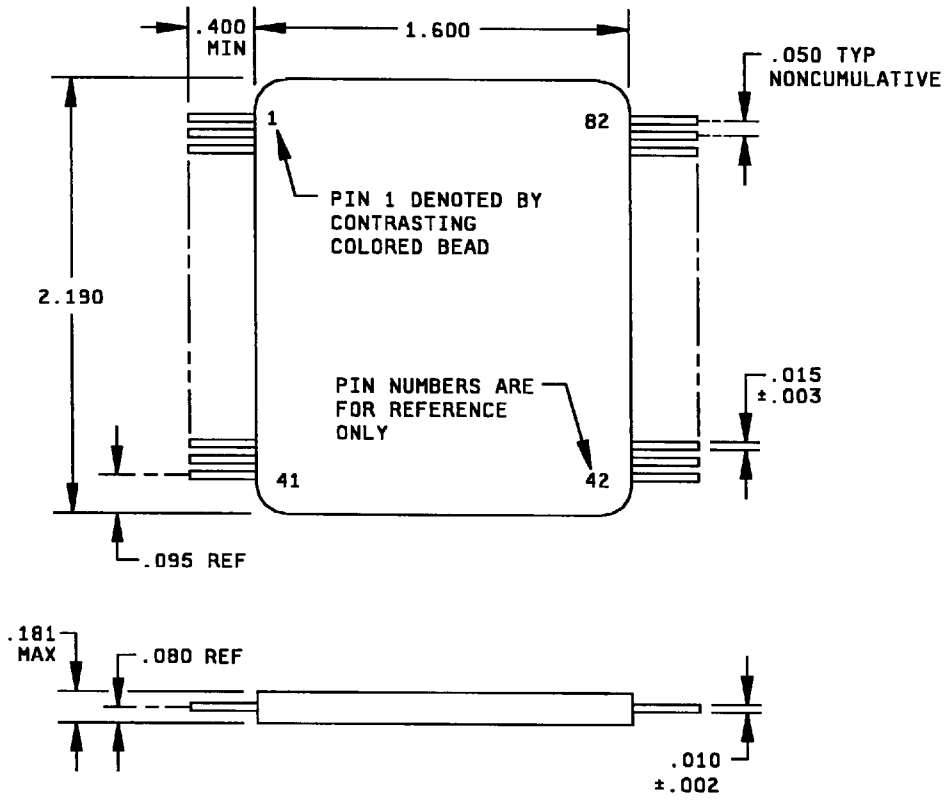


Inches	mm
.005	0.13
.01	0.30
.018	0.46
.050	1.27
.056	1.42
.075	1.91
.100	2.54
.11	2.8
.25	6.4
1.500	38.10
1.650	41.91
1.800	45.72
1.870	47.50
1.900	48.26
2.100	53.34

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Unless otherwise specified, tolerance is ±.005 (0.13 mm) for three place decimals and ±.01 (0.3 mm) for two place decimals.

FIGURE 1. Case outline(s).

Case outline Y.



Inches	mm
.002	0.05
.003	0.08
.005	0.13
.010	0.30
.015	0.38
.050	1.27
.080	2.03
.095	2.41
.181	4.60
.400	10.16
1.600	40.16
2.190	55.63

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Unless otherwise specified, tolerance is ±.005 (0.13 mm) for three place decimals and ±.01 (0.3 mm) for two place decimals.

FIGURE 1. Case outline(s) - Continued.

All device types Terminal number Case X	Case Y	Function	Description
1	2	A9	Latched output of the most significant bit (MSB) in the subaddress field of the command word.
2	4	A7	Latched output of the third most significant bit in the subaddress field of the command word.
3	6	A5	Latched output of the least significant bit (LSB) in the subaddress field of the command word.
4	8	DB1	Bidirectional parallel data bus bit 1.
5	10	DB3	Bidirectional parallel data bus bit 3.
6	12	DB5	Bidirectional parallel data bus bit 5.
7	14	DB7	Bidirectional parallel data bus bit 7.
8	16	DB9	Bidirectional parallel data bus bit 9.
9	18	DB11	Bidirectional parallel data bus bit 11.
10	20	DB13	Bidirectional parallel data bus bit 13.
11	22	DB15	Bidirectional parallel data bus bit 15 (MSB).
12	24	BRO ENA	Broadcast enable - When HIGH, this input allows recognition of an RT address of all ones in the command word as a broadcast message. When LOW, it prevents response to RT address 31 unless it was the assigned terminal address.
13	26	ADDRE	Input of the MSB of the assigned terminal address.
14	28	ADDRC	Input of the 3rd MSB of the assigned terminal address.
15	30	ADDRA	Input of the LSB of the assigned terminal address.
16	32	$\overline{\text{RTADD ERR}}$	Output signal used to inform subsystem of an address parity error. If LOW, indicates parity error and the RT will not respond to any command address to a single terminal. It will respond to broadcast commands if BRO ENA is HIGH.
17	32	$\overline{\text{TXDATAOUT B}}$	LOW output to the primary side of the coupling transformer that connects to the B channel of the 1553 bus.

FIGURE 2. Terminal connections and pin functions.

All device types Terminal number Case X	Case Y	Function	Description
18	36	N/C	No connection.
19	38	GND B	Power supply return connection for the B channel tranceiver.
20	40	RXDATAIN B	Input from the HIGH side of the primary side of the coupling tranformer that connects to the B channel of the 1553 bus.
21	81	A3	Multiplexed address line output. When INCMD is LOW, or A5 through A9 are all zeroes or all ones (mode command), it represents the latched output of the 2nd MSB in the word count field of the command word. When INCMD is HIGH and A5 through A9 are not all zeroes or all ones, it represents the 2nd MSB of the current word counter. (See note 1)
22	79	A1	Multiplexed address line output. When INCMD is LOW, or A5 through A9 are all zeroes or all ones (mode command), it represents the latched output of the 2nd LSB in the word count field of the command word. When INCMD is HIGH and A5 through A9 are not all zeroes or all ones, it represents the 2nd LSB of the current word counter. (See note 1)
23	77	$\overline{\text{DTGRT}}$	Data transfer grant - Active LOW input signal from the subsystem that informs the RT, when DTREQ is asserted, to start the transfer. Once the transfer is started, DTGRT can be removed.
24	75	INCMD	In command - HIGH level output signal used to inform the subsystem that the RT is presently servicing a command. When low, A0-A4 (see note 1) represent the word count of the present command. When high, A0-A4 represent the current word counter of non-mode commands.
25	73	$\overline{\text{HS FAIL}}$	Handshake fail - Output signal that goes LOW and stays LOW whenever the subsystem fails to supply DTGRT in time to do a successful transfer. Cleared by the next NBGT.
26	71	$\overline{\text{DTSTR}}$	DATA strobe - A LOW level output pulse (166 ns) present in the middle of every data word transfer over the parallel data bus. Used to latch or strobe the data into memory, FIFOs, registers, etc. Recommend using the rising edge to clock data in. (See note 2)
27	69	DAT/$\overline{\text{CMD}}$	Address line output that is LOW whenever the command word is being transferred to the subsystem over the parallel data bus, and is HIGH whenever data words are being transferred.
28	67	$\overline{\text{RT FAIL}}$	Remote terminal failure - Latched active LOW output signal to the subsystem to flag detection of a remote terminal continuous self-test failure. Alsso set if the watchdog timeout circuit is activated. Cleared by the start of the next message transmission (status word) and set if problem is again detected.

FIGURE 2. Terminal connections and pin functions - Continued.

All device types Terminal number Case X	Case Y	Function	Description
29	65	$\overline{\text{DTREQ}}$	Data transfer request - Active LOW output signal to the subsystem indicating that the RT has data for or needs data from the subsystem and requests a data transfer over the parallel data bus. Will stay LOW until transfer is completed or transfer until transfer is completed or transfer timeout has occurred.
30	63	$\overline{\text{ADBC}}$	Accept dynamic bus control - Active LOW input signal from subsystem used to set the dynamic bus control acceptance bit in the status register if the command word was a valid, legal mode command for dynamic bus control.
31	61	TEST 2	Factory test point - DO NOT USE. (See note 3)
32	59	A10	Latched output of the T/R bit in the command word.
33	57	$\overline{\text{ILL CMD(ME)}}$	Illegal command - Active LOW input signal from the subsystem, strobed in on the rising edge of INCMD. Used to define the command word as illegal and to set the message error bit in the status register.
34	55	$\overline{\text{SS REQ}}$	Subsystem service request - Input from the subsystem used to control the service request bit in the status register. If LOW when the status word is updated, the service request bit will be set; if HIGH, it will be cleared.
35	53	$\overline{\text{BITEN}}$	Built-in-test word enable - LOW level output pulse (500 ns), present when the built-in-test word is enabled on the parallel data bus. (See note 4)
36	51	$\overline{\text{RXDATAIN A}}$	Input from the LOW side of the primary side of the coupling transformer that connects to the A channel of the 1553 bus.
37	49	V_L A	+5 volt input power supply connection for the A channel transceiver.
38	47	V_{EE} A	-15 / -12 volt input power supply connection for the A channel transceiver.
39	45	TXDATAOUT A	HIGH output to the primary side of the coupling transformer that connects to the A channel of the 1553 bus.
40	43	$\overline{\text{NBGT}}$	New bus grant - LOW level output pulse (166 ns) used to indicate the start of a new protocol sequence in response to the command word just received. (See note 2)
41	3	A8	Latched output of the 2nd MSB in the subaddress field of the command word.

Figure 2. Terminal connections amd pin functions - Continued.

All device types Terminal number Case X	Case Y	Function	Description
42	5	A6	Latched output of the 2nd LSB in the subaddress field of the command word.
43	7	DB0	Bidirectional parallel data bus bit 0 (LSB).
44	9	DB2	Bidirectional parallel data bus bit 2.
45	11	DB4	Bidirectional parallel data bus bit 4.
46	13	DB6	Bidirectional parallel data bus bit 6.
47	15	DB8	Bidirectional parallel data bus bit 8.
48	17	DB10	Bidirectional parallel data bus bit 10.
49	19	DB12	Bidirectional parallel data bus bit 12.
50	21	DB14	Bidirectional parallel data bus bit 14.
51	23	V_L	+5 volt input power supply connection for RTU digital logic section.
52	25	GND	Power supply return for RTU digital logic section.
53	27	ADDRD	Input of the 2nd MSB of the assigned terminal address.
54	29	ADDRB	Input of the 2nd LSB of the assigned terminal address.
55	31	ADDRP	Input of address parity bit. The combination of assigned terminal address and ADDRP must be odd parity for the RT to work.
56	33	TXDATAOUT B	HIGH, output to the primary side of the coupling transformer that connects to the B channel of the 1553 bus.
57	35	V_{EE} B	-15 / -12 volt input power supply connection for the B channel transceiver
58	37	V_L B	+5 volt input power supply connection for the B channel transceiver.
59	39	$\overline{\text{RXDATAIN B}}$	Input from the LOW side of primary side of the coupling transformer that connects to the B channel of the 1553 bus.

FIGURE 2. Terminal connections and pin functions - Continued.

All device types Terminal number Case X	Case Y	Function	Description
60	80	A2	Multiplexed address line output. When INCMD is LOW, or A5 through A9 are all zeroes or all ones (mode command), it represents the latched output of the 3rd MSB in the word count field of the command word. When INCMD is HIGH and A5 through A9 are not all zeroes or all ones, it represents the 3rd MSB of the current word counter. (See note1)
61	78	A0	Multiplexed address line output. When INCMD is LOW, or A5 through A9 are all zeroes or all ones (mode command), it represents the latched output of the LSB in the word count field of the command. When INCMD is HIGH and A5 through A9 are not all zeroes or all ones, it represents the LSB of the current word counter. (See note 1)
62	76	$\overline{\text{DTACK}}$	Data transfer acknowledge - Active LOW output signal during data transfers to or from the subsystem indicating the RTU has received the DTGRT in response to DTREQ and is presently doing the transfer. Can be connected directly to pin 67, case X or pin 66, case case Y (BUF ENA) for control of 3-state data buffers; and to 3-state address buffer control lines, if they are used.
63	74	A4	Multiplexed address line output. When INCMD is LOW or A5 through A9 are all zeroes or all ones (mode command), it represents the latched output of the MSB in the word count field of the command word. When INCMD is HIGH and A5 through 9A0 arenot all zeroes or all ones, it represents the MSB of the current word counter. (See note 1)
64	72	R/$\overline{\text{W}}$	Read/Write - Output signal that controls the direction of the internal data bus buffers. Normally, the signal is LOW and the buffers drive the data bus. When data is needed from the subsystem, it goes HIGH to turn the buffers around and the RT now appears as an input. The signal is HIGH only when DTREQ is active (LOW).
65	70	$\overline{\text{GBR}}$	Good block received - LOW level output pulse (500 ns) used to flag the subsystem that a valid, legal, non-mode receive command with the correct number of data words has been received without a message error and successfully transferred to the subsystem. (See note 4)
66	68	16 MHz IN	16 MHz clock input - Input for the master clock used to run RTU circuits.
67	66	$\overline{\text{BUF ENA}}$	Buffer enable - Input used to enable or 3-state the internal data bus buffers when they are driving the bus. When LOW, the data bus buffers are enabled. Could be connected to DTACK (pin 62, case X), (pin 76, case Y) if RT is sharing the same data bus as the subsystem. (See note 5)

FIGURE 2. Terminal connections and pin functions - Continued.

All device types Terminal number Case X	Case Y	Function	Description
68	64	$\overline{\text{RESET}}$	Input resets entire RT when LOW.
69	62	$\overline{\text{RT FLAG}}$	Remote terminal flag - Input signal used to control the terminal flag bit in the status register. If LOW when the status word is updated, the terminal flag bit would be set; if HIGH, it would be cleared. Normally connected to RTFAIL (pin 28, case X),(pin 67, case Y).
70	60	TEST 1	Factory test point - DO NOT USE. (See note 6)
71	58	$\overline{\text{SS BUSY}}$	Subsystem busy - Input from the subsystem used to control the busy bit in the status register. If LOW when the status word is updated, the busy bit will be set; if HIGH, it will be cleared. If thebusy bit is set in the status register, no data will be requested from the subsystem in response to a transmit command. On receive commands, data will still be transferred to subsystem.
72	56	$\overline{\text{SS FLAG}}$	Subsystem flag - Input from the subsystem used to control the subsystem flag bit in the status register. If LOW when the status word is updated, the subsystem flag will be set; if HIGH, it wil be cleared.
73	54	$\overline{\text{MESS ERR}}$	Message error - Output signal that goes LOW and stays low whenever there is a format or word error with the received message over the 1553 data bus. Cleared by the next NBGT.
74	52	RXDATAIN A	Input from the HIGH side of the primary side of the coupling transformer that contacts to the A channel of the 1553 bus.
75	50	GND A	Power supply return connection for the A channel transceiver.
76	48	N/C	No connection.
77	46	$\overline{\text{TXDATAOUT A}}$	LOW output to the primary side of the coupling transformer that connects to the A channel of the 1553 bus.
78	44	$\overline{\text{STATEN}}$	Status word enable - LOW level active output signal present when the status word is enabled on the parallel data bus.

FIGURE 2. Terminal connections and pin functions - Continued.

NOTES:

1. Device types 03 and 04:
   When INCMD is LOW during the DTSTR immediately following NBGT, A0 through A4 are valid and equal to WC0 through WC4 of the received command word. The remaining time while INCMD is LOW and A5 through A9 are not all zeros or ones (i.e. MODE), A0 through A4 are equal to the last current word count plus one. When INCMD is HIGH and A5 through A9 are not MODE, A0 through A4 represent the current word counter. If A5 through A9 are equal to MODE, A0 through A4 are equal to WC0 through WC4 of the received command word, independent of the state of INCMD.

2. Device type 03 and 04, pulse width is typically 125 ns.

3. Pin 31 for case X and pin 61 for case Y - (TEST 2) factory test point output: This pin provides the output of the device BIT comparison output. It indicates the loop test results for every word transmitted by the device. A test can be performed by actioning the RTU to transmit while the test fixture opens the receiver lines to force an error condition. A logic 1 (high) indicates the loop test passed. Normally this pin is left open. For device types 03 and 04, (TEST 2) is not implemented and should be left open.

4. Device type 03 and 04, pulse width is typically 375 ns.

5. Pin 67 for case X and pin 66 for case Y - BUF ENA: This pin is typically tied to DTACK, causing the device to drive the shared data bus only while DTACK is active. If desired BUF ENA can be gounded. The data will remain latched on the data bus pins for 18 µs from DTSRB and 3.5 µs, (device types 03 and 04 are 19 µs and 4 µs, respectively) for the last word of a message as the devices status word or BIT word is transferred to the BC (STATEN or BITEN low). Once the STATUS or BIT word transfer is complete, the data bus will automatically again contain the last data word. The device will automatically switch the direction of the internal buffers during a transmit operation.

6. Pin 70 for case X and pin 60 for case Y - (TEST 1) factory test point: This test allows the user to force the active channel to transmit indefinitely, in order to test the built-in watchdog timer feature of the device. When this pin is grounded and the active channel is stimulated with a valid transmit command, the device will respond with a status word and continguous data (last data word loaded or STATUS WORD if none is loaded) until the built-in timeout occurs. Normally this pin is left open or an optional pull-up can be used. For device types 03 and 04, (TEST 1) is not implemented and should be left open open.

7. For case Y, pins 1, 41, 42, and 82 are no connections.

FIGURE 2. Terminal connections and pins functions - Continued.

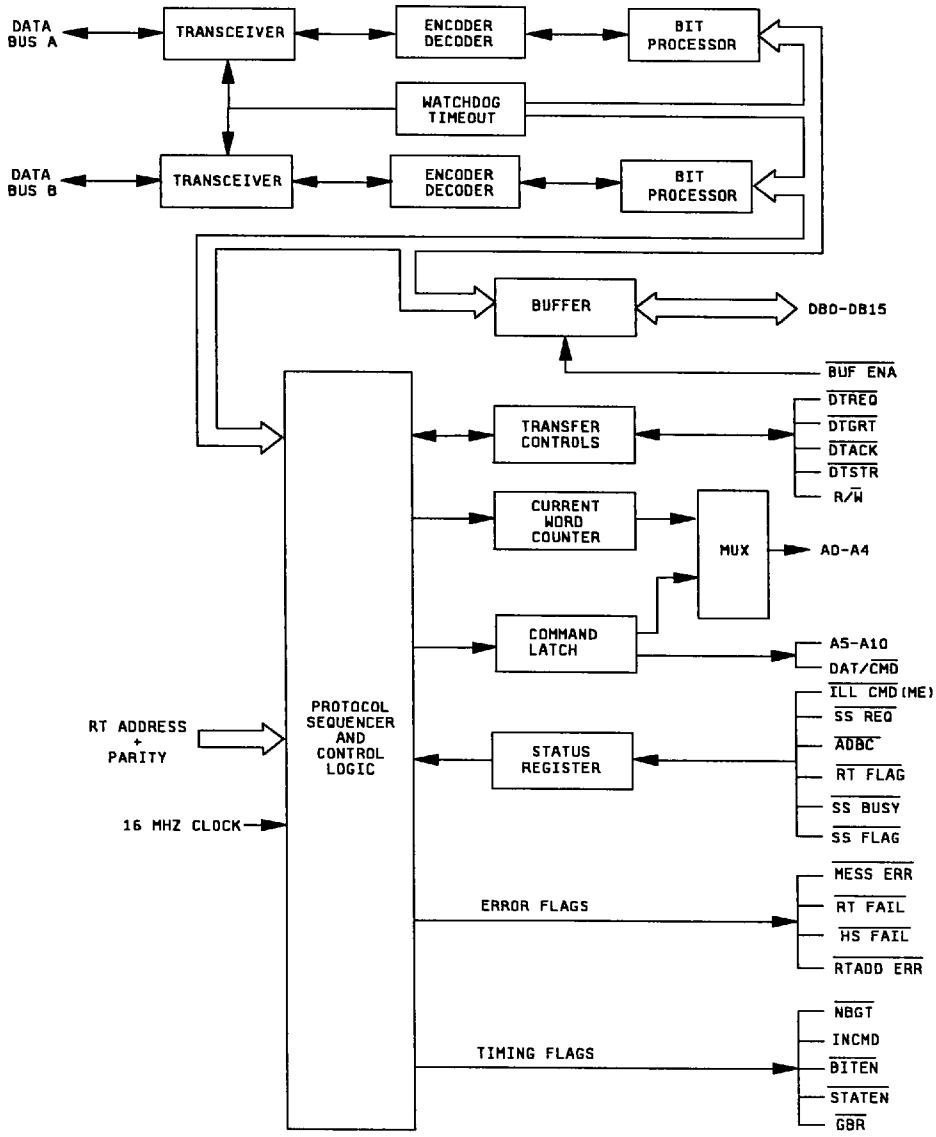


FIGURE 3. Block diagram.

TABLE II. Electrical test requirements.

MIL-PRF-38534 test requirements	Subgroups (in accordance with MIL-PRF-38534, group A test table)
Interim electrical parameters	1, 4, 9,
Final electrical parameters	1*,2,3,4,5,6,7,8,9,10,11
Group A test requirements	1,2,3,4,5,6,7,8,9,10,11
Group C end-point electrical parameters	1, 2, 3

* PDA applies to subgroup 1.

4.3 Conformance and periodic inspections. Conformance inspection (CI) and periodic inspection (PI) shall be in accordance with MIL-PRF-38534 and as specified herein.

4.3.1 Group A inspection (CI). Group A inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroup 4 (C_I and C_{IO} measurement) shall be measured only for the initial test and after process or design changes which may affect input and output capacitance.

4.3.2 Group B inspection (PI). Group B inspection shall be in accordance with MIL-PRF-38534.

4.3.3 Group C inspection (PI). Group C inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1005 of MIL-STD-883.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.3.4 Group D inspection (PI). Group D inspection shall be in accordance with MIL-PRF-38534.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38534.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-7603.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, P. O. Box 3990, Columbus, Ohio 43216-5000, or telephone (614) 692-0676.

6.6 Sources of supply. Sources of supply are listed in QML-38534. The vendors listed in QML-38534 have submitted a certificate of compliance (see 3.7 herein) to DSCC-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 98-05-14

Approved sources of supply for SMD 5962-89798 are listed below for immediate acquisition only and shall be added to QML-38534 during the next revision. QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of QML-38534.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8979801XA	19645	BUS-65142-140
5962-8979801XC	19645	BUS-65142-110
5962-8979801YA	19645	BUS-65144-140
5962-8979801YC	19645	BUS-65144-110
5962-8979802XA	19645	BUS-65143-140
5962-8979802XC	19645	BUS-65143-110
5962-8979802YA	19645	BUS-65145-140
5962-8979802YC	19645	BUS-65145-110
5962-8979803XA	88379	CT2542
5962-8979803XC	88379	CT2542
5962-8979803YA	88379	CT2542-FP
5962-8979803YC	88379	CT2542-FP
5962-8979804XA	88379	CT2543
5962-8979804XC	88379	CT2543
5962-8979804YA	88379	CT2543-FP
5962-8979804YC	88379	CT2543-FP

1/ The lead finish shown for each PIN, representing a hermetic package, is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
19645	ILC Data Device Corporation 105 Wilbur Place Bohemia, NY 11716-2482
88379	Aeroflex Circuit Technology Corporation 35 South Service Road Plainview, NY 11803-4193

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.