

256Kx16 CMOS, High Speed Programmable, Static RAM Module

The EDI8M16256C is a 4096K-bit high speed CMOS Static RAM Module consisting of sixteen (16) 256Kx1 Static RAMs in leadless chip carriers surface-mounted onto a multilayered ceramic substrate. Four Chip Select lines are provided (one for each 256Kx4 array) allowing the user to configure the memory into a 256Kx16, 512Kx8 or 1024Kx4 organizations.

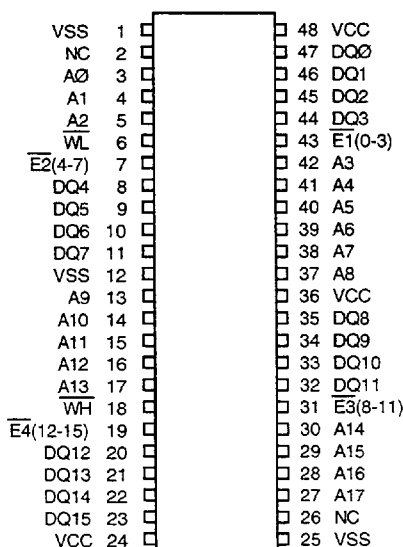
The EDI8M16256C is available with access times as fast as 45ns. The module is a high density, 48 pin sidebraced DIP on 900 mil centers.

All inputs and outputs are TTL compatible and operate from a single 5V supply. Multiple ground pins are provided for maximum noise immunity.

Fully asynchronous circuitry requires no clocks or refreshing for operation.

EDI Military Modules are built with RAMs that are compliant to MIL-STD-883, paragraph 1.2.1.

Pin Configuration and Block Diagram



Features

High Density 4096K-bit CMOS Static Random Access Memory Module

- Access Times 45, 55, and 70ns
- Fully Static, No Clocks
- Inputs and Outputs Directly TTL Compatible
- Customer Configured Memory, as 256Kx16, 512Kx8 or 1024Kx4

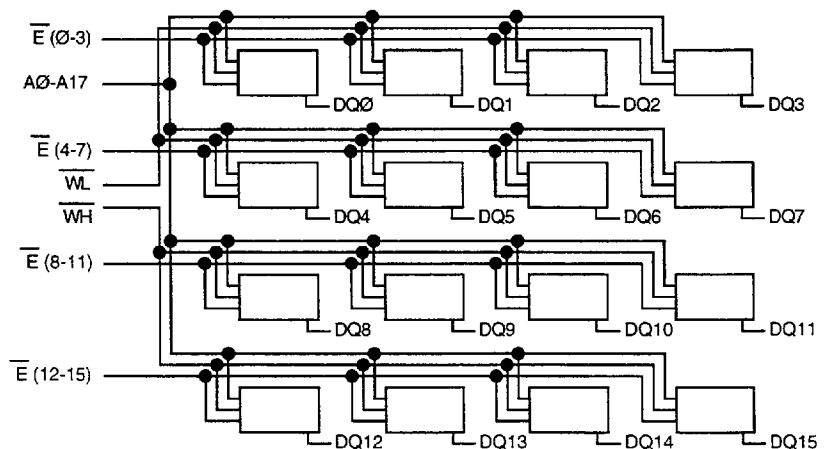
48 Pin Dual-in-line Package, No. 109

- Multiple Ground Pins for Maximum Noise Immunity

Single +5V ($\pm 10\%$) Supply Operation

Pin Names

A0-A17	Address Inputs
E1-E4	Chip Enables
WL, WH	Write Enables
DQ0-DQ15	Data Input/Output
VCC	Power (+5V $\pm 10\%$)
VSS	Ground



Absolute Maximum Ratings*

Voltage on any pin relative to VSS -0.5V to 7.0V
 Operating Temperature TA (Ambient)
 Industrial -40°C to +85°C
 Military -55°C to +125°C
 Storage Temperature, Ceramic -65°C to +150°C
 Power Dissipation 8 Watts
 Output Current 20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels VSS to 3.0V
 Input Rise and Fall Times 5ns
 Input and Output Timing Levels 1.5V
 Output Load. 1TTL, CL = 30pF
 (note: For TEHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

Parameter	Sym	Conditions	Mode	Min	Typ*	Max	Units
Operating Power Supply Current	ICC1	$\overline{W}, \overline{E} = \text{VIL}, \text{I/O} = 0\text{mA}, \text{Min Cycle}$	x16	--	1300	2000	mA
			x8	--	700	1200	
			x4	--	350	800	
Standby (TTL) Power Supply Current	ICC2	$\overline{E} \geq \text{VIH}, \text{VIN} \leq \text{VIL} \text{ or } \text{VIN} \geq \text{VIH}$	--	32	400	mA	
Full Standby Power Supply Current	ICC3	$\overline{E} \geq \text{VCC}-0.2\text{V}$ $\text{VIN} \geq \text{VCC}-0.2\text{V} \text{ or } \text{VIN} \leq 0.2\text{V}$	--	16	160	mA	
Input Leakage Current	ILI	$\text{VIN} = 0\text{V to VCC}$	--	--	± 50	μA	
Output Leakage Current	ILO	$\text{V I/O} = 0\text{V to VCC}$	--	--	± 50	μA	
Output High Voltage	VOH	$\text{IOH} = -4.0\text{mA}$	2.4	--	--	V	
Output Low Voltage	VOL	$\text{IOL} = 8.0\text{mA}$	--	--	0.4	V	

*Typical: TA = 25°C, VCC = 5.0V

Truth Table

\overline{E}	\overline{W}	Mode	Output	Power
H	X	Standby	HIGH Z	ICC2, ICC3
L	H	Read	DOUT	ICC1
L	L	Write	HIGH Z	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Units
Address Lines	CI	140	pF
Enable Line (\overline{E})	CE	40	pF
Write Lines ($\overline{WL}, \overline{WH}$)	CW	60	pF
Data Lines (DQpins)	CD/Q	25	pF

These parameters are sampled, not 100% tested.

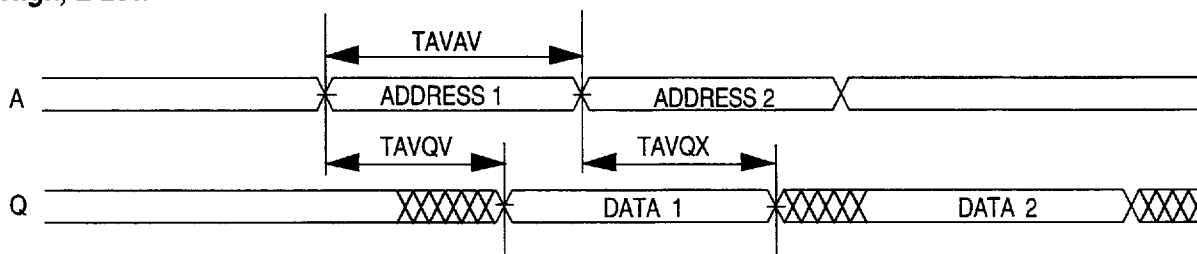
AC Characteristics

Read Cycle

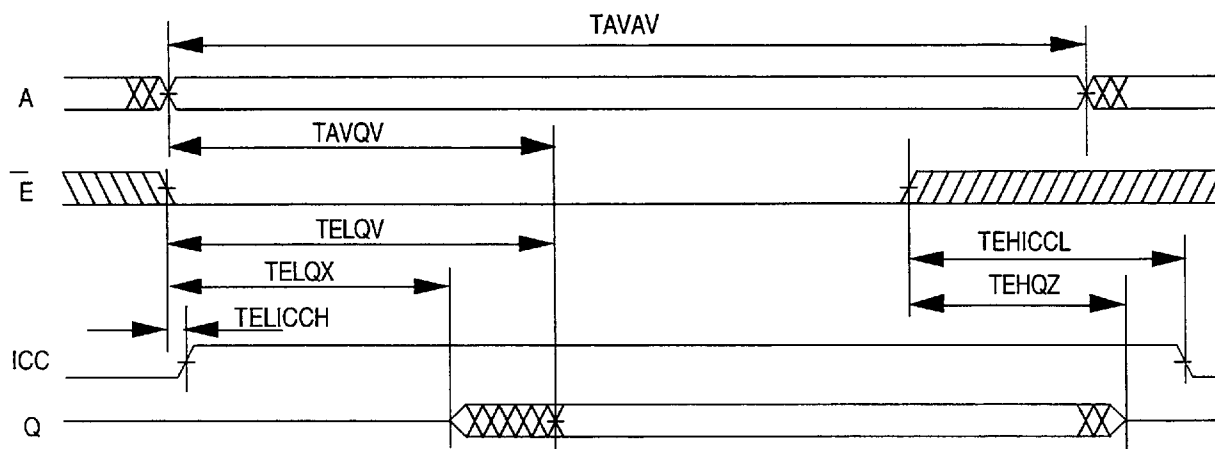
Parameter	Symbol		45ns		55ns		70ns		Unit
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV	TRC	45		55		70		ns
Address Access Time	TAVQV	TAA		45		55		70	ns
Chip Enable Access Time	TELQV	TACS		45		55		70	ns
Chip Enable to Output Low Z (1)	TELQX	TCLZ	5		5		5		ns
Chip Enable to Output in High Z (1)	TEHQZ	TCHZ	0	20	0	20	0	20	ns
Output Hold from Address Change	TAVQX	TOH	5		5		5		ns
Chip Enable to Power Up (1)	TELICCH	TPU	0		0		0		ns
Chip Disable to Power Down (1)	TEHICCL	TPD	0	45	0	55	0	70	ns

Note 1: Parameter guaranteed, but not tested.

Read Cycle 1 W High, E Low



Read Cycle 2 W High



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Military

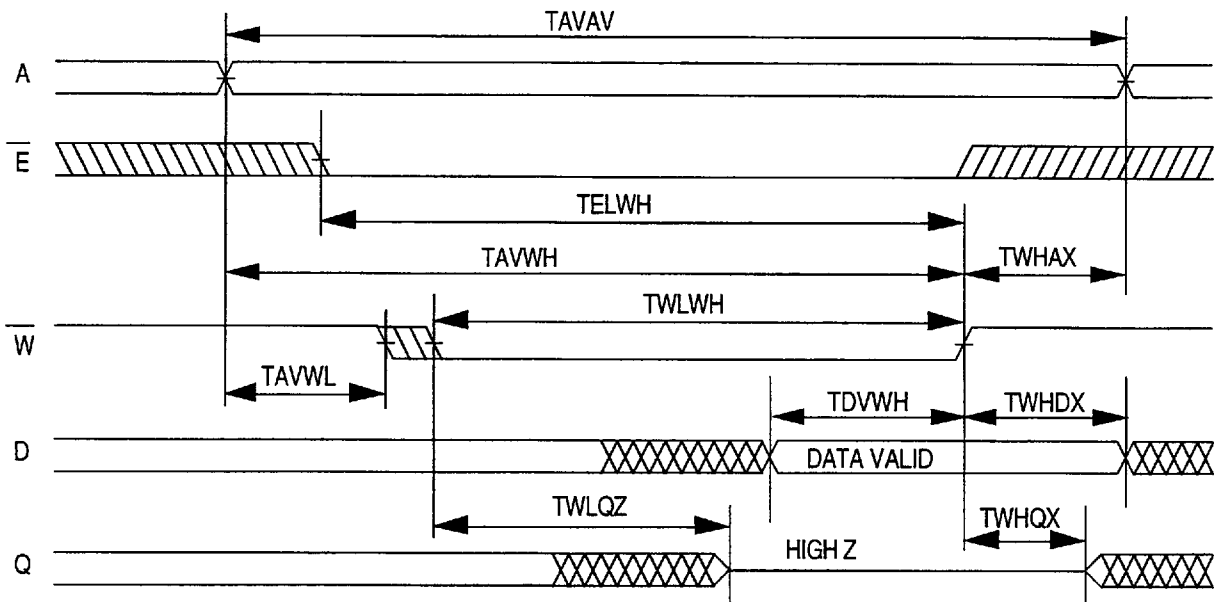
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AC Characteristics
Write Cycle

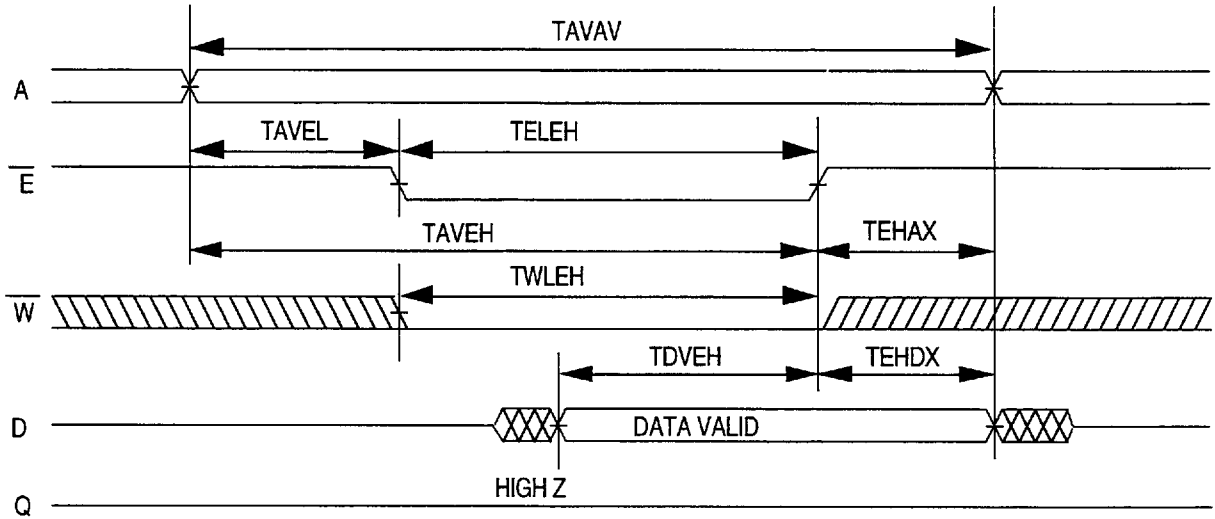
Parameter	Symbol		45ns		55ns		70ns		Unit
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV	TWC	45		55		70		ns
Chip Enable to	TELWH	TCW	35		40		45		ns
End of Write	TELEH	TCW	35		40		45		ns
Address Setup Time	TAVWL	TAS	0		0		0		ns
	TAVEL	TAS	0		0		0		ns
Address Valid to End of Write	TAVWH	TAW	35		40		45		ns
	TAVEH	TAW	35		40		45		ns
Write Pulse Width	TWLWH	TWP	25		30		40		ns
	TWLEH	TWP	25		30		40		ns
Write Recovery Time	TWHAX	TWR	5		5		5		ns
	TEHAX	TWR	5		5		5		ns
Data Hold Time	TWHDX	TDH	0		0		0		ns
	TEHDX	TDH	0		0		0		ns
Write to Output in High Z (1)	TWLQZ	TWHZ	0	30	0	30	0	35	ns
Data to Write Time	TDVWH	TDW	25		25		40		ns
	TDVEH	TDW	25		25		40		ns
Output Active from End of Write (1)	TWHQX	TWLZ	0		0		0		ns

Note 1: Parameter guaranteed, but not tested.

Write Cycle 1
W Controlled



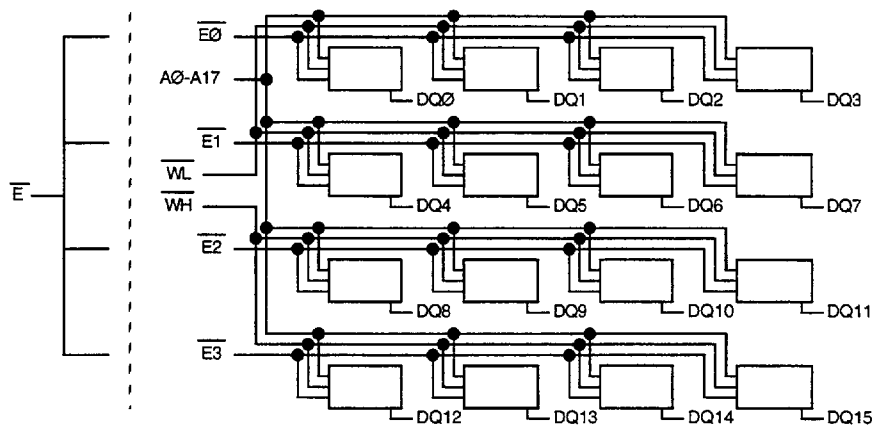
Write Cycle 2
 \overline{E} Controlled



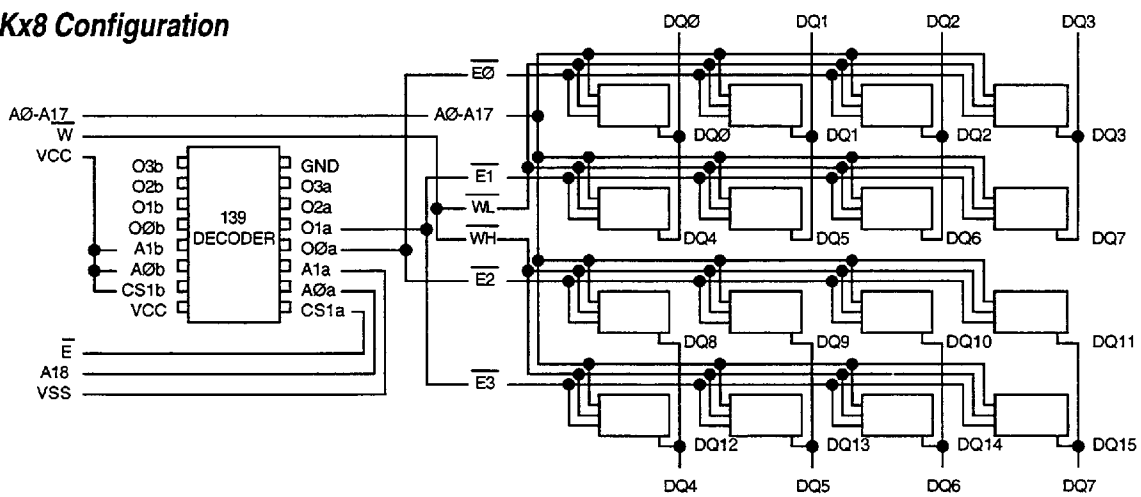
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Device Configurations for 139 Decoder Applications

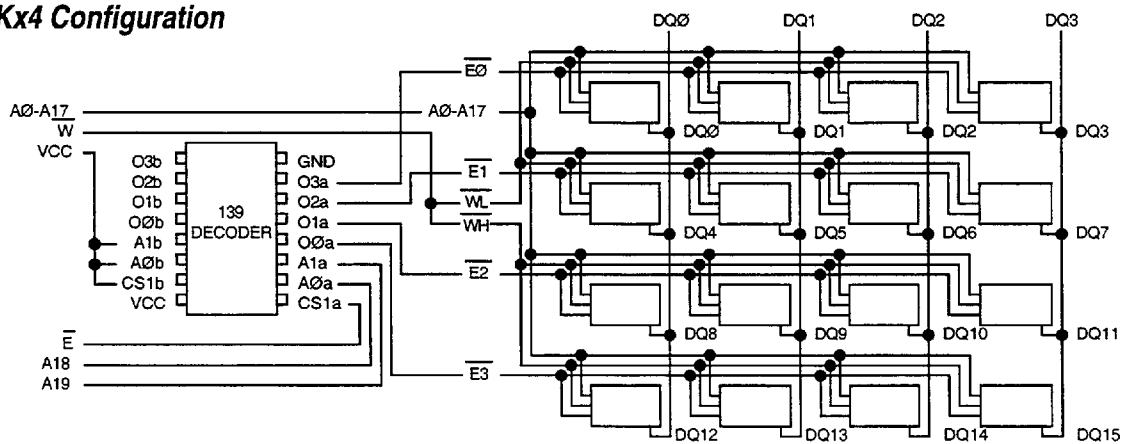
256Kx16 Configuration



512Kx8 Configuration



1024Kx4 Configuration

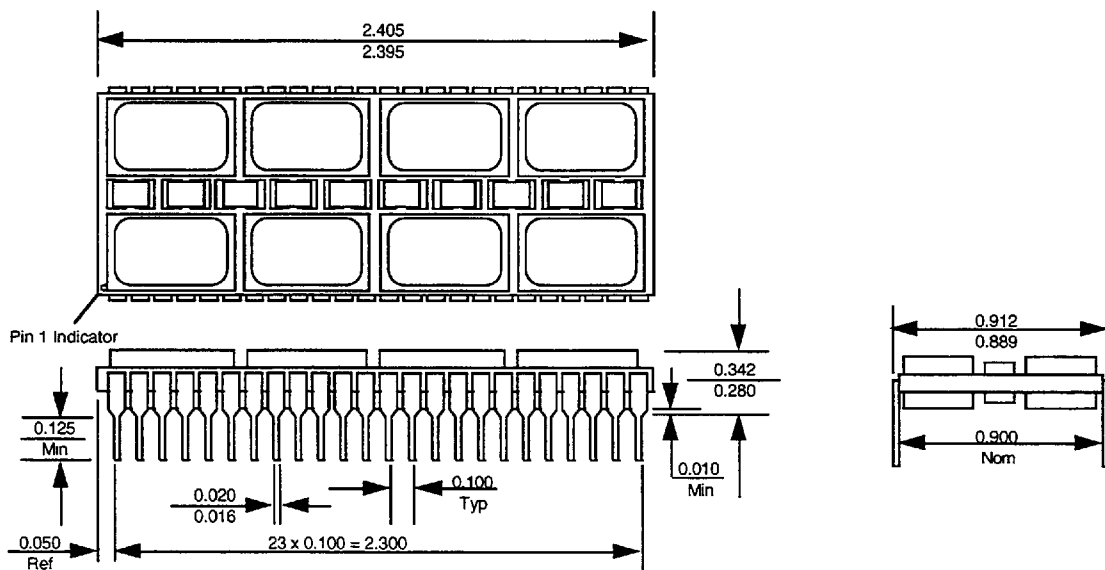


Ordering Information

Part No.	Speed (ns)	Leads	Package Style	No.
EDI8M16256C45C9B	45	48	0.9 DIP	109
EDI8M16256C55C9B	55	48	0.9 DIP	109
EDI8M16256C70C9B	70	48	0.9 DIP	109

Package Description

Package No. 109
48 Pin Dual-in-line Package,
Ceramic Leadless Chip Carriers
on a Sidebrazed Ceramic Substrate,
900 mils Wide



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